

KEC

SEMICONDUCTOR
TECHNICAL DATA

KMA4D5P20X

P-CH Trench MOSFET

General Description

It's mainly suitable for battery pack or power management in cell phone, and PDA.

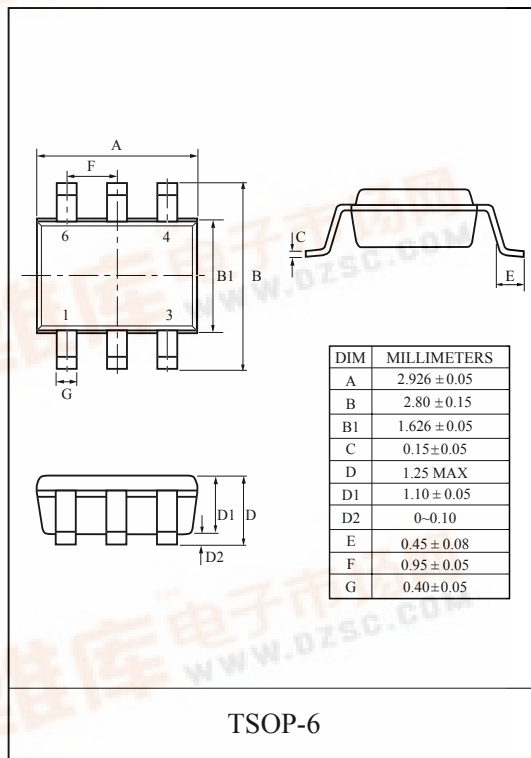
FEATURES

- $V_{DS} = -20V$, $I_D = -4.5A$.
- Drain-Source ON Resistance.
 - : $R_{DS(ON)} = 60m\ \Omega$ (Max.) @ $V_{GS} = -4.5V$, $I_D = -4.5A$
 - : $R_{DS(ON)} = 110m\ \Omega$ (Max.) @ $V_{GS} = -2.5V$, $I_D = -3.3A$
- Super High Dense Cell Design for Extremely Low $R_{DS(ON)}$

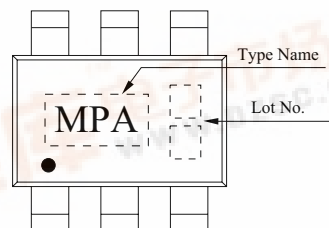
MAXIMUM RATING ($T_a = 25^\circ C$)

CHARACTERISTIC		SYMBOL	RATING	UNIT
Drain-Source Voltage		V_{DSS}	-20	V
Gate-Source Voltage		V_{GSS}	± 12	V
Drain Current	DC	I_D^*	± 4.5	A
	Pulsed	I_{DP}^*	± 16	
Continuous Source Current		I_S	-1.3	A
Drain Power Dissipation	$T_a = 25^\circ C$	P_D^*	2.0	W
	$T_a = 70^\circ C$		1.3	
Maximum Junction Temperature		T_j	150	$^\circ C$
Storage Temperature Range		T_{stg}	$-55 \sim 150$	$^\circ C$
Thermal Resistance, Junction to Ambient		R_{thJA}^*	62.5	$^\circ C/W$

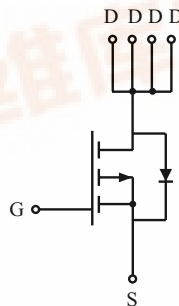
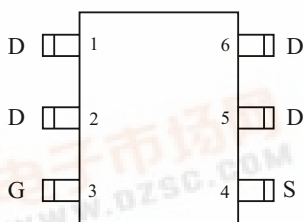
* : Surface Mounted on $1'' \times 1''$ FR4 Board, $t \leq 5sec$.



Marking



PIN CONNECTION (TOP VIEW)



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ELECTRICAL CHARACTERISTICS (Ta=25℃)

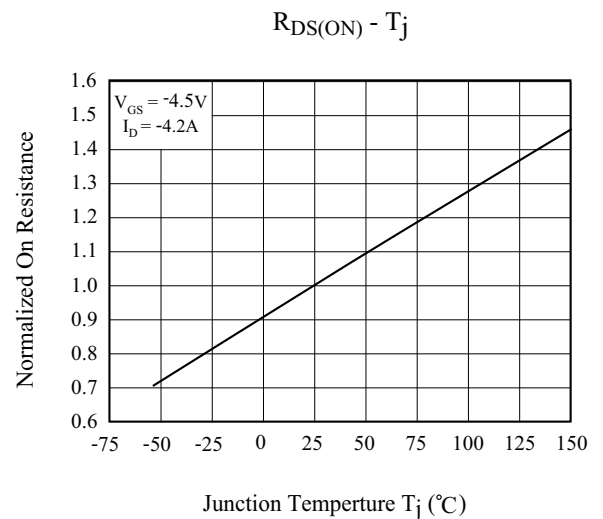
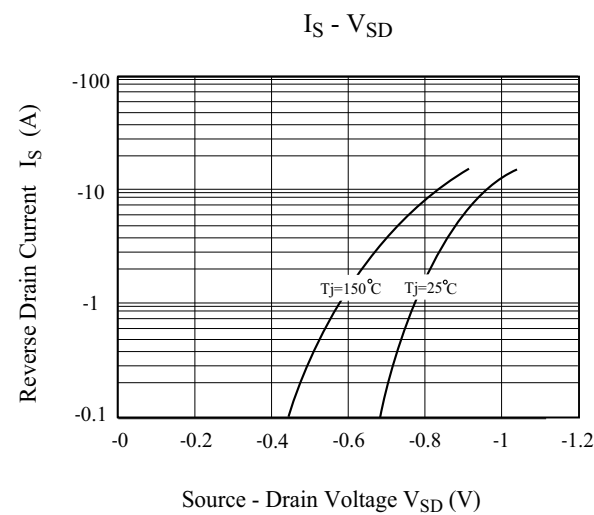
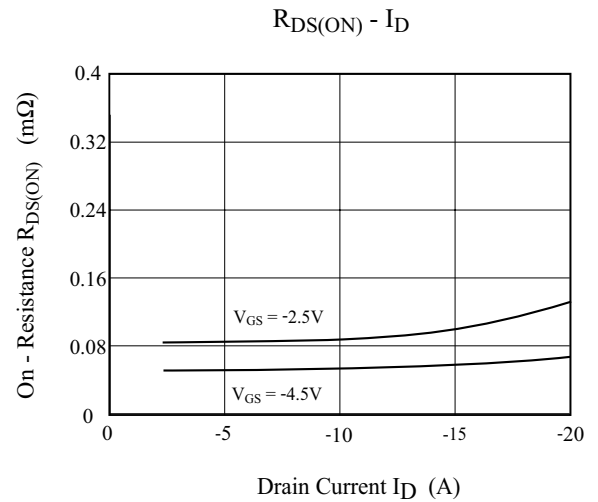
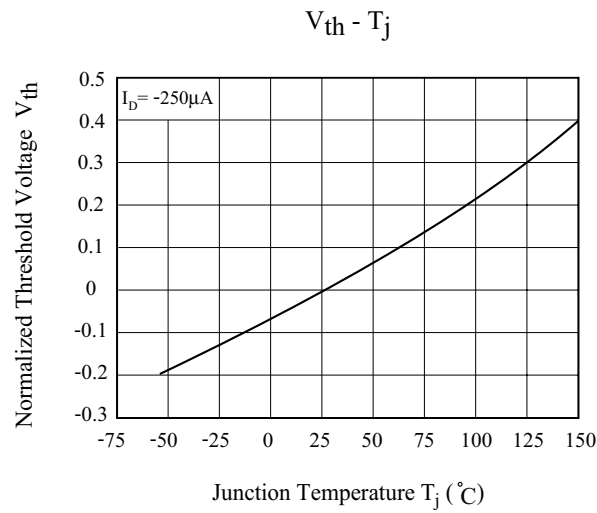
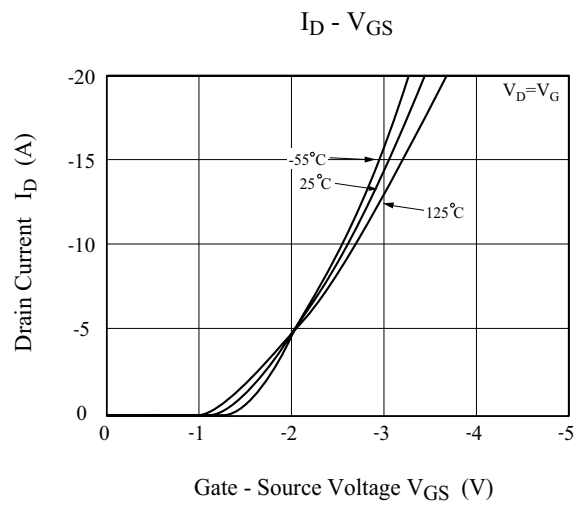
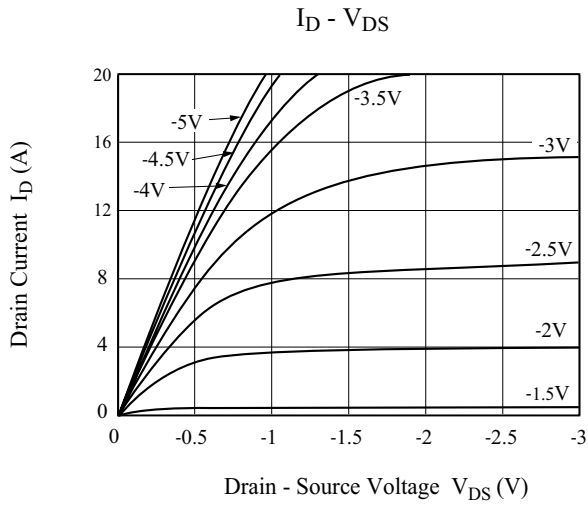
CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Static						
Drain-Source Breakdown Voltage	BV_{DSS}	$I_D=-250\mu A, V_{GS}=0V$	-20	-	-	V
Drain Cut-off Current	I_{DSS}	$V_{GS}=0V, V_{DS}=-20V$	-	-	-1	μA
		$V_{GS}=0V, V_{DS}=-16V, T_j=70^{\circ}C$ (Note 3)	-	-	-5	
Gate Threshold Voltage	V_{th}	$V_{DS}=V_{GS}, I_D=-250\mu A$	-0.6	-	-1.3	V
Gate Leakage Current	I_{GSS}	$V_{GS}=\pm 12V, V_{DS}=0V$	-	-	± 100	nA
Drain-Source ON Resistance	$R_{DS(ON)}$	$V_{GS}=-4.5V, I_D=-4.5A$ (Note 2)	-	49	60	m Ω
		$V_{GS}=-2.5V, I_D=-3.3A$ (Note 2)	-	85	110	
Forward Transconductance	g_{fs}	$V_{DS}=-5V, I_D=-4.5A$ (Note 2)	-	7	-	S
Dynamic (Note 3)						
Total Gate Charge	Q_g	$V_{DS}=-10V, R_D=2.2\Omega$ $V_{GS}=-4.5V$ (Fig.1)	-	8.5	-	nC
Gate-Source Charge	Q_{gs}		-	1.8	-	
Gate-Drain Charge	Q_{gd}		-	2.9	-	
Turn-on Delay time	$t_{d(on)}$	$V_{DS}=-10V, R_D=2.2\Omega$ $V_{GS}=-4.5V, R_G=6\Omega$ (Fig.2)	-	12	-	ns
Turn-on Rise time	t_r		-	32	-	
Turn-off Delay time	$t_{d(off)}$		-	64	-	
Turn-off Fall time	t_f		-	40	-	
Source-Drain Diode Ratings						
Continuous Source Current	I_S	$V_{GS} < V_{th}$ (Note 1)	-	-	-1.3	A
Diode Forward Voltage	V_{SD}	$I_S=-4.5A, V_{GS}=0V$ (Note 2)	-	-	-1.3	V

Note 1) Based on thermal dissipation from junction to ambient while mounted on a 1" × 1" FR4 Board.

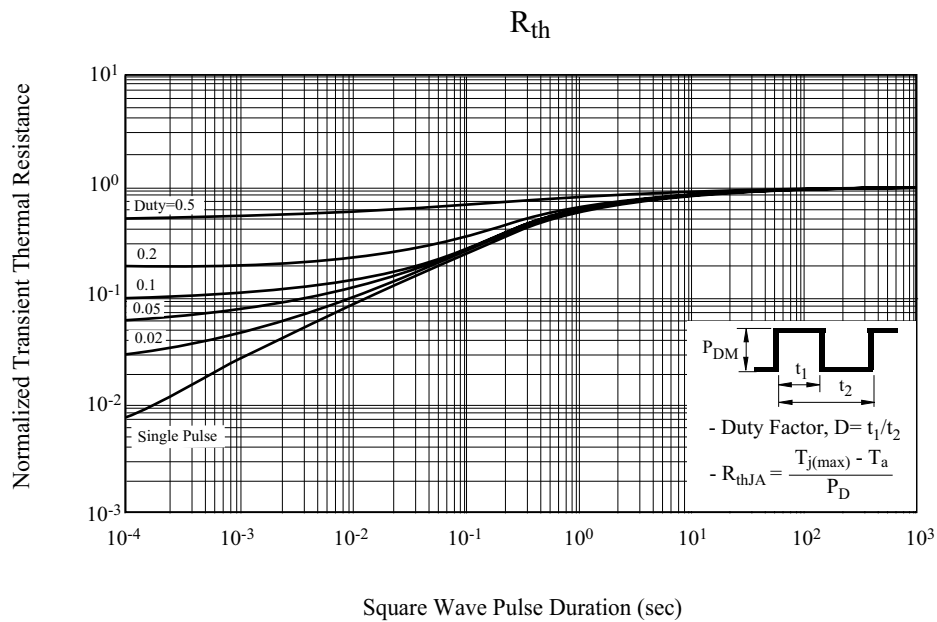
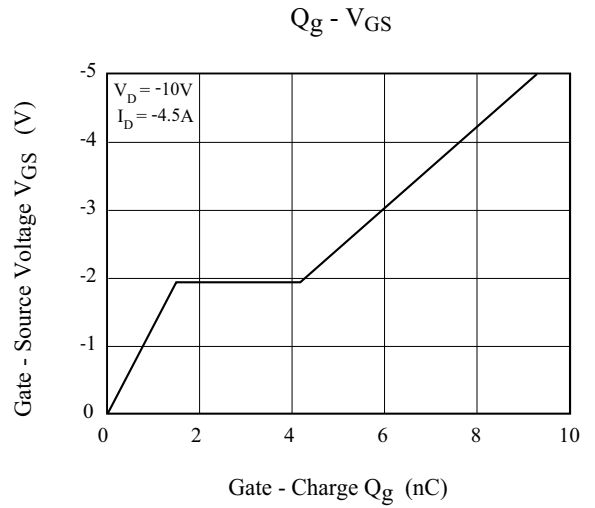
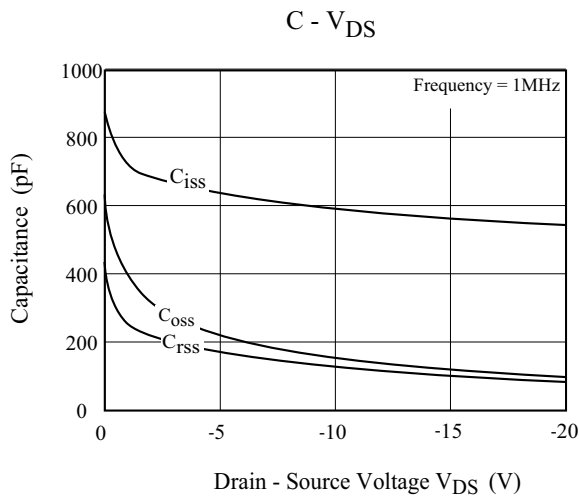
Note 2) Pulse test : Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$

Note 3) Guaranteed by design, not subject to production testing.

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Fig. 1 Gate Charge

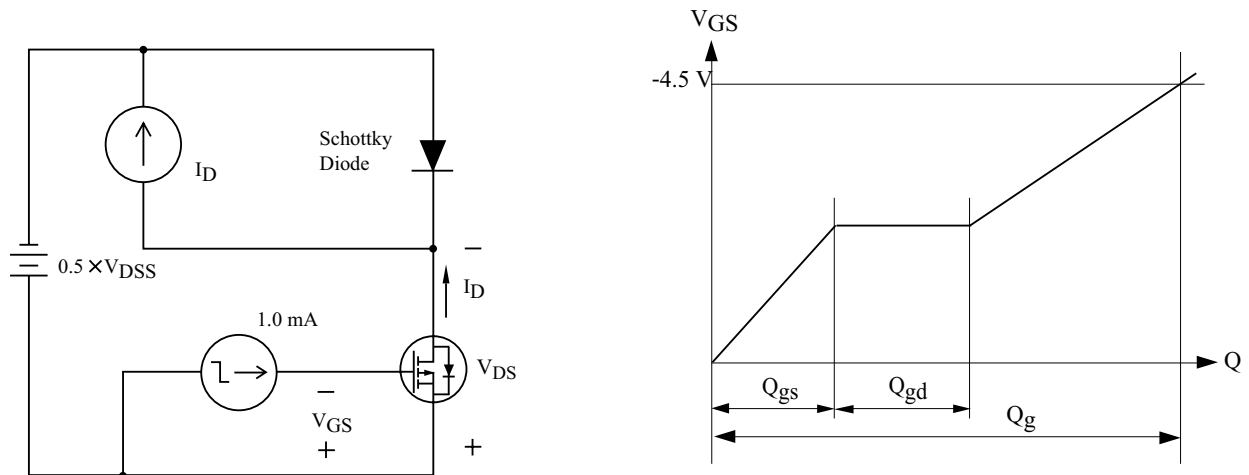


Fig. 2 Resistive Load Switching

