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Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

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TBB1008

Twin Build in Biasing Circuit MOS FET IC
VHF/UHF RF Amplifier

ADE-208-1599 (Z)

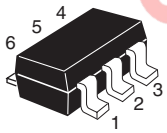
Rev.0
Jun. 2002

Features

- Small SMD package CMPAK-6 built in twin BBFET; To reduce using parts cost & PC board space.
- Suitable for World Standard Tuner RF amplifier.
- Very useful for total tuner cost reduction.
- Withstanding to ESD; Build in ESD absorbing diode. Withstand up to 200 V at C = 200 pF, Rs = 0 conditions.
- Provide mini mold packages; CMPAK-6

Outline

CMPAK-6



1. Gate-1(1)
2. Source
3. Drain(1)
4. Drain(2)
5. Gate-2
6. Gate-1(2)

Notes: 1. Marking is “HM”.
2. TBB1008 is individual type number of HITACHI TWIN BBFET.

Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DS}	6	V
Gate1 to source voltage	V_{G1S}	+6 -0	V
Gate2 to source voltage	V_{G2S}	+6 -0	V
Drain current	I_D	30	mA
Channel power dissipation	Pch[*3]	250	mW
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

Notes: 3. Value on the glass epoxy board (50 mm × 40 mm × 1 mm).

Electrical Characteristics

The below specification are applicable for UHF unit (FET1)

(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	6	—	—	V	I_D = 200 µA, V_{G1S} = V_{G2S} = 0
Gate1 to source breakdown voltage	$V_{(BR)G1SS}$	+6	—	—	V	I_{G1} = +10 µA, V_{G2S} = V_{DS} = 0
Gate2 to source breakdown voltage	$V_{(BR)G2SS}$	+6	—	—	V	I_{G2} = +10 µA, V_{G1S} = V_{DS} = 0
Gate1 to source cutoff current	I_{G1SS}	—	—	+100	nA	V_{G1S} = +5 V, V_{G2S} = V_{DS} = 0
Gate2 to source cutoff current	I_{G2SS}	—	—	+100	nA	V_{G2S} = +5 V, V_{G1S} = V_{DS} = 0
Gate1 to source cutoff voltage	$V_{G1S(off)}$	0.5	0.7	1.0	V	V_{DS} = 5 V, V_{G2S} = 4 V, I_D = 100 µA
Gate2 to source cutoff voltage	$V_{G2S(off)}$	0.5	0.7	1.0	V	V_{DS} = 5 V, V_{G1S} = 5 V, I_D = 100 µA
Drain current	$I_{D(op)}$	13	17	21	mA	V_{DS} = 5 V, V_{G1} = 5 V V_{G2S} = 4 V, R_G = 100 kΩ
Forward transfer admittance	$\|y_{fs}\|$	21	26	32	mS	V_{DS} = 5 V, V_{G1} = 5 V, V_{G2S} = 4 V R_G = 100 kΩ, f = 1 kHz
Input capacitance	Ciss	1.4	1.8	2.2	pF	V_{DS} = 5 V, V_{G1} = 5 V
Output capacitance	Coss	1.0	1.4	1.8	pF	V_{G2S} =4 V, R_G = 100 kΩ
Reverse transfer capacitance	Crss	—	0.02	0.04	pF	f = 1 MHz
Power gain	PG	16	21	—	dB	V_{DS} = V_{G1} = 5 V, V_{G2S} = 4 V R_G = 100 kΩ, f = 900 MHz Zi = S11*, Zo = S22* (:PG)
Noise figure	NF	—	1.7	2.5	dB	Zi = S11opt (:NF)

The below specification are applicable for VHF unit (FET2)

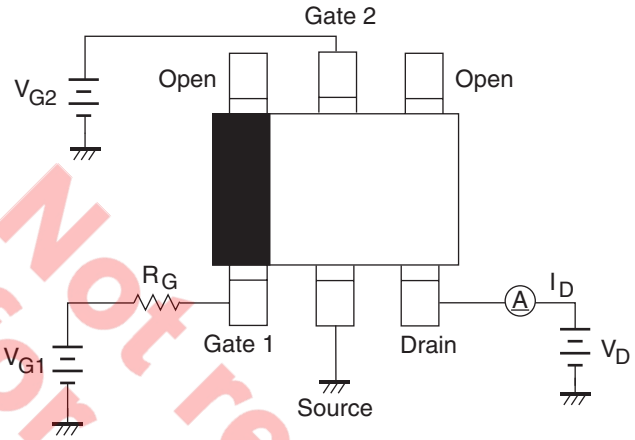
(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	6	—	—	V	I_D = 200 µA, V_{G1S} = V_{G2S} = 0
Gate1 to source breakdown voltage	$V_{(BR)G1SS}$	+6	—	—	V	I_{G1} = +10 µA, V_{G2S} = V_{DS} = 0
Gate2 to source breakdown voltage	$V_{(BR)G2SS}$	+6	—	—	V	I_{G2} = +10 µA, V_{G1S} = V_{DS} = 0
Gate1 to source cutoff current	I_{G1SS}	—	—	+100	nA	V_{G1S} = +5 V, V_{G2S} = V_{DS} = 0
Gate2 to source cutoff current	I_{G2SS}	—	—	+100	nA	V_{G2S} = +5 V, V_{G1S} = V_{DS} = 0
Gate1 to source cutoff voltage	$V_{G1S(off)}$	0.5	0.75	1.0	V	V_{DS} = 5 V, V_{G2S} = 4 V, I_D = 100 µA
Gate2 to source cutoff voltage	$V_{G2S(off)}$	0.5	0.75	1.0	V	V_{DS} = 5 V, V_{G1S} = 5 V, I_D = 100 µA
Drain current	$I_{D(op)}$	16	20	24	mA	V_{DS} = 5 V, V_{G1} = 5 V, V_{G2S} = 4 V R_G = 100 kΩ
Forward transfer admittance	$\|y_{fs}\|$	27	32	38	mS	V_{DS} = 5 V, V_{G1} = 5 V, V_{G2S} =4 V R_G = 100 kΩ, f = 1 kHz
Input capacitance	Ciss	2.3	2.7	3.1	pF	V_{DS} = 5 V, V_{G1} = 5 V
Output capacitance	Coss	1.4	1.8	2.2	pF	V_{G2S} =4 V, R_G = 100 kΩ
Reverse transfer capacitance	Crss	—	0.03	0.05	pF	f = 1 MHz
Power gain	PG	24	29	—	dB	V_{DS} = V_{G1} = 5 V, V_{G2S} = 4 V
Noise figure	NF	—	1.2	1.7	dB	R_G = 100 kΩ, f = 200 MHz

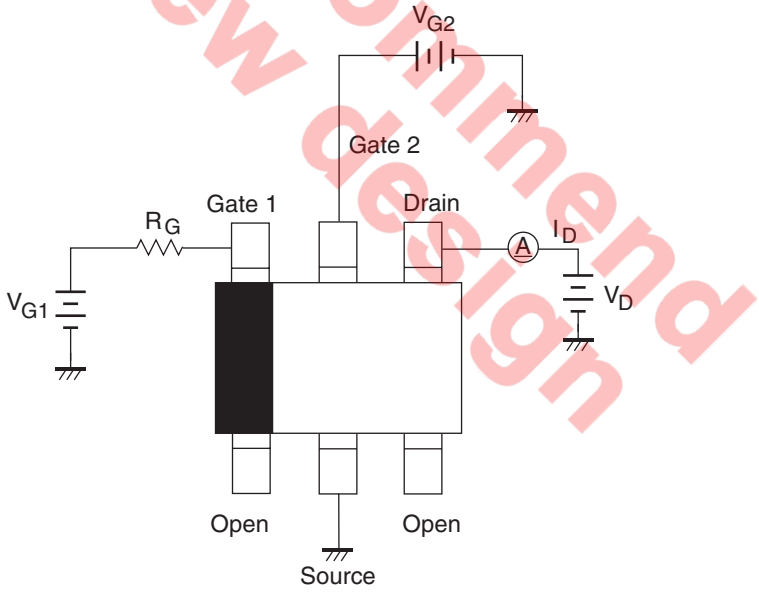
Test Circuits

• **DC Biasing Circuit for Operating Characteristic Items** ($I_{D(op)}$, |yfs|, Ciss, Coss, Crss, NF, PG)

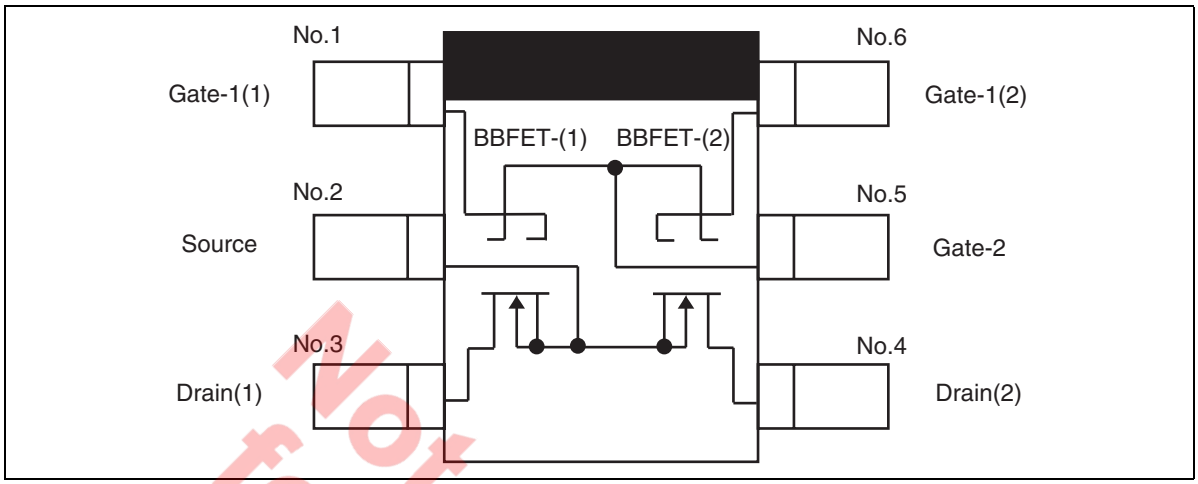
• Measurment of FET1



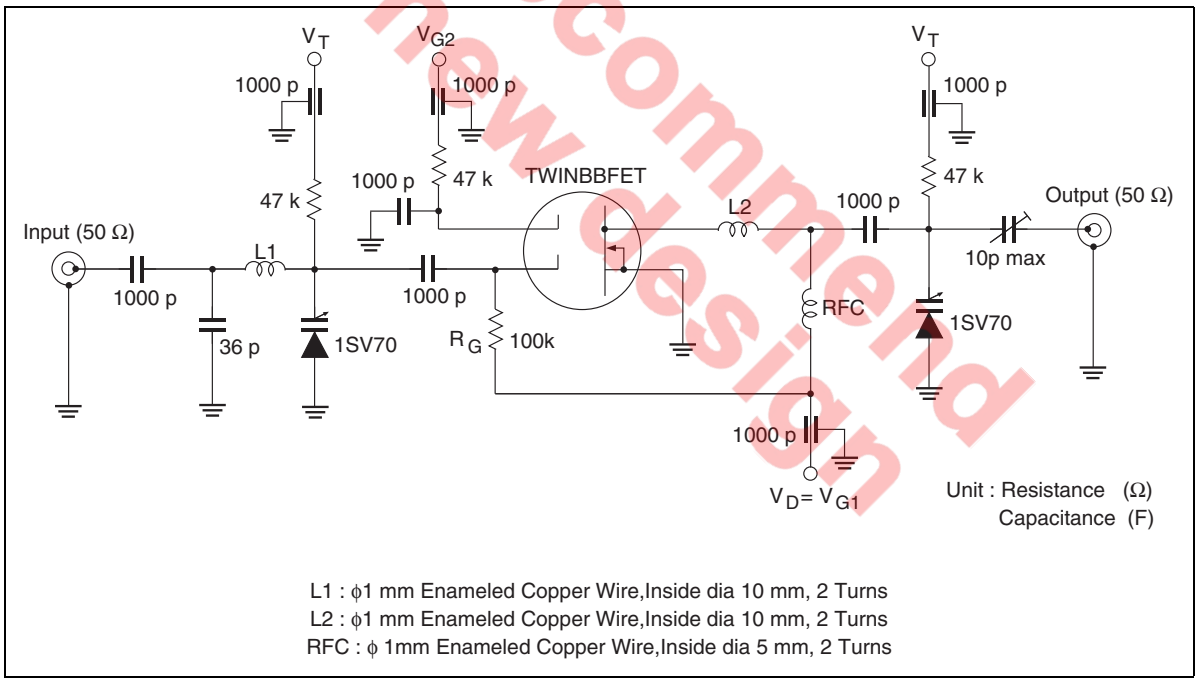
• Measurment of FET2



• **Equivalent Circuit**

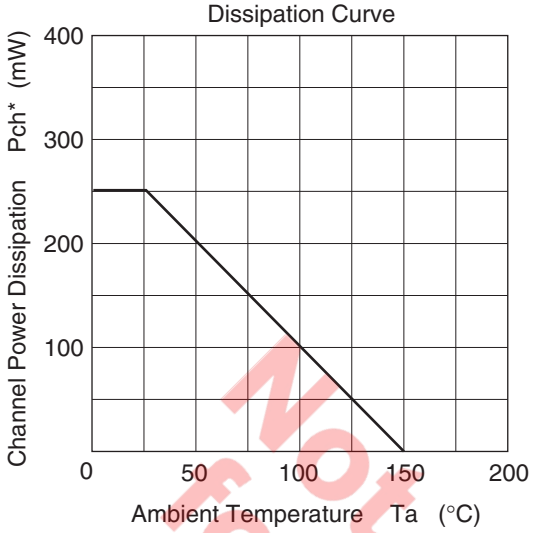


• **200 MHz Power Gain, Noise Figure Test Circuit**



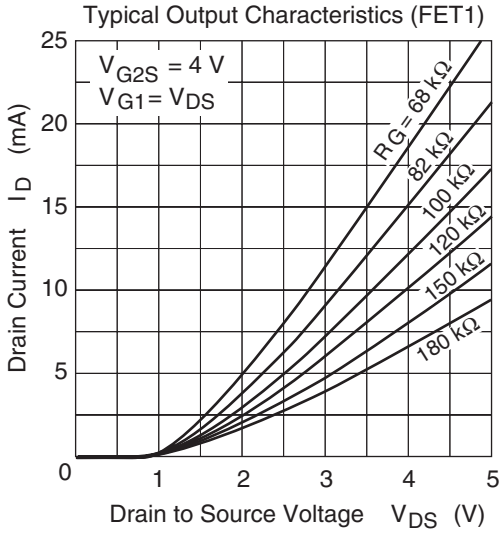
L1 : ϕ1 mm Enameled Copper Wire,Inside dia 10 mm, 2 Turns
L2 : ϕ1 mm Enameled Copper Wire,Inside dia 10 mm, 2 Turns
RFC : ϕ 1mm Enameled Copper Wire,Inside dia 5 mm, 2 Turns

Maximum Channel Power Dissipation Curve

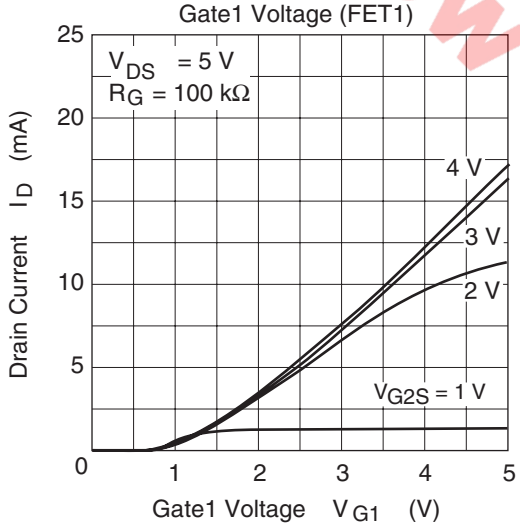


* Value on the glass epoxy board (50mm × 40mm × 1mm)

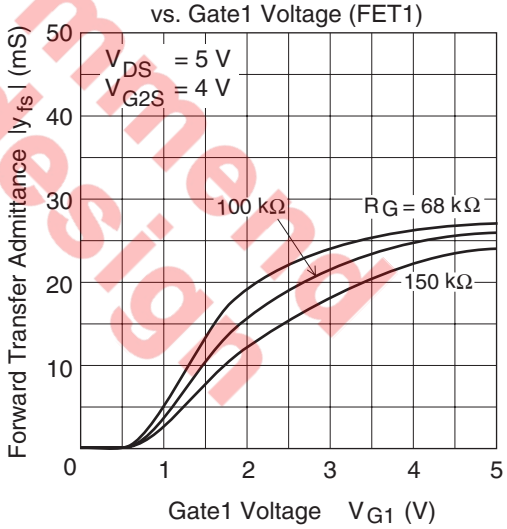
Typical Output Characteristics (FET1)

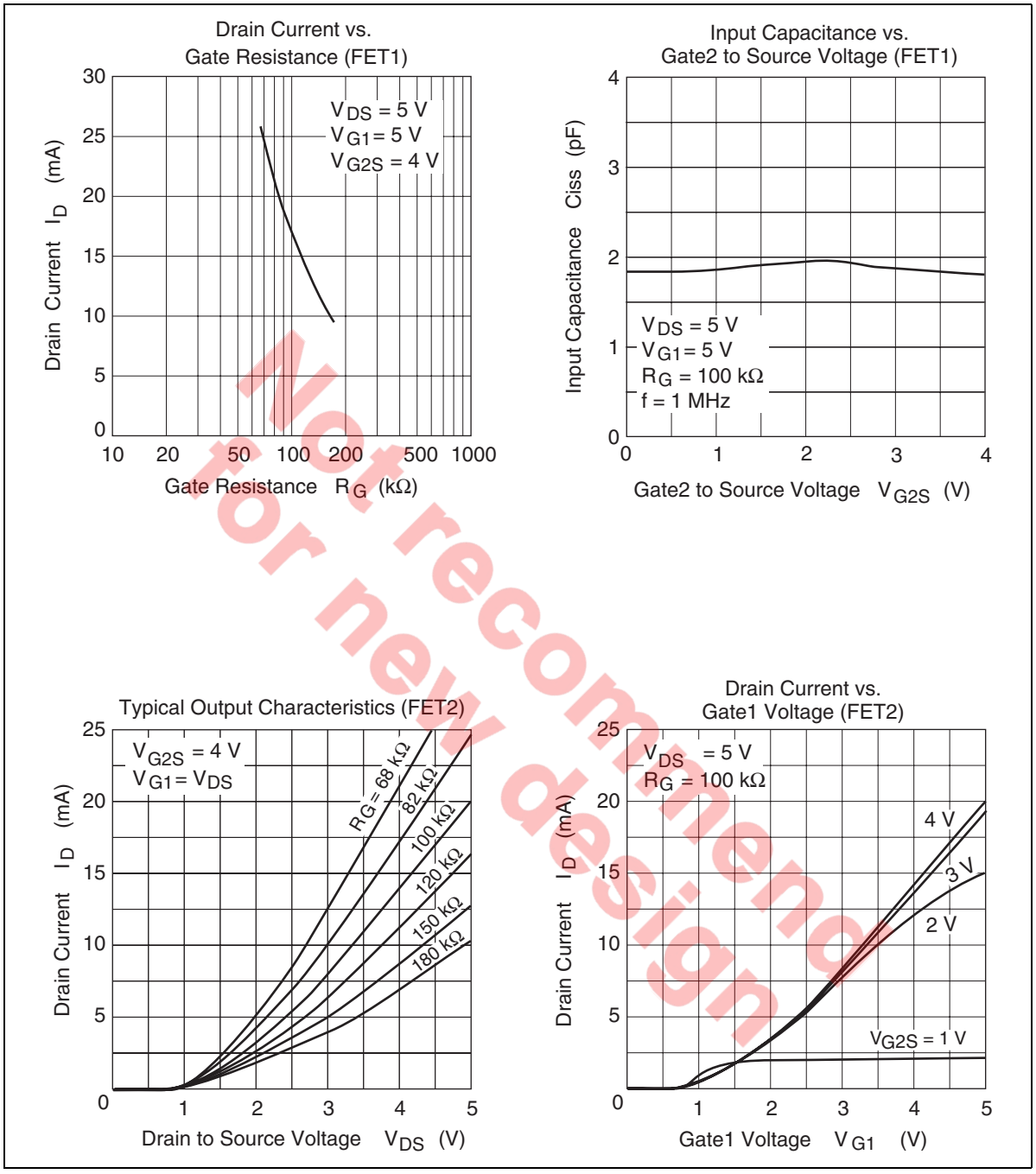


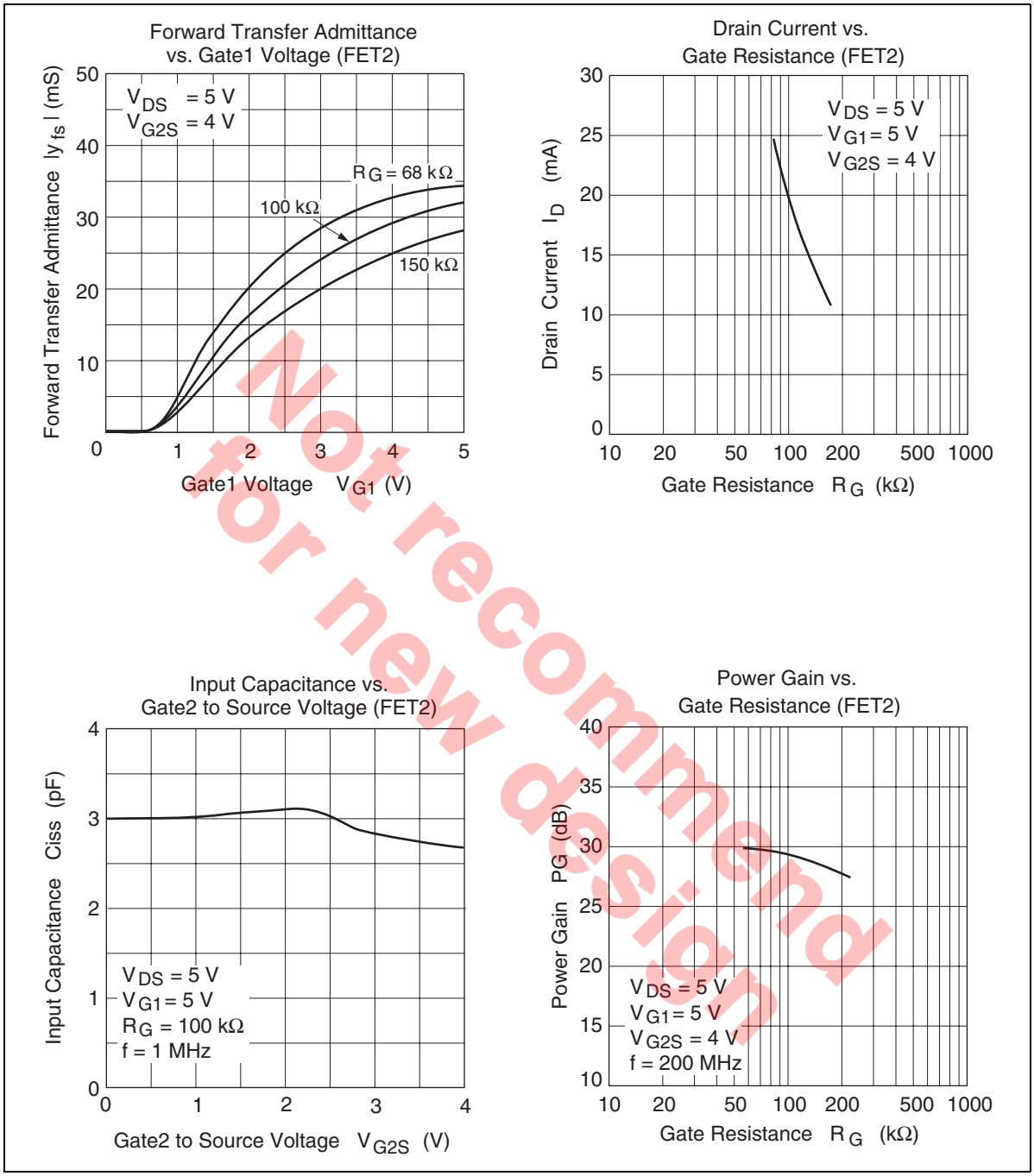
Drain Current vs. Gate1 Voltage (FET1)

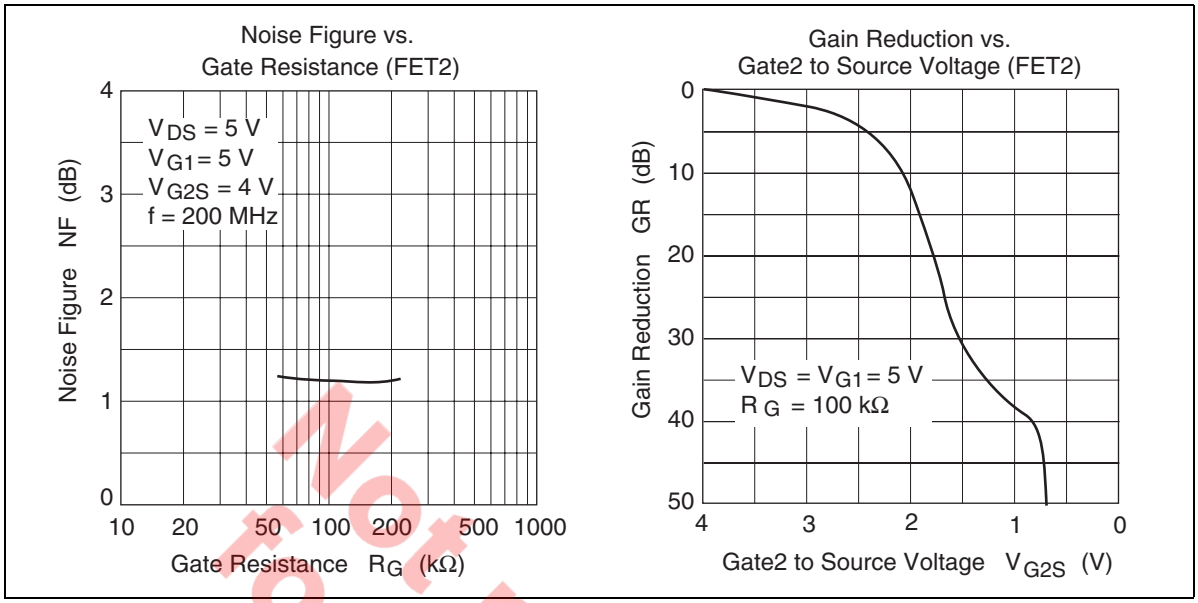


Forward Transfer Admittance vs. Gate1 Voltage (FET1)



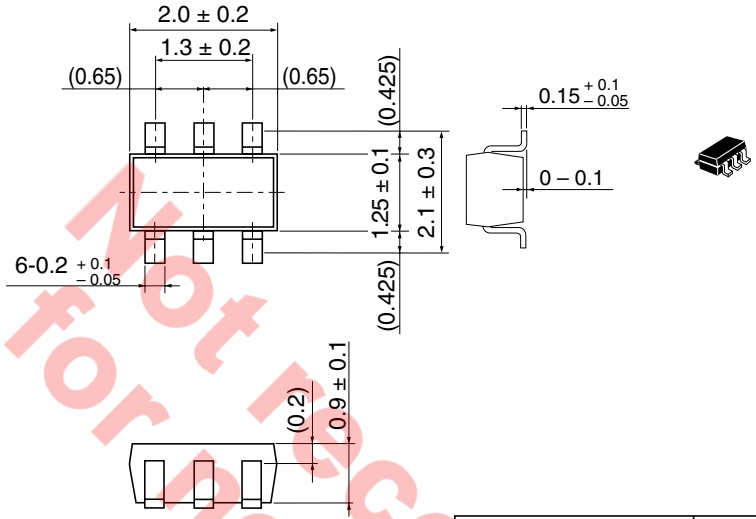






Package Dimensions

As of January, 2002
Unit: mm



Hitachi Code	CMPAK-6
JEDEC	—
JEITA	Conforms
Mass (reference value)	0.006 g

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