TBB1010

Twin Build in Biasing Circuit MOS FET IC
VHF/VHF RF Amplifier

ADE-208-1607B (Z)

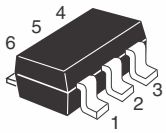
3rd. Edition
Feb. 2003

Features

- Small SMD package CMPAK-6 built in twin BBFET; To reduce using parts cost & PC board space.
- High |yfs|=29mS ×2
- Suitable for World Standard Tuner RF amplifier.
- Very useful for total tuner cost reduction.
- Withstanding to ESD; Build in ESD absorbing diode. Withstand up to 200 V at C = 200 pF, Rs = 0 conditions.
- Provide mini mold packages; CMPAK-6

Outline

CMPAK-6



1. Drain(1)
2. Source
3. Drain(2)
4. Gate-1(2)
5. Gate-2
6. Gate-1(1)

Notes:
1. Marking is “KM”.
2. TBB1010 is individual type number of HITACHI TWIN BBFET.

Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DS}	6	V
Gate1 to source voltage	V_{G1S}	+6 -0	V
Gate2 to source voltage	V_{G2S}	+6 -0	V
Drain current	I_D	30	mA
Channel power dissipation	Pch[*3]	250	mW
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

Notes: 3. Value on the glass epoxy board (50mm × 40mm × 1mm).

Electrical Characteristics

(Ta = 25°C)

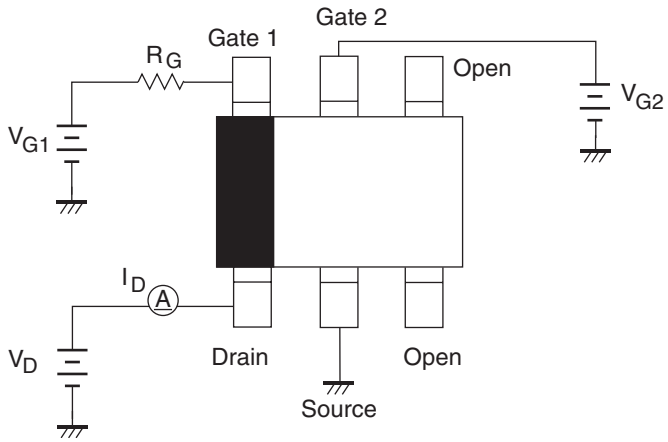
The below specification are applicable for FET1 and FET2 unit

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	6	—	—	V	I_D = 200 µA, V_{G1S} = V_{G2S} = 0
Gate1 to source breakdown voltage	$V_{(BR)G1SS}$	+6	—	—	V	I_{G1} = +10 µA, V_{G2S} = V_{DS} = 0
Gate2 to source breakdown voltage	$V_{(BR)G2SS}$	+6	—	—	V	I_{G2} = +10 µA, V_{G1S} = V_{DS} = 0
Gate1 to source cutoff current	I_{G1SS}	—	—	+100	nA	V_{G1S} = +5 V, V_{G2S} = V_{DS} = 0
Gate2 to source cutoff current	I_{G2SS}	—	—	+100	nA	V_{G2S} = +5 V, V_{G1S} = V_{DS} = 0
Gate1 to source cutoff voltage	$V_{G1S(off)}$	0.6	—	1.1	V	V_{DS} = 5 V, V_{G2S} = 4 V, I_D = 100 µA
Gate2 to source cutoff voltage	$V_{G2S(off)}$	0.6	—	1.1	V	V_{DS} = 5 V, V_{G1S} = 5 V, I_D = 100 µA
Drain current	$I_{D(op)}$	12	16	20	mA	V_{DS} = 5 V, V_{G1} = 5 V V_{G2S} = 4 V, R_G = 120 kΩ
Forward transfer admittance	$\|y_{fs}\|$	24	29	—	mS	V_{DS} = 5 V, V_{G1} = 5 V, V_{G2S} =4V R_G = 120 kΩ, f = 1 kHz
Input capacitance	Ciss	1.7	2.1	2.5	pF	V_{DS} = 5 V, V_{G1} = 5 V
Output capacitance	Coss	1.0	1.4	1.8	pF	V_{G2S} =4 V, R_G = 120 kΩ
Reverse transfer capacitance	Crss	—	0.03	0.05	pF	f = 1 MHz
Power gain	PG	25	30	—	dB	V_{DS} = V_{G1} = 5 V, V_{G2S} = 4 V
Noise figure	NF	—	1.1	1.8	dB	R_G = 120 kΩ, f = 200 MHz

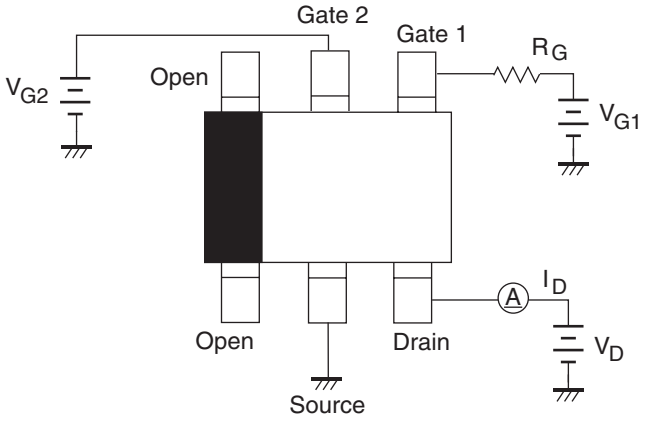
Test Circuits

- **DC Biasing Circuit for Operating Characteristic Items** ($I_{D(op)}$, |yfs|, Ciss, Coss, Crss, NF, PG)

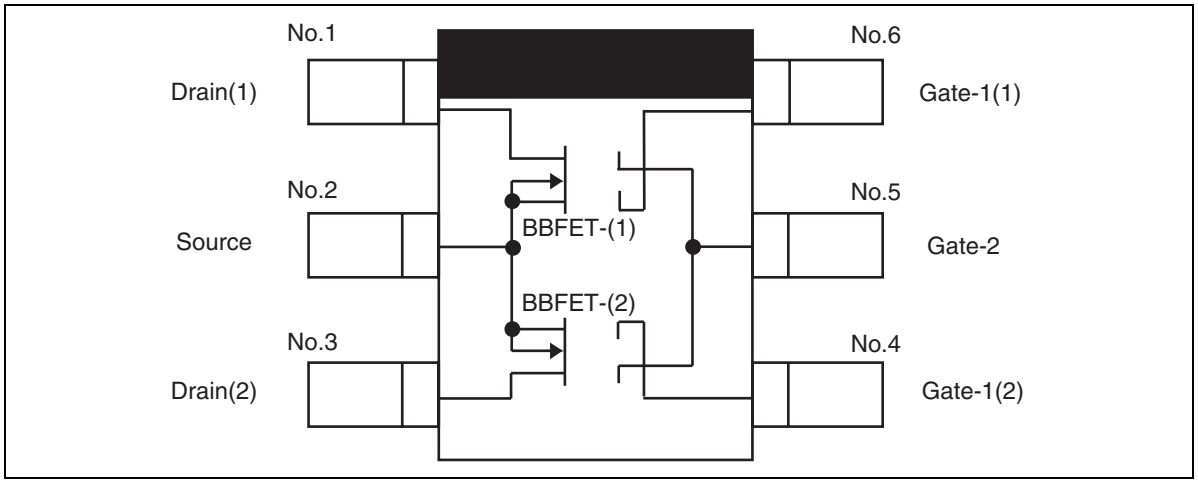
Measurment of FET1



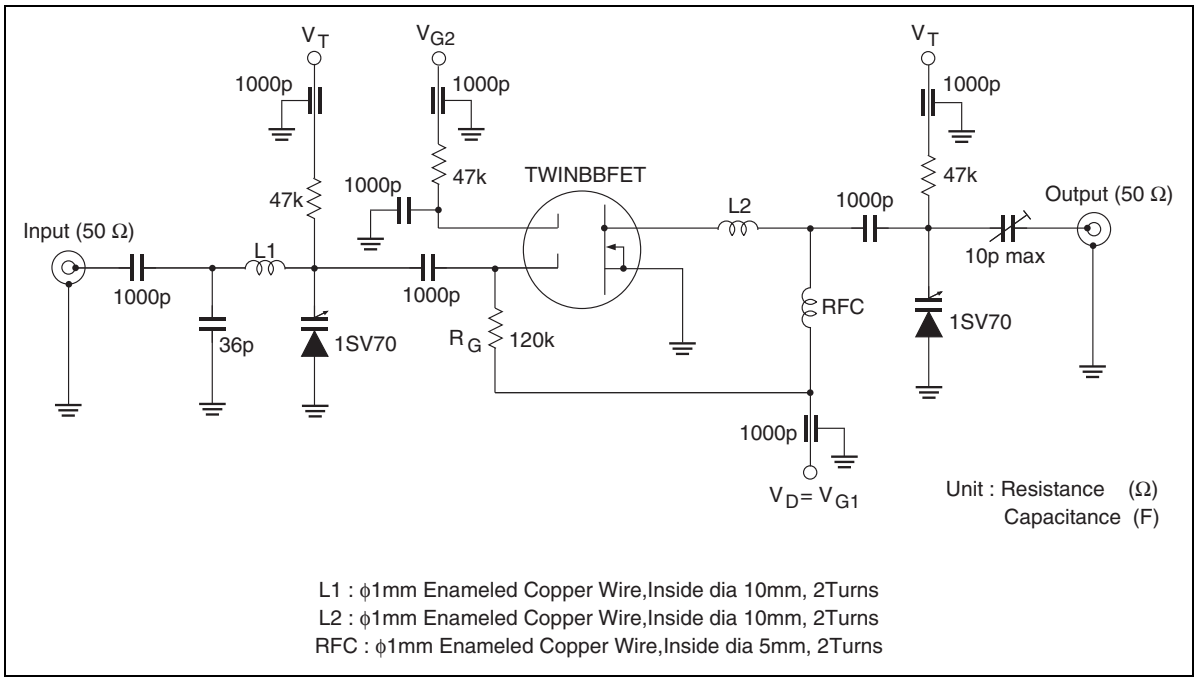
Measurment of FET2



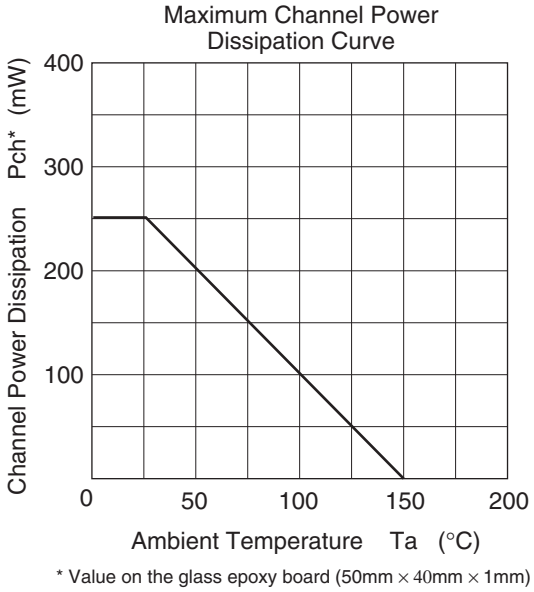
- **Equivalent Circuit**



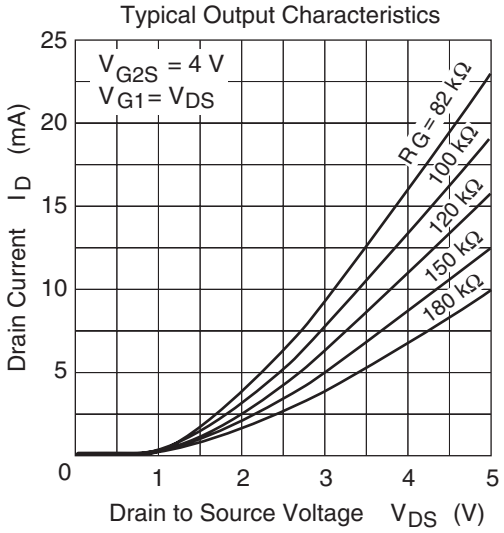
- **200 MHz Power Gain, Noise Figure Test Circuit**

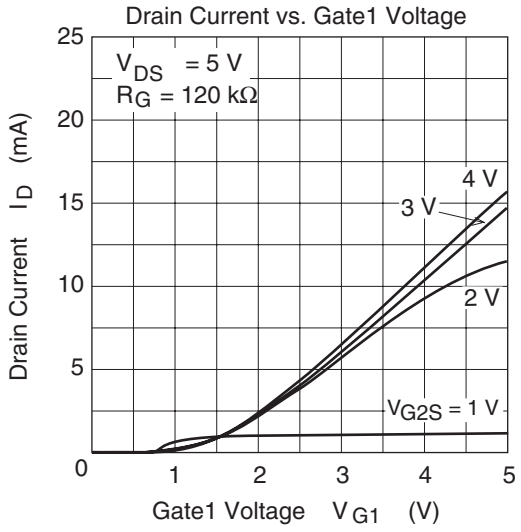


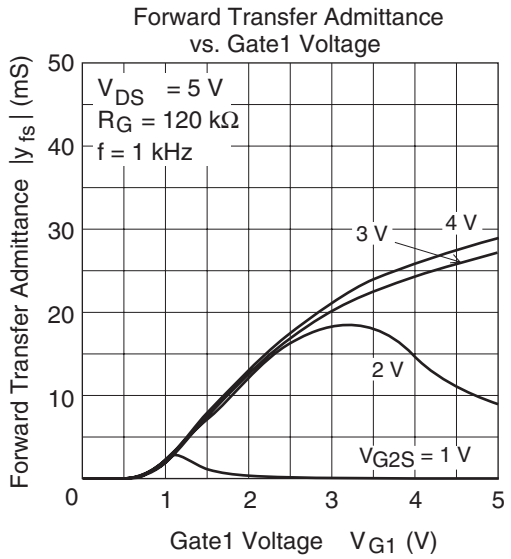
L1 : ϕ1mm Enameled Copper Wire,Inside dia 10mm, 2Turns
L2 : ϕ1mm Enameled Copper Wire,Inside dia 10mm, 2Turns
RFC : ϕ1mm Enameled Copper Wire,Inside dia 5mm, 2Turns



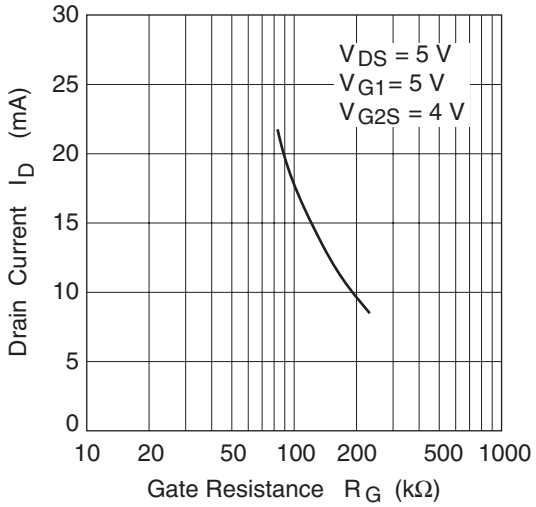
* Value on the glass epoxy board (50mm × 40mm × 1mm)



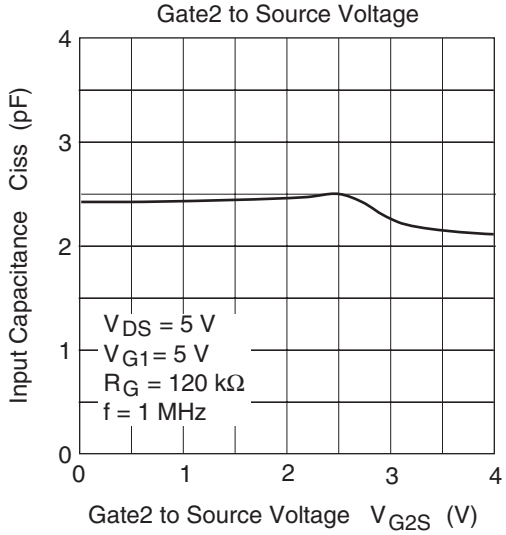




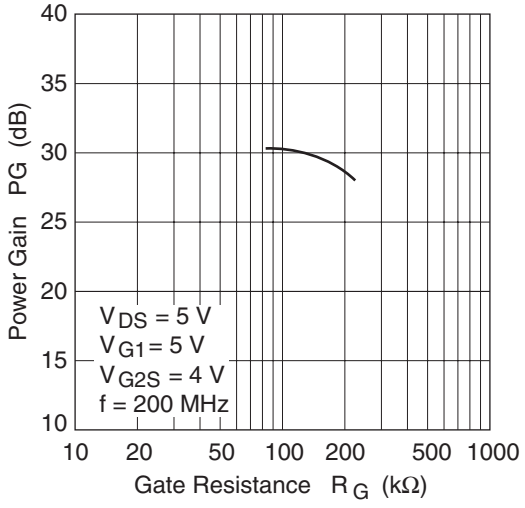
Drain Current vs. Gate Resistance



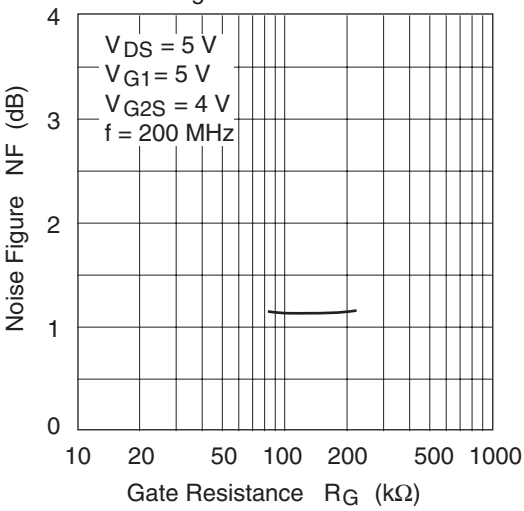
Input Capacitance vs. Gate2 to Source Voltage

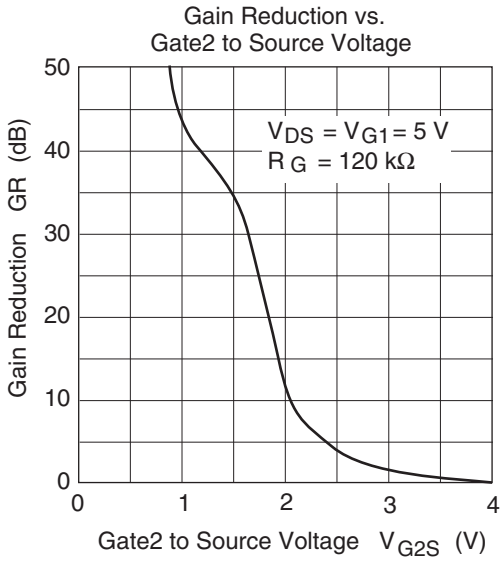


Power Gain vs. Gate Resistance



Noise Figure vs. Gate Resistance

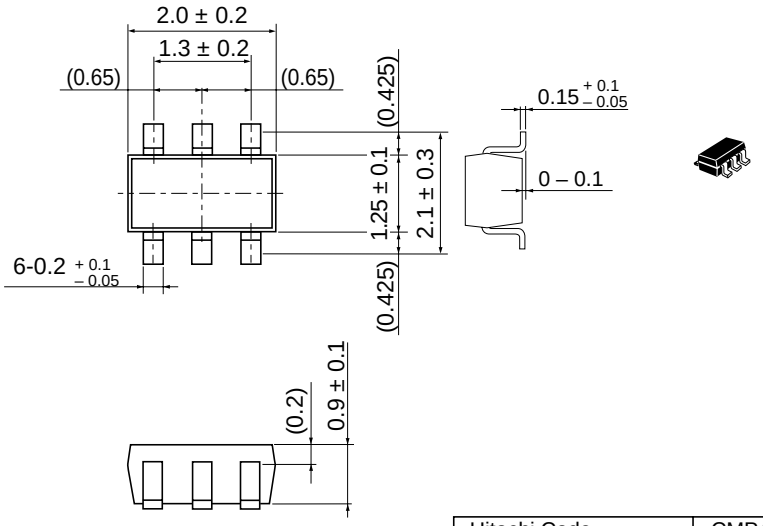



Gain Reduction vs.
Gate2 to Source Voltage
V_{DS} = V_{G1} = 5 V
R_G = 120 kΩ
Gain Reduction GR (dB)
50
40
30
20
10
0
0
1
2
3
4
Gate2 to Source Voltage V_{G2S} (V)

Package Dimensions

As of July, 2002

Unit: mm



Hitachi Code	CMPAK-6
JEDEC	—
JEITA	Conforms
Mass (reference value)	0.006 g

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