

TB2902HQ

TOSHIBA Bi-CMOS Digital Integrated Circuit Silicon Monolithic

TB2902HQ

Maximum Power 41 W BTL × 4-ch Audio Power IC

The TB2902HQ is 4ch audio amplifier for car audio application. This IC can generate high power, high quality sound output, POUT MAX = 41 W, using a pure complementary P-ch and N-ch DMOS output stage.

The built-in self diagnosis function which is included can be controlled via I²C BUS.

In addition, stand-by and mute function, and various Protection feature are included.

Features

- High power output : POUT MAX (1) = 41 W (typ.) (VCC = 14.4 V, f = 1 kHz, JEITA max, RL = 4 Ω) : POUT MAX (2) = 37 W (typ.) (VCC = 13.7 V, f = 1 kHz, JEITA max, RL = 4 Ω) : POUT MAX (3) = 70 W (typ.) (VCC = 14.4 V, f = 1 kHz, JEITA max, RL = 2 Ω) : POUT (1) = 27 W (typ.) (VCC = 14.4 V, f = 1 kHz, THD = 10%, RL = 4 Ω) : POUT (2) = 23 W (typ.) (VCC = 13.2 V, f = 1 kHz, THD = 10%, RL = 4 Ω) : POUT (3) = 45 W (typ.) (VCC = 14.4 V, f = 1 kHz, THD = 10%, RL = 2 Ω)
- Low distortion ratio: THD = 0.015% (typ.)

$$(V_{CC} = 13.2 \text{ V}, \text{ f} = 1 \text{ kHz}, P_{OUT} = 5 \text{ W}, \text{ R}_{L} = 4 \Omega)$$

- Low noise: $V_{NO} = 90 \ \mu Vrms$ (typ.)
 - $(V_{CC} = 13.2 \text{ V}, \text{ Rg} = 0 \Omega, \text{ BW} = 20 \text{ Hz to } 20 \text{ kHz}, \text{ RL} = 4 \Omega)$
- Built in stand by & muting function: controlled via I²C Bus (pin 16)
- Built in clipping detection (pin 4)
- Built in I²C Bus for stand-by, mute, voltage gain control, self diagnosis: Output short detection, offset detection, tweeter or speaker open detection (pin 22 and 25)
- Built-in various protection circuits (Note 1, Note 2) Thermal shut down, over-voltage, out to GND, out to V_{CC}, out to out short circuit
- Operating supply voltage: $V_{CC (opr)} = 9$ to $18 \text{ V} (R_L = 4 \Omega)$



- Note 1: Install the product correctly. Otherwise, it may result in break down, damage and/or degradation to the product or equipment.
- Note 2: These protection functions are intended to avoid some output short circuits or other abnormal conditions temporarily. These protect functions do not warrant to prevent the IC from being damaged.

- In case of the product would be operated with exceeded guaranteed operating ranges, these protection features may not operate and some output short circuits may result in the IC being damaged.



Weight: 7.7 g (typ.)



Block Diagram



Some of the functional blocks, circuits, or constants labels in the block diagram may have been omitted or simplified for clarity.

Caution and Application Information (description is made referring only on the single channel.)

1. Voltage Gain Adjustment

This IC has no NF (negative feedback) Pins. Therefore, the voltage gain can not be adjusted (except by software). However, this feature makes possible space and cost saving.



Figure 1 Block Diagram

The amplifier gain, $G_V = 26dB$, is calculated using the expression below: The voltage gain of amp.1: $G_{V1} = 0dB$ The voltage gain of amp.2A, B: $G_{V2} = 20dB$ The voltage gain of BTL connection: $G_V (BTL) = 6dB$ Therefore, the total voltage gain is decided by expression below. $G_V = G_{V1} + G_{V2} + G_V (BTL) = 0 + 20 + 6 = 26dB$

In the case when $G_V = 12dB$ selected via I²C, G_{V1} changed from 0dB to -14dB so that the output dynamic range is reduced as the output of Amp.1 is attenuated.

2. Muting Time Constant and Pop Noise Suppression when V_{CC} Rapidly Falls (pin 16)

The capacitor C4 at pin 16 is for muting time constant to suppress the pop noise. The larger value capacitor is used, the lower pop noise becomes but the longer the muting time from the mute ON command sent to muting an output sound actually. The charge period, which makes the delay of muting after "Mute On" command is written, is MIN=30msec, MAX=180msec in case of C4 (Pin 16) = 1 uF, Vcc=9 to 18V and Tj = -40 to 150 degrees condition.

As the V_{CC} is rapidly falling, the IC internal low voltage muting operates to eliminate the large pop noise basically.

If the effect of the internal low voltage muting is not enough in such a case, make this pin 16 set at low: 5 V and less by external circuit for more effective to suppress the pop noise.



Figure 2 Pin 16 Muting Circuit

In this case, this pin 16 has to be released from setting at low before going back to play mode. Additionally, the initial state after turning the amplifier "ON" or after turning stand by "off" by I^2C Bus is muted, so that it is necessary to send a "mute off" command to change from this condition to play mode.

Caution on the use of the muting function

The audio muting function is enabled when pin 16 is <u>not</u> set Low. While the time constant of the muting function is determined by the value of C4, the designer should take into account the possible generation of pop noise during switching operations. The pop noise which is generated when the power or muting function is turned ON/OFF will vary according to the time constant set by capacitor C4 value.

In the case when C4 value is large and the time constant is long, pop noise will be suppressed during the time interval when the voltage on pin 16 is falling.

However, the pop noise may become apparent as a "peaky" sound if the mute ON or OFF command is sent from μ Controller while the voltage at pin 16 is rising.

3. Clip Detection

The output clip detection terminal, pin 4, has an open collector output structure on chip as shown in Figure 3. In the case when the output waveform is clipping, the clip detection circuit is operated and the NPN Tr. is turned on.

It is possible to improve the audio output quality by controlling the volume and/or tone control circuits through a low pass filter (L.P.F) smoothing circuit as shown in Figure 3.

The sensitivity of the circuit to clipping level can be selected T.H.D. = 1% or 10% via I²C bus. In the event that this function is not used, pin4 should be left open circuit.



Figure 3 Clip Detection

4. External Component Values

Component	Recommended		Eff	ect	
Name	Value	Purpose	Lower than Recommended Value	Higher than Recommended Value	Notes
C1	0.22 μF	To eliminate DC	Cut-off frequency becomes higher	Cut-off frequency becomes lower	Pop noise is concerned with this capacitor.
		To reduce ripple			
C2	10 μF	To determine the time of turn on diag	Power ON/OFF time and turn ON diag cycle shorter	Power ON/OFF time and turn ON diag cycle longer	
C3	0.1 μF	To provide sufficient oscillation margin	Reduces noise and provides s	ufficient oscillation margin	
C4	1 μF	To reduce pop noise	Pop noise becomes larger Muting ON/OFF time is shorter	Pop noise becomes smaller Muting ON/OFF time is longer	
C5	3900 μF	Ripple filter	Power supply ripple filtering		

Note 3: In case of the recommended value not used.

5. Fast Mute Mode

This feature will normally be used to suppress pop noise resulting from V_{CC} transients during engine cranking condition.

The fast mute mode can be entered on receipt of a command via I²C bus.

Using the IB2 register and setting to 'one' the bit D6, it is possible to generate a fast I^2C mute command. If a fast mute command is received, this IC will operate and will discharge the capacitor C4 at pin16.

Therefore the Pop sound will be reduced compared to the condition when Fast Mute is not used in the engine cranking condition.

6. Explanation for Self Diagnosis Via I²C

(1) Bus map

[Slave Address]

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Details	Hex
							0	Write Mode	
							1	Read Mode	
1	1	0	1	1	0	0	_		D8H

[WRITE]

• Sub address

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Details	Hex	
0								Page Mode (auto increment) OFF		
1								Page Mode (auto increment) ON		
_	0	0	0	0	0	0	1	Control Byte1	01H	
—	0	0	0	0	0	1	0	Control Byte2	02H	

• Control byte1 (01H)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Function
0	0	0	0	0	0	0	1	Clip Det 1% to 10% change
0	0	0	0	0	0	1	0	R-ch Muting off (play)
0	0	0	0	0	1	0	0	Fch Muting off (play)
0	0	0	0	1	0	0	0	R-ch Gain 26dB to 12dB
0	0	0	1	0	0	0	0	Fch Gain 26dB to 12dB
0	0	1	0	0	0	0	0	Offset Det Enable
0	1	0	0	0	0	0	0	Diag Cycle Enable
1	_							Turn-on Select (normal/repeatedly)

• Control byte2 (02H)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Function
0	0	0	0	0	0	0	1	R-ch Iccq become Lower
0	0	0	0	0	0	1	0	Fch Iccq become Lower
0	0	0	0	0	1	0	0	Current Detection Enable
0	0	0	0	1	0	0	0	Line Drive Diag
0	0	0	1	0	0	0	0	Stand By OFF (play)
0	0	1	0	0	0	0	0	Clip Det Pin change to Offset Det
—	1		—	—	—	_	—	Fast mute ON/OFF
1	0	0	0	0	0	0	0	Current Detection. Level change from 500 mA (max) to 300 mA (max)

Note 4: Self mute circuit is included on chip and is in independent from I^2C bus stage. Self mute operating voltage is $V_{CC} = 7.8 V$

Note 5: Auto Increment is available.

If control byte 1 is chosen by sub address, it is not necessary to send byte 2 in cases when both byte 1 and 2 are to be written.

Ex) In case of sub address = byte1 chosen: Sub address byte 1 → byte 1 writing → Sub address byte 2 → byte 2 writing: available Sub address byte 1 → byte 1 writing ------- → byte 2 writing: available

[READ]

Byte 1

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	At "Bit = 1" Condition
0	0	0	0	0	0	0	1	Ch1 Short to GND
0	0	0	0	0	0	1	0	Ch1 Short to V _{CC}
0	0	0	0	0	1	0	0	Ch1 Open load or Offset Detected
0	0	0	0	1	0	0	0	Ch1 Short load
0	0	0	1	0	0	0	0	Ch1 Diagnosis condition (bit = 1: permanent, 0: turn-on)
0	0	1	0	0	0	0	0	Ch1 Current Detection (at IB2 D2 = 1 = enable only) (IB2 $D7 = 0$; bit = 1; <250 mA 0 ; >500 mA)
0	0	I	0	0	0	0	0	(IB2 - D7 = 0. bit = 1. <250 mA, 0. >300 mA) (IB2 - D7 = 1: bit = 1: <100 mA, 0: >300 mA)
0	1	0	0	0	0	0	0	Bit = 1: Diag. Cycle terminated, 0: Not terminated
1	0	0	0	0	0	0	0	TSD Mute ON (thermal warning)

Byte 2

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	At "Bit = 1" Condition
0	0	0	0	0	0	0	1	Ch2 Short to GND
0	0	0	0	0	0	1	0	Ch2 Short to V _{CC}
0	0	0	0	0	1	0	0	Ch2 Open load or Offset Detected
0	0	0	0	1	0	0	0	Ch2 Short load
0	0	0	1	0	0	0	0	Ch2 Diagnosis condition (bit = 1: permanent, 0: turn-on)
0	0	1	0	0	0	0	0	Ch2 Current Detection (at IB2 D2 = 1 = enable only) (IB2 - D7 = 0: bit = 1: <250 mA, 0: >500 mA) (IB2 - D7 = 1: bit = 1: <100 mA, 0: >300 mA)
0	1	0	0	0	0	0	0	Current sensor activated (D6 = 1)
1	0	0	0	0	0	0	_	Offset detection activated (D7 = 1)

Byte 3

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	At "Bit = 1" Condition
0	0	0	0	0	0	0	1	Ch3 Short to GND
0	0	0	0	0	0	1	0	Ch3 Short to V _{CC}
0	0	0	0	0	1	0	0	Ch3 Open load or Offset Detected
0	0	0	0	1	0	0	0	Ch3 Short load
0	0	0	1	0	0	0	0	Ch3 Diagnosis condition (bit = 1: permanent, 0: turn-on)
								Ch3 Current Detection (at IB2 D2 = 1 = enable only)
0	0	1	0	0	0	0	0	(IB2 – D7 = 0: bit = 1: <250 mA, 0: >500 mA)
								(IB2 - D7 = 1: bit = 1: <100 mA, 0: >300 mA)
_	1	_	_	_	_	_	_	Diagnotic status (= IB1 – D6 bit = 1: diag enable)
1	_			_	_	_		Stand-by status (= IB2 – D4 bit = 1: play)

Byte 4

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	At "Bit = 1" Condition
0	0	0	0	0	0	0	1	Ch4 Short to GND
0	0	0	0	0	0	1	0	Ch4 2 Short to VCC
0	0	0	0	0	1	0	0	Ch4 Open load or Offset Detected
0	0	0	0	1	0	0	0	Ch4 Short load
0	0	0	1	0	0	0	0	Ch4 Diagnosis condition (bit = 1: permanent, 0: turn-on)
0	0	1	0	0	0	0	0	Ch4 Current Detection (at IB2 D2 = 1 = enable only) (IB2 - D7 = 0: bit = 1: <250 mA, 0: >500 mA) (IB2 - D7 = 1: bit = 1: <100 mA, 0: >300 mA)
_	_	_		_		_	_	x
	_	_	_	_	_	_		x

Note 6: Short circuit protection can be operated channel by channel.

EX) If channel 1 output is shorted, channel 1 is protected but other channels are available.

Caution: sub address 0x15 (15H) is for our internal testing only. Do not apply for your using.

(2) Description for turn on diagnosis

This IC can determine whether the conditions listed below occur or not at turn ON:

-Short to GND -Short to VCC -Output to output short -Speaker open

As first "switch on", the write data is sent to "turn ON" the IC.

If the turn on diagnostic is activated at this time, the write data, with the diagnostic cycle byte: IB1 D6 set at 1, is sent at the same time

The result of self diagnosis can be obtained from the read data sent after the turn on diagnostic data permitted time, as below Figure:



Figure 4 Diagnosis Timing Chart



Figure 5 Number of Times Turn ON Diagnosis Timing Chart



B) Repetition mode



The turn ON diagnostic acquisition time is determined by the ripple filter capacitance C2 and the equivalent internal resistance Rr as below expression.

Acquisition time = $2 \times C2 \times Rr = 4400 \times C2$ (typ.)

Rr is fixed in internal circuit and it is not varied by the fluctuation of power supply V_{CC} voltage. C2 value determines the time from power ON (standby off) to the appearance of sound signal from output and the characteristic for ripple rejection ratio, too. So, take care with the decision on C2 value.

If the turn ON diagnosis is not used, in other words the diagnostic cycle defeat command is sent, the waveform of ripple terminal voltage will change but the time from turning on to the output signal appearance will not change as illustrated below in Figure 6.



Figure 6 Turn on Diagnosis Timing Chart when Turn on diagnosis not used.

(3) Description for permanent diagnosis

This IC can provide permanent diagnosis under the following conditions, whether they occur before or after turning ON:

-Short to GND -Short to VCC -Output to output short circuit -Output offset detection -Current detection for tweeter open

This permanent diagnosis is available not only with the diagnostic cycle byte: IB1 D6 set at 1 but also when set at 0.

Additionally, the signal can be obtained by entering just a read command. It is not necessary to write the data.

With permanent diagnosis fault detection, the first read data after fault removal will still show a Fault. Therefore, it is necessary to obtain 3 or more readings in order to prevent a miss judgment. For example, the speaker sometimes makes a large counter electro motive force which this IC could recognize as a fault event.

Additionally, this permanent diagnosis is automatically on after the turning on diagnosis operation finished therefore there is no need to send the extra command.



Figure 7 Permanent Diagnosis Timing Chart for Each Short Detection

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Regarding operation of the output offset detection, The software always detects the output offset but the result is not latched internally as shown in the Figure below:

Figure 8 Software Output Offset Detection Timing Chart

However, this detection has to be performed in real time: Time voltage offset (Tvos) between read and next read is set at Tvos = 1/the lowest signal frequency ,or more. For instance Tvos > 50 ms if the lowest output signal frequency is 20 Hz, and to obtain 2 or more readings in order not to make a misjudgment

Additionaly, the threshold level is designed at +/–2 V.

The output from the terminal of pin 4 can be changed from clip detector to offset detector output by sending the write command via I^2C .

If the L.P.F output voltage has become a half of pull up voltage for a while, firstly the signal output volume goes down (cliping detector function). After that, it can be judged that the abnormal output offset has occurred, if the L.P.F. output voltage does not rise above half of pull up voltage.



Figure 9 Hardware Output Offset Detection

When the current detector for Tweeter open check is used, it is necessary to take care as below:

- Need to input the pulse or signal which is the higher out of audience frequency for example $f=20\ kHz$

- The pulse or signal input timing has to be after mute off (play mode)
- At least, the read timing has to be after 1 cycle of input pulse or signal and more, the recommadation cycles are 3 cycle and more if can.
- The level of input pulse or signal is more than the detection threshold level 300 mA or 500 mA. For instance, if the tweeter impedance is 20 Ω at f = 20 kHz which is same as input signal frequency, the output minimum voltage is: Vout = 500 mA \times 20 Ω = 10 V and more.



Figure 10 Tweeter Open Detection Timing Chart

Finally, if DB1 D7 = 1 then the temperature of IC chip is close to the thermal shutdown point. This warning bit becomes high, about 10 degrees below the temperature at which the overtemperature protection operates.

- Note 7: Timing charts may have been simplified for ease of reading.
- Note 8: Please arrange to read all self-diagnosis functions twice or more and apply judgment in order to avoid false triggering.

<Since the first diagnostic result has low confidence, please diagnose 2 times or more.>

(4) Multiple faults

The self diagnosis shows as below tables when there are multi fault connection for the audio outputs.

At Turning ON:

	S.GND (out+)	S.GND (out-)	S.V _{CC}	Out to Out. S	Open L
S.GND (out+)	S.GND	S.GND	S.Load	S.GND	S.GND + No open
S.GND (out-)		S.GND	S.Load	S.GND	S.GND + No open
S.V _{CC}			S.V _{CC} + S.Load	S.V _{CC} + S.Load	S.V _{CC} + S.Load + open or No open
Out to Out.S				S.Load	S.Load + No open
Open L					Open

At Permanent:

	S.GND (out+)	S.GND (out-)	S.V _{CC}	Out to Out. S	Open L
S.GND (out+)	S.GND	S.GND	S.GND or S.V _{CC} (Note 10)	S.GND	S.GND (Note 9)
S.GND (out-)		S.GND	S.GND or S.V _{CC} (Note 10)	S.GND	S.GND (Note 9)
S.V _{CC}			S.V _{CC}	S.V _{CC}	S.V _{CC} (Note 9)
Out to Out.S				S.Load + S.GND	N/A
Open L					Normal

Note 9: If the DC offset detection mode is ON, the information which the DC offset is appeared is added.

Note10: The chance which they can read this exact information is only one time although in case of other diagnosis, the more times sending read command, the higher the confidence of the result.

For example,

- a) ch1+ is connected to GND
- b) ch1– is connected to VCC
- c) They can read or get the "Short to GND" information when the uP send the Read command.
- d) Next, however, they can not get the "Short to GND" or "Short to V_{CC} " information when the uP send the Read command again.

Note 11: Please arrange to read all self-diagnosis functions twice or more and apply judgment in order to avoid false triggering.

(5) Explanation of I²C bus commands

Below the "ADDRESS BYTE", presently the address byte is fixed at 216 dec = D8hex = 101100xbin.

- /	٩d	d	ress	Se	lect	ion	is	D8	hexa	a:
-----	----	---	------	----	------	-----	----	----	------	----

A7	Address bit	1
A6	Address bit	1
A5	Address bit	0
A4	Address bit	1
A3	Address bit	1
A2	Address bit	0
A1	Address bit	0
A0 (R/W)	Read/Write bit	Х

X: 0 = Write instruction to device; 1 = Read instruction to device

- If R/W = 0, the Up Sends Two Instruction Bytes, IB1 and IB2:

IB1 Instruction Byte:

Bit	
D7	Turn-on diag timing
	Normal (D7 = 1)
	Repeat (D7 = 0)
D6	Diagnostic cycle enable (D6 = 1)
	Diagnostic cycle defeat (D6 = 0)
D5	Offset Detection enable (D5 = 1)
	Offset Detection defeat (D5 = 0)
D4	Front Channel
	Gain = 26dB (D4 = 0)
	Gain = 12dB (D4 = 1)
D3	Rear Channel
	Gain = 26dB (D3 = 0)
	Gain = 12dB (D3 = 1)
D2	Mute front channels $(D2 = 0)$
	Unmute front channels (D2 = 1)
D1	Mute rear channels $(D1 = 0)$
	Unmute rear channels (D1 = 1)
D0	CD 1% (D0 = 0)
	CD 10% (D0 = 1)

IB2 Instruction Byte:

Bit	
D7	Current Det 500 mA (max) (D7 = 0)
	Current Det 300 mA (max) (D7 = 1)
D6	Fast mute on $(D6 = 1)$ off $(D6 = 0)$
D5	Pin4 Clip Detection (D5 = 0)
	Pin4 Offset Detection (D5 = 1)
D4	Std-by on-PA not working (D4 = 0)
	Std-by off-PA working (D4 = 1)
D3	Amplifier mode diagnostic (D3 = 0)
	Line driver mode diagnostic (D3 = 1)
D2	Current Det. diag enabled (D2 = 1)
	Current Det. diag defeat $(D2 = 0)$
D1	Front Channels
	Work standard mode (D1 = 0)
	Work Low Iccq mode (D1 = 1)
D0	Rear Channels
	Work standard mode (D1 = 0)
	Work Low Iccq mode (D1 = 1)

- If R/W = 1, the Power Amplifier Sends Four Diagnostics Bytes, DB1, DB2, DB3 and DB4: DB1 Diagnostic Byte:

Bit							
D7	Thermal warning active (D7 = 1)						
D6	Diag not actived or not terminated (D6 = 0)						
	Diag terminated (D6 = 1)						
D5	Channel 1 current detection						
	Output peak current < 250 mA (IB2 – D7 = 0) – open load (D5 = 1)						
	Output peak current < 100 mA (IB2 – D7 = 1) – open load (D5 = 1)						
	Output peak current $> 500 \text{ mA} (IB2 - D7 = 0) - \text{normal load} (D5 = 0)$						
	Output peak current > 300 mA (IB2 – D7 = 1) – normal load (D5 = 0)						
D4	Channel 1						
	Turn-on diagnostic (D4 = 0)						
	Permanent diagnostic (D4 = 1)						
D3	Channel 1						
	Normal load (D3 = 0)						
	Short load (D3 = 1)						
D2	Channel 1						
	Turn-on diag: No open load (D2 = 0) Open load detected (D2 = 1)						
	Offset diag: No output offset (D2 = 0) Output offset detected (D2 = 1)						
D1	Channel 1						
	No short to V_{CC} (D1 = 0)						
	Short to V_{CC} (D1 = 1)						
D0	Channel 1						
	No short to GND (D0 = 0)						
	Short to GND (D0 = 1)						

DB2 Diagnostic Byte:

Bit							
D7	Offset detection not activated (D7 = 0)						
	Offset detection activated (D7 = 1)						
D6	Current sensor not activated (D6 = 0)						
	Current sensor activated (D6 = 1)						
D5	Channel 2 current detection						
	Output peak current < 250 mA (IB2 – D7 = 0) – open load (D5 = 1)						
	Output peak current < 100 mA (IB2 – D7 = 1) – open load (D5 = 1)						
	Output peak current $> 500 \text{ mA} (IB2 - D7 = 0) - \text{normal load} (D5 = 0)$						
	Output peak current > 300 mA (IB2 – D7 = 1) – normal load (D5 = 0)						
D4	Channel 2						
	Turn-on diagnostic (D4 = 0)						
	Permanent diagnostic (D4 = 1)						
D3	Channel 2						
	Normal load (D3 = 0)						
	Short load (D3 = 1)						
D2	Channel 2						
	Turn-on diag: No open load $(D2 = 0)$ Open load detected $(D2 = 1)$						
	Offset diag: No output offset (D2 = 0) Output offset detected (D2 = 1)						
D1	Channel 2						
	No short to V_{CC} (D1 = 0)						
	Short to V_{CC} (D1 = 1)						
D0	Channel 2						
	No short to $GND (D0 = 0)$						
	Short to GND (D0 = 1)						

Note 12: DBx (D5) is effective only at the time of "Current detection enable".

DB3 Diagnostic Byte:

Bit							
D7	Stand-by status (= IB2 – D4)						
D6	Diagnostic status (= IB1 – D6)						
D5	Channel 3 current detection						
	Output peak current < 250 mA (IB2 - D7 = 0) - open load (D5 = 1)						
	Output peak current < 100 mA (IB2 – D7 = 1) – open load (D5 = 1)						
	Output peak current $> 500 \text{ mA} (IB2 - D7 = 0) - \text{normal load} (D5 = 0)$						
	Output peak current > 300 mA (IB2 – D7 = 1) – normal load (D5 = 0)						
D4	Channel 3						
	Turn-on diagnostic (D4 = 0)						
	Permanent diagnostic (D4 = 1)						
D3	Channel 3						
	Normal load (D3 = 0)						
	Short load (D3 = 1)						
D2	Channel 3						
	Turn-on diag: No open load (D2 = 0) Open load detected (D2 = 1)						
	Offset diag: No output offset (D2 = 0) Output offset detected (D2 = 1)						
D1	Channel 3						
	No short to V_{CC} (D1 = 0)						
	Short to V_{CC} (D1 = 1)						
D0	Channel 3						
	No short to $GND (D0 = 0)$						
	Short to GND (D0 = 1)						

DB4 Diagnostic Byte:

Bit							
D7	X						
D6	x						
D5	Channel 4 current detection						
	Output peak current < 250 mA (IB2 - D7 = 0) - open load (D5 = 1)						
	Output peak current < 100 mA (IB2 - D7 = 1) - open load (D5 = 1)						
	Output peak current > 500 mA (IB2 - D7 = 0) - normal load (D5 = 0)						
	Output peak current > 300 mA (IB2 - D7 = 1) - normal load (D5 = 0)						
D4	Channel 4						
	Turn-on diagnostic (D4 = 0)						
	Permanent diagnostic (D4 = 1)						
D3	Channel 4						
	Normal load (D3 = 0)						
	Short load (D3 = 1)						
D2	Channel 4						
	Turn-on diag: No open load (D2 = 0) Open load detected (D2 = 1)						
	Offset diag: No output offset (D2 = 0) Output offset detected (D2 = 1)						
D1	Channel 4						
	No short to V_{CC} (D1 = 0)						
	Short to V_{CC} (D1 = 1)						
D0	Channel 4						
	No short to $GND (D0 = 0)$						
	Short to GND (D0 = 1)						

Note 13: DBx (D5) is effective only at the time of "Current detection enable".

7. Caution for use

Turn on diagnosis mode



The comparator detect the voltage between speaker both ends.

If that voltage is larger, this detector judges "output load open", while, if it is smaller, this detector judges the "short load".

But, in case of output shorted to VCC or shorted to GND condition, the voltage between speaker will be surely changed.

Therefore, this system can not present exact information, for example, "Short to VCC" and "Short load" are showed though output is shorted to Vcc but no short load.

In this case, the result as DET2 shall be dropped or ignored and DET1 is effective as DET1 is prior to DET2.

Permanent diagnosis mode

Please arrange to read all self-diagnosis functions twice or more and apply judgment in order to avoid false triggering. <Since the first diagnostic result has low confidence, please diagnose 2 times or more.>

Automatic turn on muting

The automatic turn on muting operates from when the turn on write command is sent, it is continued until the Pin 10 ripple pin voltage reaches to about 5.6V.

During this automatic turn on muting operation, output sound can not appear even if the mute off write command is sent because the internal muting circuit operates.

The automatic turn on muting operation period is MIN=0.1 sec, MAX=1.0 sec in case of C2 (Pin 10) = 10 uF, Vcc=9 to 18V and Tj = -40 to 150 degrees condition.

When the Turn on diagnosis is enable, the automatic muting period starts after Turn on diag cycle period. This period is in proportion to the value of the C2 so that the characteristic of C2 shall be had a care, for example, temperature, variation and so on.



Figure 11 Automatic Turn on Muting Timing Chart

Examples of Bytes Sequence

1 - Turn-On Diagnostic - Write Operation

Start Address byte with $D0 = 0$ ACK Sub-address $D0 = 1$ ACK IB with $D6 = 1$ ACK IB2 ACK	STOP
--	------

Note 14: Auto increment

2 - Turn-On Diagnostic - Read Operation

	Start Address byte with D0 = 1 ACK	DB1	ACK	DB2	ACK	DB3	ACK	DB4	ACK	STOP
--	------------------------------------	-----	-----	-----	-----	-----	-----	-----	-----	------

3a - Turn-On of the Power Amplifier with 26dB Gain, Mute On, Diagnostic Defeat.

Start	Address byte with $D0 = 0$	ACK	Sub-address D0 = 1	ACK	IB 1	ACK	IB2	ACK	STOP
				X0X0000X		XXX1X0XX			

Note 15: Auto increment

3b - Turn-Off of the Power Amplifier

Start	Address byte with $D0 = 0$	ACK	Sub-address D0 = 1	ACK	IB 1	ACK	IB2	ACK	STOP
				X0XXXXXX		XXX0XXXX			

Note 16: Auto increment

4 - Offset Detection Procedure Enable

Start	Address byte with $D0 = 0$	ACK	Sub-address D0 = 1	ACK	IB 1	ACK	IB2	ACK	STOP
					XX1XX11X		XXX1X0XX		

Note 17: Auto increment

5 - Offset detection procedure stop and reading operation (the results are valid only for the offset detection bits (D2 of the bytes DB1, DB2, DB3, DB4).

Start Address byte with D0 = 1 ACK DB1 ACK DB2 ACK DB3 ACK DB4 ACK STOP	Ρ
---	---

I²C Bus control format outline

The BUS control format of TB2902HQ is based on the Philips I^2C bus control format.

Data Transmission Format



Purchase of TOSHIBA I²C components conveys a license under the Philips I²C Patent Rights to use these components in an I²C system, provided that the system conforms to the I²C Standard Specification as defined by Philips.

TB2902HQ I²C Bus Transmission Format

(1) Write mode

In addition to usual transmission, it corresponds to continuation transmission and the auto increment mode as a transmission format. After a transmission end, in case data transmission is newly, it is necessary to open the term beyond 1 clock.

1) Continuation transmission

(An address to change is specified. At this time, MSB of a sub-address is set as 0.)



2) Auto increment

(Sub address are set to increment from N one by one. MSB of a sub-address is set as 1.)



(2) Read mode

The slave address became the read mode by changing the 8 Bit of the slave address from 0 to 1. The data output from TB2902HQ starts after the micro controller receives the ACK 1 bit which follows a slave address.

Stop condition are shown in the under the map.

The micro controller shall send the stop condition P after it sent the reversed Acknowledge (high) in case of the read mode finished.

The data transmission became not available condition if the micro controller intended to send the stop condition P expect for this procedure because this IC occupies the data bus until the micro controller send the start conditions again.

S	Slave ADD (R)	А	DATA1	А	DATA2	А	DATA3	А	DATA4	Ā	Ρ
send a DATA from microcontroller.											
	send a DATA	froi	n TB290)2H	Q.						

Maximum Ratings (Ta = 25°C)

Characteristics	Symbol	Rating	Unit	
Peak supply voltage (0.2 s)	V _{CC (surge)}	50	V	
DC supply voltage	V _{CC (DC)}	28	V	
Operation supply voltage	V _{CC (opr)}	18	V	
Output current (peak)	I _{O (peak)}	9	А	
Power dissipation	P _D 125 (Note 19)		W	
Operation temperature	T _{opr}	-40 to 85	°C	
Storage temperature	T _{stg}	-55 to 150	°C	

Note 19: Package thermal resistance θj -T = 1°C/W (typ.) (Ta = 25°C, with infinite heat sink)

The absolute maximum ratings of a semiconductor device are a set of specified parameter values, which must not be exceeded during operation, even for an instant. If any of these rating would be exceeded during operation, the device electrical characteristics may be irreparably altered and the reliability and lifetime of the device can no longer be guaranteed. Moreover, these operations with exceeded ratings may cause break down, damage and/or degradation to any other equipment. Applications using the device should be designed such that each maximum rating will never be exceeded in any operating conditions. Before using, creating and/or producing designs, refer to and comply with the precautions and conditions set forth in this documents.

Electrical Characteristics

(unless otherwise specified, V_{CC} = 13.2 V, f = 1 kHz, R_L = 4 Ω , Ta = 25°C)

Characteristics	Symbol	Test Circuit	Test Condition	Min	Тур.	Max	Unit	
Quiescent current	I _{CCQ} — V _{IN} = 0		$V_{IN} = 0$	_	200	300	mA	
	P _{OUT} MAX (1)	_	V _{CC} = 14.4 V, max POWER	_	41	_		
Output power	P _{OUT} MAX (2)	_	V _{CC} = 13.7 V, max POWER	—	37	—	w	
	P _{OUT} (1)	—	$V_{CC} = 14.4 \text{ V}, \text{ THD} = 10\%$	24	27	_		
	P _{OUT} (2)	—	THD = 10%	—	23	—		
	P _{OUT} MAX (3)	_	V _{CC} = 14.4 V, max POWER	_	70	_	W	
Output power (RL = 2 Ω)	P _{OUT} MAX (4)	_	V _{CC} = 13.7 V, max POWER	_	64	_		
	P _{OUT} (3)	_	V _{CC} = 14.4 V, THD = 10%	42	45	_		
	P _{OUT} (4)	_	THD = 10%	_	39	_		
	THD (1)	_	P _{OUT} = 5 W	_	0.015	0.1	0/	
Total harmonic distortion	THD (2)	_	Vo = 2 Vrms, G _V = 12dB	_	0.01	0.1	70	
	G _V (1)	_	V _{OUT} = 0.775 Vrms	25	26	27		
Voltage gain	G _V (2)	_	$V_{OUT} = 0.775 \text{ Vrms},$ $G_V = 12dB$	11	12	13	dB	
Voltage gain ratio	ΔG_V	_	V _{OUT} = 0.775 Vrms	-1	0	1	dB	
	Vno (1)	_	Rg = 0 Ω, DIN45405		100			
	Vno (2)	_	$R_g = 0 \Omega$, BW = 20 Hz to 20 kHz	_	90	200	\/rmo	
Output noise voitage	Vno (3)	_	$R_g = 0 \Omega$, BW = 20 Hz to 20 kHz $G_V = 12$ dB	_	30	50	μvims	
Ripple rejection ratio	R.R.	_	fripple = 100 Hz, R_g = 620 Ω Vrip = 0.775 Vrms	40	50		dB	
Cross talk	C.T.	_	$R_g = 620 \Omega$ V _{OUT} = 0.775 Vrms	_	65	_	dB	
Output offset voltage	VOFFSET	—	—	-150	0	150	mV	
Input resistance	RIN	—	—	_	90	_	kΩ	
Standby current	ISB	_	Stand-by condition by BUS	—	30	60	μΑ	
Ctond by 8 muto control voltage	VSM H		For operation, mute enable	7.0		V _{CC}	V	
Stand by a mule control voltage	VSM L	_	For mute, stand by OFF	0	—	5.0	v	
Mute attenuation	ATT M	_	Mute: ON V _{OUT} = 7.75 Vrms \rightarrow Mute: OFF	80	90	_	dB	
	CD (1)	_	Low (01H D = 0)		1	2.5		
Clip det THD level	CD (2)	—	High (01H D = 1)	5	10	15	%	

Note 20: ISB specification will be decided to after final evaluation on tolerance spls.

Diagnosis/Bus Specification

Characteristics	Test Condition	Min	Тур.	Max	Unit						
Turn on diagnosis (power amplifier mode)											
Short to GND det.	Under stand-by condition	_	_	1.2	V						
Short to V _{CC} det.		V _{CC} – 1.2	_		V						
Shorted load		_	_	0.5	Ω						
Open load		85	_		Ω						
Normal load		1.5	_	45	Ω						
Turn on diagnosis (line driver mode)											
Short to GND det.	Under stand-by condition	_	_	1.2	V						
Short to V _{CC} det.		V _{CC} – 1.2	—	—	V						
Shorted load		_	_	2	Ω						
Open load		330	_	_	Ω						
Normal load		6	_	180	Ω						
Permanent diagnosis (power amplifier a	and line driver mode)										
Short to GND det.	Power amplifier in mute or play	_	_	1.2	V						
Short to V _{CC} det.		V _{CC} – 1.2	—	—	V						
Shorted load	Power amp mode only	—	0.5		Ω						
Offset detection	Power amplifier in play (no signal)	_	+/-2		V						
Current detector threshold 1		250		500	mA						
Current detector threshold 2		100		300	mA						
I ² C bus interface											
Clock frequency			400		kHz						

Test Circuit



Components in the test circuits are only used to obtain and confirm the device characteristics. These components and circuits do not warrant to prevent the application equipment from malfunction or failure.

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Supply voltage V_{CC} (V)



Ambient temperature Ta (°C)

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Package Dimensions

HZIP25-P-1.00F

Unit: mm



Weight: 7.7 g (typ.)

About solderability, following conditions were confirmed

Solderability

(1) Use of Sn-63Pb solder Bath

- solder bath temperature = 230°C
- dipping time = 5 seconds
- \cdot the number of times = once
- use of R-type flux
- (2) Use of Sn-3.0Ag-0.5Cu solder Bath
 - solder bath temperature = 245°C
 - dipping time = 5 seconds
 - $\cdot \,$ the number of times = once
 - · use of R-type flux

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 product.