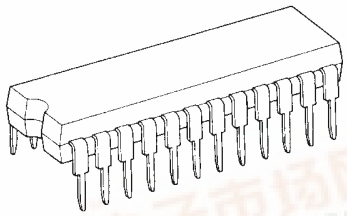
TOSHIBA Bi- CMOS INTEGRATED CIRCUIT SILICON MONOLITHIC

TB62706BNG, TB62706BFG

16BIT SHIFT REGISTER, LATCHES & CONSTANT CURRENT DRIVERS

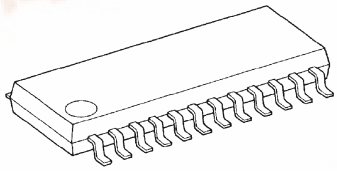
The TB62706BNG, TB62706BFG are specifically designed for LED and LED DISPLAY constant current drivers.
This constant current output circuits are able to set up external resistor (I_{OUT} = 5~90 mA). (Note)
These devices are monolithic integrated circuit designed to be used together with Bi- CMOS process.
The devices consist of 16bit shift register, latch, AND- GATE and Constant Current Drivers.
These products are Pb free.

TB62706BNG



SDIP24-P-300-1.78

TB62706BFG



SSOP24-P-300-1.00B

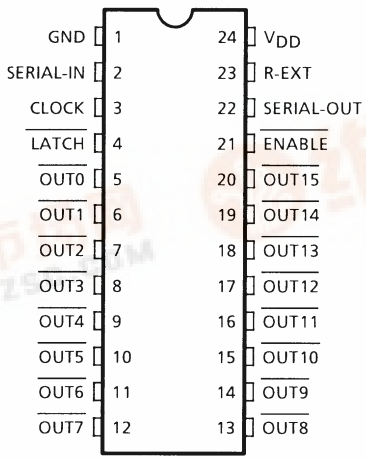
Weight
SDIP24-P-300-1.78 : 1.22 g (typ.)
SSOP24-P-300-1.00B : 0.32 g (typ.)

FEATURES

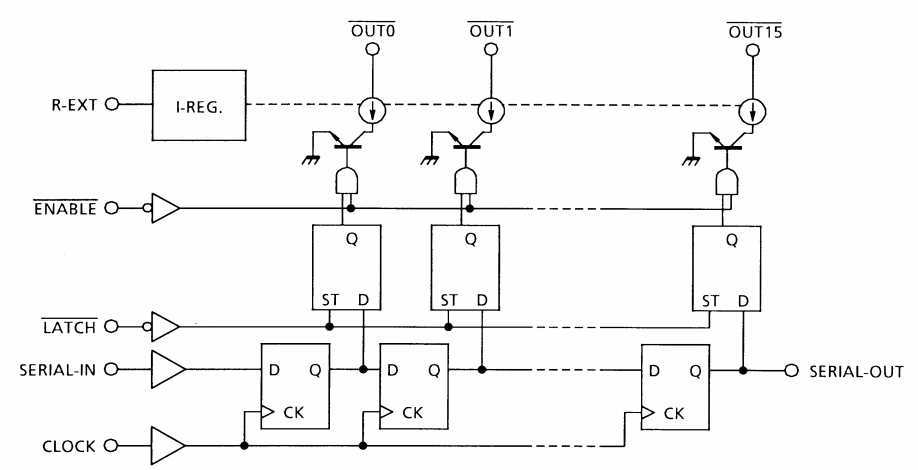
- Constant Current Output : Can set up all output current with one resister for 5 to 90 mA.
- Maximum Clock Frequency : f_{CLK} = 15 (MHz) (Cascade Connected Operate, T_{opr} = 25°C)
- 5 V C- MOS Compatible Input
- Package: SDIP24- P- 300- 1.78 (TB62706BNG)
  SSOP24- P- 300- 1.00B (TB62706BFG)
- Constant Output Current Matching:

OUTPUT- GND VOLTAGE	CURRENT MATCHING	OUTPUT CURRENT
=0.4 V	±6.0%	5~40 mA
=0.7 V	±6.0%	5~90 mA

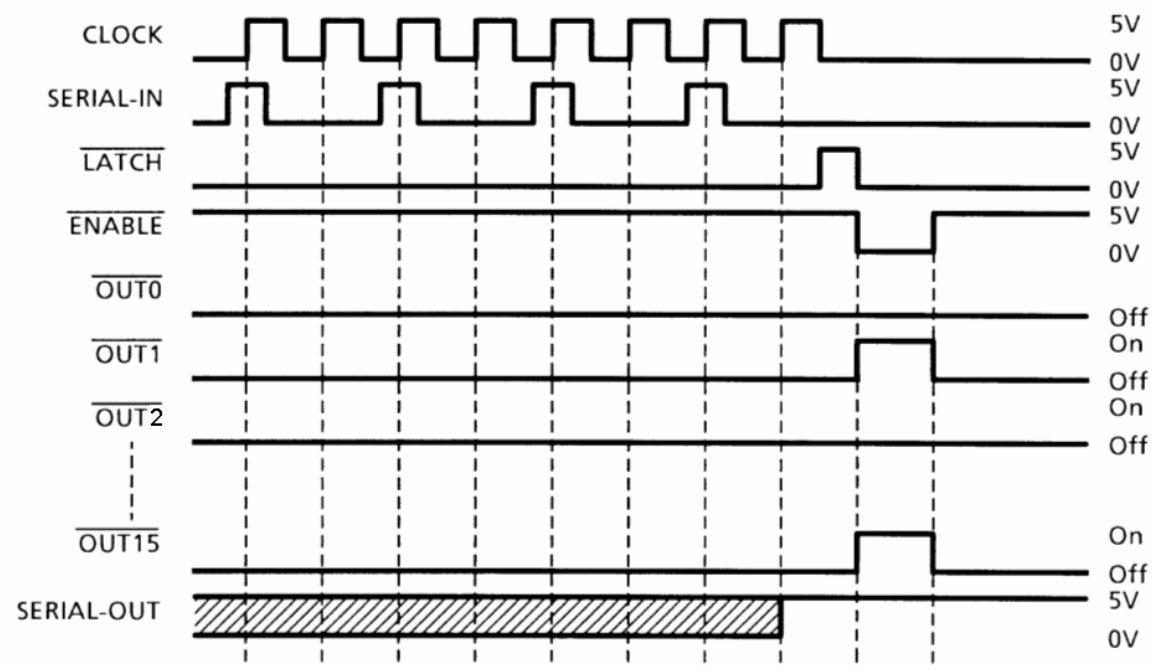
PIN CONNECTION (Top view)



BLOCK DIAGRAM



TIMING DIAGRAM



Note: Latches are level sensitive, not rising edges sensitive and not syncronus CLOCK.
Input of LATCH- terminal to H Level, data passes latches, and input to L level, data hold latches.
Input of ENABLE- terminal to H level, all output (OUT0~15) do off.

TERMINAL DISCRIPTION

PIN No.	PIN NAME	FUNCTION
1	GND	GND terminal for control logic.
2	SERIAL- IN	Input terminal of a serial- data for shift- register.
3	CLOCK	Input terminal of a clock for data shift to up- edge.
4	$\overline{\text{LATCH}}$	Input terminal of a data strobe. Latches passes data with “H” level input of LATCH - terminal, and hold data with "L" level input.
5~20	$\overline{\text{OUT0 ~ 15}}$	Output terminals.
21	$\overline{\text{ENABLE}}$	Input terminal of output enable. All outputs (OUT0~15) do off with “H” level input of ENABLE - terminal, and do on with "L" level input.
22	SERIAL- OUT	Output terminal of a serial- data for next SERIAL- IN terminal.
23	R- EXT	Input terminal of connects with a resister for to set up all output current.
24	V_{DD}	5 V Supply voltage terminal.

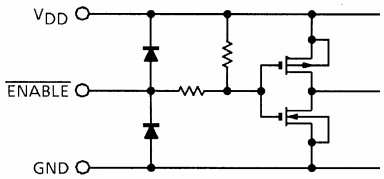
TRUTH TABLE

CLOCK	$\overline{\text{LATCH}}$	$\overline{\text{ENABLE}}$	SERIAL- IN	$\overline{\text{OUT0}} \cdots \overline{\text{OUT7}} \cdots \overline{\text{OUT15}}$	SERIAL- OUT
UP	H	L	D_n	$D_n \cdots D_{n-7} \cdots D_{n-15}$	D_{n-15}
UP	L	L	D_{n+1}	No change	D_{n-14}
UP	H	L	D_{n+2}	$D_{n+2} \cdots D_{n-5} \cdots D_{n-13}$	D_{n-13}
DOWN	X	L	D_{n+3}	$D_{n+2} \cdots D_{n-5} \cdots D_{n-13}$	D_{n-13}
DOWN	X	H	D_{n+3}	Off	D_{n-13}

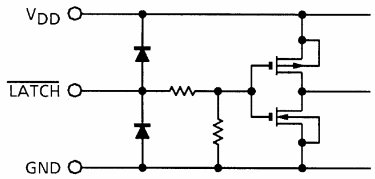
Note: $\overline{\text{OUT0 ~ 15}}$ = on in case of D_n = H level and $\overline{\text{OUT0 ~ 15}}$ = off in case of D_n = L level.
A resistor is connected with R- EXT and GND accompanied with outside, and it is necessary that a correct power supply voltage is supplied.

EQUIVALENT CIRCUIT OF INPUTS AND OUTPUTS

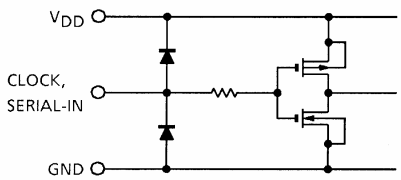
1. $\overline{\text{ENABLE}}$ terminal



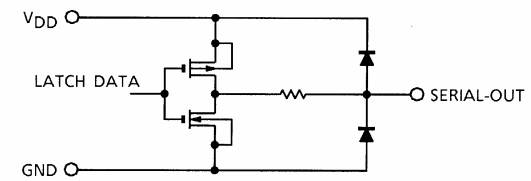
2. $\overline{\text{LATCH}}$ terminal



3. CLOCK, SERIAL- IN terminal



4. SERIAL- OUT terminal



MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	0~7.0	V
Input Voltage	V_{IN}	- 0.4~V_{DD} + 0.4	V
Output Current	I_{OUT}	90	mA
Output Voltage	V_{OUT}	- 0.5~17.0	V
Clock Frequency	f_{CK}	15	MHz
GND Terminal Current	I_{GND}	1440	mA
Power Dissipation	P_D	1.78 (BNG- type : ON PCB, Ta = 25°C)	W
		1.00 (BFG- type : ON PCB, Ta = 25°C)	
Tharmal Resistance	$R_{th\ (j-a)}$	BNG : 70 (BN- type : ON PCB)	°C / W
		BFG : 120 (BF- type : ON PCB)	
Operating Temperature	T_{opr}	- 40~85	°C
Storage Temperature	T_{stg}	- 55~150	°C

Note: BN- type :Ambient temperature delated above 25°C in the proportion of 14.2 mW / °C
BF- type : Ambient temperature delated above 25°C in the proportion of 8.3 mW / °C

RECOMMENDED OPERATING CONDITION (Ta = - 40~85°C unless otherwise noted)

CHARACTERISTIC	SYMBOL	CONDITION	MIN	TYP.	MAX	UNIT
Supply Voltage	V_{DD}	–	4.5	5.0	5.5	V
Output Voltage	V_{OUT}	–	–	–	15.0	V
Output Current	I_O	OUTn, DC 1 circuit	5	–	88	mA
	I_{OH}	SERIAL- OUT	–	–	1.0	
	I_{OL}	SERIAL- OUT	–	–	- 1.0	
Input Voltage	V_{IH}	–	0.7 V_{DD}	–	V_{DD} +0.3	V
	V_{IL}	–	- 0.3	–	0.3 V_{DD}	
$\overline{\text{LATCH}}$ Pulse Width	$t_{w\,\overline{LAT}}$	V_{DD} = 4.5~5.5 V	100	–	–	ns
CLOCK Pulse Width	$t_{w\ CLK}$		50	–	–	ns
$\overline{\text{ENABLE}}$ Pulse Width	$t_{w\,\overline{EN}}$		4500	–	–	ns
Set- Up Time for DATA	$t_{setup\ (D)}$		60	–	–	ns
Hold Time for DATA	$t_{hold\ (D)}$		20	–	–	ns
Set- Up Time for $\overline{\text{LATCH}}$	$t_{setup\ (L)}$		100	–	–	ns
Hold Time for $\overline{\text{LATCH}}$	$t_{hold\ (L)}$		60	–	–	ns
Clock Frequency	f_{CLK}	Cascade operation	–	–	10.0	MHz
Power Dissipation	P_D	Ta = 85°C (BNG- type)	–	–	0.92	W
		Ta = 85°C (BFG- type)	–	–	0.50	

ELECTRICAL CHARACTERISTICS (V_{DD} = 5.0 V, Ta = 25°C unless otherwise noted)

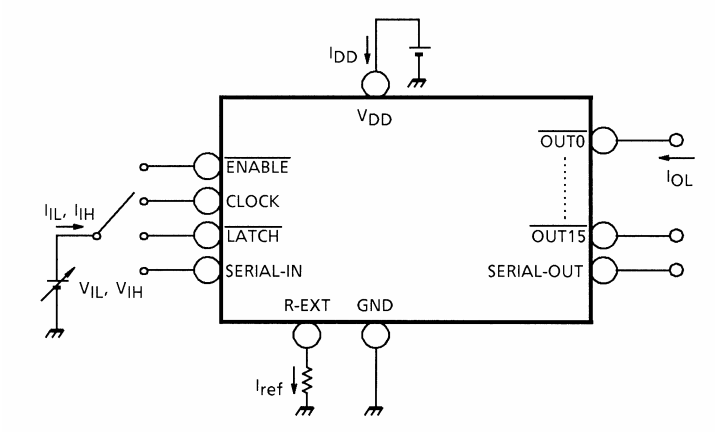
CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	CONDITION		MIN	TYP.	MAX	UNIT
Input Voltage	"H" Level	V_{IH}	–	Ta = - 40~85°C		0.7 V_{DD}	–	V_{DD}	V
	"L" Level	V_{IL}	–	Ta = - 40~85°C		GND	–	0.3 V_{DD}	
Output Leakage Current		I_{OH}	–	V_{OH} = 15.0 V		–	–	10	μA
Output Voltage	SERIAL- OUT	V_{OL}	–	I_{OL} = 1.0 mA		–	–	0.4	V
		V_{OH}	–	I_{OH} = - 1.0 mA		4.6	–	–	
Output Current 1		I_{OL1}	–	V_{CE} = 0.7 V	R_{EXT} = 470 Ω (Include current matching)	34.1	40.0	45.9	mA
		I_{OL2}	–	V_{CE} = 0.4 V		33.7	39.5	45.3	
	Current Skew	$D I_{OL1}$	–	I_O = 40 mA, V_{CE} = 0.4 V	R_{EXT} = 470 Ω	–	±1.5	±6.0	%
Output Current 2		I_{OL3}	–	V_{CE} = 1.0 V	R_{EXT} = 250 Ω (Include current matching)	64.2	75.5	86.8	mA
		I_{OL4}	–	V_{CE} = 0.7 V		63.8	75.0	86.2	
	Current Skew	$D I_{OL2}$	–	I_O = 75 mA, V_{CE} = 0.7 V	R_{EXT} = 250 Ω	–	±1.5	±6.0	%
Supply Voltage Regulation		% / V_{DD}	–	R_{EXT} = 470 Ω, Ta = - 40~85°C		–	1.5	5.0	% / V
Pull- Up Resistor		$R_{IN (up)}$	–	–		150	300	600	Ω
Pull- Down Resistor		$R_{IN (down)}$	–	–		100	200	400	Ω
Supply Current	"OFF"	$I_{DD (off) 1}$	–	R_{EXT} = Open, $\overline{OUT0 \sim 15}$ = off		–	0.6	1.2	mA
		$I_{DD (off) 2}$	–	R_{EXT} = 470 Ω, $\overline{OUT0 \sim 15}$ = off		3.5	5.8	8.0	
		$I_{DD (off) 3}$	–	R_{EXT} = 250 Ω, $\overline{OUT0 \sim 15}$ = off		6.5	10.7	15.0	
	"ON"	$I_{DD (on) 1}$	–	R_{EXT} = 470 Ω, $\overline{OUT0 \sim 15}$ = on		10.0	16.0	22.0	
		$I_{DD (on) 2}$	–	R_{EXT} = 250 Ω, $\overline{OUT0 \sim 15}$ = on		18.0	28.3	38.5	

SWITCHING CHARACTERISTICS (Ta = 25°C unless otherwise noted)

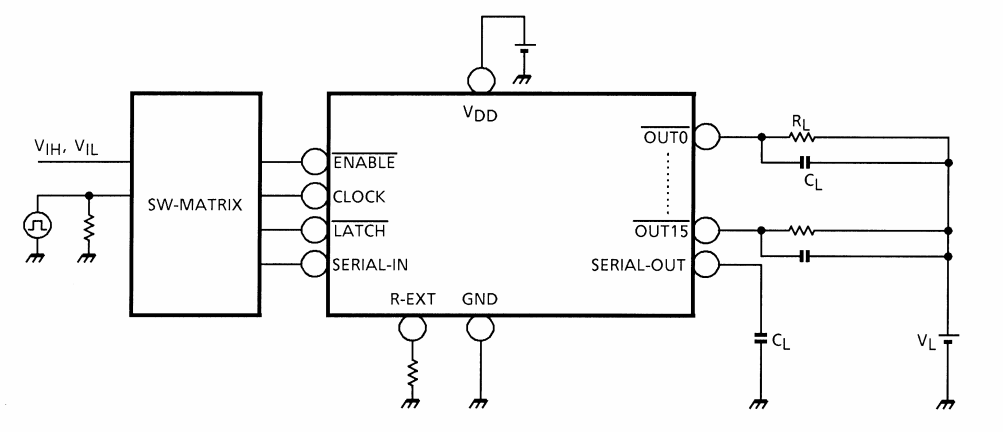
CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	CONDITION	MIN	TYP	MAX	UNIT
Propagation Delay Time ("L" to "H")	CLK- $\overline{OUTn}$	t_{pLH}	–	V_{DD} = 5.0 V V_{CE} = 0.4 V V_{IH} = V_{DD} V_{IL} = GND R_{EXT} = 470 Ω V_L = 3.0 V R_L = 65 Ω C_L = 10.5 pF	–	1200	1500	ns
	$\overline{LATCH}$ - $\overline{OUTn}$				–	1200	1500	
	$\overline{ENABLE}$ - $\overline{OUTn}$				–	1200	1500	
	CLK- SOUT				15	30	70	
Propagation Delay Time ("H" to "L")	CLK- $\overline{OUTn}$	t_{pHL}	–		–	700	1000	ns
	$\overline{LATCH}$ - $\overline{OUTn}$				–	700	1000	
	$\overline{ENABLE}$ - $\overline{OUTn}$				–	700	1000	
	CLK- SOUT				15	30	70	
Pulse Width	CLK	$t_{w\ CLK}$	–		–	20	30	ns
	$\overline{LATCH}$	$t_{w\ \overline{LAT}}$	–		–	10	25	ns
Set- up Time	L- H	$t_{setup\ (L)}$	–		–	25	50	ns
	H- L	$t_{setup\ (C)}$			–	25	50	ns
Hold Time	L- H	$t_{hold\ (L)}$	–		–	0	15	ns
	H- L	$t_{hold\ (C)}$			–	0	15	ns
Maximum CLOCK Rise Time		t_r	–		–	–	10	µs
Maximum CLOCK Fall Time		t_f	–		–	–	10	µs
Output Rise Time		t_{or}	–		150	300	600	ns
Output Fall Time		t_{of}	–		150	300	600	ns

TEST CIRCUIT

DC characteristic



AC characteristic

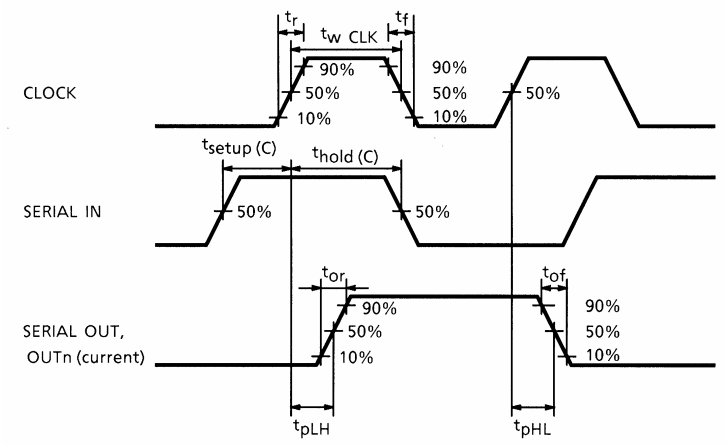


PRECAUTIONS for USING

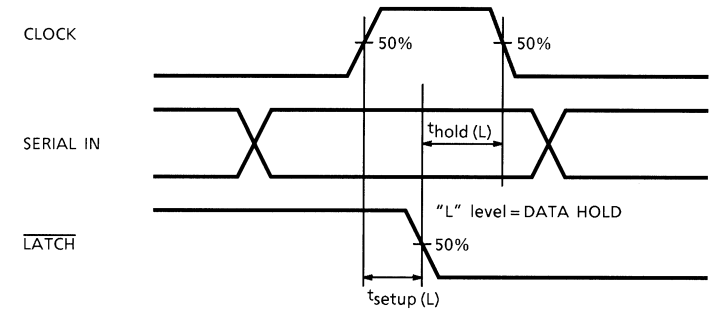
Utmost care is necessary in the design of the output line, V_{CC} (V_{DD}) and GND line since IC may be destroyed due to short- circuit between outputs, air contamination fault, or fault by improper grounding.

TIMING WAVEFORM

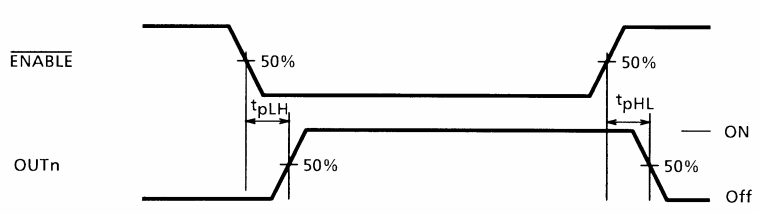
1. CLOCK- SERIAL OUT, OUTn

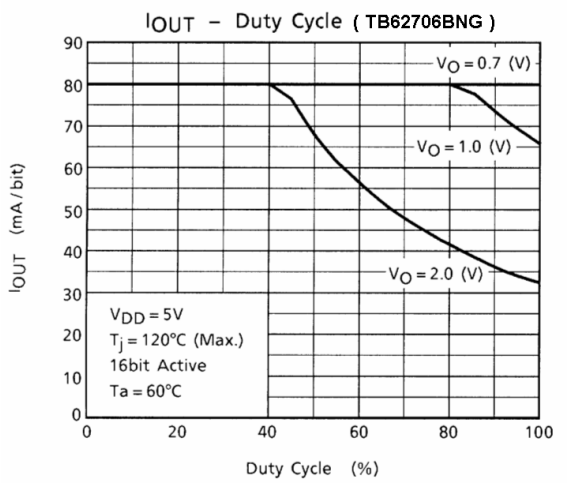


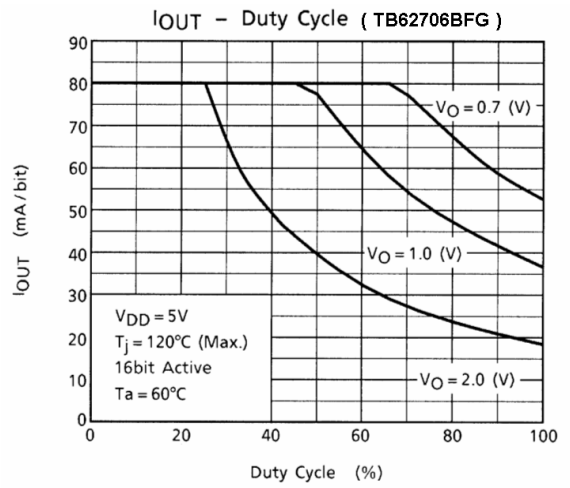
2. CLOCK- $\overline{\text{LATCH}}$

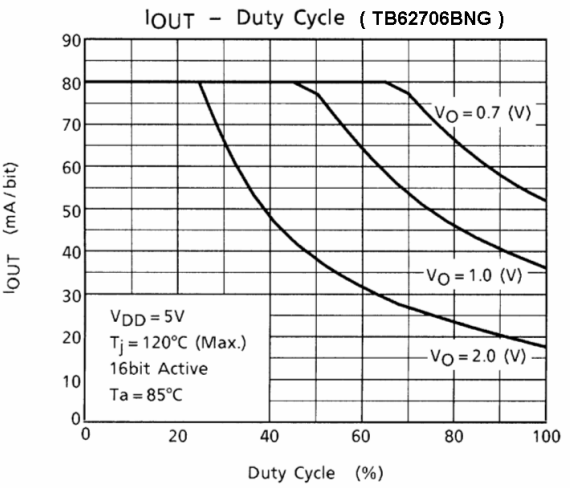


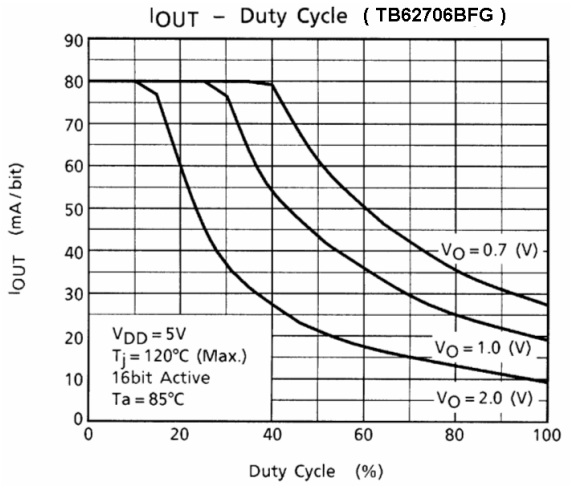
3. $\overline{\text{ENABLE}}$ - OUTn

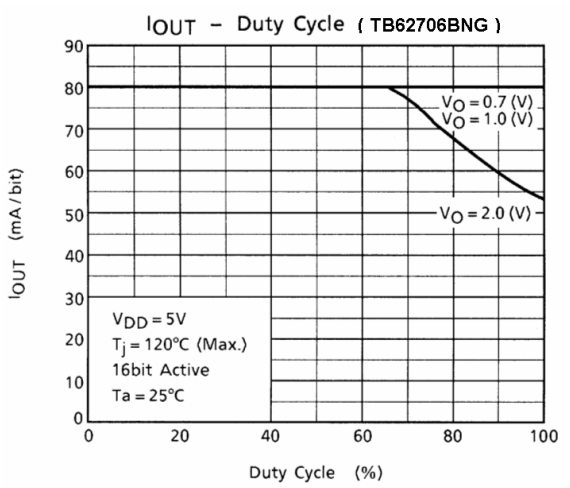


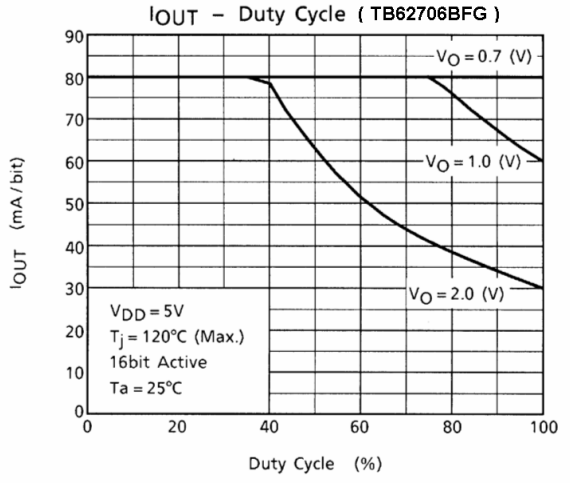

IOUT – Duty Cycle (TB62706BNG)
IOUT (mA/bit)
Duty Cycle (%)
VO = 0.7 (V)
VO = 1.0 (V)
VO = 2.0 (V)
VDD = 5V
Tj = 120°C (Max.)
16bit Active
Ta = 60°C


IOUT – Duty Cycle (TB62706BFG)
IOUT (mA/bit)
Duty Cycle (%)
VO = 0.7 (V)
VO = 1.0 (V)
VO = 2.0 (V)
VDD = 5V
Tj = 120°C (Max.)
16bit Active
Ta = 60°C


IOUT – Duty Cycle (TB62706BNG)
IOUT (mA/bit)
Duty Cycle (%)
VO = 0.7 (V)
VO = 1.0 (V)
VO = 2.0 (V)
VDD = 5V
Tj = 120°C (Max.)
16bit Active
Ta = 85°C


IOUT – Duty Cycle (TB62706BFG)
IOUT (mA/bit)
Duty Cycle (%)
VO = 0.7 (V)
VO = 1.0 (V)
VO = 2.0 (V)
VDD = 5V
Tj = 120°C (Max.)
16bit Active
Ta = 85°C


IOUT – Duty Cycle (TB62706BNG)
IOUT (mA/bit)
Duty Cycle (%)
VO = 0.7 (V)
VO = 1.0 (V)
VO = 2.0 (V)
VDD = 5V
Tj = 120°C (Max.)
16bit Active
Ta = 25°C


IOUT – Duty Cycle (TB62706BFG)
IOUT (mA/bit)
Duty Cycle (%)
VO = 0.7 (V)
VO = 1.0 (V)
VO = 2.0 (V)
VDD = 5V
Tj = 120°C (Max.)
16bit Active
Ta = 25°C

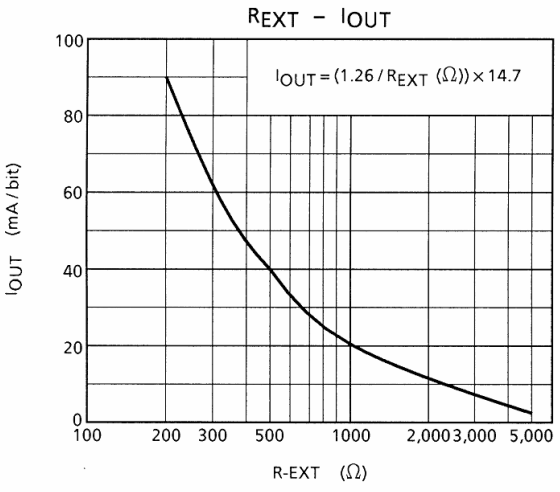
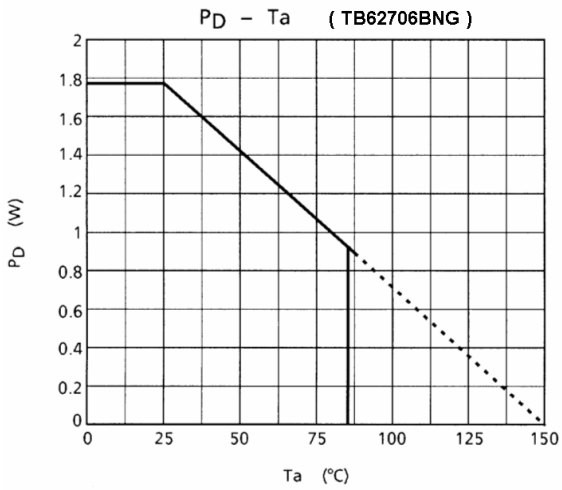
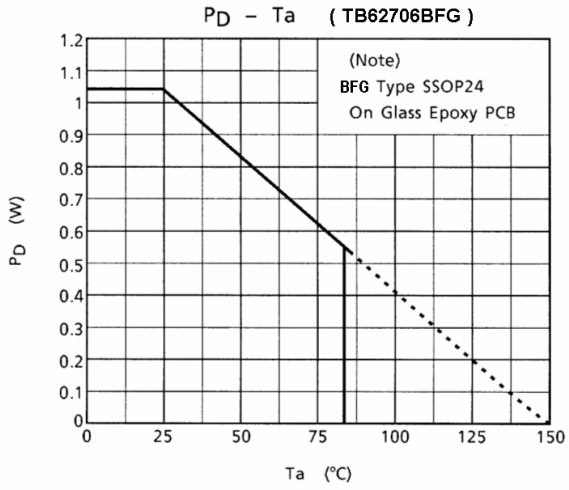

REXT – IOUT
IOUT = (1.26 / REXT (Ω)) × 14.7
IOUT (mA / bit)
R-EXT (Ω)
100
80
60
40
20
0
100
200
300
500
1000
2,000
3,000
5,000

Fig.1


PD – Ta (TB62706BNG)
PD (W)
Ta (°C)
2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
0
25
50
75
100
125
150


PD – Ta (TB62706BFG)
(Note)
BFG Type SSOP24
On Glass Epoxy PCB
PD (W)
Ta (°C)
1.2
1.1
1
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0
0
25
50
75
100
125
150

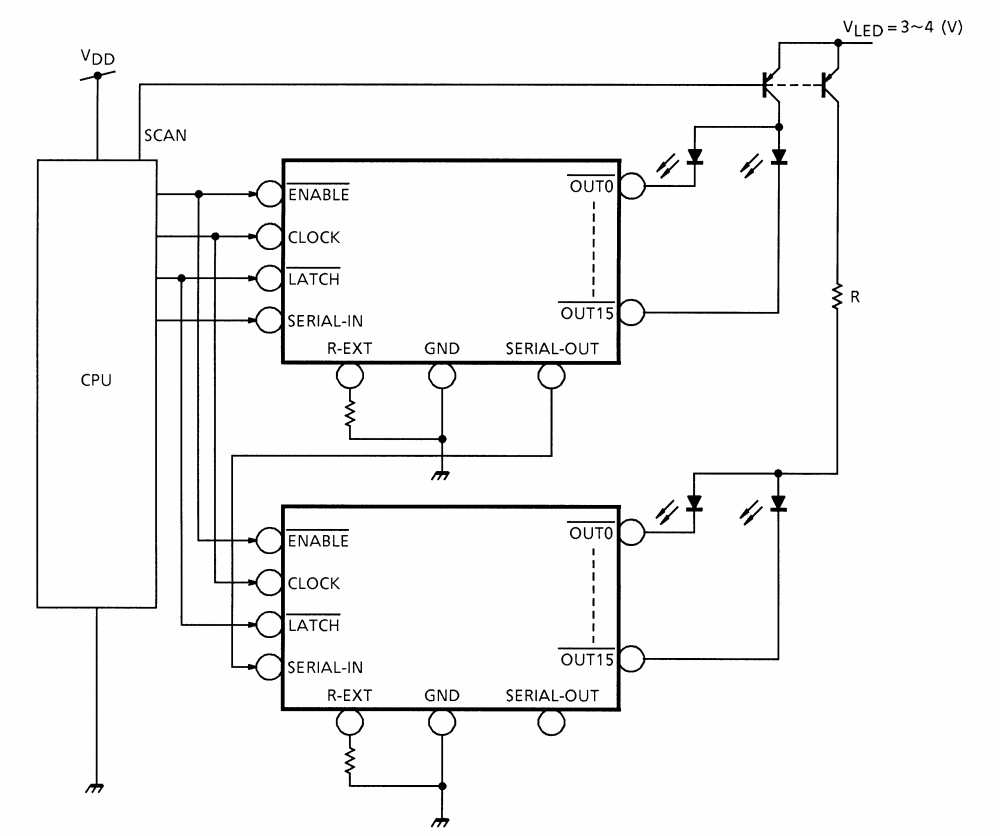
LED DRIVER TB6270X SERIES APPICATION NOTE

[1] Output current (I_{OUT})
I_{OUT} is set by the enternal resistor (R- EXT) as shown in Fig.1.

[2] Total supply voltage (VLED)
This device can operate 0.4~0.7V (V_O).
When a higher voltage is input to the device, the excess voltage is consumed inside the device, that leads to power dissipation.
In order to minimize power dissipation and loss, we would like to recommend to set the total supply voltage as shown below,

V_{LED} (total supply voltage) = V_{CE} (T_r V_{sat}) + V_f (LED Forward voltage) + V_O (I_C supply voltage)

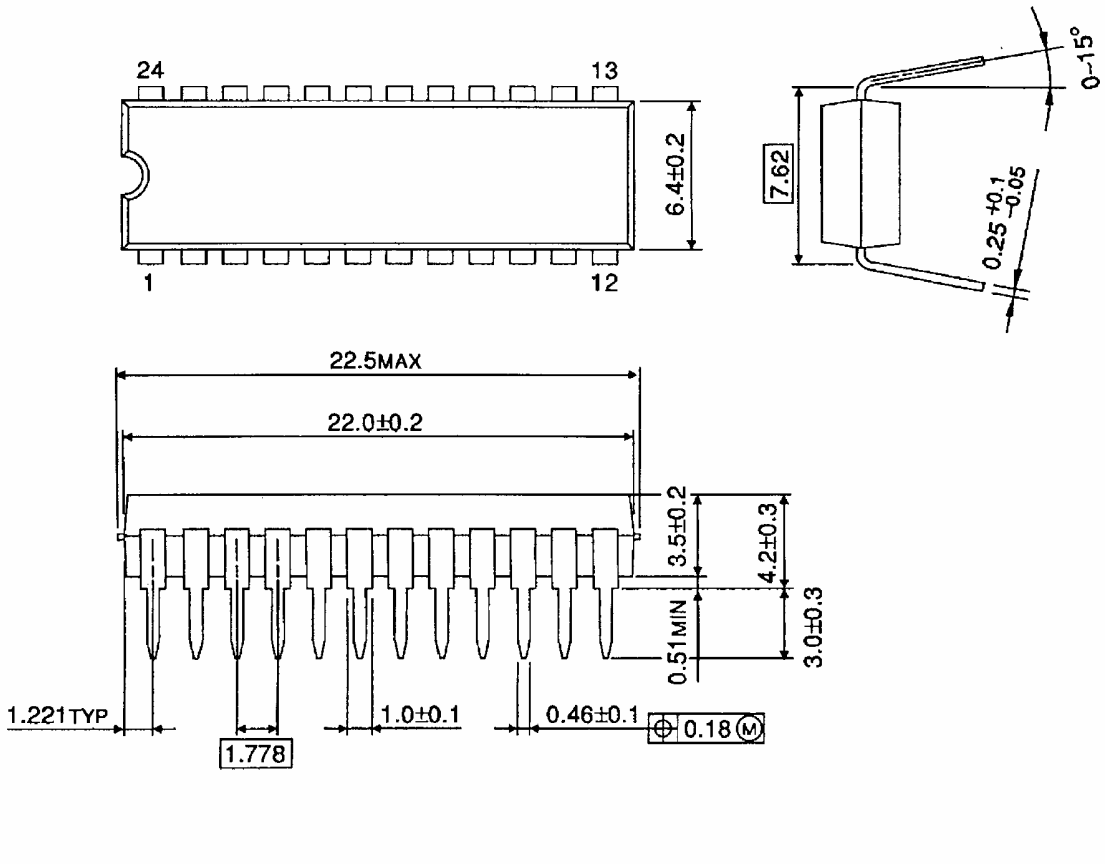
When the total supply is too high considering the power dissipation of this device, an additional R can decrease the supply voltage (V_O).



[3] Pattern layout
This device owns only one ground pin that means signal ground pin and power ground pin are common.
If ground pattern layout contains large inductance and impedance, and the voltage between ground and LATCH, CLOCK terminals exceeds 2.5 V by switching noise in operation, this device may miss- operate. So we would lile you to pay attention to pattern layout to minimize inductance.

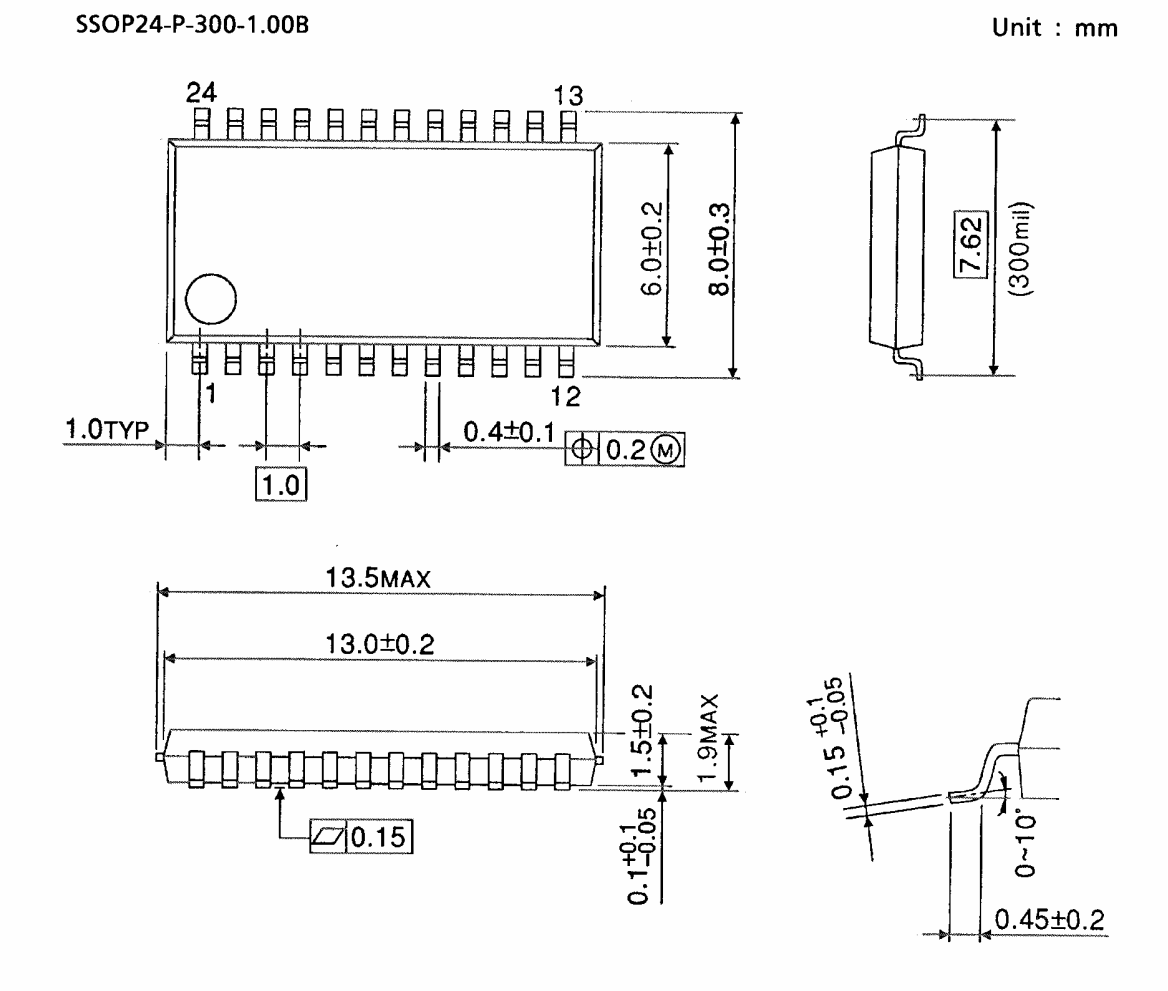
Package Dimensions

SDIP24-P-300-1.78 Unit : mm



Weight: 1.22 g (typ.)

Package Dimensions



Weight: 0.32 g (typ.)

About solderability, following conditions were confirmed

- Solderability

  (1) Use of Sn-63Pb solder Bath
  - · solder bath temperature = 230°C
  - · dipping time = 5 seconds
  - · the number of times = once
  - · use of R-type flux

  (2) Use of Sn-3.0Ag-0.5Cu solder Bath
  - · solder bath temperature = 245°C
  - · dipping time = 5 seconds
  - · the number of times = once
  - · use of R-type flux

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