

**TOSHIBA****TCD2950D****Preliminary** TOSHIBA CCD Image Sensor CCD (charge coupled device)

# TCD2950D

The TCD2950D is a high sensitive and low dark current 10680 elements  $\times$  6 line CCD color image sensor which includes CCD drive circuit and clamp circuit. The sensor is designed for scanner.

The device contains a row of 10680 elements  $\times$  6 line staggered photodiodes which provide a 96 lines/mm (2400DPI) across a A4 size paper. The device is operated by 5 V pulse, and 12 V power supply.

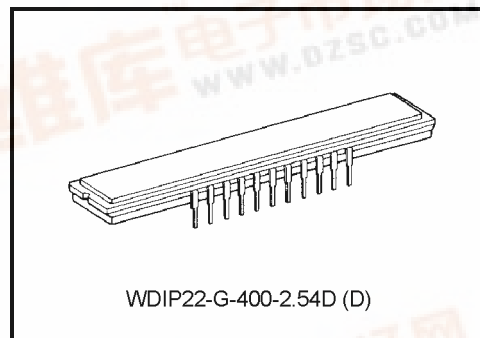
## Features

- Number of image sensing elements: 10680 elements  $\times$  6 line
- Image sensing element size: 2.8  $\mu\text{m}$  by 4  $\mu\text{m}$  on 4  $\mu\text{m}$  centers
- Photo sensing region: High sensitive and low dark current PN photodiode
- Distance between photodiode array: 64  $\mu\text{m}$  (16 lines)
- Clock: 2 phase (5 V)
- Power supply: 12 V power supply voltage
- Internal circuit: Clamp circuit
- Package: 22 pin Cerdip package
- Color filter: Red, green, blue

## Maximum Ratings (Note1)

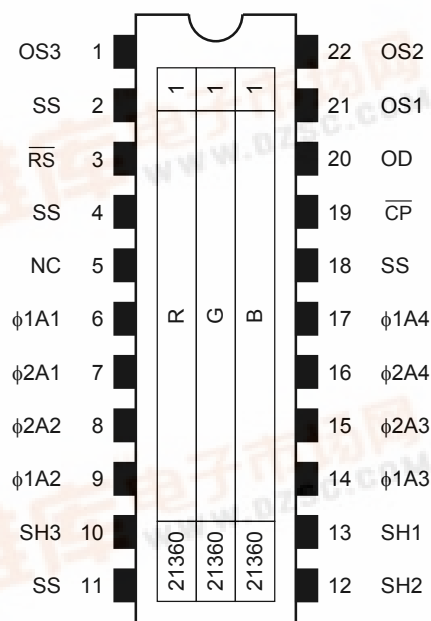
Characteristics	Symbol	Rating	Unit
Clock pulse voltage	$V_{\phi}$	-0.3~8.0	V
Shift pulse voltage	$V_{SH}$		
Reset pulse voltage	$V_{RS}$		
Clamp pulse voltage	$V_{CP}$		
Power supply voltage	$V_{OD}$	-0.3~15	V
Operating temperature	$T_{opr}$	0~60	$^{\circ}\text{C}$
Storage temperature	$T_{stg}$	-25~85	$^{\circ}\text{C}$

Note1: All voltage are with respect to SS terminals (ground).

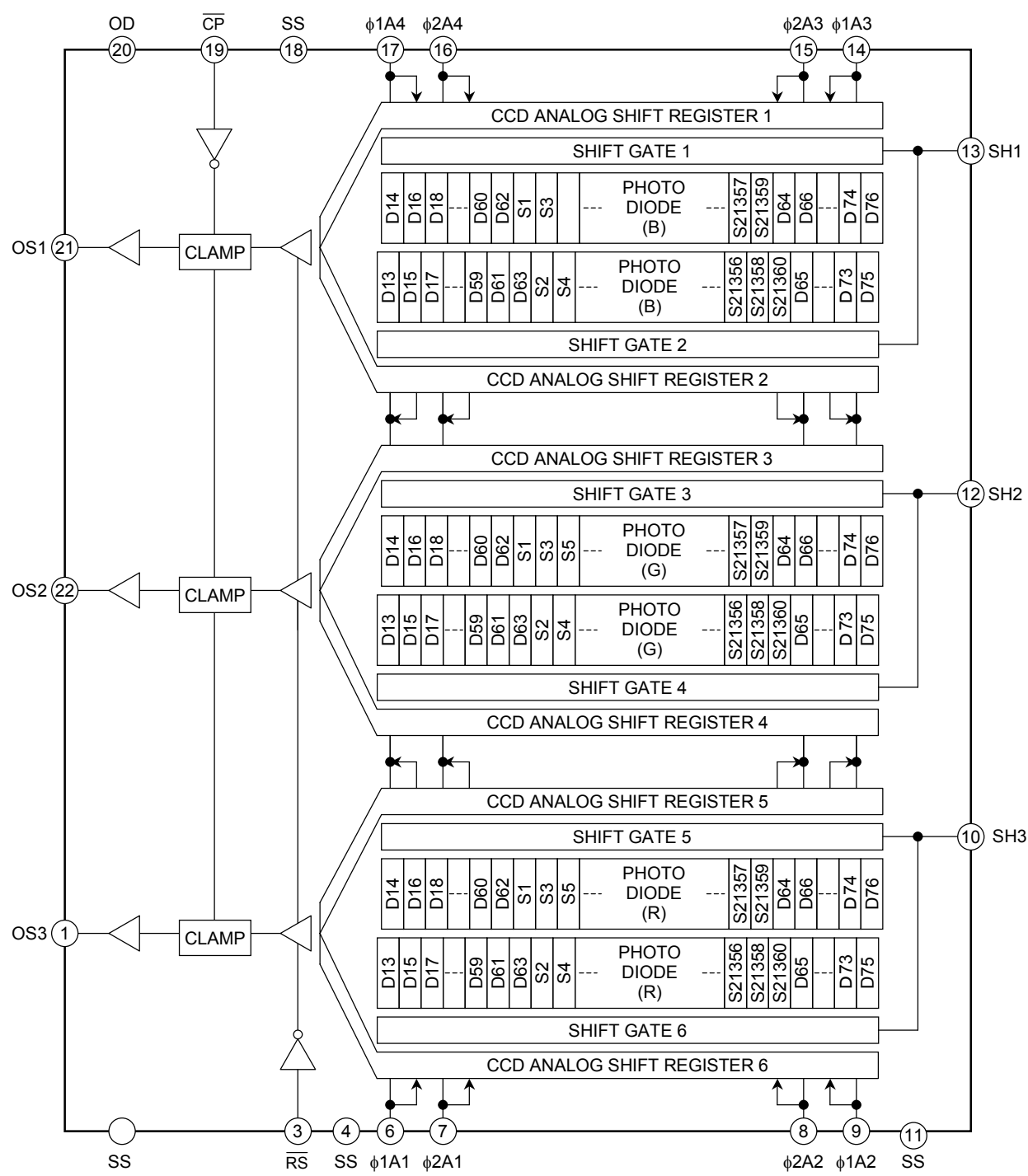


Weight: 5.2 g (typ.)

## Pin Connections (top view)



Circuit Diagram



**Optical/Electrical Characteristics**

(Ta = 25°C, V<sub>OD</sub> = 12 V, V<sub>φ</sub> = V<sub>SH</sub> = V<sub>RS</sub> = V<sub>CP</sub> = 5 V (pulse), f<sub>φ</sub> = 1 MHz, f<sub>RS</sub> = 2 MHz, t<sub>INT</sub> = 11 ms, LIGHT SOURCE = A LIGHT SOURCE + CM500S FILTER (t = 1 mm), LOAD RESISTANCE = 100 kΩ)

Characteristics		Symbol	Min	Typ.	Max	Unit	Note
Sensitivity	Red	R <sub>(R)</sub>	0.9	1.4	1.9	V/lx·s	(Note 2)
	Green	R <sub>(G)</sub>	1.3	1.9	2.5		
	Blue	R <sub>(B)</sub>	0.9	1.3	1.7		
Photo response non uniformity		PRNU (1)	—	15	20	%	(Note 3)
		PRNU (3)	—	3	12	mV	(Note 4)
Register imbalance		RI	—	1	—	%	(Note 5)
Saturation Output Voltage		V <sub>SAT</sub>	2.9	3.5	—	V	(Note 6)
Saturation Exposure		SE	1.16	1.84	—	lx·s	(Note 7)
Dark signal Voltage		V <sub>DRK</sub>	—	0.5	2.0	mV	(Note 8)
Dark Signal Non Uniformity		DSNU	—	2.0	7.0	mV	(Note 8)
DC Power Dissipation		P <sub>D</sub>	—	420	585	mW	—
Total Transfer Efficiency		TTE	92	98	—	%	—
Output Impedance		Z <sub>O</sub>	—	0.3	1.0	kΩ	—
DC Compensation Output Voltage		V <sub>OS</sub>	5.0	6.0	7.0	V	(Note 9)
Random Noise		N <sub>Dσ</sub>	—	0.8	—	mV	(Note 10)
Reset Noise		V <sub>RSN</sub>	—	0.3	1.0	V	(Note 9)
Masking Noise		V <sub>MS</sub>	—	0.2	1.0	V	(Note 9)

Note 2: Sensitivity is defined for each color of signal outputs average when the photosensitive surface is applied with the light of uniform illumination and uniform color temperature.

Note 3: PRNU (1) is defined for each color on a single chip by the expressions below when the photosensitive surface is applied with the light of uniform illumination and uniform color temperature.

$$\text{PRNU (1)} = \frac{\Delta x}{\bar{x}} \times 100 (\%)$$

Where  $\bar{x}$  is average of total signal output and  $\Delta X$  is the maximum deviation from  $\bar{x}$ .  
The amount of incident light is shown below.

Red = 1/2·SE  
Green = 1/2·SE  
Blue = 1/4·SE

Note 4: PRNU (3) is defined as maximum voltage with next pixels, where measured at 5% of SE (typ.).

Note 5: Register imbalance is defined as follows.

$$\text{RI} = \frac{\sum_{n=1}^{21359} |x_n - x_{(n+1)}|}{21359 \times \bar{x}} \times 100 (\%)$$

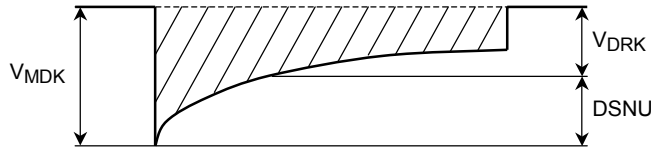
Note 6: V<sub>SAT</sub> is defined as minimum saturation output of all effective pixels.

Note 7: Definition of SE

$$\text{SE} = \frac{V_{\text{SAT}}}{R_G} (\text{lx} \cdot \text{s})$$

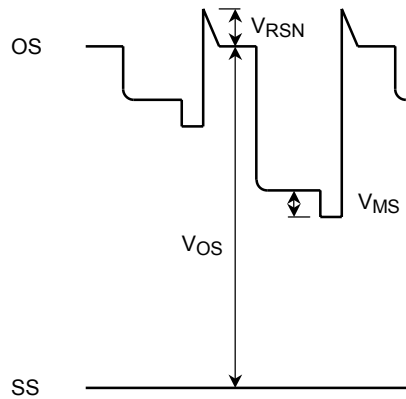
Note 8:  $V_{DRK}$  is defined as average dark signal voltage of all effective pixels.

$DSNU$  is defined as different voltage between  $V_{DRK}$  and  $V_{MDK}$  when  $V_{MDK}$  is maximum dark signal voltage.

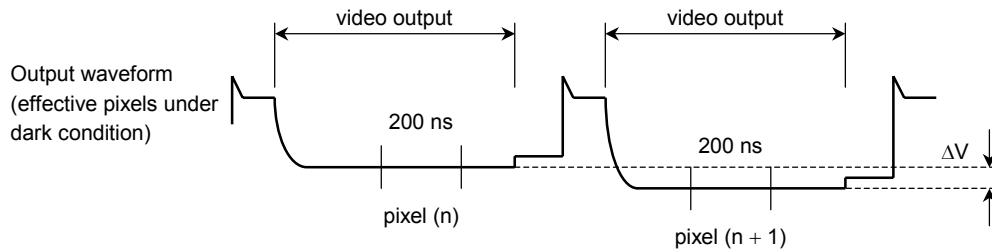


Note 9: DC signal output voltage is defined as follows. Reset noise voltage is defined as follows.

Masking noise voltage is defined as follows.



Note 10: Random noise is defined as the standard deviation (sigma) of the output level difference between two adjacent effective pixels under no illumination (i.e. dark conditions) calculated by the following procedure.



- (1) Two adjacent pixels (pixel  $n$  and  $n + 1$ ) in one reading are fixed as measurement points.
- (2) Each of the output level at video output periods averaged over 200 ns period to get  $V(n)$  and  $V(n + 1)$ .
- (3)  $V(n + 1)$  is subtracted from  $V(n)$  to get  $\Delta V$ .  

$$\Delta V = V(n) - V(n + 1)$$
- (4) The standard deviation of  $\Delta V$  is calculated after procedure (2) and (3) are repeated 30 times (30 readings).

$$\overline{\Delta V} = \frac{1}{30} \sum_{i=1}^{30} |\Delta V_i|$$

$$\sigma = \sqrt{\frac{1}{30} \sum_{i=1}^{30} (|\Delta V_i| - \overline{\Delta V})^2}$$

- (5) Procedure (2), (3) and (4) are repeated 10 times to get sigma value.
- (6) 10 sigma values are averaged.

$$\overline{\sigma} = \frac{1}{10} \sum_{j=1}^{10} \sigma_j$$

- (7)  $\overline{\sigma}$  value calculated using the above procedure is observed  $\sqrt{2}$  times larger than that measured relative to the ground level. So we specify random noise as follows.

$$ND\sigma = \frac{1}{\sqrt{2}} \overline{\sigma}$$

## Operating Condition

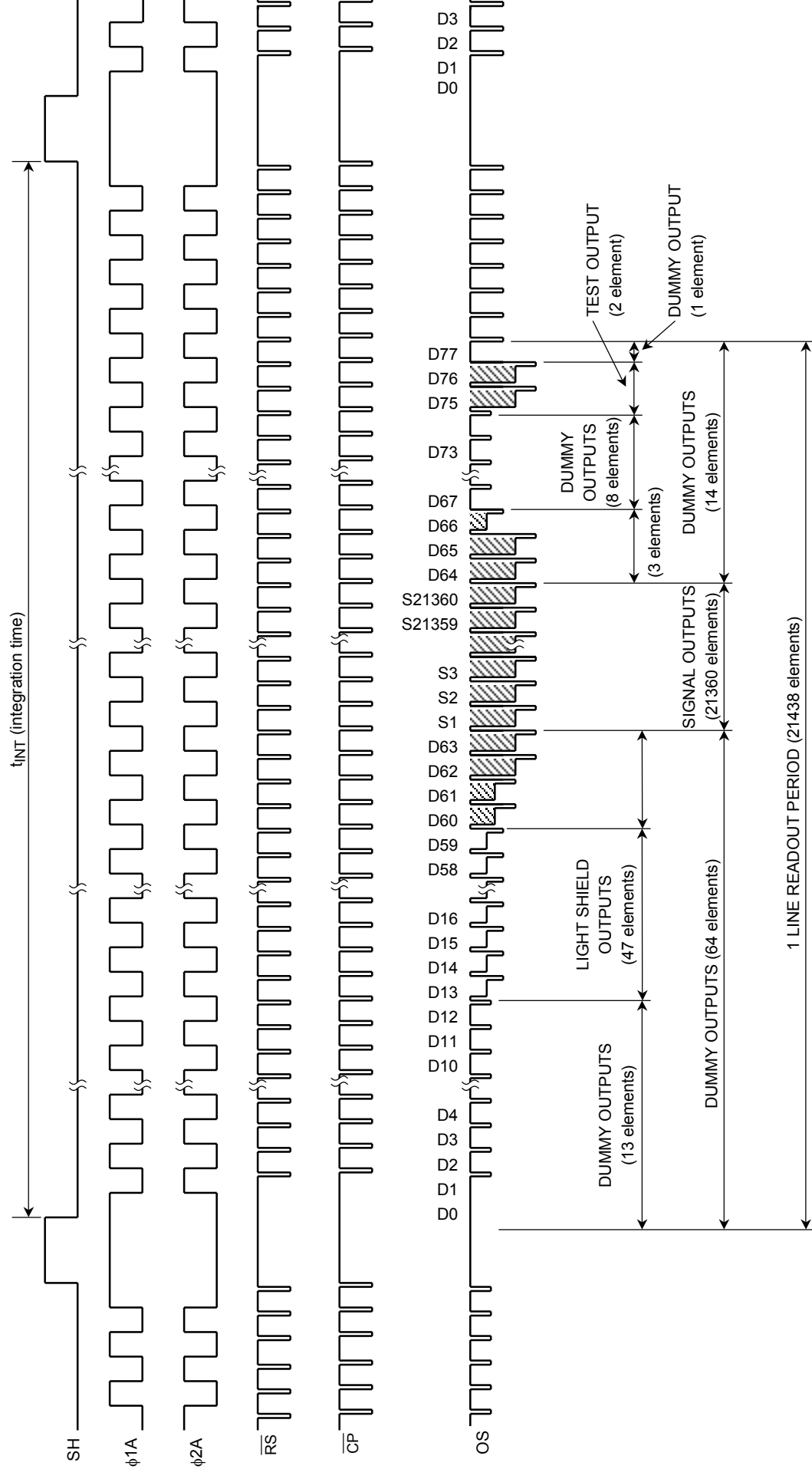
Characteristics		Symbol	Min	Typ.	Max	Unit	Note
Clock pulse voltage	"H" level	$V_{\phi A}$	4.5	5.0	5.5	V	
	"L" level		0	—	0.3		
Shift pulse voltage	"H" level	$V_{SH}$	4.5	5.0	5.5	V	
	"L" level		0	—	0.5		
Reset pulse voltage	"H" level	$\overline{V_{RS}}$	4.5	5.0	5.5	V	
	"L" level		0	—	0.5		
Clamp pulse voltage	"H" level	$\overline{V_{CP}}$	4.5	5.0	5.5	V	
	"L" level		0	—	0.5		
Power supply voltage		$V_{OD}$	11.4	12.0	13.0	V	

## Clock Characteristics (Ta = 25°C)

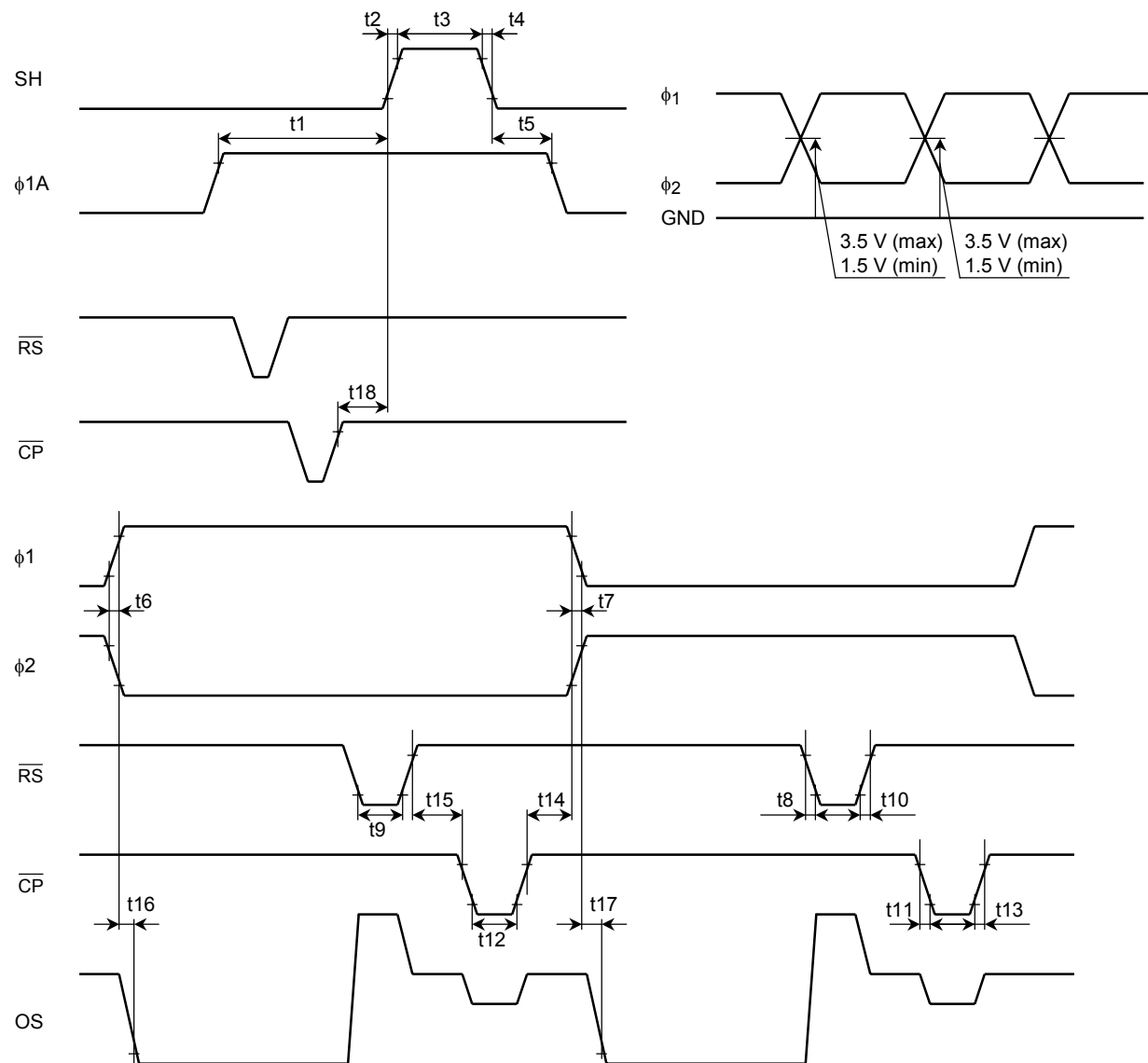
Characteristics	Symbol	Min	Typ.	Max	Unit
Clock pulse frequency	$f_{\phi A}$	0.15	1.0	10	MHz
Reset pulse frequency	$\overline{f_{RS}}$	0.3	2.0	10	MHz
Clamp pulse frequency	$\overline{f_{CP}}$	0.3	2.0	10	MHz
Clock capacitance (Note 11)	$C_{\phi A}$	—	400	—	pF
Shift gate capacitance	$C_{SH}$	—	50	—	pF
Reset gate capacitance	$\overline{C_{RS}}$	—	10	—	pF
Clamp gate capacitance	$\overline{C_{CP}}$	—	10	—	pF

Note 11:  $V_{OD} = 12\text{ V}$

## Timing Chart (bit clamp mode)



**Timing Requirements**



## Timing Requirements

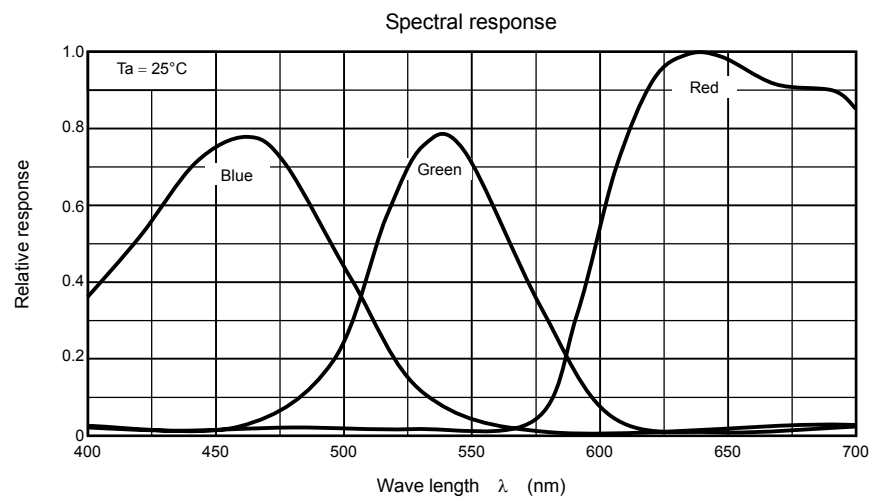
Characteristics	Symbol	Min	Typ. (Note11)	Max	Unit
Pulse timing of SH and $\phi 1A$	t1	110	1000	—	ns
	t5	200	1000	—	
SH pulse rise time, fall time	t2, t4	0	50	—	ns
SH pulse width	t3	1000	2000	—	ns
$\phi 1$ , $\phi 2$ pulse rise time, fall time	t6, t7	0	50	—	ns
$\overline{RS}$ pulse rise time, fall time	t8, t10	0	20	—	ns
$\overline{RS}$ pulse width (Note 12)	t9	15	100	—	ns
$\overline{CP}$ pulse rise time, fall time	t11, t13	0	20	—	ns
$\overline{CP}$ pulse width	t12	20	100	—	ns
Pulse timing of $\phi 1A$ , $\phi 2A$ and $\overline{CP}$	t14	10	40	—	ns
Pulse timing of $\overline{RS}$ and $\overline{CP}$	t15	0	100	—	ns
Video data delay time (Note 13)	t16, t17	—	15	—	ns
Pulse timing of SH and $\overline{CP}$	t18	0	500	—	ns

Note 12: TYP is the case of  $f_{\overline{RS}} = 2.0 \text{ MHz}$ .

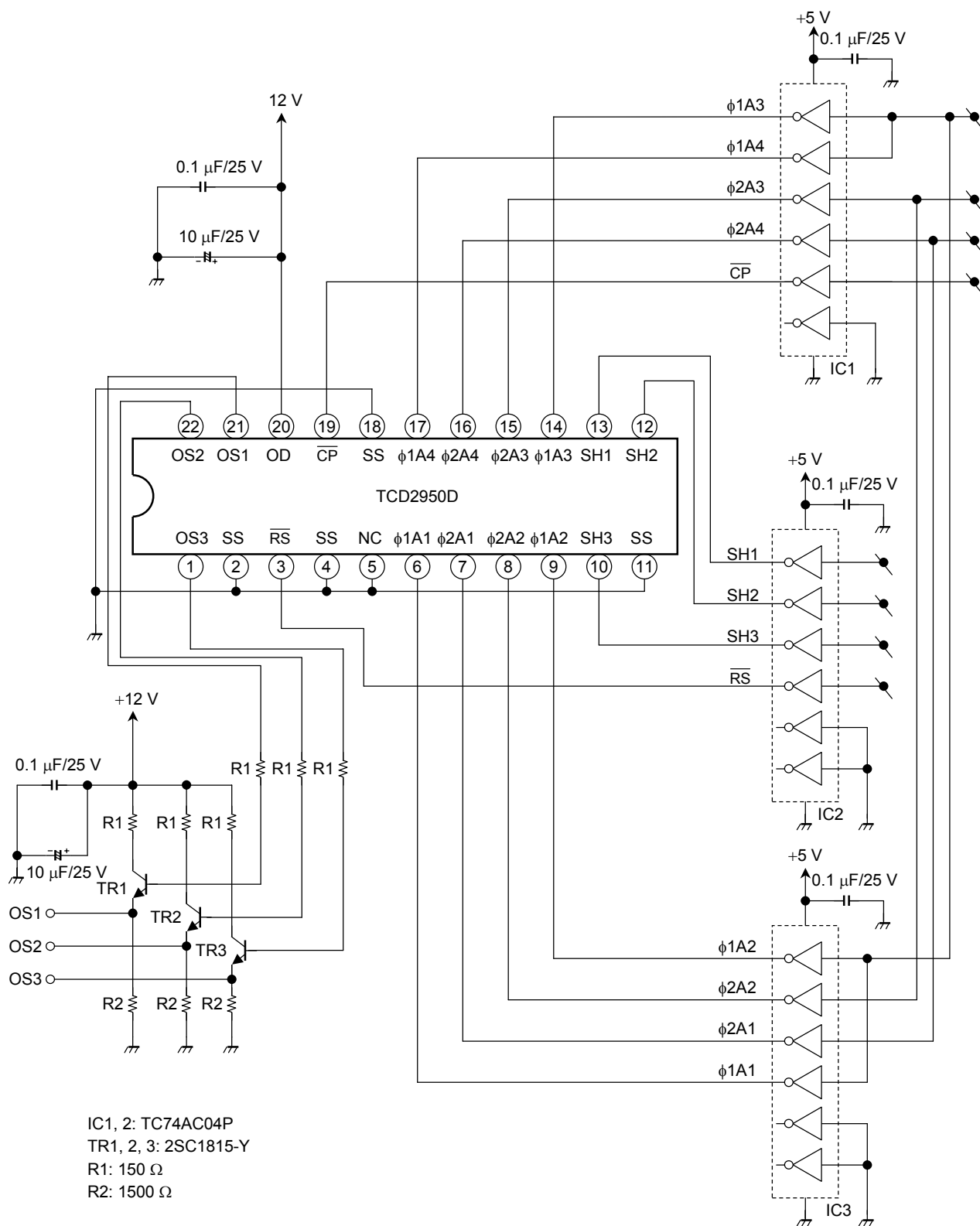
Note 13: Load resistance is 100 k $\Omega$ .



Typical Spectral Response



## Typical Drive Circuit



**Caution****1. Window Glass**

The dust and stain on the glass window of the package degrade optical performance of CCD sensor.

Keep the glass window clean by saturating a cotton swab in alcohol and lightly wiping the surface, and allow the glass to dry, by blowing with filtered dry N<sub>2</sub>. Care should be taken to avoid mechanical or thermal shock because the glass window is easily to damage.

**2. Electrostatic Breakdown**

Store in shorting clip or in conductive foam to avoid electrostatic breakdown.

CCD Image Sensor is protected against static electricity, but interior puncture mode device due to static electricity is sometimes detected. In handling the device, it is necessary to execute the following static electricity preventive measures, in order to prevent the trouble rate increase of the manufacturing system due to static electricity.

- a. Prevent the generation of static electricity due to friction by making the work with bare hands or by putting on cotton gloves and non-charging working clothes.
- b. Discharge the static electricity by providing earth plate or earth wire on the floor, door or stand of the work room.
- c. Ground the tools such as soldering iron, radio cutting pliers or pincer.

It is not necessarily required to execute all precaution items for static electricity.

It is all right to mitigate the precautions by confirming that the trouble rate within the prescribed range.

**3. Incident Light**

CCD sensor is sensitive to infrared light. Note that infrared light component degrades resolution and PRNU of CCD sensor.

**4. Lead Frame Forming**

Since this package is not strong against mechanical stress, you should not reform the lead frame.

We recommend to use a IC-inserter when you assemble to PCB.

**5. Soldering**

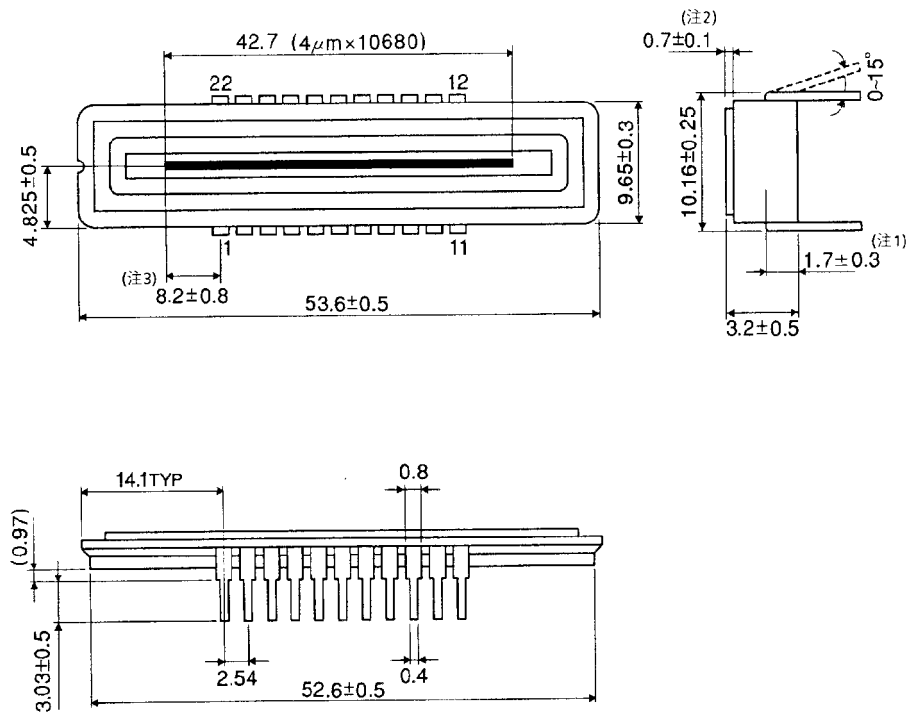
Soldering by the solder flow method cannot be guaranteed because this method may have deleterious effects on prevention of window glass soiling and heat resistance.

Using a soldering iron, complete soldering within ten seconds for lead temperatures of up to 260°C, or within three seconds for lead temperatures of up to 350°C.

Package Dimensions

WDIP22-G-400-2.54D (D)

Unit: mm



- (Note1): TOP OF CHIP TO BOTTOM OF PACKAGE  
(Note2): GLASS THICKNESS (n = 1.5)  
(Note3): No.1 SENSOR ELEMENT (S1) TO CENTER OF No.1 PIN.

Weight: 5.2 g (typ.)

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