

TOSHIBA C²MOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TCM8240MD

Ver 1.2

13/Nov/04

TENTATIVE

1.3 Mega pixel sensor chip

TCM8240MD is an area color image sensor, at 1.3 Mega-pixels of array resolution (1300x 1040), incorporating a camera signal processor. The optical format is 1/3.3 inch, of which small size is suitable for built-in camera module application. Use of the CMOS process makes possible low power consumption operations. This sensor provides superb picture quality thanks to Toshiba's advanced sensor technology and Toshiba's sophisticated signal processing technology.

Features

1. General

- Large flexibility in external clock frequency range by PLL operation (JPEG is not available in case of w/o PLL operation)
- Frame rate : up to 15 fps for every resolution
- Output data rate reduction for full 1.3 Mega resolution by JPEG compression
- Dual power supply : Either 2.5+/-0.2V or 2.8 +/- 0.2 V, and 1.6+/-0.1V
- Operation temperature : -20 to + 60 degree C
- Storage temperature: -30 to +85 degree C

2. Sensor

- Optical size : 1/3.3 inch optical format
- Effective pixel numbers : 1300(H) x 1040(V)
- Output pixel number : 1280(H) x1024 (V) maximum
- Pixel pitch : 3.3um(H)x3.3um(V) (square pixel)
- Image size : 4.29 mm(H) x 3.43mm(V)
- Color filter : Primary color filter, Bayer arrangement

3. Camera signal processing

- Digital output mode
Output terminals: 8bit parallel data output along with DCLK, HBLK, and VBLK
(1) YUV=4:2:2 or RGB=5:6:5 data (multiplexed 8bit parallel output)
(2) JPEG encoded data (8 bit parallel) for full 1.3 Mega data
- Multi-step digital zoom for downsized VGA, QVGA, QQVGA, CIF, QCIF and subQCIF
- Vertical and horizontal flip
- ALC (automatic luminance level control) with fluorescent flicker-less operation
- AWB (automatic white balance)
- Automatic blemish detection and correction
- Strobe pulse for flash trigger

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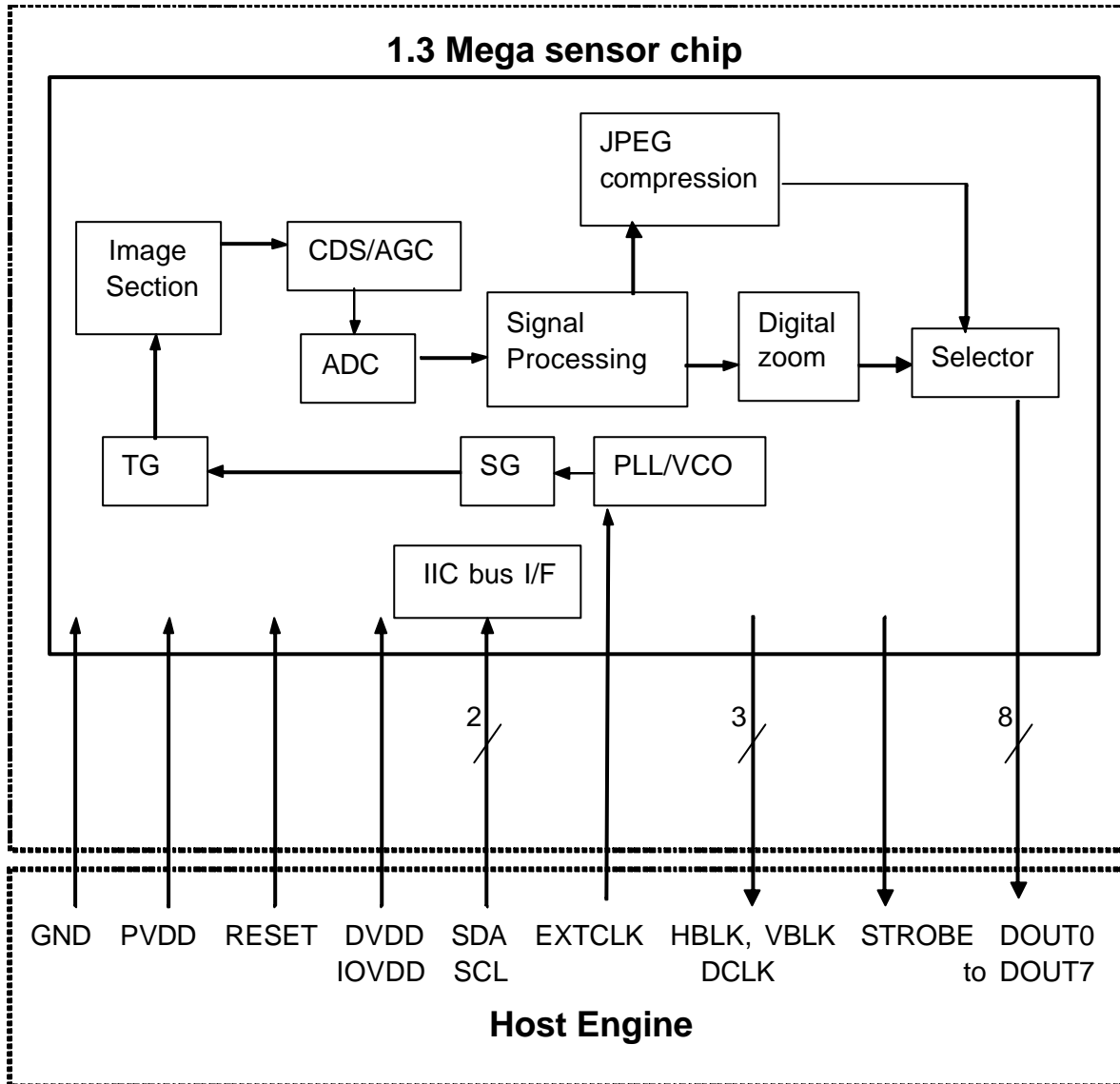
CHANGE HISTORY

| | |
|----------------------------------|-------------------------|
| Specifications draft V0.4 | December 9, '03 |
| Specifications draft V1.0 | October 14, '04 |
| Specifications draft V1.1 | October 14, '04 |
| Specifications draft V1.2 | November 13, '04 |

LIST OF ABBREVIATION

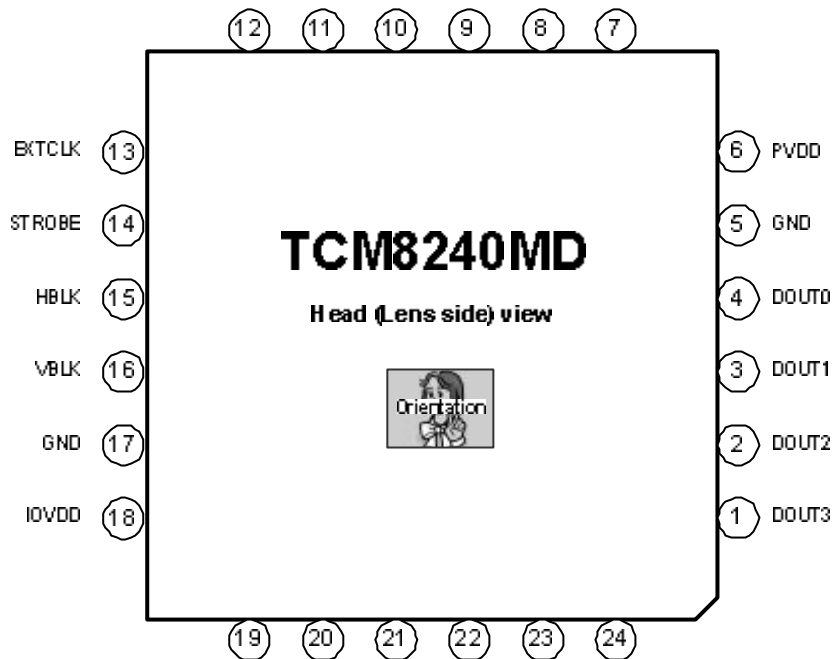
| | |
|-----|---------------------------------------|
| VGA | Video Graphic Array |
| CIF | Common Intermediate Format |
| CDS | Correlated Double Sampling |
| AGC | Automatic Gain Control |
| ADC | Analog to Digital Converter |
| TG | Timing Generator |
| SG | Sync Signal Generator |
| PLL | Phase Locked Loop |
| VCO | Voltage Controlled Oscillator |
| AWB | Automatic white Balance |
| OB | Optical black |
| ALC | Automatic Luminance level control |
| SOI | Start of Image (in JPEG data stream) |
| EOI | End of Image (in JPEG data stream) |
| MCU | Minimum Coded Unit |
| DQT | Define Quantization table |
| DHT | Define Huffman Table |
| SOF | Start of Frame |
| SOS | Start of Scan |
| DRI | Define Restart Interval |

BLOCK DIAGRAM



PIN DESCRIPTION

| PIN No. | SYMBOL | I/O | DESCRIPTION |
|---------|--------|-----|---------------------------------------|
| 1 | DOUT3 | O | Data output |
| 2 | DOUT2 | O | Data output |
| 3 | DOUT1 | O | Data output |
| 4 | DOUT0 | O | Data output (LSB) |
| 5 | GND | | GND |
| 6 | PVDD | I | Power supply 2.8+/-0.2V or 2.5+/-0.2V |
| 7 | RESET | I | Reset pulse to initialize |
| 8 | SCL | I | Clock for I2C bus |
| 9 | GND | | GND |
| 10 | SDA | I/O | Data for I2C bus |
| 11 | GND | | GND |
| 12 | DVDD | I | Power supply 1.8+/-0.1V |
| 13 | EXTCLK | I | External clock input |
| 14 | STROBE | O | Trigger pulse for flash strobe |
| 15 | HBLK | O | Horizontal data blanking period |
| 16 | VBLK | O | Vertical data blanking period |
| 17 | GND | | GND |
| 18 | IOVDD | I | Power supply 2.8+/-0.2V or 2.5+/-0.2V |
| 19 | DCLK | O | Clock for output data |
| 20 | GND | | GND |
| 21 | DOUT7 | O | Data output (MSB) |
| 22 | DOUT8 | O | Data output |
| 23 | DOUT5 | O | Data output |
| 24 | DOUT4 | O | Data output |



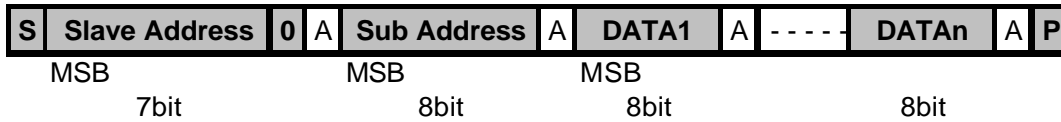
I/O INTERNAL CIRCUITS

| NAME | I/O | INTERFACE CIRCUIT |
|-----------------------------------------------|-----|-------------------|
| RESET | I | |
| SCL | I | |
| SDA | I/O | |
| EXTCLK | I | |
| DOUT0 to DOUT7, HBLK, VBLK, DCLK,STROBE | O | |

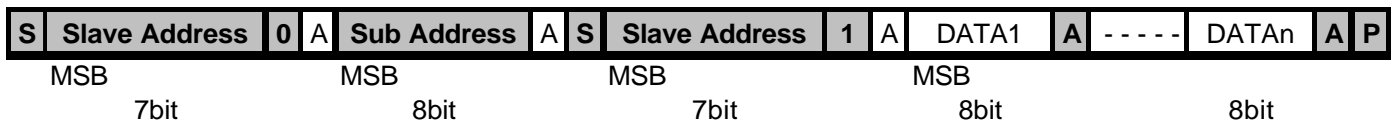
CONTROL I/F

TCM8240MD control interface configuration is based on fast mode IIC bus.
Register setting can be changed via IIC bus.

Write mode

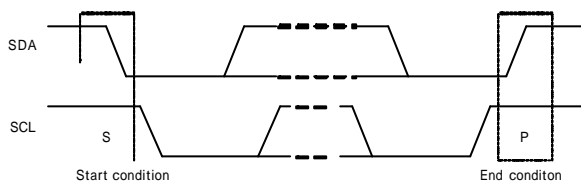


Read mode

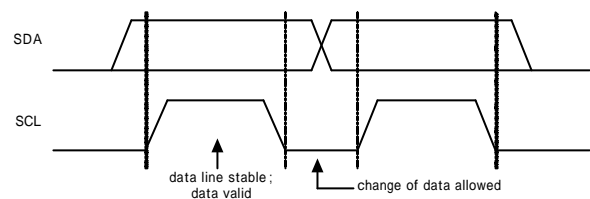


S : Start condition , P : End condition , A : Acknowledge, A : not Acknowledge

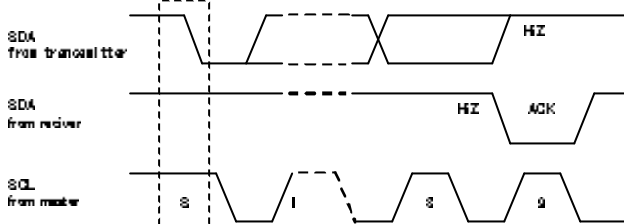
Start condition , End condition



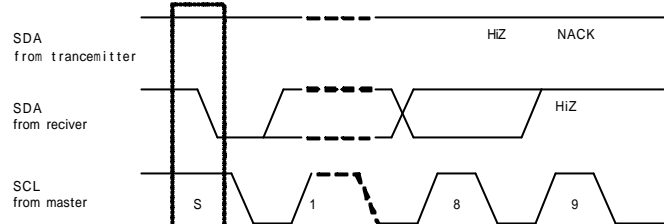
Bit Transfer



Acknowledge



Not Acknowledge



Slave address

| | | | | | | | |
|-----------|-----------|-----------|-----------|-----------|-----------|-----------|------------|
| A6 | A5 | A4 | A3 | A2 | A1 | A0 | R/W |
| 0 | 1 | 1 | 1 | 1 | 0 | 1 | 1/0 |

7bit Slave address is used.

Purchase of TOSHIBA I²C components conveys a license under the Philips I²C Patent Rights to use these components in an I²C system, provided that the system conforms to the I²C Standard Specification as defined by Philips.

INTERNAL REGISTER

| Address [Dec.] | Address [Hex.] | Data (D7) | (D6) | (D5) | (D4) | (D3) | (D2) | (D1) | (D0) | Initial [Hex.] |
|-------------------|-------------------|-----------------|--------------|---------------|---------------|----------------|--------------|---------------|----------|-------------------|
| 0 | 00 | | | | | | | | | 00 |
| 1 | 01 | | | | | | | | | 00 |
| 2 | 02 | STANDBYSW | SRST | | | | | | | 00 |
| 3 | 03 | | | | DCLKPOL | PLLMODE[3:0] | | | | C0 |
| 4 | 04 | DOUTOFF | JPEGON | PICMODE[1:0] | | SELRGB | PICSIZ[2:0] | | | 80 |
| 5 | 05 | FRM_SPD[1:0] | | | | | | | LRINV | 40 |
| 6 | 06 | UDINV | | | | | | | | 18 |
| 7 | 07 | | | | | | | | | 00 |
| 8 | 08 | | | | | | | | | 08 |
| 9 | 09 | | | | | | | | | 00 |
| 10 | 0A | | | | | | | | | 08 |
| 11 | 0B | | | | | | | | | 36 |
| 12 | 0C | | | | | | | | | 00 |
| 13 | 0D | | | | | VSUPCNT[1:0] | | | | 00 |
| 14 | 0E | | | | | | | | | AC |
| 15 | 0F | | | | | | | | | 00 |
| 16 | 10 | | | | | | | | | FA |
| 17 | 11 | | | | | | | | | 02 |
| 18 | 12 | | | | | | | | | 20 |
| 19 | 13 | | | | | | | | | B2 |
| 20 | 14 | | | | | | | | | 33 |
| 21 | 15 | | | | | | | | | 32 |
| 22 | 16 | | | | | | | | | 28 |
| 23 | 17 | | | | | | | | | 00 |
| 24 | 18 | | | | | | | | | 00 |
| 25 | 19 | | | | | | | | | 00 |
| 26 | 1A | H_COUNT[7:0] | | | | | | | | B3 |
| 27 | 1B | V_COUNT[3:0] | | | | | | H_COUNT[9:8] | | B2 |
| 28 | 1C | | | V_COUNT[9:4] | | | | | | A1 |
| 29 | 1D | | | F_COUNT[5:0] | | | | | | 00 |
| 30 | 1E | SP_COUNT[7:0] | | | | | | | | 00 |
| 31 | 1F | | | | | SP_COUNT[11:8] | | | | 04 |
| 32 | 20 | | | | | | | | | 73 |
| 33 | 21 | | | | | | | | | 01 |
| 34 | 22 | STSET_SW | STSET_POL | | | STSET_REG | ST_MODE[2:0] | | | 07 |
| 35 | 23 | | | | | STOUT_POL | STOUT_W[1:0] | ST_OUTSIG | | F0 |
| 36 | 24 | | | | | | | | | 5E |
| 37 | 25 | | | | | | | | | 10 |
| 38 | 26 | | | | | | | | | 01 |
| 39 | 27 | | | | | | | | | 32 |
| 40 | 28 | | | | | | | | | 40 |
| 41 | 29 | | | | | | | | | 58 |
| 42 | 2A | | | | | | | | | 20 |
| 43 | 2B | | | | | | | | | 10 |
| 44 | 2C | FRAME_LV[7:0] | | | | | | | | 00 |
| 45 | 2D | | CB_MODE[2:0] | | | | | FRAME_LV[9:8] | | 0E |
| 46 | 2E | DINSW | | | | | | | | 44 |
| 47 | 2F | | | | | | | | | 00 |
| 48 | 30 | | | | | | | | | 00 |
| 49 | 31 | APCSW | | | | | | | | 03 |
| 50 | 32 | | | | | | | | | FF |
| 51 | 33 | IDRS[1:0] | | AGMAX_PPED[0] | AGMIN_PPED[0] | PPEDB[0] | PPEDGB[0] | PPEDGR[0] | PPEDR[0] | 00 |
| 52 | 34 | PPEDR[8:1] | | | | | | | | 80 |
| 53 | 35 | PPEDGR[8:1] | | | | | | | | 78 |
| 54 | 36 | PPEDGB[8:1] | | | | | | | | 78 |
| 55 | 37 | PPEDB[8:1] | | | | | | | | 80 |
| 56 | 38 | AGMIN_PPED[8:1] | | | | | | | | 80 |
| 57 | 39 | AGMAX_PPED[8:1] | | | | | | | | 80 |
| 58 | 3A | | | | | | | | | 80 |
| 59 | 3B | | | | | | | | | 80 |
| 60 | 3C | | | | | | | | | 80 |
| 61 | 3D | | | | | | | | | 80 |
| 62 | 3E | PWB_R[7:0] | | | | | | | | 66 |
| 63 | 3F | PWB_GR[7:0] | | | | | | | | 80 |

The registers of gray mesh (unassigned registers) are not able to read and write via I²C bus.

“*” registers are read only.

Don't touch TESTMODE registers.

| Address [Dec] | Address [Hex] | Data (D7) | (D6) | (D5) | (D4) | (D3) | (D2) | (D1) | (D0) | Initial [Hex] |
|---------------|---------------|-----------------|-----------------|-----------------|--------------|---------------|-------------|--------------|------|---------------|
| 64 | 40 | PWB_GB[7:0] | | | | | | | | 80 |
| 65 | 41 | PWB_B[7:0] | | | | | | | | 96 |
| 66 | 42 | PWB_BM[1:0] | PWB_GBM[1:0] | PWB_GRM[1:0] | PWB_RM[1:0] | | | | | 41 |
| 67 | 43 | LSCSW | | | | | | | | 00 |
| 68 | 44 | LSC_RG[7:0] | | | | | | | | FF |
| 69 | 45 | LSC_GG[7:0] | | | | | | | | FF |
| 70 | 46 | LSC_BG[7:0] | | | | | | | | FF |
| 71 | 47 | HLCC_SW | | | | | | | | 84 |
| 72 | 48 | ALC_SW | F_AUTO_SW | F_AUTO_DLY[1:0] | ALC_SSW | ALC_CSW[2:0] | | | | 85 |
| 73 | 49 | ALCL[7:0] | | | | | | | | 50 |
| 74 | 4A | ALC_MODE[4:0] | | | | | | ALCL[9:8] | | 48 |
| 75 | 4B | ALC_DLY[1:0] | ALCH[5:0] | | | | | | | C7 |
| 76 | 4C | ALC_DLY[9:2] | | | | | | | | 00 |
| 77 | 4D | L8P100S[7:0] | | | | | | | | EE |
| 78 | 4E | ALC_SPD[3:0] | | | | L8P100S[11:8] | | | | 14 |
| 79 | 4F | L8P120S[7:0] | | | | | | | | 1C |
| 80 | 50 | ALC_HOLD | | | | L8P120S[11:8] | | | | 04 |
| 81 | 51 | EVS_MIN[7:0] | | | | | | | | 00 |
| 82 | 52 | EVS_SW[1:0] | EVS_CUDSW | | | | | EVS_MIN[9:8] | | 20 |
| 83 | 53 | EVS_MAX[7:0] | | | | | | | | FF |
| 84 | 54 | EVS_MODE[4:0] | | | | | | EVS_MAX[9:8] | | 03 |
| 85 | 55 | HS_ES_LIM[2:0] | | | | MHSS[3:0] | | | | 80 |
| 86 | 56 | MES[7:0] | | | | | | | | 3B |
| 87 | 57 | MES[15:8] | | | | | | | | 01 |
| 88 | 58 | LS_ES_LIM[3:0] | | | | | | MES[17:16] | | 50 |
| 89 | 59 | MDG[7:0] | | | | | | | | 00 |
| 90 | 5A | AG_MIN[7:0] | | | | | | | | 3F |
| 91 | 5B | AG_MAX[7:0] | | | | | | | | E7 |
| 92 | 5C | MAG[7:0] | | | | | | | | 80 |
| 93 | 5D | ALC_AG_POLE | | | | | | MAG[9:8] | | 03 |
| 94 | 5E | ASC_AG[7:0] | | | | | | | | 00 |
| 95 | 5F | ACDET_SW | AC5060HZ | ACDET_DLY[1:0] | | | | ASC_AG[9:8] | | 43 |
| 96 | 60 | | | | | | | | | 08 |
| 97 | 61 | | | | | | | | | 08 |
| 98 | 62 | | | | | | | | | 00 |
| 99 | 63 | | | | | | | | | 80 |
| 100 | 64 | | | | | | | | | 00 |
| 101 | 65 | IDRE_SW | | | IDRE_CR[1:0] | IDRE_CL[1:0] | | | | 80 |
| 102 | 66 | APBC_SW | PBC_SW[3:0] | | | | | | | D8 |
| 103 | 67 | PBC_MODE[7:0] | | | | | | | | BF |
| 104 | 68 | PBC1LV[7:0] | | | | | | | | 10 |
| 105 | 69 | PBC2LV[7:0] | | | | | | | | 10 |
| 106 | 6A | PBC3LV[7:0] | | | | | | | | 60 |
| 107 | 6B | PBC4LV[7:0] | | | | | | | | 18 |
| 108 | 6C | VDS_HLPFSW[1:0] | HDS_VLPFSW[1:0] | | | | | | | 02 |
| 109 | 6D | AWB_SW | AWB_MODE[1:0] | AWB_LOCK | | | | | | 21 |
| 110 | 6E | AWB_WAIT[1:0] | YLCUT_SW | RGCUT_SW | | | AWB_PN[2:0] | | | 06 |
| 111 | 6F | | | | | | | | | 00 |
| 112 | 70 | | | | | | | | | 40 |
| 113 | 71 | | | | | | | | | C0 |
| 114 | 72 | | | | | | | | | 80 |
| 115 | 73 | | | | | | | | | 80 |
| 116 | 74 | | | | | | | | | 80 |
| 117 | 75 | | | | | | | | | 88 |
| 118 | 76 | | | | | | | | | 10 |
| 119 | 77 | | | | | | | | | F0 |
| 120 | 78 | YLCUT_L[7:0] | | | | | | | | 40 |
| 121 | 79 | YLCUT_H[7:0] | | | | | | | | C0 |
| 122 | 7A | UVIS_NC[7:0] | | | | | | | | 08 |
| 123 | 7B | AWB_SSP[7:0] | | | | | | | | FF |
| 124 | 7C | AWB_MSP[7:0] | | | | | | | | FF |
| 125 | 7D | WBG_SMIN[7:0] | | | | | | | | 33 |
| 126 | 7E | WBG_SMAX[7:0] | | | | | | | | 50 |
| 127 | 7F | WBG_MMIN[7:0] | | | | | | | | 20 |

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 Don't touch TESTMODE registers.

| Address [Dec.] | Address [Hex.] | Data (D7) | (D6) | (D5) | (D4) | (D3) | (D2) | (D1) | (D0) | Initial [Hex.] |
|-------------------|-------------------|---------------|------|--------------|------|---------------|------|------|------|-------------------|
| 128 | 80 | WBG_MMAX[7:0] | | | | | | | | 80 |
| 129 | 81 | WB_MRG[7:0] | | | | | | | | 40 |
| 130 | 82 | WB_MBG[7:0] | | | | | | | | 40 |
| 131 | 83 | ST_MRG[7:0] | | | | | | | | 40 |
| 132 | 84 | ST_MBG[7:0] | | | | | | | | 40 |
| 133 | 85 | | | | | | | | | 00 |
| 134 | 86 | CLM_G[7:0] | | | | | | | | 80 |
| 135 | 87 | CLM_S[7:0] | | | | | | | | 80 |
| 136 | 88 | CLM_MIN[7:0] | | | | | | | | 00 |
| 137 | 89 | CLM_MAX[7:0] | | | | | | | | FF |
| 138 | 8A | YUV_G[7:0] | | | | | | | | 00 |
| 139 | 8B | YUV_S[7:0] | | | | | | | | 00 |
| 140 | 8C | YUV_MIN[7:0] | | | | | | | | 00 |
| 141 | 8D | YUV_MAX[7:0] | | | | | | | | 00 |
| 142 | 8E | | | | | | | | | 80 |
| 143 | 8F | | | | | | | | | 80 |
| 144 | 90 | UV_G[7:0] | | | | | | | | 80 |
| 145 | 91 | UV_S[7:0] | | | | | | | | 80 |
| 146 | 92 | | | | | | | | | 00 |
| 147 | 93 | CCB_SW | | | | | | | | A0 |
| 148 | 94 | | | | | | | | | 05 |
| 149 | 95 | SCLPFG[7:0] | | | | | | | | 80 |
| 150 | 96 | CBGMIN_L[7:0] | | | | | | | | A0 |
| 151 | 97 | CBGMIN_H[7:0] | | | | | | | | E0 |
| 152 | 98 | CBU_YL[7:0] | | | | | | | | 60 |
| 153 | 99 | CBD_YL[7:0] | | | | | | | | A8 |
| 154 | 9A | LCSMODE[3:0] | | | | | | | | 03 |
| 155 | 9B | | | | | | | | | 60 |
| 156 | 9C | | | | | | | | | 60 |
| 157 | 9D | LPFMODE | | | | RGBLPFSW[3:0] | | | | 05 |
| 158 | 9E | LPF_FC[7:0] | | | | | | | | 80 |
| 159 | 9F | CLM_ANRSW | | | | | | | | 00 |
| 160 | A0 | CLM_GC[7:0] | | | | | | | | 08 |
| 161 | A1 | CLM_RMG[7:0] | | | | | | | | 80 |
| 162 | A2 | CLM_RMB[7:0] | | | | | | | | 40 |
| 163 | A3 | CLM_GMR[7:0] | | | | | | | | 80 |
| 164 | A4 | CLM_GMB[7:0] | | | | | | | | 80 |
| 165 | A5 | CLM_BMR[7:0] | | | | | | | | 40 |
| 166 | A6 | CLM_BMG[7:0] | | | | | | | | 80 |
| 167 | A7 | MWB_RG[7:0] | | | | | | | | 80 |
| 168 | A8 | MWB_BG[7:0] | | | | | | | | 80 |
| 169 | A9 | ABB_SW | | | | | | | | 07 |
| 170 | AA | | | | | | | | | 80 |
| 171 | AB | | | | | | | | | 00 |
| 172 | AC | | | | | | | | | 00 |
| 173 | AD | | | | | | | | | 00 |
| 174 | AE | | | | | | | | | 80 |
| 175 | AF | | | | | | | | | 00 |
| 176 | B0 | | | | | | | | | 00 |
| 177 | B1 | | | | | | | | | 80 |
| 178 | B2 | R_BKLV[7:0] | | | | | | | | 00 |
| 179 | B3 | | | | | R_BKLV[11:8] | | | | 08 |
| 180 | B4 | G_BKLV[7:0] | | | | | | | | 00 |
| 181 | B5 | | | | | G_BKLV[11:8] | | | | 08 |
| 182 | B6 | B_BKLV[7:0] | | | | | | | | 00 |
| 183 | B7 | | | | | B_BKLV[11:8] | | | | 08 |
| 184 | B8 | GAM_SW[1:0] | | GAM_SCW[5:0] | | | | | | FF |
| 185 | B9 | | | GAM_SCH[5:0] | | | | | | 00 |
| 186 | BA | | | MCC_RMG[5:0] | | | | | | 00 |
| 187 | BB | | | MCC_RMB[5:0] | | | | | | 00 |
| 188 | BC | | | MCC_GMR[5:0] | | | | | | 00 |
| 189 | BD | | | MCC_GMB[5:0] | | | | | | 00 |
| 190 | BE | | | MCC_BMR[5:0] | | | | | | 00 |
| 191 | BF | | | MCC_BMG[5:0] | | | | | | 00 |

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|-------------------|-------------------|-----------------|---------------|-----------------|------------|-------------|----------|-------------|----------|-------------------|
| 192 | C0 | HDCVHSW | | | | HDCVH_PC | | | | 88 |
| 193 | C1 | HDCVH_NC[7:0] | | | | | | | | 0F |
| 194 | C2 | HDCVH_G[7:0] | | | | | | | | 40 |
| 195 | C3 | HDCHSW | | HDCH_FS[1:0] | | HDCH_PC | | | | 08 |
| 196 | C4 | HDCH_NC[7:0] | | | | | | | | 00 |
| 197 | C5 | HDCH_G[7:0] | | | | | | | | 00 |
| 198 | C6 | HDCMHSW | HDCMH_FS[2:0] | | | HDCMH_PC | | | | 08 |
| 199 | C7 | HDCMH_NC[7:0] | | | | | | | | 00 |
| 200 | C8 | HDCMH_G[7:0] | | | | | | | | 00 |
| 201 | C9 | VDC_PG[1:0] | | | | VDC_PC | | | | 08 |
| 202 | CA | VDC_NC[7:0] | | | | | | | | 0F |
| 203 | CB | VDC_G[7:0] | | | | | | | | 40 |
| 204 | CC | | | | | | | | | 36 |
| 205 | CD | HDC_PL[7:0] | | | | | | | | 60 |
| 206 | CE | VDC_PL[7:0] | | | | | | | | 60 |
| 207 | CF | HDC_MG[7:0] | | | | | | | | 48 |
| 208 | D0 | VDC_MG[7:0] | | | | | | | | 60 |
| 209 | D1 | | | | | | | | | 00 |
| 210 | D2 | | | | | | | | | 00 |
| 211 | D3 | NEPO | | Y_MATSW | DA_MODE | | | | | 38 |
| 212 | D4 | UV_ACSSW | | CONTRAST_R[5:0] | | | | | | 20 |
| 213 | D5 | | | CONTRAST_G[5:0] | | | | | | 20 |
| 214 | D6 | | | CONTRAST_B[5:0] | | | | | | 20 |
| 215 | D7 | CONTRAST_Y[7:0] | | | | | | | | 40 |
| 216 | D8 | SEPIA | | BRIGHT_R[5:0] | | | | | | 10 |
| 217 | D9 | | | BRIGHT_G[5:0] | | | | | | 10 |
| 218 | DA | | | BRIGHT_B[5:0] | | | | | | 10 |
| 219 | DB | BRIGHT_Y[7:0] | | | | | | | | 90 |
| 220 | DC | | RMYA[6:0] | | | | | | | 40 |
| 221 | DD | RMYG[7:0] | | | | | | | | B6 |
| 222 | DE | | BMYA[6:0] | | | | | | | 40 |
| 223 | DF | BMYG[7:0] | | | | | | | | 8F |
| 224 | E0 | | AVGSW | ZOOMMODE[5:0] | | | | | | 80 |
| 225 | E1 | ZHCORE[2:0] | | | ZHDTL[4:0] | | | | | 88 |
| 226 | E2 | ZVCORE[2:0] | | | ZVDTL4:0] | | | | | 88 |
| 227 | E3 | | | | | | | | | 00 |
| 228 | E4 | | | | | | | | | 80 |
| 229 | E5 | | | | | | | | | 10 |
| 230 | E6 | | | | | | | | | 00 |
| 231 | E7 | | | | | | | | | 00 |
| 232 | E8 | | | | | | | | | 00 |
| 233 | E9 | DYQTG[7:0] | | | | | | | | 10 |
| 234 | EA | DUVQTG[7:0] | | | | | | | | 10 |
| 235 | EB | | | | | | | | | 00 |
| 236 | EC | | | | | | | | | 00 |
| 237 | ED | | | | | | | | | 00 |
| 238 | EE | | | VQTSEL[1:0] | | UQTSEL[1:0] | | YQTSEL[1:0] | | 14 |
| 239 | EF | | | VHTSELAC | VHTSELDC | UHTSELAC | UHTSELDC | YHTSELAC | YHTSELDC | 3C |
| 240 | F0 | DRI[15:8] | | | | | | | | 00 |
| 241 | F1 | DRI[7:0] | | | | | | | | 00 |
| 242 | F2 | | | | | | | | | 00 |
| 243 | F3 | | | | | | | | | 00 |
| 244 | F4 | | | | | | | | | 00 |
| 245 | F5 | | | | | | | | | 00 |
| 246 | F6 | ENCDCNT[23:16] | | | | | | | | 00 |
| 247 | F7 | ENCDCNT[15:8] | | | | | | | | 00 |
| 248 | F8 | ENCDCNT[7:0] | | | | | | | | 00 |
| 249 | F9 | | | | | | | | | 00 |
| 250 | FA | FULL_ERRN | ENC_ERRN | | | | | | | 00 |
| 251 | FB | | | | | | | | | 00 |
| 252 | FC | | | | | | | | | 00 |
| 253 | FD | | | | | | | | | 00 |
| 254 | FE | | | | | | | | | 00 |
| 255 | FF | | | | | | | | | 00 |

The registers of gray mesh (unassigned registers) are not able to read and write via I²C bus.

“*” registers are read only.

Don't touch TESTMODE registers.

OUTLINE OF INTERNAL REGISTER

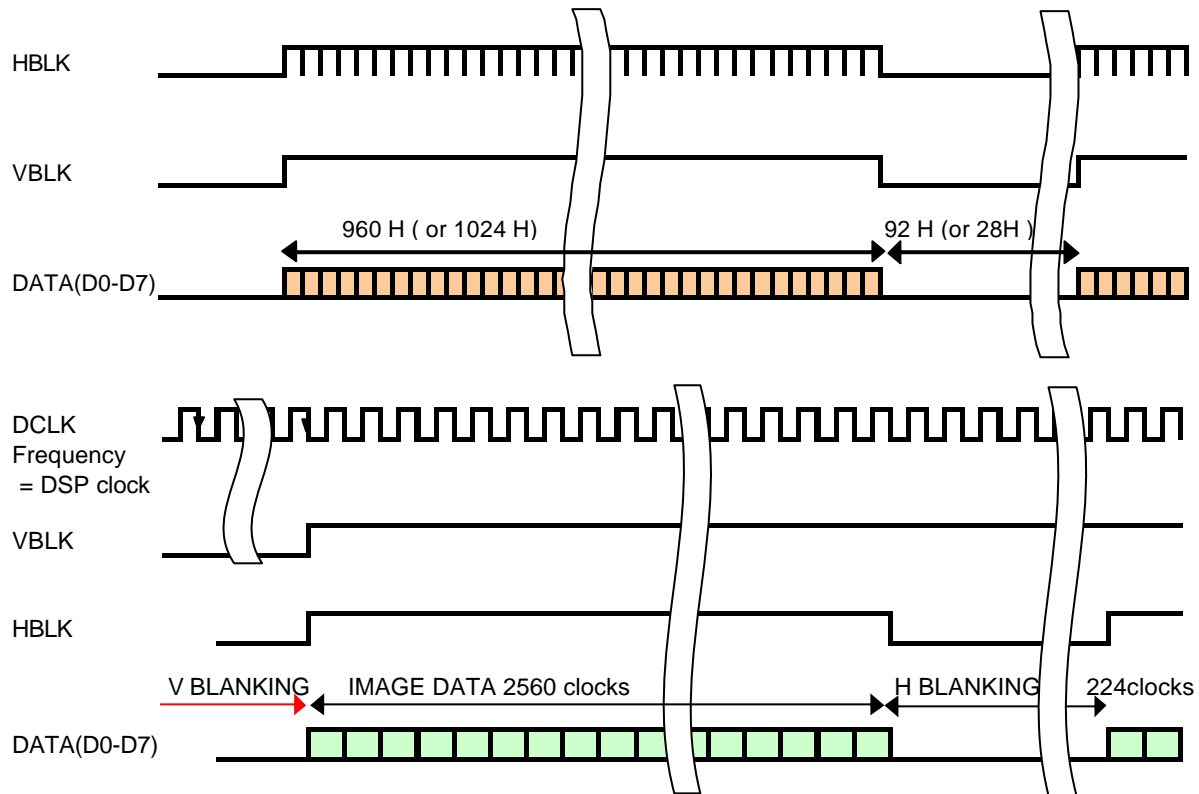
- * Frame rate setting (15ps, 7.5fps)
- * Picture size setting of digital output (4VGA, SXCA, VGA, QVGA, QQVGA, CIF, QCIF, subQCIF)
- * Selection of digital data output format (8bit YUV422, RGB565)
- * JPEG ON/OFF
- * Color signal adjustment (Carrier boost, Linear matrix, YUV matrix, saturation, etc.)
- * Luminance signal adjustment (Contrast, Brightness, Gamma, H,V edge enhancement)
- * ALC(Automatic Luminance level Control) ON/OFF
- * ALC mode setting (area selection, speed selection, flicker reduction mode setting)
- * AWB ON/OFF
- * Vertical and Horizontal flip
- * Standby mode setting
- * Some kinds of correction setting (Lens shading correction etc.)

8bit parallel image data

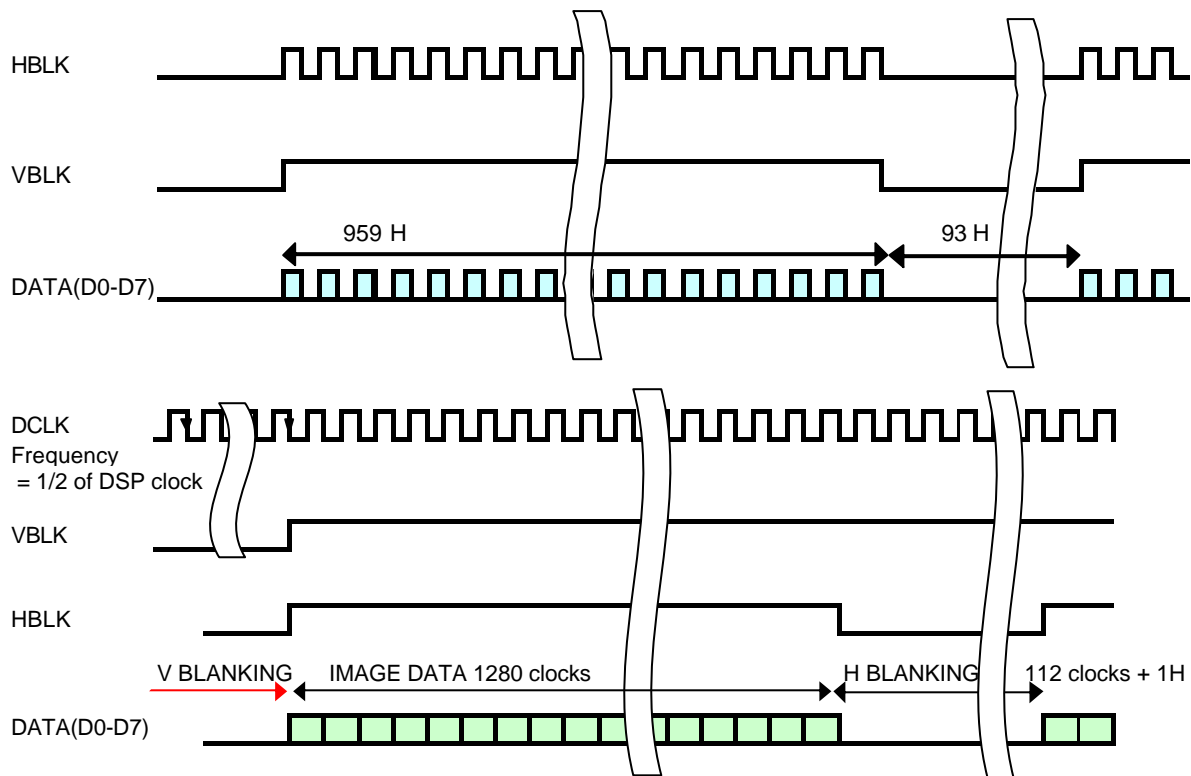
| | YUV mode | | | | RGB mode | |
|-------|----------|-------|-------|---------|----------|-----|
| | 1st | 2nd | 3rd | 4th | 1st | 2nd |
| DOUT0 | U0(n) | Y0(n) | V0(n) | Y0(n+1) | B0 | G3 |
| DOUT1 | U1(n) | Y1(n) | V1(n) | Y1(n+1) | B1 | G4 |
| DOUT2 | U2(n) | Y2(n) | V2(n) | Y2(n+1) | B2 | G5 |
| DOUT3 | U3(n) | Y3(n) | V3(n) | Y3(n+1) | B3 | R0 |
| DOUT4 | U4(n) | Y4(n) | V4(n) | Y4(n+1) | B4 | R1 |
| DOUT5 | U5(n) | Y5(n) | V5(n) | Y5(n+1) | G0 | R2 |
| DOUT6 | U6(n) | Y6(n) | V6(n) | Y6(n+1) | G1 | R3 |
| DOUT7 | U7(n) | Y7(n) | V7(n) | Y7(n+1) | G2 | R4 |

DATA OUTPUT TIMING CHART
 Timing chart for each output picture size

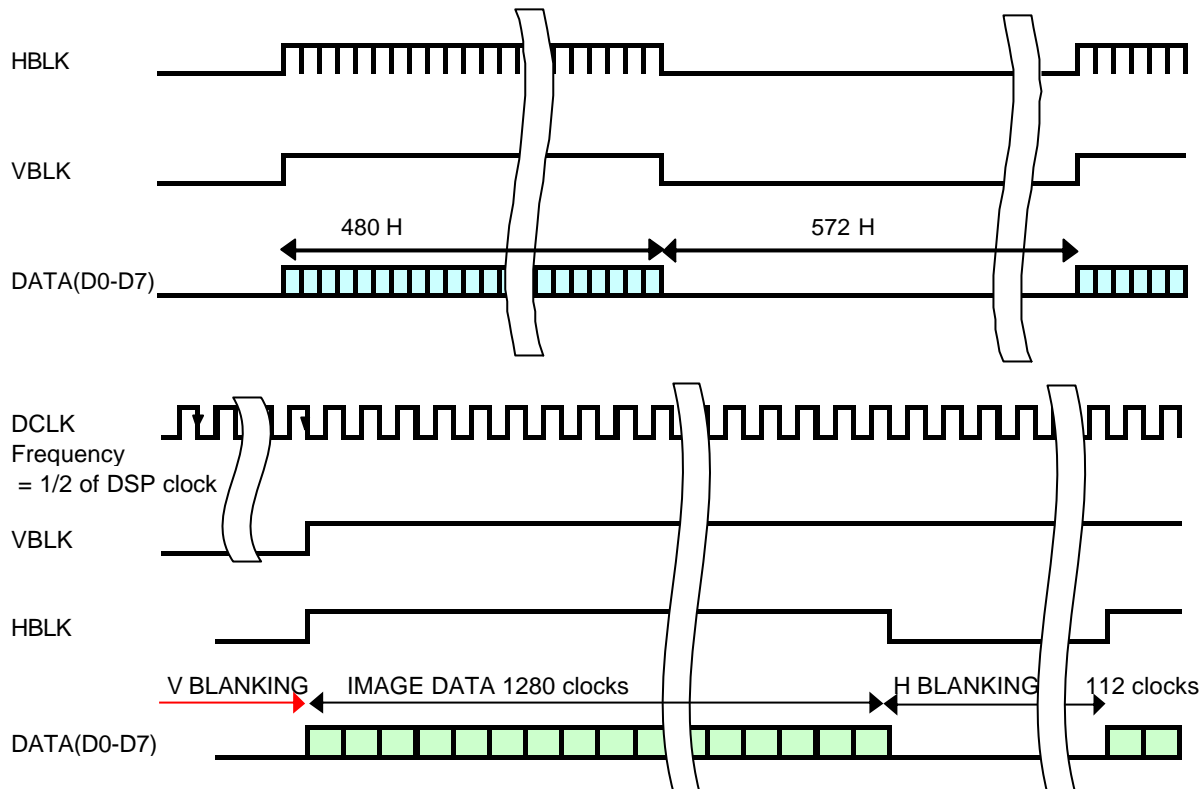
Full Mega output without JPEG



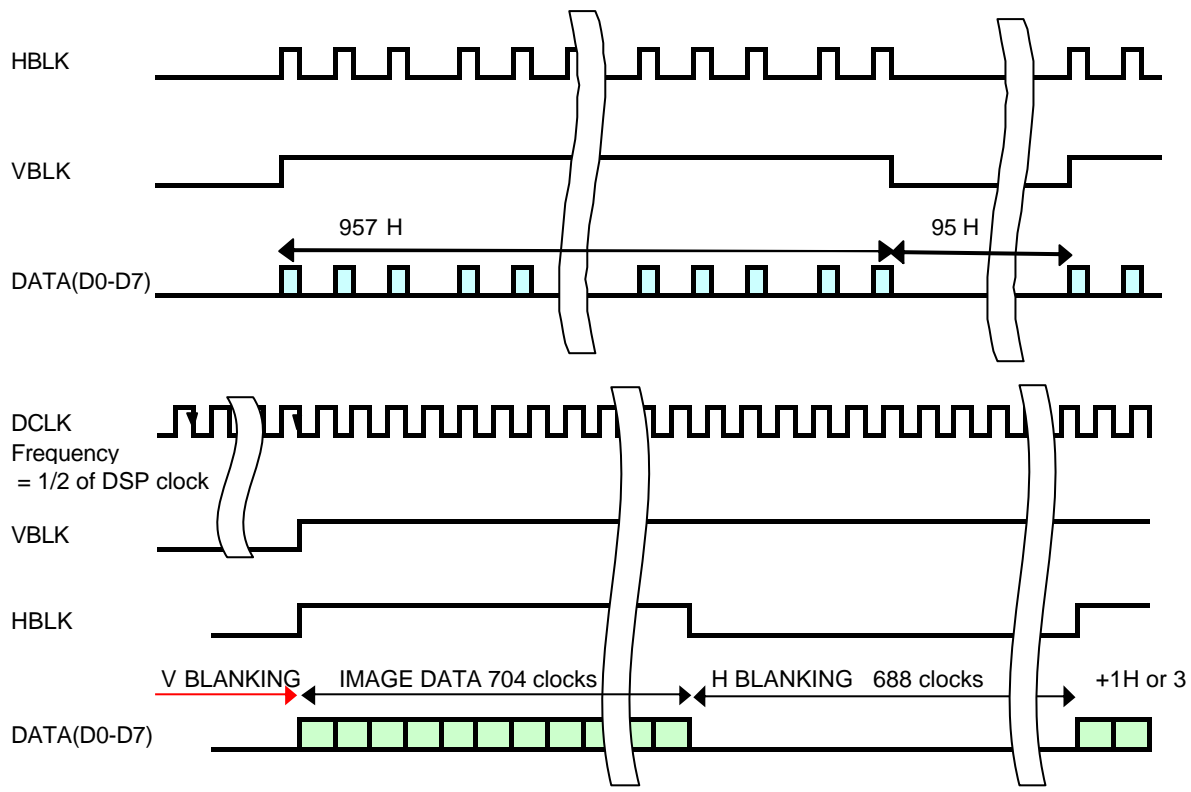
VGA (x1: no zooming)



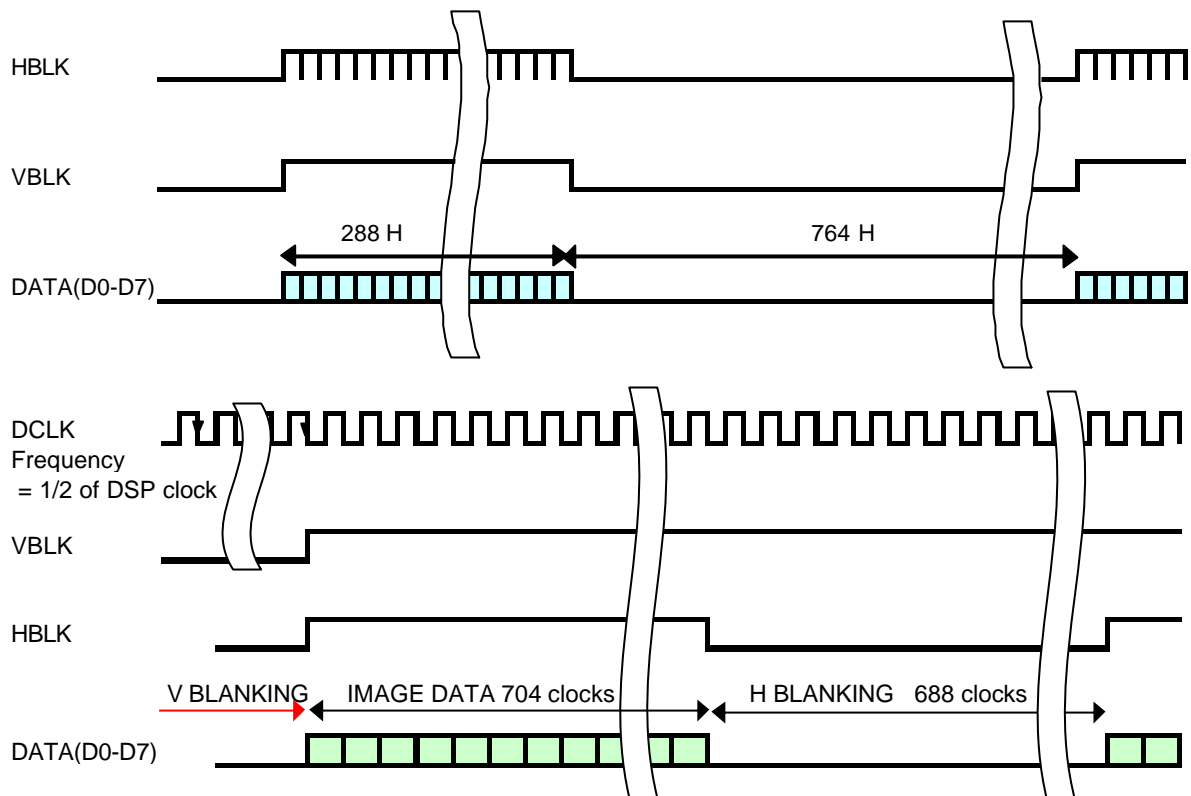
VGA (at maximum magnification x2)



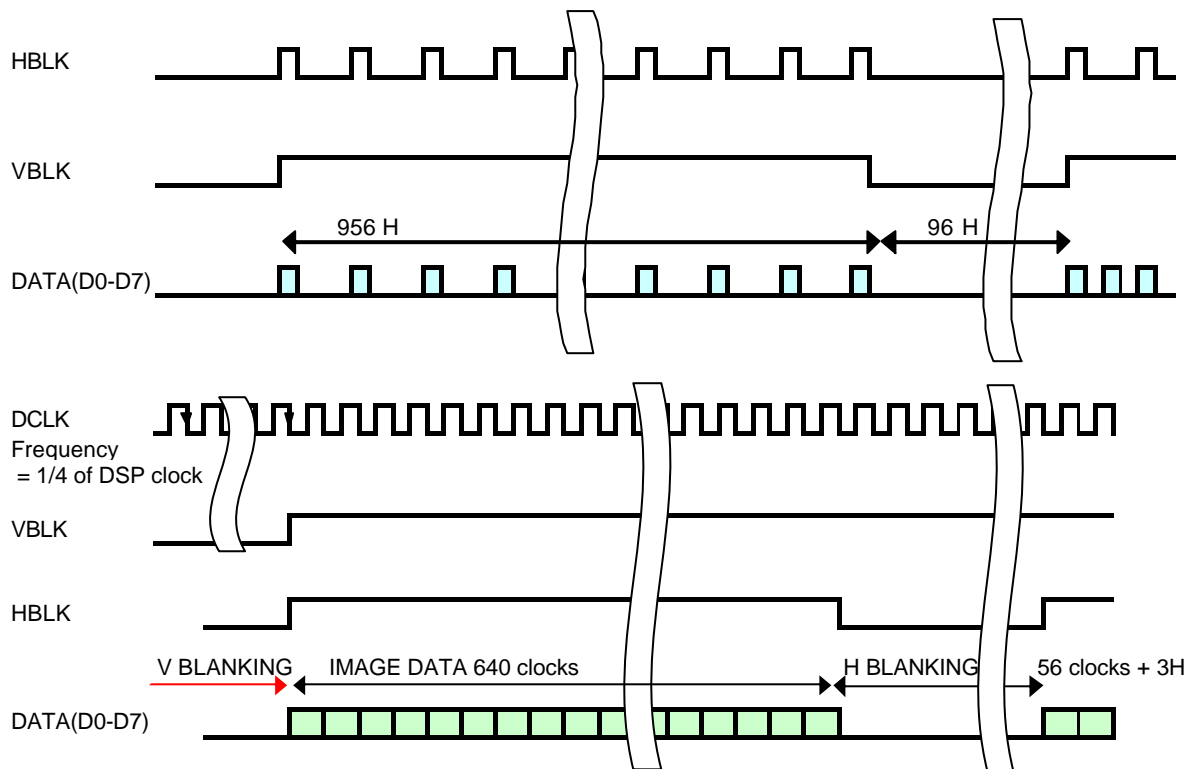
CIF (x1: no zooming)



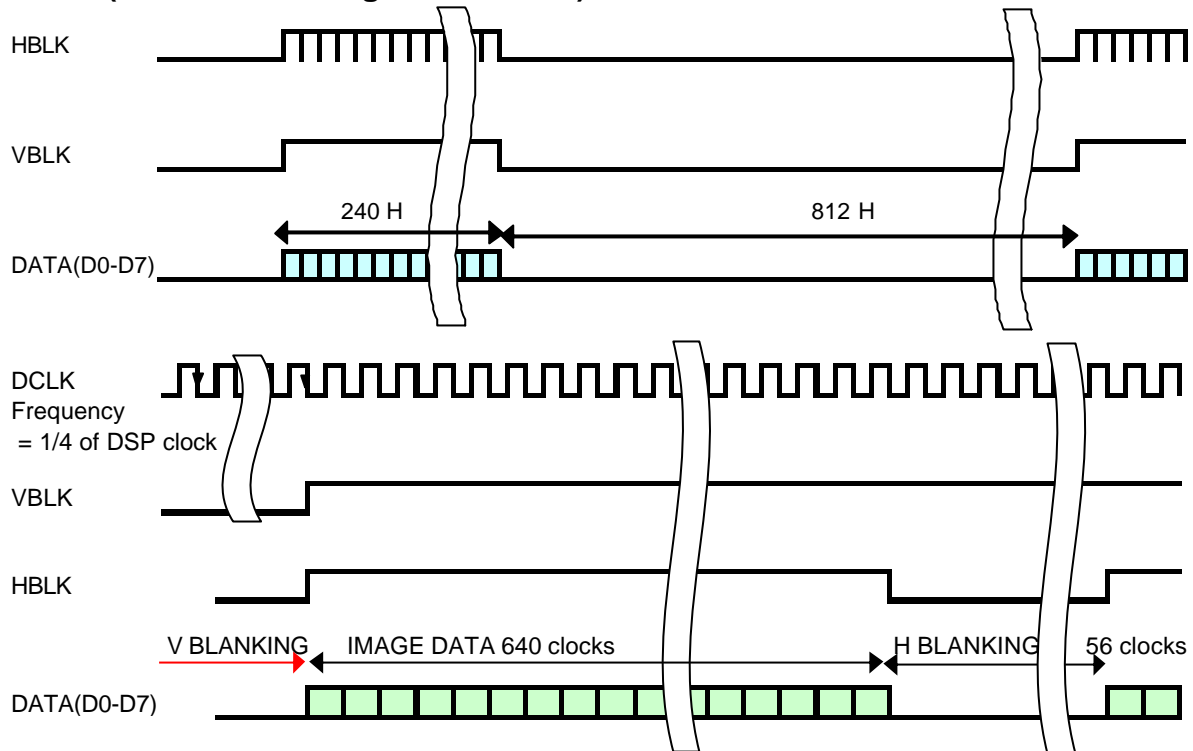
CIF (at maximum magnification)



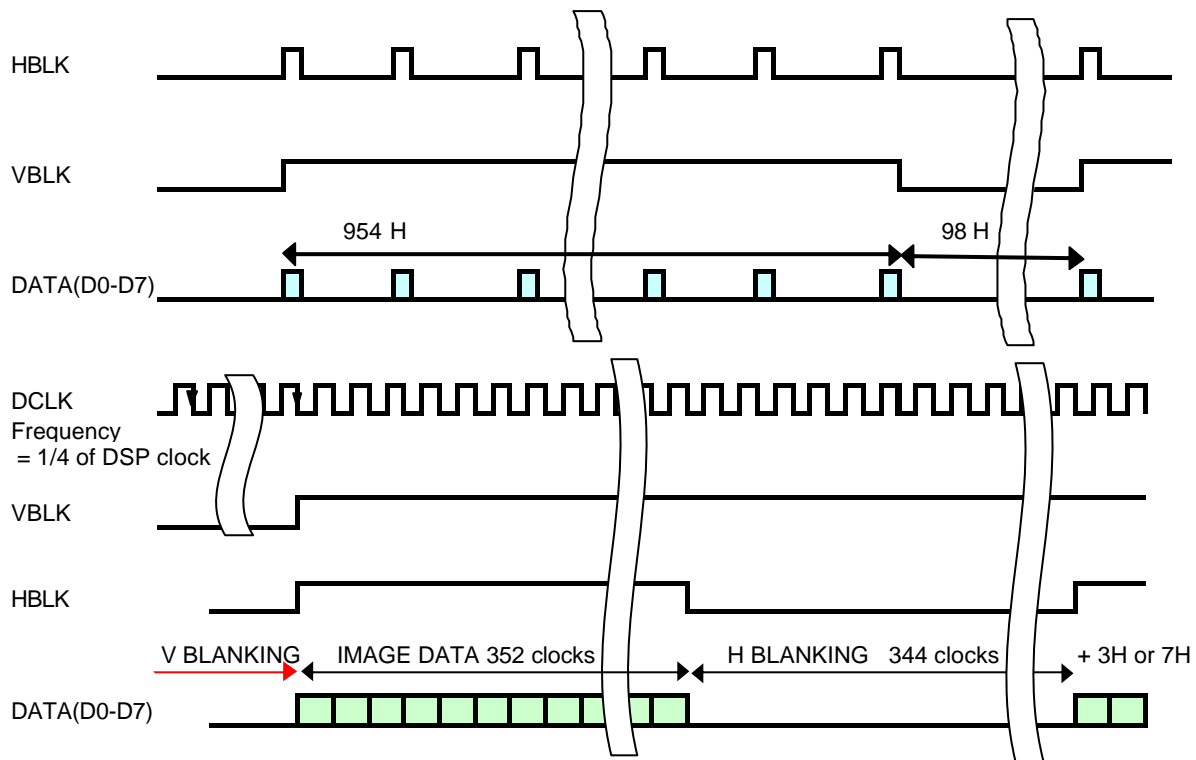
QVGA (x1: no digital zooming)



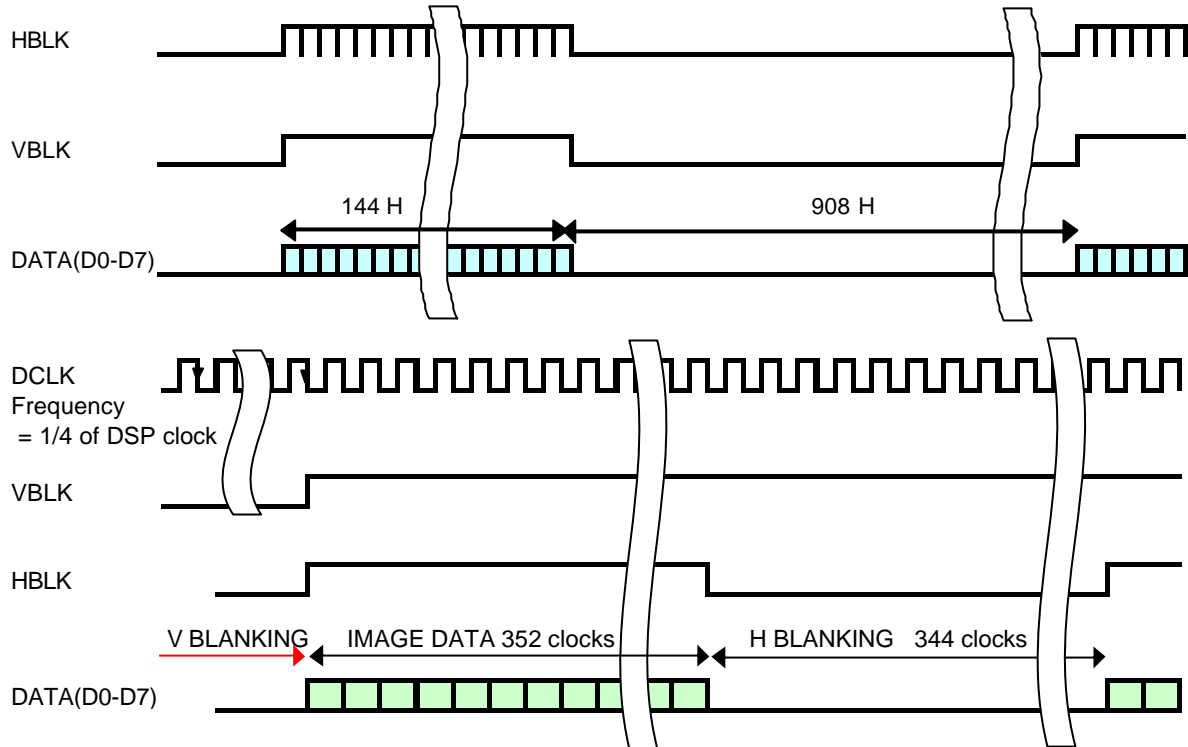
QVGA (at maximum magnification. X4)



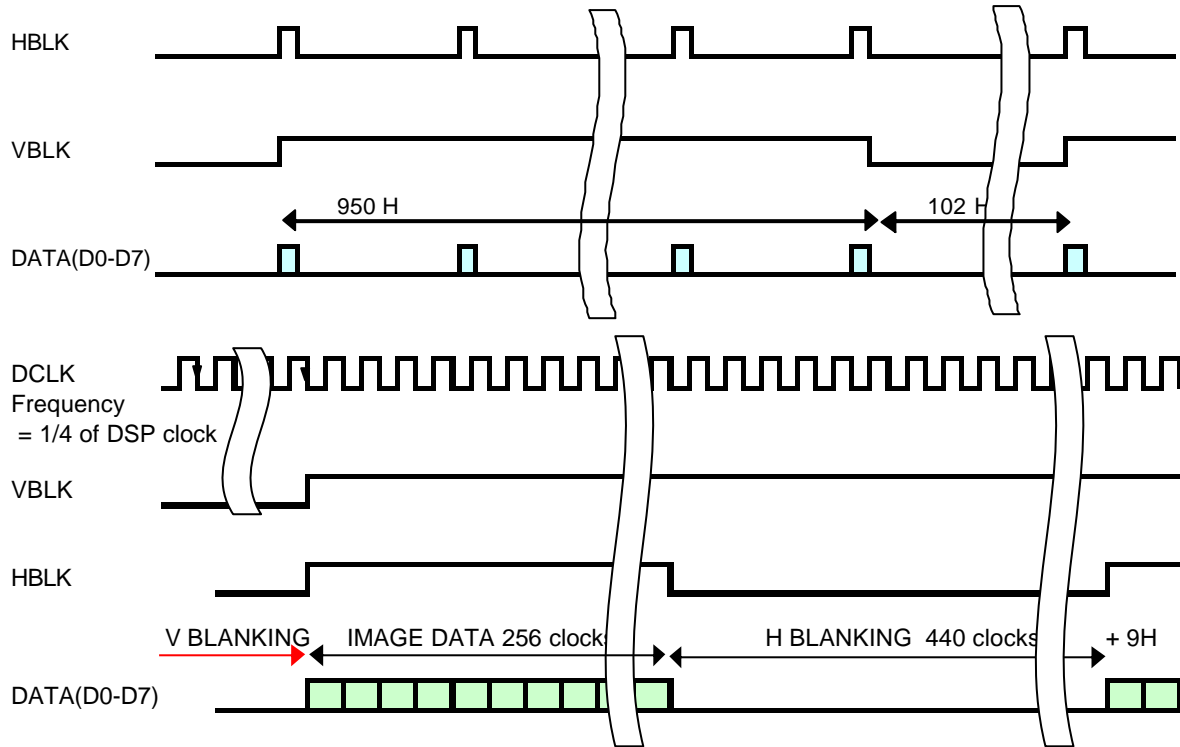
QCIF (x1: no digital zooming)



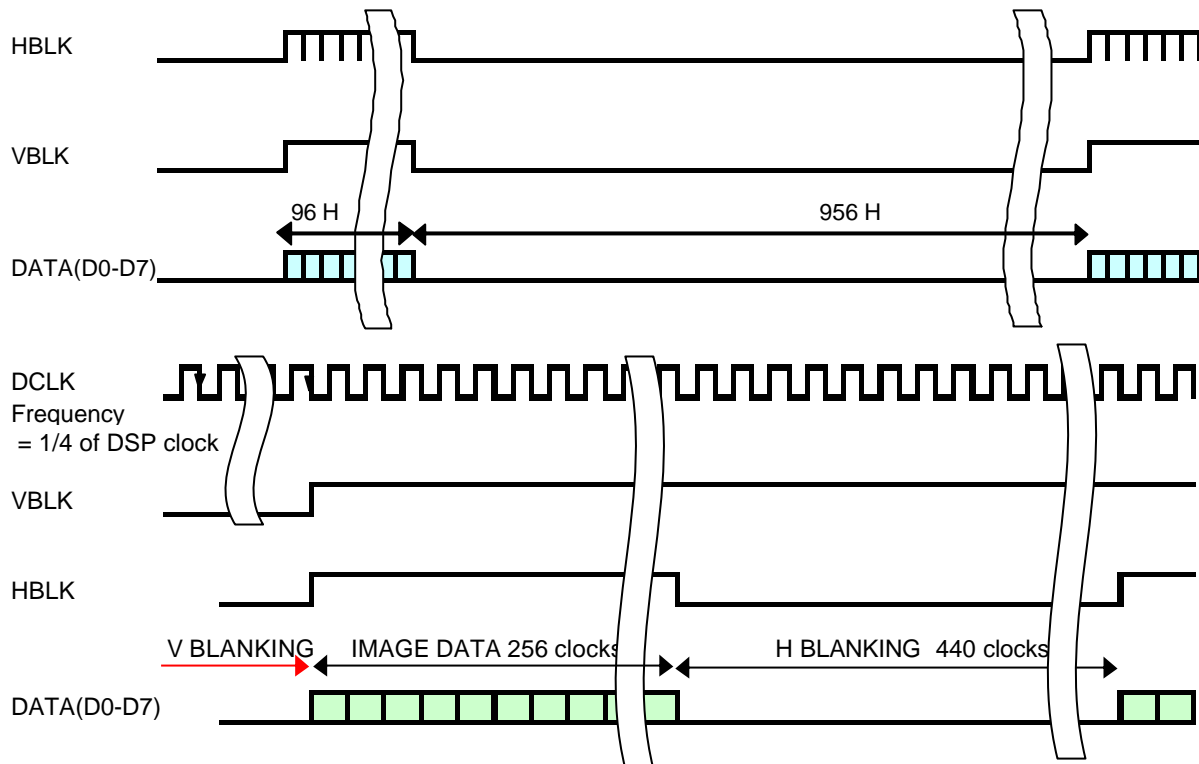
QCIF (at maximum magnification : x 6.67)



subQCIF (x1: no digital zooming)

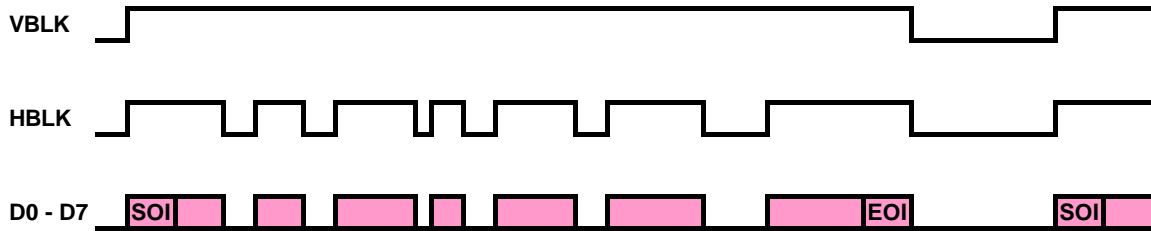


subQCIF (at maximum magnification: x 10)



Remark: the downsized picture has generally intermittent output by line, but in a horizontal line the image data are put together to form a continuous stream.

JPEG encoded full Mega

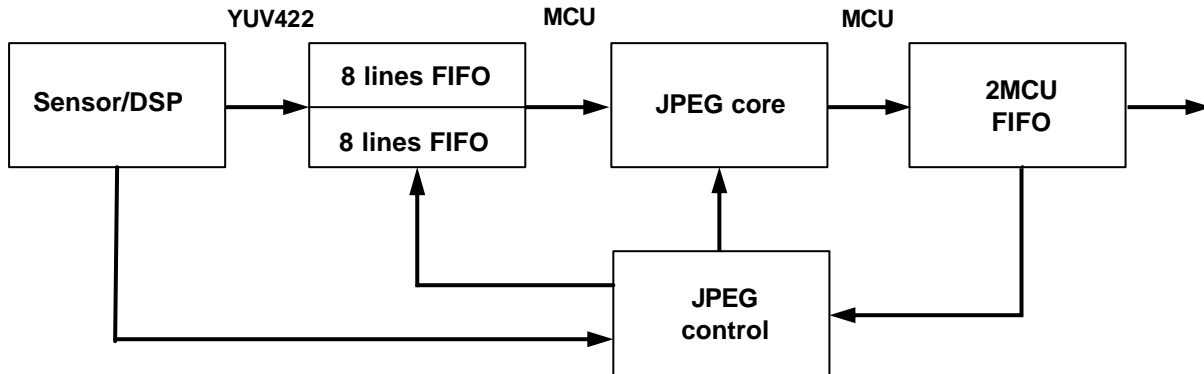


JPEG encoded data contains the standardized marker codes such as SOI and EOI. HBLK is set to high when JPEG data are output. The data length of one packet is multiple of MCU. It is using 8 lines buffer memories (FIFO) when JPEG encoding. It is limited for the writing not to surpass the reading because the writing speed is earlier than the reading speed. It is not limitation for low level period of HBLK. Also, following register setting, it is available to output by 4 bytes unit (multiple). HBLK is for data enable and high level period continues clock of 4 multiples. It is not limitation for low level period of HBLK. Also, when the JPEG data of 1V period is not 4 multiples, the data of address A5h makes to add after address FFh and address D9h because it needs to become 4 multiples.

* Setting of reading 4 bytes unit
Address E6h D[3] J4BYTESW “High” setting: JPEG output by 4 bytes unit

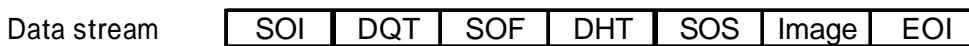
JPEG DATA FORMAT

Block diagram



JPEG data structure

The following figure shows JPEG data structure.



| | | |
|------------|-----------------|--------------------------|
| SOI | Marker code | 16'hFFD8 |
| DQT | Marker code | 16'hFFDB |
| SOF | Marker code | 16'hFFC0 |
| DHT | Marker code | 16'hFFC4 |
| SOS | Marker code | 16'hFFDA |
| Image data | MCU1 ~ MCU10240 | (for 1280 x 1024 pixels) |
| EOI(16bit) | Marker code | 16'hFFD9 |

The following tables show the data structure of DQT,SOF,DHT and SOS respectively.

The host can adjust the picture quality mode (namely compression ratio) by sending a specific quantization table or by sending Q table gain via IIC bus.

The JPEG encoded data are once stored an internal FIFO memory before outputting.

When data overflow in FIFO happens due to locally increased JPEG data (locally very low compression) , data transmission is stopped after FE code addition and an error flag is written in the register table.

After the host accesses the error flag register, the error flag is automatically reset.

DQT structure

| | Code (Hex) | Meaning |
|-----|------------|----------------------------|
| +00 | FF | Marker Prefix |
| +01 | DB | DQT |
| +02 | 00 | Length of field |
| | C5 | 2+(1+64)*3=197 (Byte) |
| +04 | 00 | Y: Pq=0, Nq=0 |
| +05 | : | Quantization table Y : Q0 |
| | : | : |
| | : | : |
| | : | : |
| | : | Quantization table Y : Q63 |
| +45 | 01 | U: Pq=0, Nq=1 |
| +46 | : | Quantization table U : Q0 |
| | : | : |
| | : | : |
| | : | : |
| | : | Quantization table U : Q63 |
| +86 | 02 | V: Pq=0, Nq=0 |
| +87 | : | Quantization table V : Q0 |
| | : | : |
| | : | : |
| | : | : |
| | : | Quantization table V : Q63 |

SOF structure

| | Code (Hex) | Meaning |
|-----|------------|--------------------------|
| +00 | FF | Marker Prefix |
| +01 | C0 | SOF |
| +02 | 00 | Length of field |
| +03 | C5 | 2+1+2+1+2*3=17 (Byte) |
| +04 | 00 | Data precision (bits) |
| +05 | XX | vertical lines |
| +06 | YY | XXYY (Hex) lines |
| +07 | WW | horizontal lines |
| +08 | ZZ | WWZZ (Hex) lines |
| +09 | 03 | Components |
| +0A | 01 | Components number (1:Y) |
| +0B | 21 | H0=2, V0=1(4:2:2) |
| +0C | 00 | Quantization designation |
| +0D | 02 | Components number (2:U) |
| +0E | 11 | H1=1, V1=1 |
| +0F | 01 | Quantization designation |
| +10 | 03 | Components number (2:U) |
| +11 | 11 | H2=1, V2=1 |
| +13 | 02 | Quantization designation |

DHT structure

| | Code (Hex) | Meaning |
|-----|------------|-------------------------------------|
| +00 | FF | Marker Prefix |
| +01 | C4 | DHT |
| +02 | 01 | Length of field |
| | A2 | $2+(1+16+12+1+16+162)*2=418$ (Byte) |
| +04 | 00 | Table number Y-DC : 00 |
| | | DHT parameter |
| | 10 | Table number Y-AC : 10 |
| | | DHT parameter |
| | 01 | Table number C-DC : 01 |
| | | DHT parameter |
| | 11 | Table number C-AC : 11 |
| | | DHT parameter |
| | 00 | Table number Y-DC : 00 |
| | | DHT parameter |
| | 10 | Table number Y-AC : 10 |
| | | DHT parameter |
| | 01 | Table number C-DC : 01 |
| | | DHT parameter |
| | 11 | Table number C-AC : 11 |
| | | DHT parameter |

Remark : the current JPEG logic core outputs two sets of Huffmann table.

SOS structure

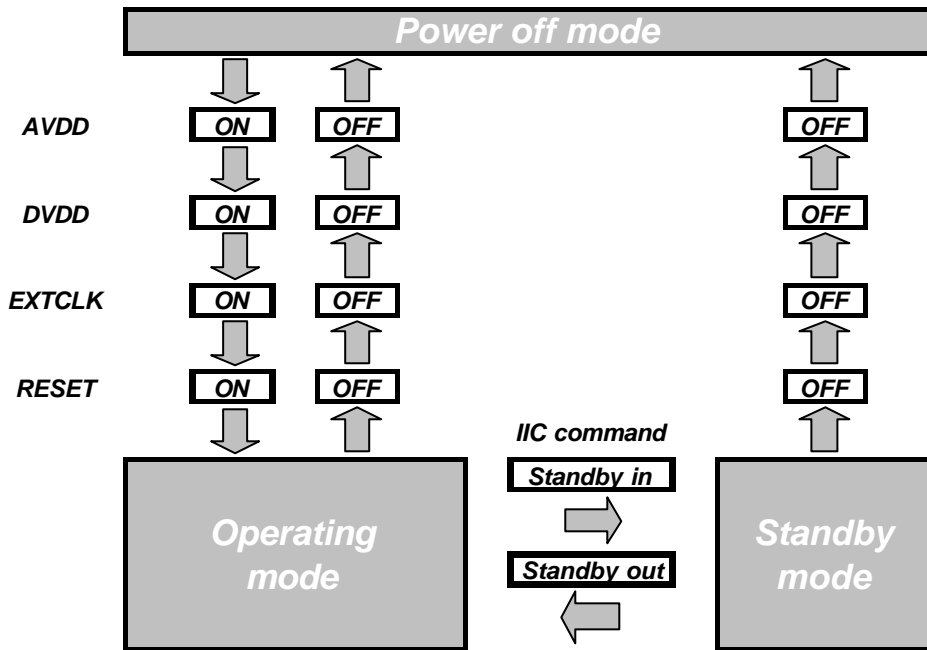
| | Code (Hex) | Meaning |
|-----|------------|---------------------------------------|
| +00 | FF | Marker Prefix |
| +01 | DA | SOS |
| +02 | 00 | Length of field |
| | 0C | $2+1+3*2+3=12$ (Byte) |
| +04 | 03 | Components in scan |
| +05 | 01 | Components selector Y:01 |
| +06 | 00 | Huffmann table selector Y:00 |
| +07 | 02 | Components selector U:02 |
| +08 | 11 | Huffmann table selector C:11 |
| +09 | 03 | Components selector V:03 |
| +0A | 11 | Huffmann table selector C:11 |
| +0B | 00 | Scan start position in block |
| +0C | 3F | Scan end position in block |
| +0D | 00 | Successive approximation Bit position |

OPERATING FLOW

The sensor chip supports the operating mode and the standby mode as shown in the following figure.

power management

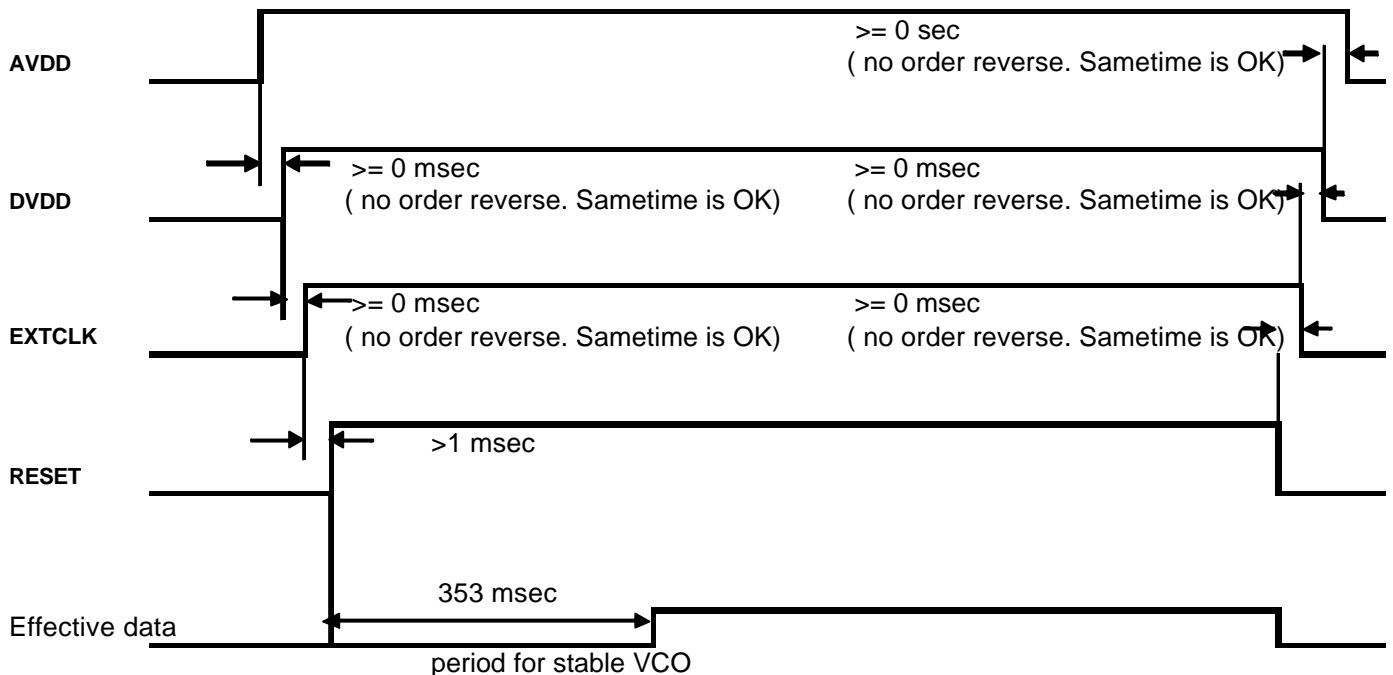
In power off mode, the output pins are not in High-Z status.



In standby mode, the latest status of output pins is restored. If the host sends "Lowfixed" command before sleep command, all the output pins are set to "Low".

Powering order and timing margin are shown in the following figure.

Timing description in power sequence



When 1.6V power line is higher than 2.5V power line, the current is provided from 1.6V power line to 2.5V power line via internal protection diode.

When 2.5V power line is open, the current is provided to 2.5V power line from 1.6V power line via internal protection diode. Then 1V is provided at 2.5V power line and 1.6V is provided at 1.6V power line.

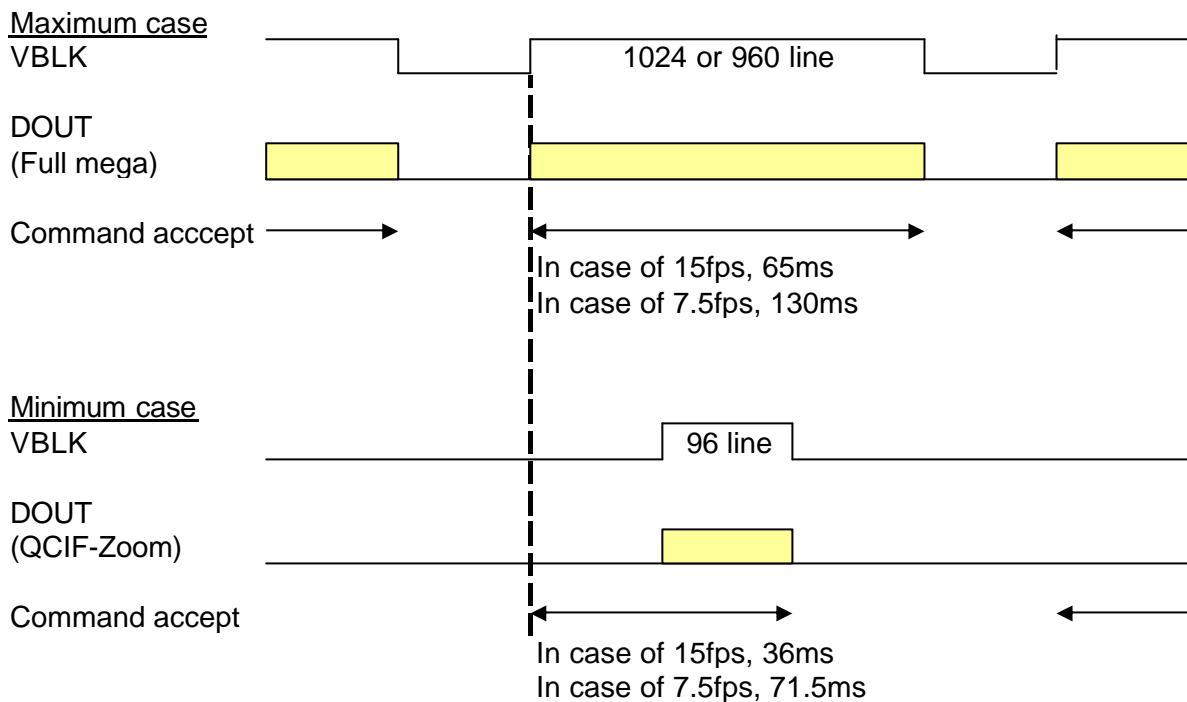
When 2.5V power line is connected to GND, 1.6V power line is shorted to GND at low impedance.

These conditions can not be guaranteed and it need to consideration to design.

Acceptable period for command setting

The following figure shows the command acceptable period. In general the status of the next frame data is immediately reflected by the command, but in case of the commands dealing with sensor operation such as exposure time setting, the frame after next is reflected. Register setting is available between top of full mega pixel image and end of image.

The minimum period happens in case of sub QCIF maximum zooming. The command acceptable period after VBLK turns high is 36 msec for 15 fps operation and 71.5 msec for 7.5fps.



MAXIMUM RATING

| CHARACTERISTICS | SYMBOL | RATING | UNITS |
|----------------------|--------------------------------------------|-----------------|----------|
| Power supply voltage | PVDD (AVDD25), IOVDD (IOVDD25, IOAVD25) | -0.3 to 3.6 | V |
| | DVDD (AVDD15, DVDD15) | -0.3 to 3.0 | V |
| Input voltage | V_{IN} | -0.3 to VDD+0.3 | V |
| Storage tempature | T_{stg} | -30 to 85 | Degree C |

RECOMMENDED OPERATION CONDITION

| CHARACTERISTICS | SYMBOL | MIN | TYP | MAX | UNITS |
|-----------------------|---------------------------------------------|-----------|-----|-----|----------|
| Power supply voltage | PVDD (AVDD25), IOVDD (IOVDD25, IOAVDD25) | 2.6 | 2.8 | 3.0 | V |
| | | 2.3 | 2.5 | 2.7 | V |
| | DVDD (AVDD15, DVDD15) | 1.5 | 1.6 | 1.7 | V |
| Input voltage | V_{IN} | 0 to VDD | | | V |
| Operating temperature | T_{OPR} | -20 to 60 | | | Degree C |

Note;

* If using 2.5V operation, must input setting command. (Default setting is 2.8V operation.)

ELECTRICAL CHARACTERISTICS

DC Characteristics (Ta=25 degree C, PVDD=IOVDD=2.8V, DVDD=1.6V)

1. POWER CONSUMPTION

(Ta=25 degree C, PVDD=IOVDD=2.5V, DVDD=1.6V, 15fps operation, dark condition)

| ITEM | | CONDITION | | MIN | TYP | MAX | UNITS |
|---------|-------------|--------------|---------------------|-----|-----|------|-------|
| POWER * | IOVDD, PVDD | Normal mode | Output data: YUV | - | 20 | 30 | mA |
| | DVDD | | | - | 100 | 150 | mA |
| | IOVDD, PVDD | | Output data: JPEG * | - | 10 | 15 | mA |
| | DVDD | | | - | 90 | 140 | mA |
| | IOVDD, PVDD | Standby mode | Ta=60 degree C | - | - | 11 | μA |
| | DVDD | | | - | - | 5100 | μA |

Note;

* Measurement condition: Machbeth chart(full)

* JPEG table is standard.

2. EXTCLK

| ITEM | | SYMBOL | CONDITION | MIN | TYP | MAX | UNITS |
|------------------|--------------------------|------------------------|------------------------|-------------|-----|-------------|-------|
| Rectanglar shape | HIGH level input voltage | V _{IH} EXTCLK | - | IOVDD x 0.8 | - | - | V |
| | LOW level input voltage | V _{IL} EXTCLK | - | - | - | IOVDD x 0.2 | V |
| | HIGH level input current | I _{IH} EXTCLK | V _{IN} =IOVDD | -10 | - | 10 | μA |
| | LOW level input current | I _{IL} EXTCLK | V _{IN} =GND | -10 | - | 10 | μA |
| | DUTY * | - | - | 45/55 | - | 55/45 | % |

Note;

* Duty is referred to 50% level of input EXTCLK.

3. SCL, SDA

| ITEM | | SYMBOL | CONDITION | MIN | TYP | MAX | UNITS |
|------|--------------------------|---------------------|----------------------|-------------|-------|-------------|-------|
| SCL | HIGH level input voltage | V _{IH} SCL | - | IOVDD x 0.7 | IOVDD | 3.3 | V |
| | LOW level input voltage | V _{IL} SCL | - | 0 | - | IOVDD x 0.3 | V |
| SDA | HIGH level input voltage | V _{IH} SDA | - | IOVDD x 0.7 | IOVDD | 3.3 | V |
| | LOW level input voltage | V _{IL} SDA | - | 0 | - | IOVDD x 0.3 | V |
| | LOW level output voltage | V _{OL} SDA | I _{OL} =4mA | 0 | - | 0.4 | V |

4. DOUT7-0, HBLK, VBLK, STROBE, DCLK

| ITEM | | SYMBOL | CONDITION | MIN | TYP | MAX | UNITS |
|-----------------------------------|---------------------------|----------------------|-----------------------|-----|-------|-----|-------|
| DOUT7-0, HBLK, VBLK, STROBE, DCLK | HIGH level output voltage | V _{OH} DATA | I _{OH} =-2mA | 2.4 | IOVDD | - | V |
| | LOW level output voltage | V _{OL} DATA | I _{OL} =2mA | 0 | - | 0.4 | V |

5. RESET

| ITEM | | SYMBOL | CONDITION | MIN | TYP | MAX | UNITS |
|-------|--------------------------|-----------------------|------------------------|-------------|-----|-------------|-------|
| RESET | HIGH level input voltage | V _{IH} RESET | - | IOVDD x 0.8 | - | - | V |
| | LOW level input voltage | V _{IL} RESET | - | - | - | IOVDD x 0.2 | V |
| | HIGH level input current | I _{IH} RESET | V _{IN} =GND | -10 | - | 10 | μA |
| | LOW level input current | I _{IL} RESET | V _{IN} =IOVDD | -10 | - | 10 | μA |

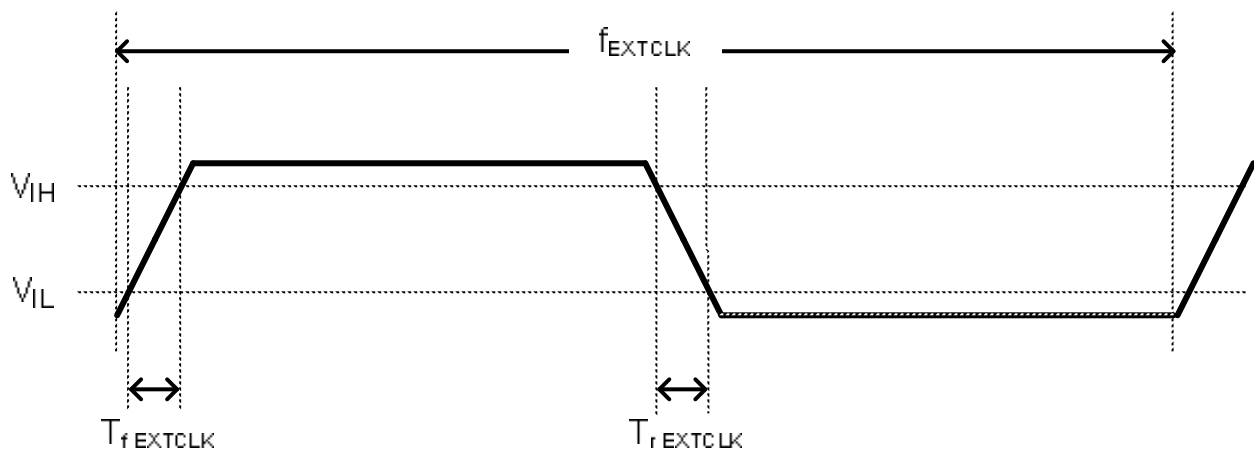
AC Characteristics (Ta=25 degree C, PVDD=IOVDD=2.8V, DVDD=1.6V)

1. EXTCLK

| ITEM | SYMBOL | MIN | TYP | MAX | UNITS | NOTE |
|-----------------|---------------|-----|-----|-----|-------|------|
| Clock frequency | f_{EXTCLK} | 6 | - | 20 | MHz | |
| Rise time | $t_{rEXTCLK}$ | - | - | 5 | ns | * 1 |
| Fall time | $t_{fEXTCLK}$ | - | - | 5 | ns | |

Note;

ALL values referred to V_{IHmin} and V_{ILmax} levels.

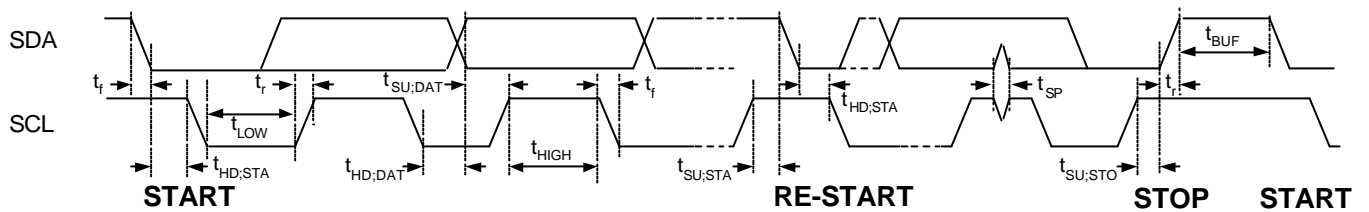


2. SCL, SDA

| ITEM | | SYMBOL | MIN | MAX | UNITS | NOTE |
|-----------------------------------------------------------------------------------------------|------------------------|-----------------|-----|-----|---------|------|
| SCL | Clock frequency | f_{SCL} | 0 | 400 | kHz | *1 |
| | Low period | $t_{LOW\ SCL}$ | 1.3 | - | μs | |
| | High period | $t_{HIGH\ SCL}$ | 0.6 | - | μs | |
| | Rise time | $t_r\ SCL$ | - | 300 | μs | |
| | Fall time | $t_f\ SCL$ | - | 300 | μs | |
| SDA | Rise time | $t_r\ SDA$ | - | 300 | μs | |
| | Fall time | $t_f\ SDA$ | - | 300 | μs | |
| Hold time (repeated) START condition After this period, the first clock pulse is generated | | $t_{HD\ STA}$ | 0.6 | - | μs | |
| Setup time for a repeated START condition | | $t_{SU\ STA}$ | 0.6 | - | μs | |
| Data hold time | | $t_{HD\ DAT}$ | 0 | - | μs | |
| Data setup time | | $t_{SU\ DAT}$ | 100 | - | μs | |
| Setup time for STOP condition | | $t_{SU\ STO}$ | 0.6 | - | μs | |
| Width of spike pulse | Normal | t_{SP1} | 0 | 50 | μs | |
| | Wakeup from sleep mode | t_{SP2} | 0 | 20 | μs | |

Note;

* All values referred to V_{IHmin} and V_{ILmax} levels.



3. DOUT7-0, DCLK, HBLK, VBLK

| ITEM | | SYMBOL | MIN | MAX | UNITS | NOTE |
|------------------------|-----------|---------------|-----|-----|---------|------|
| DCLK | Rise time | t_r DCLK | - | 6 | μ s | |
| | Fall time | t_f DCLK | - | 6 | μ s | |
| DOUT7-0, HBLK, VBLK | Rise time | t_r DATA | - | 6 | μ s | |
| | Fall time | t_f DATA | - | 6 | μ s | |
| Data hold time | | t_{HD} DATA | 10 | - | μ s | |
| Data setup time | | t_{SU} DATA | 10 | - | μ s | |

Note;

* All values referred to V_{OHmin} and V_{OLmax} levels.

