



TC1413/TC1413N

3A High-Speed MOSFET Drivers

Features

- Latch-Up Protected: Will Withstand 500mA Reverse Current
- Input Will Withstand Negative Inputs Up to 5V
- ESD Protected: 4kV
- High Peak Output Current: 3A
- Wide Operating Range
 - 4.5V to 16V
- High Capacitive Load Drive Capability: 1800pF in 20nsec
- Short Delay Time: 35nsec Typ
- Consistent Delay Times With Changes in Supply Voltage
- Matched Delay Times
- Low Supply Current
 - With Logic "1" Input: 500 μ A
 - With Logic "0" Input: 100 μ A
- Low Output Impedance: 2.7 Ω
- Pinout Same as TC1410/TC1411/TC1412

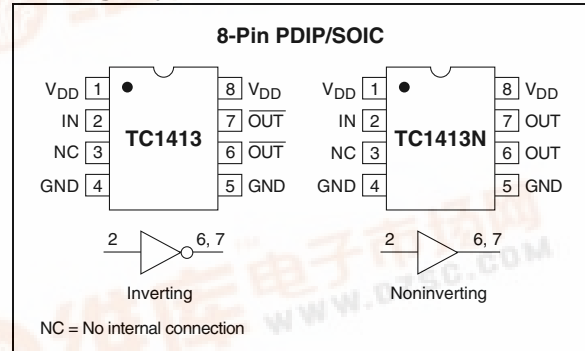
Applications

- Switch Mode Power Supplies
- Line Drivers
- Pulse Transformer Drive
- Relay Driver

Device Selection Table

Part Number	Package	Temp. Range
TC1413COA	8-Pin SOIC	0°C to +70°C
TC1413CPA	8-Pin PDIP	0°C to +70°C
TC1413EOA	8-Pin SOIC	-40°C to +85°C
TC1413EPA	8-Pin PDIP	-40°C to +85°C
TC1413NCOA	8-Pin SOIC	0°C to +70°C
TC1413NCPA	8-Pin PDIP	0°C to +70°C
TC1413NEOA	8-Pin SOIC	-40°C to +85°C
TC1413NEPA	8-Pin PDIP	-40°C to +85°C

Package Type



General Description

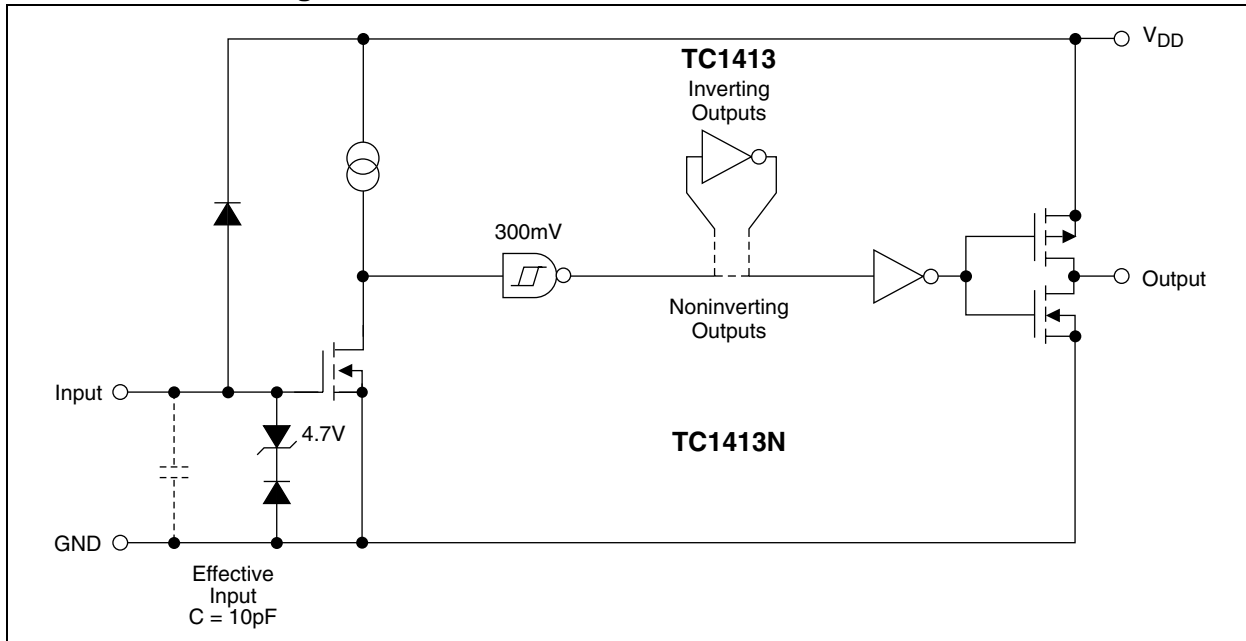
The TC1413/TC1413N are 3A CMOS buffer/drivers. They will not latch up under any conditions within their power and voltage ratings. They are not subject to damage when up to 5V of noise spiking of either polarity occurs on the ground pin. They can accept, without damage or logic upset, up to 500mA of current of either polarity being forced back into their output. All terminals are fully protected against up to 4kV of electrostatic discharge.

As MOSFET drivers, the TC1413/TC1413N can easily charge an 1800pF gate capacitance in 20nsec with matched rise and fall times, and provide low enough impedance in both the ON and the OFF states to ensure the MOSFET's intended state will not be affected, even by large transients. The rise and fall time edges are matched to allow driving short-duration inputs with greater accuracy.



TC1413/TC1413N

Functional Block Diagram



TC1413/TC1413N

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings*

Supply Voltage.....	+20V
Input Voltage.....	$V_{DD} + 0.3V$ to GND – 5.0V
Power Dissipation ($T_A \leq 70^\circ C$)	
PDIP	730mW
SOIC	470mW
Package Thermal Resistance	
PDIP $R_{\theta J-A}$	125°C/W
PDIP $R_{\theta J-C}$	42°C/W
SOIC $R_{\theta J-A}$	155°C/W
SOIC $R_{\theta J-C}$	45°C/W
Operating Temperature Range	
C Version	0°C to +70°C
E Version	-40°C to +85°C
Storage Temperature Range	-65°C to +150°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

TC1413/TC1413N ELECTRICAL SPECIFICATIONS

Electrical Characteristics: Over operating temperature range with $4.5V \leq V_{DD} \leq 16V$, unless otherwise noted. Typical values are measured at $T_A = +25^\circ C$, $V_{DD} = 16V$.

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
Input						
V_{IH}	Logic 1, High Input Voltage	2.0	—	—	V	
V_{IL}	Logic 0, Low Input Voltage	—	—	0.8	V	
I_{IN}	Input Current	-1 -10	—	1 10	μA	$0V \leq V_{IN} \leq V_{DD}$, $T_A = +25^\circ C$ $-40^\circ C \leq T_A \leq +85^\circ C$
Output						
V_{OH}	High Output Voltage	$V_{DD} - 0.025$	—	—	V	DC Test
V_{OL}	Low Output Voltage	—	—	0.025	V	DC Test
R_O	Output Resistance	—	2.7 3.3 3.3	4 5 5	Ω	$V_{DD} = 16V$, $I_O = 10mA$, $T_A = +25^\circ C$, $0^\circ C \leq T_A \leq +70^\circ C$ $-40^\circ C \leq T_A \leq +85^\circ C$
I_{PK}	Peak Output Current	—	2.0	—	A	$V_{DD} = 16V$
I_{REV}	Latch-Up Protection Withstand Reverse Current	—	0.5	—	A	Duty cycle $\leq 2\%$, $t \leq 300\mu sec$, $V_{DD} = 16V$

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TC1413/TC1413N ELECTRICAL SPECIFICATIONS (CONTINUED)

Electrical Characteristics: Over operating temperature range with $4.5V \leq V_{DD} \leq 16V$, unless otherwise noted. Typical values are measured at $T_A = +25^\circ C$, $V_{DD} = 16V$.

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
Switching Time (Note 1)						
t_R	Rise Time	—	20 22 24	28 33 33	nsec	$T_A = +25^\circ C$, $0^\circ C \leq T_A \leq +70^\circ C$ $-40^\circ C \leq T_A \leq +85^\circ C$, Figure 3-2
t_F	Fall Time	—	20 22 24	28 33 33	nsec	$T_A = +25^\circ C$, $0^\circ C \leq T_A \leq +70^\circ C$ $-40^\circ C \leq T_A \leq +85^\circ C$, Figure 3-2
t_{D1}	Delay Time	—	35 40 40	45 50 50	nsec	$T_A = +25^\circ C$, $0^\circ C \leq T_A \leq +70^\circ C$ $-40^\circ C \leq T_A \leq +85^\circ C$, Figure 3-2
t_{D2}	Delay Time	—	35 40 40	45 50 50	nsec	$T_A = +25^\circ C$, $0^\circ C \leq T_A \leq +70^\circ C$ $-40^\circ C \leq T_A \leq +85^\circ C$, Figure 3-2
Power Supply						
I_S	Power Supply Current	— —	0.5 0.1	1.0 0.15	mA	$V_{IN} = 3V$, $V_{DD} = 16V$ $V_{IN} = 0V$

Note 1: Switching times ensured by design.

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2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 2-1.

TABLE 2-1: PIN FUNCTION TABLE

Pin No. (8-Pin PDIP, SOIC)	Symbol	Description
1	V_{DD}	Supply input, 4.5V to 16V.
2	INPUT	Control input.
3	NC	No connection.
4	GND	Ground.
5	GND	Ground.
6	OUTPUT	CMOS totem-pole output, common to pin 7.
7	OUTPUT	CMOS totem-pole output, common to pin 6.
8	V_{DD}	Supply Input, 4.5V to 16V.

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3.0 APPLICATIONS INFORMATION

FIGURE 3-1: THERMAL DERATING CURVE

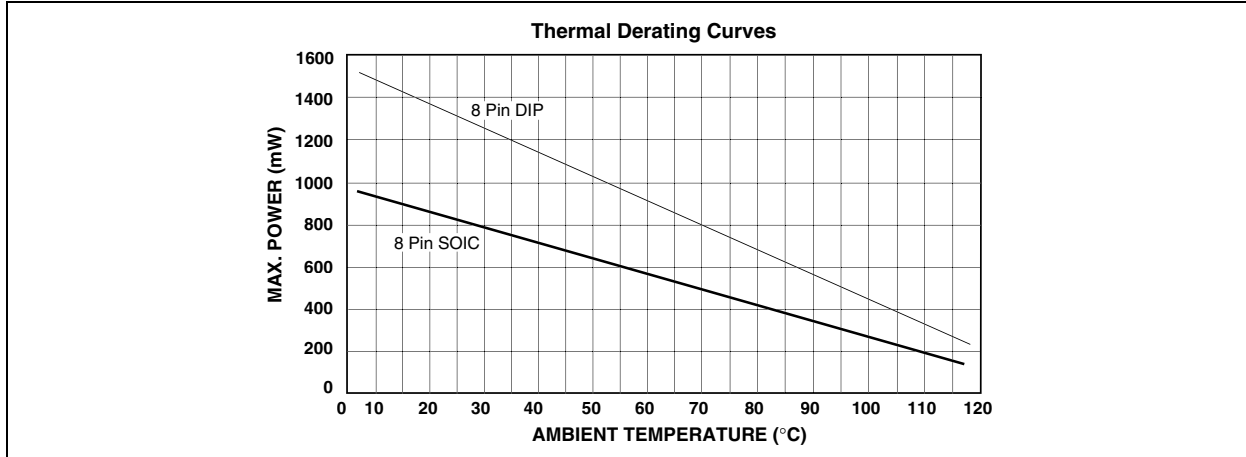
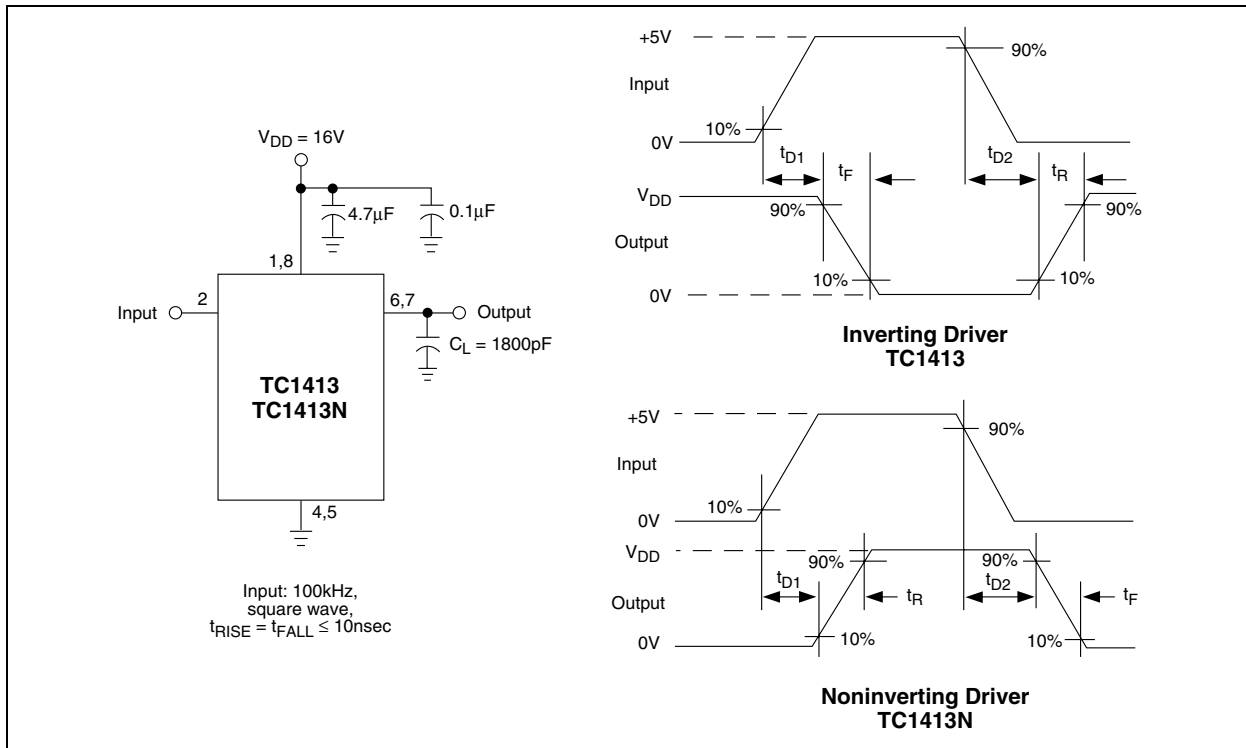


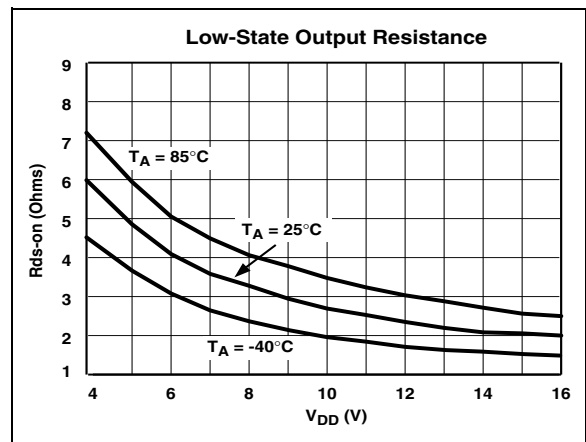
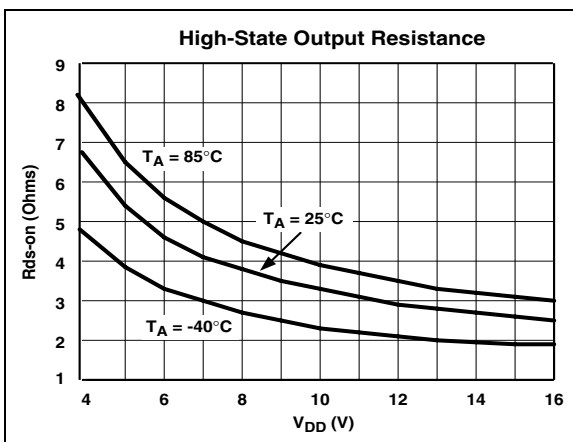
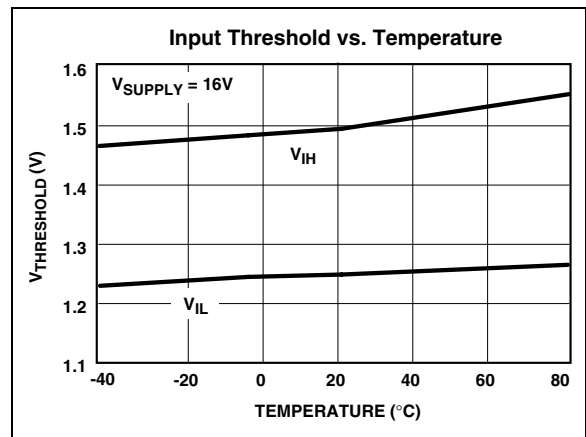
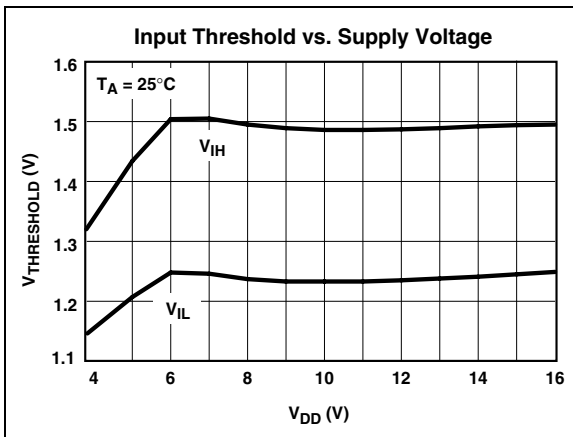
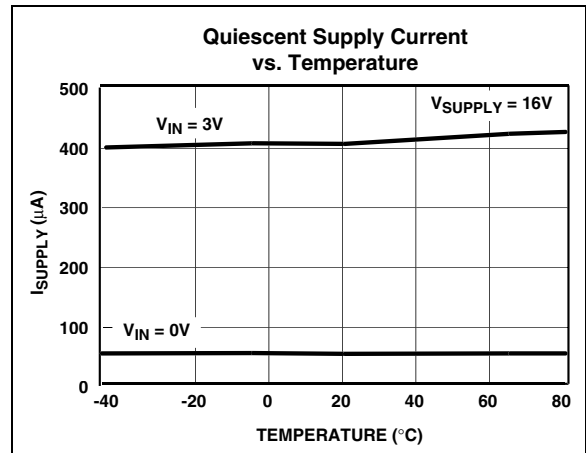
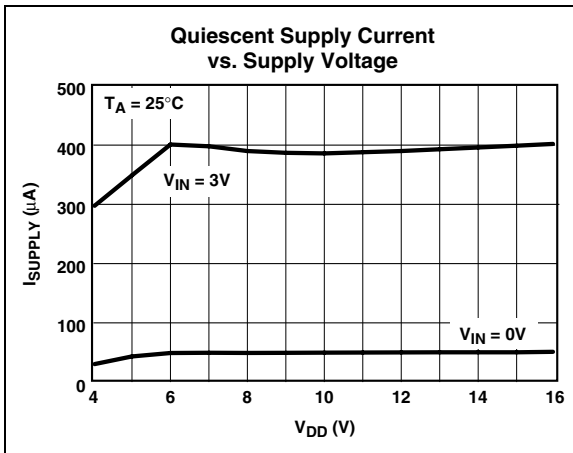
FIGURE 3-2: SWITCHING TIME TEST CIRCUIT



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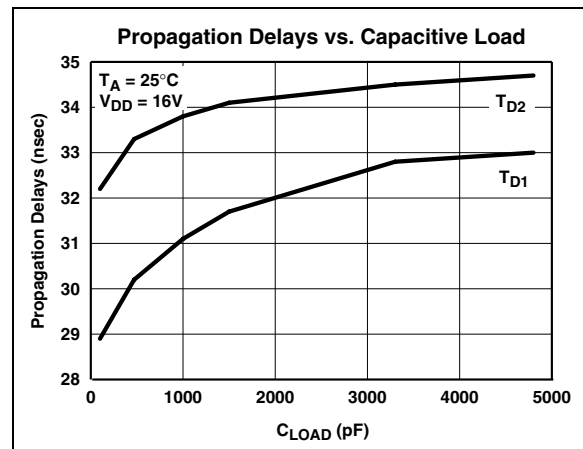
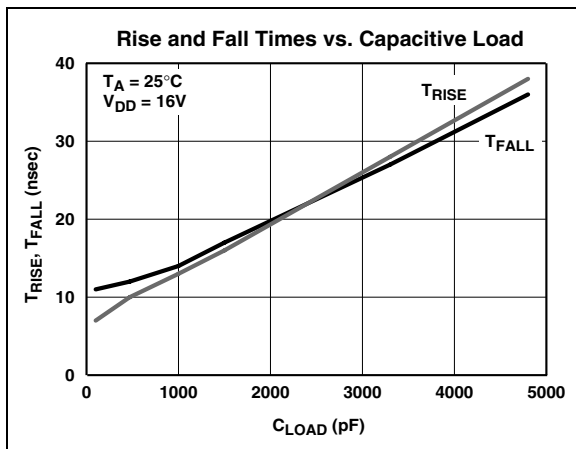
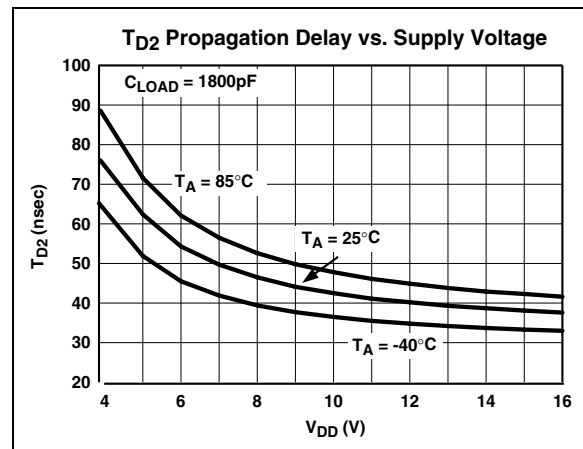
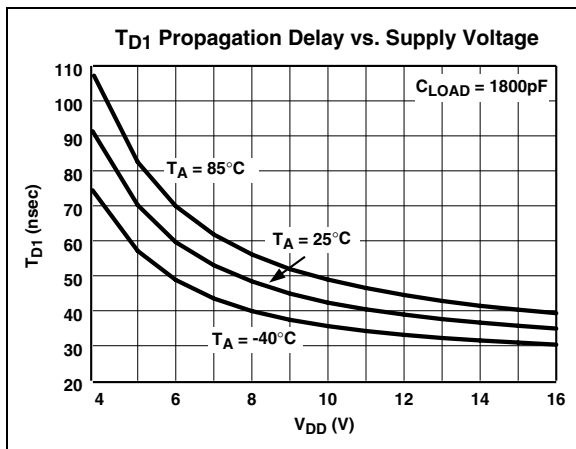
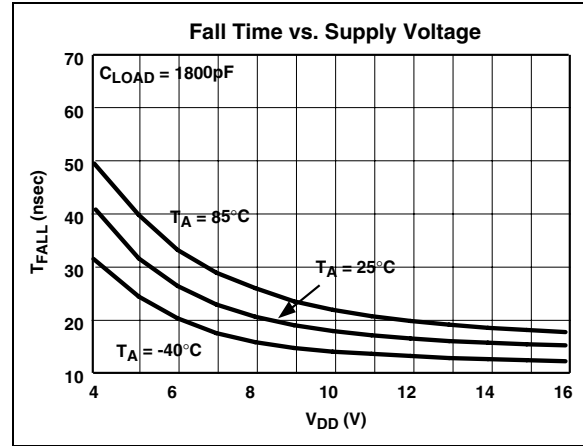
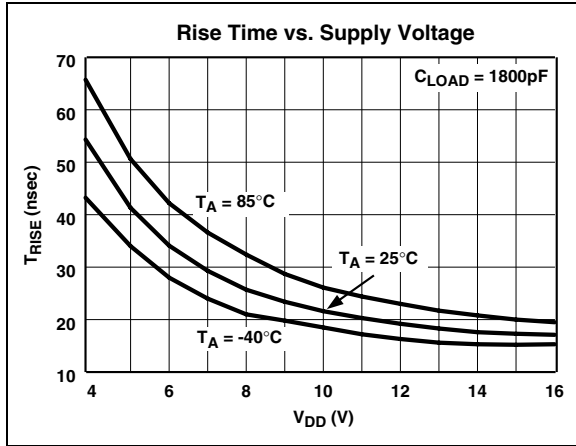
4.0 TYPICAL CHARACTERISTICS

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.



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TYPICAL CHARACTERISTICS (CONTINUED)



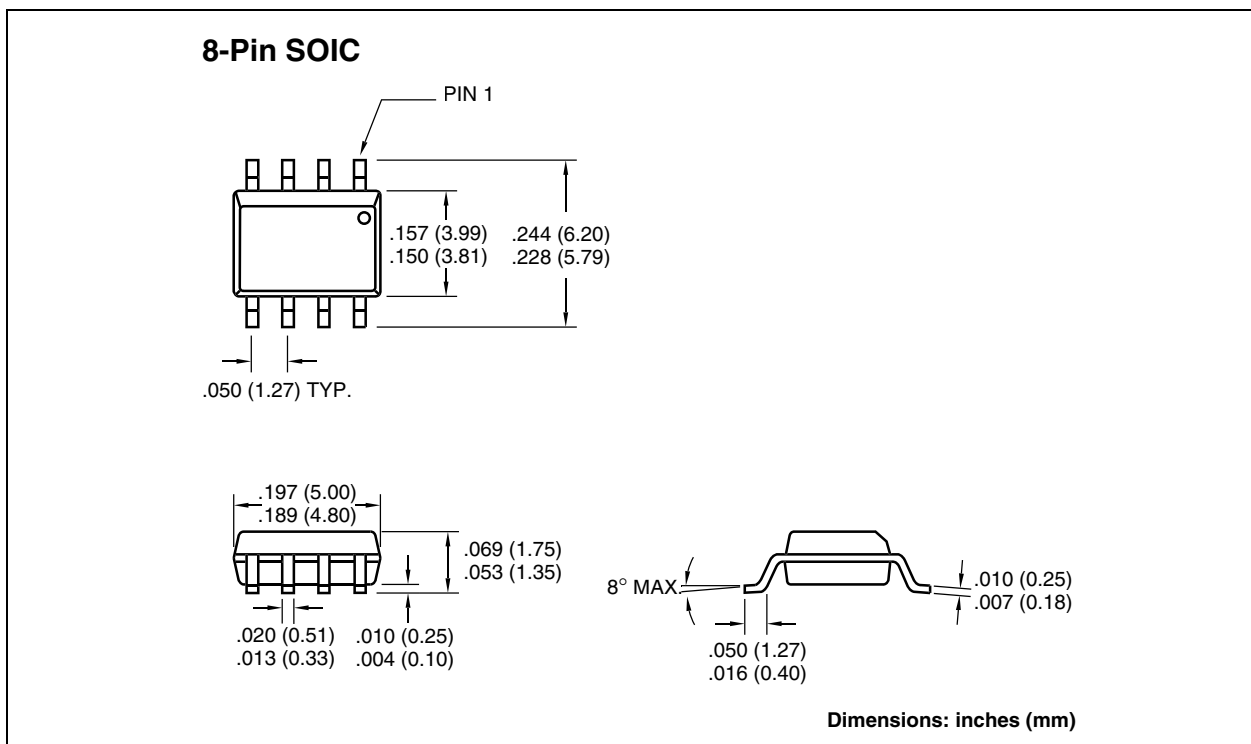
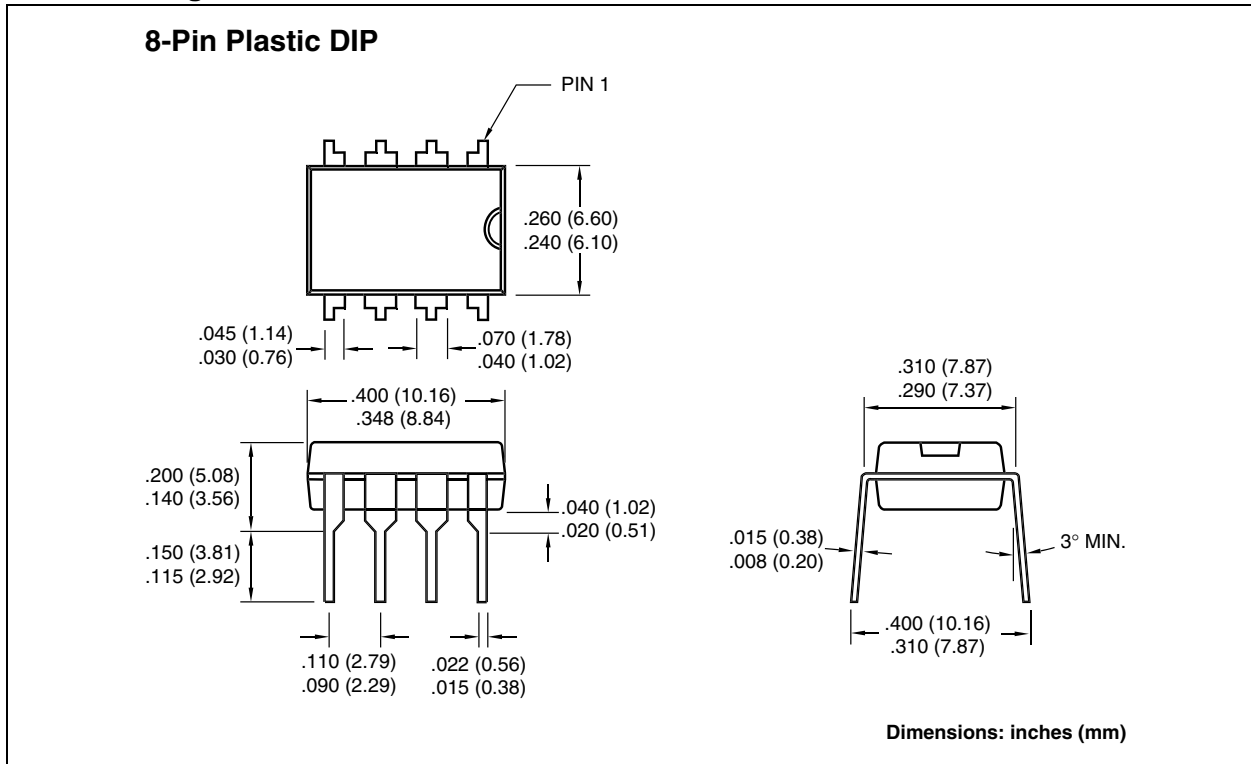
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5.0 PACKAGING INFORMATION

5.1 Package Marking Information

Package marking data not available at this time.

5.2 Package Dimensions



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NOTES:

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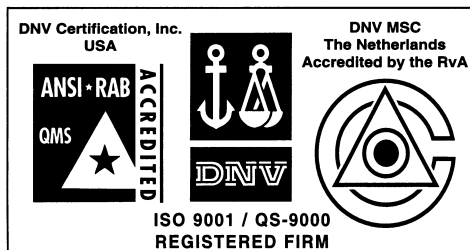
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