N- and P-Channel Enhancement-Mode Dual MOSFET

Features

- Low threshold
- Low on resistance
- Low input capacitance
- Fast switching speeds
- Freedom from secondary breakdown
- Low input and output leakage
- Independent, electrically isolated N- and P-channels

Applications

- Medical ultrasound transmitters
- High voltage pulsers
- Amplifiers
- Buffers
- Piezoelectric transducer drivers
- General purpose line drivers
- Logic level interface

General Description

The Supertex TC2320TG consists of a high voltage, low threshold N- and P-channel MOSFET in an SO-8 package. These low threshold enhancement-mode (normally-off) transistors utilize an advanced vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Ordering Information

Device	Package Options	BV_{DSS}/BV_{DGS} (V)		$R_{DS(ON)}$ (max) (Ω)	
	8-Lead SOIC (Narrow Body)	N-Channel	P-Channel	N-Channel	P-Channel
TC2320	TC2320TG-G	200	-200	7.0	12

-G indicates package is RoHS compliant ('Green')

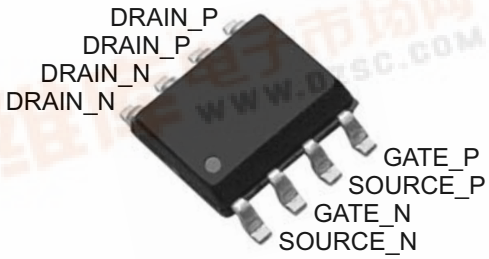
Absolute Maximum Ratings

Parameter	Value
Drain to source voltage	BV_{DSS}
Drain to gate voltage	BV_{DGS}
Gate to source voltage	±20V
Operating and storage temperature	-55°C to +150°C
Soldering temperature*	+300°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

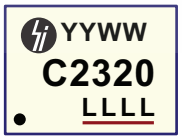
** Distance of 1.6mm from case for 10 seconds.*

Pin Configuration



8-Lead SOIC (TG)

Product Marking



YY = Year Sealed
WW = Week Sealed
L = Lot Number
_____ = "Green" Packaging

8-Lead SOIC (TG)

N-Channel Electrical Characteristics *(@ 25°C unless otherwise specified)*

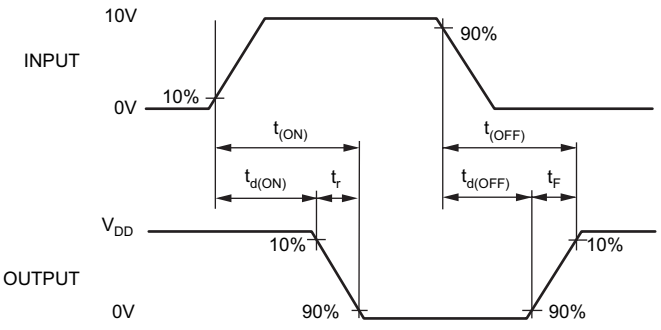
Symbol	Parameter	Min	Typ	Max	Units	Conditions
BV_{DSS}	Drain-to-source breakdown voltage	200	-	-	V	V_{GS} = 0V, I_D = 100µA
$V_{GS(th)}$	Gate threshold voltage	0.6	-	2.0	V	V_{GS} = V_{DS}, I_D = 1.0mA
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with temperature	-	-	-4.5	mV/°C	V_{GS} = V_{DS}, I_D = 1.0mA
I_{GSS}	Gate body leakage	-	-	100	nA	V_{GS} = ±20V, V_{DS} = 0V
I_{DSS}	Zero gate voltage drain current	-	-	1.0	µA	V_{GS} = 0V, V_{DS} = 100V
		-	-	10.0	µA	V_{GS} = 0V, V_{DS} = Max rating
		-	-	1.0	mA	V_{GS} = 0V, T_A = 125°C V_{DS} = 0.8 Max Rating
$I_{D(ON)}$	ON-state drain current	0.6	-	-	A	V_{GS} = 4.5V, V_{DS} = 25V
		1.2	-	-		V_{GS} = 10V, V_{DS} = 25V
$R_{DS(ON)}$	Static drain-to-source ON-state resistance	-	-	8.0	Ω	V_{GS} = 4.5V, I_D = 150mA
		-	-	7.0		V_{GS} = 10V, I_D = 1.0A
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with temperature	150	-	1.0	%/°C	V_{GS} = 4.5V, I_D =150mA
G_{FS}	Forward transconductance	-	-	-	mmho	V_{DS} = 25V, I_D = 200mA
C_{ISS}	Input capacitance	-	-	110	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz
C_{OSS}	Common source output capacitance	-	-	60		
C_{RSS}	Reverse transfer capacitance	-	-	23		
$t_{d(ON)}$	Turn-ON delay time	-	-	20	ns	V_{DD} =25V, I_D = 150mA, R_{GEN} = 25Ω
t_r	Rise time	-	-	15		
$t_{d(OFF)}$	Turn-OFF delay time	-	-	25		
t_f	Fall time	-	-	25		
V_{SD}	Diode forward voltage drop	-	-	1.8	V	V_{GS} = 0V, I_{SD} = 200mA
t_{rr}	Reverse recovery time	-	300	-	ns	V_{GS} = 0V, I_{SD} = 200mA

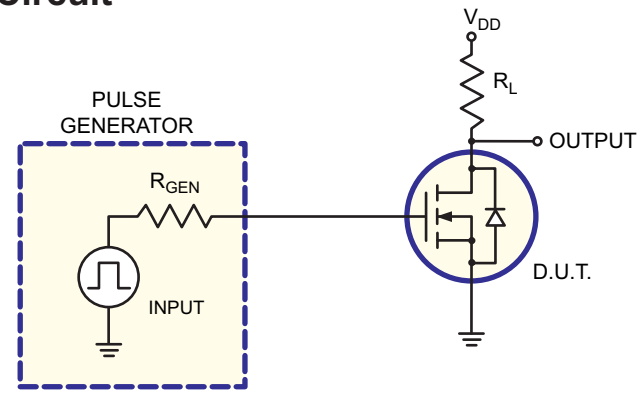
Notes:

1.All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)

2.All A.C. parameters sample tested.

N- Channel Switching Waveforms and Test Circuit





P-Channel Electrical Characteristics *(@ 25°C unless otherwise specified)*

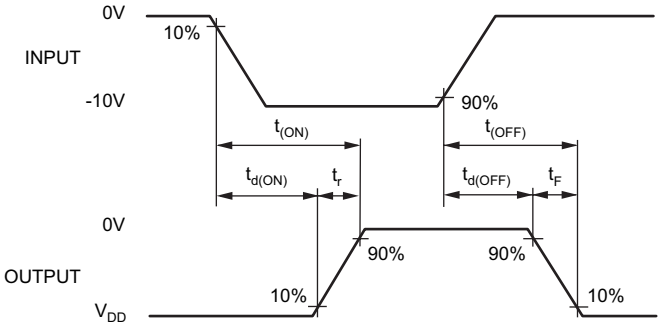
Symbol	Parameter	Min	Typ	Max	Units	Conditions
BV_{DSS}	Drain-to-source breakdown voltage	-200	-	-	V	V_{GS} = 0V, I_D = -2.0mA
$V_{GS(th)}$	Gate threshold voltage	-1.0	-	-2.4	V	V_{GS} = V_{DS}, I_D = -1.0mA
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with temperature	-	-	4.5	mV/°C	V_{GS} = V_{DS}, I_D = -1.0mA
I_{GSS}	Gate body leakage	-	-	-100	nA	V_{GS} = ±20V, V_{DS} = 0V
I_{DSS}	Zero gate voltage drain current	-	-	-10	µA	V_{GS} = 0V, V_{DS} = Max rating
		-	-	-1.0	mA	V_{GS} = 0V, T_A = 125°C, V_{DS} = 0.8 Max Rating
$I_{D(ON)}$	ON-state drain current	-0.25	-0.7	-	A	V_{GS} = -4.5V, V_{DS} = -25V
		-0.75	-2.1	-		V_{GS} = -10V, V_{DS} = -25V
$R_{DS(ON)}$	Static drain-to-source ON-state resistance	-	10	15	Ω	V_{GS} = -4.5V, I_D = -100mA
		-	8.0	12		V_{GS} = -10V, I_D = -200mA
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with temperature	100	-	1.7	%/°C	V_{GS} = -10V, I_D =-200mA
G_{FS}	Forward transconductance	-	250	-	mmho	V_{DS} = -25V, I_D = -200mA
C_{ISS}	Input capacitance	-	75	125	pF	V_{GS} = 0V, V_{DS} = -25V, f = 1.0MHz
C_{OSS}	Common source output capacitance	-	20	85		
C_{RSS}	Reverse transfer capacitance	-	10	35		
$t_{d(ON)}$	Turn-ON delay time	-	-	10	ns	---
t_r	Rise time	-	-	15		
$t_{d(OFF)}$	Turn-OFF delay time	-	-	20		
t_f	Fall time	-	-	15		
V_{SD}	Diode forward voltage drop	-	-	-1.8	V	V_{GS} = 0V, I_{SD} = -0.5A
t_{rr}	Reverse recovery time	-	300	-	ns	V_{GS} = 0V, I_{SD} = -0.5A

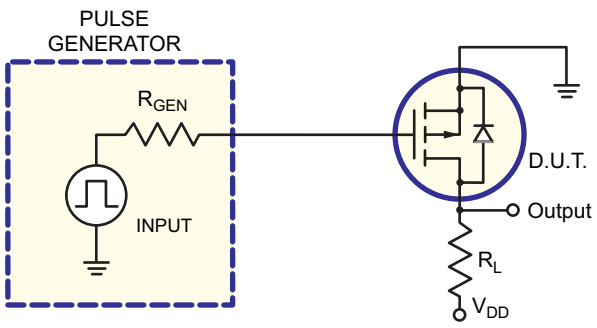
Notes:

1.All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)

2.All A.C. parameters sample tested.

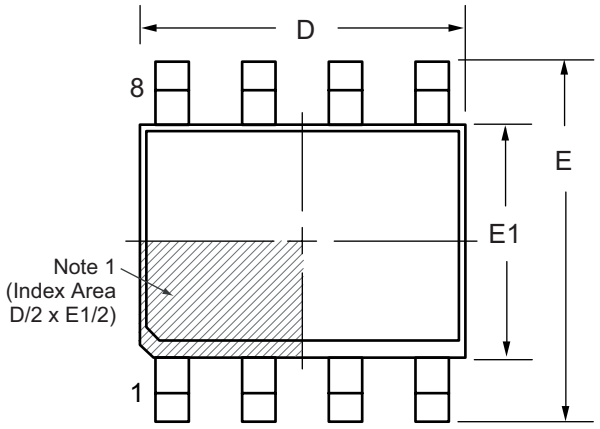
P- Channel Switching Waveforms and Test Circuit



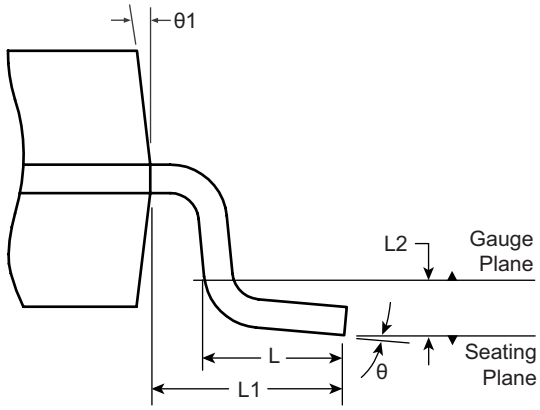


8-Lead SOIC (Narrow Body) Package Outline (TG)

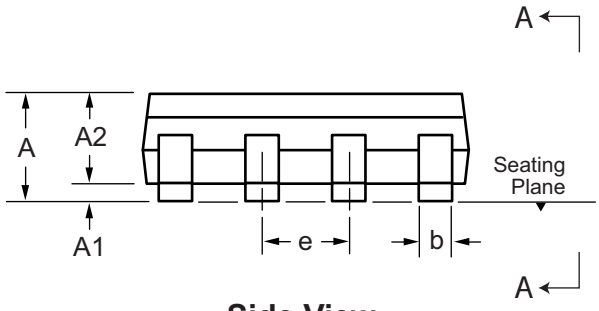
4.9x3.9mm body, 1.75mm height (max), 1.27mm pitch



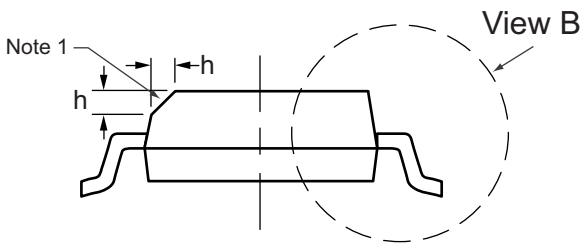
Top View



View B



Side View



View A-A

Note 1:

This chamfer feature is optional. If it is not present, then a Pin 1 identifier must be located in the index area indicated.The Pin 1 identifier may be either a mold, or an embedded metal or marked feature.

Symbol		A	A1	A2	b	D	E	E1	e	h	L	L1	L2	θ	θ1
Dimension (mm)	MIN	1.35	0.10	1.25	0.31	4.80	5.80	3.80	1.27 BSC	0.25	0.40	1.04 REF	0.25 BSC	0°	5°
	NOM	-	-	-	-	4.90	6.00	3.90		-	-			-	-
	MAX	1.75	0.25	1.50	0.51	5.00	6.20	4.00		0.50	1.27			8°	15°

JEDEC Registration MS-012, Variation AA, Issue E, Sept. 2005.

Drawings not to scale.

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)

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