查询TC6133AF供应商

INTEGRATED CIRCUIT

TOSHIBA

TECHNICAL DATA

TOSHIBA AREA IMAGE SENSOR

TC6133AF

CCD(Charge Coupled Device)

OUTLINE

The CMOS LSI of TC6133AF was developed to drive the TCD5241BD, TCD5251BD, TCD5240D and TCD5250D. The TC6133AF can be combined with a vertical clock driver to constitute the CCD area image sensor driving circuit.

FEATURES

- Generation of all timing pulses required to drive TCD5241BD, TCD5251BD, TCD5240D, and TCD5250D.
- Correspondence with electronic shutter from 1/50 s, 1/60 s to 1/10000 s.
- Generation of sampling pulses for the CDS signal processing.
- Generation of controlling pulse for the electronic shutter iris.



Weight: 0.33g (Typ.)

MAXIMUM RATINGS $(V_{SS} = 0V)$

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V _{DD}	-0.3~7.0	V
Input Voltage	VIN	-0.3~V _{DD} +0.3	V
Input Current	IIN	± 10	mA
Storage Temperature	T _{stg}	-40~125	°C

RECOMMENDED OPERATING CONDITIONS $(V_{SS} = 0V)$

_		-	
CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	4.50~5.50	V
Operating Temperature	T _{opr}	- 20~70	°C

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TC6133AF – 1
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TC6133AF

TECHNICAL DATA

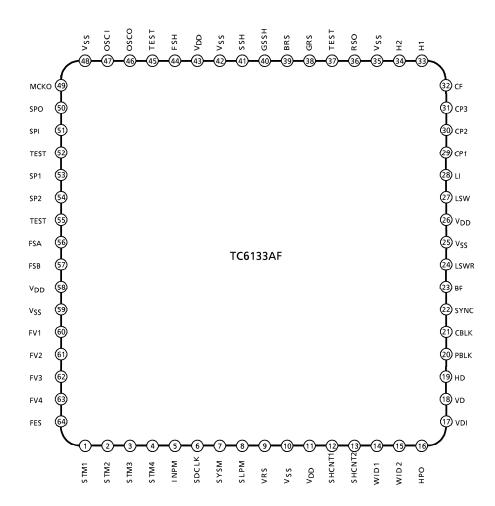
ELECTRICAL CHARACTERISTICS ($V_{SS} = 0V$, $V_{DD} = 4.75 \sim 5.25V$, $Ta = 0 \sim 70^{\circ}C$)

CHARACTER	ISTIC	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Innut Valtaga	"H" Level	V _{IH}		3.5	_	_	V
Input Voltage	"L" Level	V_{IL}		_	_	1.5	V
	"H" Level	1	$V_{IN} = V_{DD}$	- 10	_	10	μΑ
Innut Current	n Levei	lін	$V_{IN} = V_{DD}$, (included PULL-DOWN)	10 —	_	200	
Input Current	"L" Level	Iμ	V _{IN} = V _{SS}	- 10	_	10	
			V _{IN} = V _{SS} , (included PULL-UP)	- 200	_	- 10	- 10
	"H" Level	VOH	I _{OH} = -8mA, H1A, H2A	2.4	_	_	V
Output Voltage			$I_{OH} = -4mA$ except H1A, H2A	2.4			
		V _{OL}	I _{OL} = 8mA, H1A, H2A			0.4	
			I _{OL} =4mA except H1A, H2A]		0.4	
Static Consumption Current		I _{DD}	$C_L = 0pF, V_{DD} = 5V, Ta = 25^{\circ}C$		_	200	μ A

TC6133AF – 2				
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PIN CONNECTION



TC6133AF – 3

1994 – 10 – 24

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TC6133AF
TECHNICAL DATA

PIN FUNCTION

PIN No.	SYMBOL	I/O	POLARITY	FUNCTION
1	STM1	(PULL DOWN)	_	
2	STM2	(PULL DOWN)	_	Shutter period setting terminal.
3	STM3	(PULL DOWN)	_	(See the attached table for the shutter period.)
4	STM4	(PULL DOWN)	_	
5	INPM	(PULL DOWN)	_	Open for normal use.
6	SDCLK	(PULL DOWN)	_	Open for normal use.
7	SYSM	I (PULL DOWN)	_	Terminal for switching PAL or NTSC mode NTSC mode in L level - PAL mode in H level
8	SLPM	(PULL DOWN)	_	Terminal for switching change mode of the electronic shutter. - Step mode in L level - Slope mode in H level
9	VRS	I (PULL UP)	_	Vertical reset input is normally opened.
10	VSS	_	_	GND
11	V_{DD}	_	_	Connected to power supply 5.0V ± 0.5V.
12	SHCNT1	(PULL DOWN)	_	Input terminal for controlling electronic shutter iris.
13	SHCNT2	(PULL DOWN)	_	
14	WID1	0	\Box	Window pulse for sampling controlling iris signal. H level
15	WID2	0	Л	indicates 100% of horizontal period and 80% of vertical period within an effective scanning.
16	НРО	0	几	Horizontal transfer control pulse. This pulse is output within horizontal flyback time to indcate that horizontal CCD transfer period has stopped.
17	VDI	(PULL DOWN)	_	Input terminal for controlling pulse for shutter data. This terminal is normally connected to VD terminal (18 pin).
18	VD	0	Л	Vertical drive pulse output.
19	HD	0	几	Horizontal drive pulse output.

TC6133AF – 4
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INTEGRATED CIRCUIT **TOSHIBA**

TC6133AF

TECHNICAL DATA

PIN	CVAADOL	1/0	DOL A DITY	FUNCTION
No.	SYMBOL	1/0	POLARITY	FUNCTION
20	PBLK	0	7	Pre-blanking pulse output. H level indicates the erase period.
21	CBLK	0		Composite blanking pulse output.
22	SYNC	0	T	Composite synchronization pulse output.
23	BF	0		Burst frag pulse output.
24	LSWR	I (PULL UP)	_	Reset input LSW.
25	Vss	_	1	GND
26	V_{DD}	_	_	Connected to power supply 5.0 ± 0.5 V.
27	LSW	0		Line switching output. This pulse is used for switching sub carrier of PAL system.
28	LI	0		Line identification pulse output for color identifying of CCD image sensor with line sequential color filter. This pulse alternately goes high and low every horizontal cycle, and is reset on the frame cycle. This pulse indicates H level for 2B-G line and L level for 2R-G line.
29	CP1	0	几	Clamp pulse output for clamping the OB portion of CCD signal output. This signal halts when the OB signal is not output within the vertical flyback time.
30	CP2	0	7	Clamp pulse output for signal processing. This signal is
31	CP3	0	Л	also output in the vertical flyback time.
32	CF	0	Ţ	Color field pulse output. H level indicates 1st field every 4 fields in NTSC system and every 8 fields in PAL system.
33	H1	0		Horizontal CCD drive pulse to be connected to the H1 or
34	H2	0		H2 gate of the CCD image sensor.
35	VSS	_		GND
36	RSO	0		CCD reset gate drive pulse to be connected to RS terminal of CCD image sensor through a capacitor.
37	TEST	(PULL DOWN)	_	The test terminal is normally opened.
38	GRS	1	_	Input and output terminal for adjusting RSO and SSH
39	BRS	0	phase. The BRS output is delayed with capacitor a	
40	GSSH	1	_	resistor.

TC6133AF – 5
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TC6133AF

PIN No.	SYMBOL	I/O	POLARITY	FUNCTION	
41	SSH	0	7	Signal sampling pulse output.	
42	Vss	_	_	GND	
43	V_{DD}	_	-	Connected to power supply 5.0V ± 0.5V.	
44	FSH	0	4	Feed through sampling pulse output.	
45	TEST	(PULL DOWN)	ı	The test terminal is normally opened.	
46	osco	0		Terminal for crystal oscillator. (2 fck)	
47	OSCI	I	_	NTSC 1212 fH = 19.069930MHz PAL 1236 fH = 19.312500MHz	
48	V _{SS}	_		GND	
		_			
49	MCKO	0		Clock pulse output. (fck)	
50	SPO	0		Input and output terminal for SPO and SPI phase adjusting. The SPO output is delayed with a capacitor	
51	SPI	I	_	and resistor connected to the SPI input.	
52	TEST	(PULL DOWN)	_	The test terminal is normally opened.	
53	SP1	0	7	Sampling pulse for color separation. The frequency is fck	
54	SP2	0	7	/2 and H level is output for duty ratio 25% (about 51 ns). SP1 and SP2 always shift 180 degress.	
55	TEST	(PULL DOWN)	I	The test terminal is normally opened.	
56	FSA	0		Field shift drive pulse ϕ V1 and ϕ V3 connected to the	
57	FSB	0	7	inversion type vertical clock driver.	
58	V_{DD}	_	_	Connected to power supply 5.0V ± 0.5V.	
59	VSS	_	_	GND	
60	FV1	0			
61	FV2	0	T	Vertical CCD drive pulse ϕ V1, ϕ V2, ϕ V3 and ϕ V4	
62	FV3	0	T	connected to the inversion type vertical clock driver.	
63	FV4	0	Л		
64	FES	0		Electronic shutter pulse connected the inversion type driver.	

TC6133AF – 6
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INTEGRATED CIRCUIT **TOSHIBA** TECHNICAL DATA

TC6133AF

SETTING FOR ELECTRONIC SHUTTER SPEED

The shutter speed depends on inputs on STM1-4

STM1	STM2	STM3	STM4	Shutter speed (s)
L	L	L	L	Normal
Н	L	L	L	1 / 100 (1 / 60)*
L	Н	L	L	1 / 120
Н	Н	L	L	1/250
L	L	Н	L	1 / 500
Н	L	Н	L	1 / 1000
L	Н	Н	L	1 / 2000
Н	Н	Н	L	1 / 4000
L	L	L	Н	1 / 8000
Н	L	L	Н	1 / 10000
Н	Н	Н	Н	Electronic shutter iris

^{* 1/60} s in PAL system.

• Electronic shutter change mode.

SLPM		
L	Step change	When the electronic shutter speed is set, the shutter speed is changed the set time in the next field.
Н	Slope change	When the electronic shutter speed is set, the shutter speed is changed gradually. The changing slope depends on the shutter speed.

TC6133AF – 7
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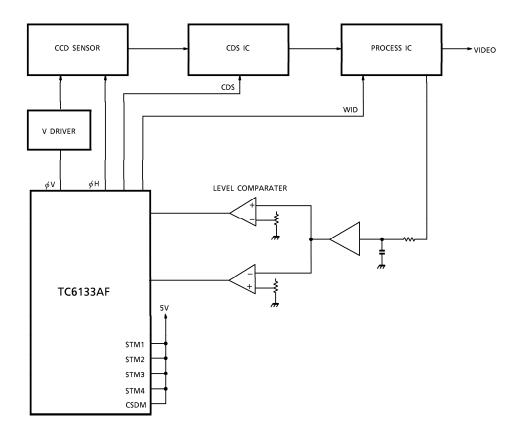
TECHNICAL DATA

• ELECTRONICS SHUTTER IRIS

If SLPM = H and STM1-4 = H, electronic shutter iris mode is available. Inputs on SHCNT1 and SHCNT2 control shutter speed.

SHCNT1	SHCNT2	
Н	L	Change at high speed
Н	Н	Keep the shutter speed
L	Н	Change at low speed

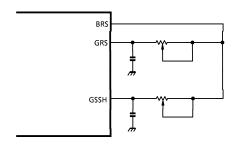
TYPICAL CIRCUIT (Electronic shutter iris)



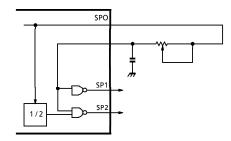
TC6133AF – 8
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PULSE PHASE ADJUSTING

• SSH, RS



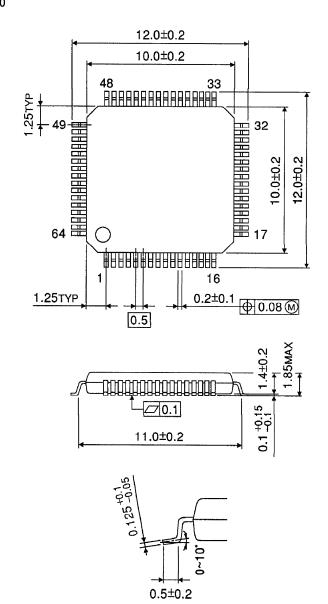
• SP1, SP2



TECHNICAL DATA

OUTLINE DRAWING QFP64-P-1010

Unit : mm



Weight: 0.33g (Typ.)

TC6133AF – 10*
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