

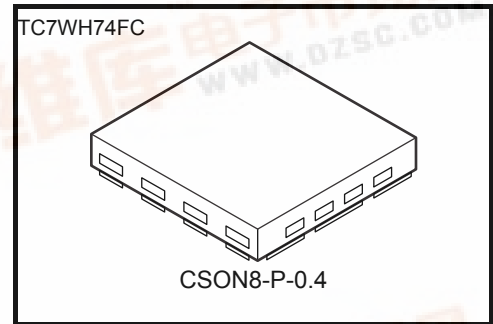
TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC7WH74FC

D-Type Flip Flop with Preset and Clear

Features

- High-speed : $f_{MAX} = 170\text{MHz}$ (Typ.) at $V_{CC} = 5\text{V}$
- Low power dissipation : $I_{CC} = 2\mu\text{A}$ (Max.) at $T_a = 25^\circ\text{C}$
- High noise immunity : $V_{NIH} = V_{NIL} = 28\%V_{CC}$ (Min.)
- Operation voltage range : $V_{CC}(\text{opr.}) = 2 \sim 5.5\text{V}$
- 5.5-V Tolerant inputs.



Weight: 0.002g (typ.)

Absolute Maximum Ratings ($T_a = 25^\circ\text{C}$)

Characteristics	Symbol	Rating	Unit
Power supply voltage	V_{CC}	-0.5~7.0	V
DC input voltage	V_{IN}	-0.5~7.0	V
DC output voltage	V_{OUT}	-0.5~ $V_{CC} + 0.5$ (Note1)	V
Input diode current	I_{IK}	-20	mA
Output diode current	I_{OK}	± 20 (Note2)	mA
DC output current	I_{OUT}	± 25	mA
DC V_{CC} /GND current	I_{CC}	± 50	mA
Power dissipation	P_D	150 (Note3)	mW
Storage temperature	T_{stg}	-65~150	$^\circ\text{C}$

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges. Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note1 : High or Low State.

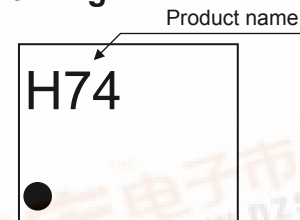
I_{OUT} absolute maximum rating must be observed.

Note2 : $V_{OUT} < \text{GND}$, $V_{OUT} > V_{CC}$

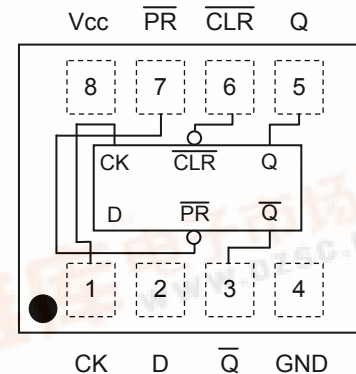
Note3 : Mounted on an FR4 board.

(25.4 mm × 25.4 mm × 1.6 t, Cu Pad: 11.56 mm²)

Marking



Pin Assignment (top view)

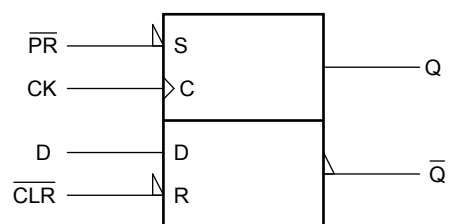


Truth Table

Inputs				Outputs		Function
$\overline{\text{CLR}}$	$\overline{\text{PR}}$	D	CK	Q	$\overline{\text{Q}}$	
L	H	X	X	L	H	Clear
H	L	X	X	H	L	Preset
L	L	X	X	H	H	—
H	H	L	\uparrow	L	H	—
H	H	H	\uparrow	H	L	—
H	H	X	\downarrow	Qn	$\overline{\text{Qn}}$	No Change

X : Don't Care

IEC Logic Diagram



Operating Ranges

Characteristics	Symbol	Rating	Unit
Power supply voltage	V_{CC}	2~5.5	V
Input voltage	V_{IN}	0~5.5	V
Output voltage	V_{OUT}	0~ V_{CC}	V
Operating temperature	T_{opr}	-40~85	°C
Input rise and fall time	dt/dv	0~100 ($V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$)	ns/V
		0~20 ($V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$)	

DC Electrical Characteristics

Characteristic	Symbol	Test condition	$T_a = 25^\circ\text{C}$			$T_a = -40\sim 85^\circ\text{C}$		Unit		
			V_{CC} (V)	Min.	Typ.	Max.	Min.		Max.	
High-level input voltage	V_{IH}	—	2.0	1.5	—	—	1.5	—	V	
			3.0~5.5	$V_{CC} \times 0.7$	—	—	$V_{CC} \times 0.7$	—		
Low-level input voltage	V_{IL}	—	2.0	—	—	0.5	—	0.5	V	
			3.0~5.5	—	—	$V_{CC} \times 0.3$	—	$V_{CC} \times 0.3$		
High-level output voltage	V_{OH}	$V_{IN} = V_{IL}$ or V_{IH}	$I_{OH} = -50 \mu\text{A}$	2.0	1.9	2.0	—	1.9	—	V
				3.0	2.9	3.0	—	2.9	—	
				4.5	4.4	4.5	—	4.4	—	
			$I_{OH} = -4 \text{ mA}$	3.0	2.58	—	—	2.48	—	
				4.5	3.94	—	—	3.80	—	
Low-level output voltage	V_{OL}	$V_{IN} = V_{IL}$ or V_{IH}	$I_{OL} = 50 \mu\text{A}$	2.0	—	0.0	0.1	—	0.1	V
				3.0	—	0.0	0.1	—	0.1	
				4.5	—	0.0	0.1	—	0.1	
			$I_{OL} = 4 \text{ mA}$	3.0	—	—	0.36	—	0.44	
				4.5	—	—	0.36	—	0.44	
Input leakage current	I_{IN}	$V_{IN} = 5.5 \text{ V}$ or GND	0~5.5	—	—	± 0.1	—	± 1.0	μA	
Quiescent supply current	I_{CC}	$V_{IN} = V_{CC}$ or GND	5.5	—	—	2.0	—	20.0	μA	

Timing Requirements (Input : $t_r = t_f = 3 \text{ ns}$)

Characteristic	Symbol	Test condition	Ta = 25°C		Ta = -40~85°C		Unit
			V _{CC} (V)	LIMIT	LIMIT	LIMIT	
Minimum pulse width (CK)	t _{W(L)}		3.3 ± 0.3	6.0	7.0	ns	
	t _{W(H)}		5.0 ± 0.5	5.0	5.0		
Minimum pulse width ($\overline{\text{CLR}}$, $\overline{\text{PR}}$)	t _{W(L)}		3.3 ± 0.3	6.0	7.0		
			5.0 ± 0.5	5.0	5.0		
Minimum set-up time	t _s		3.3 ± 0.3	7.0	7.0		
			5.0 ± 0.5	5.0	5.0		
Minimum hold time	t _h		3.3 ± 0.3	0.5	0.5		
			5.0 ± 0.5	0.5	0.5		
Minimum removal time ($\overline{\text{CLR}}$, $\overline{\text{PR}}$)	t _{rem}		3.3 ± 0.3	5.0	5.0		
			5.0 ± 0.5	3.0	3.0		

AC Electrical Characteristics (Input : $t_r = t_f = 3 \text{ ns}$)

Characteristic	Symbol	Test condition		Ta = 25°C			Ta = -40~85°C		Unit
		V _{CC} (V)	C _L (pF)	Min.	Typ.	Max.	Min.	Max.	
Propagation delay time (CK - Q , $\overline{\text{Q}}$)	t _{pLH}	3.3 ± 0.3	15	—	6.7	11.9	1.0	14.0	ns
			50	—	9.2	15.4	1.0	17.5	
	t _{pHL}	5.0 ± 0.5	15	—	4.6	7.3	1.0	8.5	
			50	—	6.1	9.3	1.0	10.5	
Propagation delay time ($\overline{\text{CLR}}$, $\overline{\text{PR}}$ - Q , $\overline{\text{Q}}$)	t _{pLH}	3.3 ± 0.3	15	—	7.6	12.3	1.0	14.5	ns
			50	—	10.1	15.8	1.0	18.0	
	t _{pHL}	5.0 ± 0.5	15	—	4.8	7.7	1.0	9.0	
			50	—	6.3	9.7	1.0	11.0	
Maximum clock frequency	f _{MAX}	3.3 ± 0.3	15	80	125	—	70	—	ns
			50	50	75	—	45	—	
		5.0 ± 0.5	15	130	170	—	110	—	
			50	90	115	—	75	—	
Input capacitance	C _{IN}	—		—	4	10	—	10	PF
Power dissipation capacitance	C _{PD}	(Note 4)		—	22	—	—	—	pF

Note 4 : C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

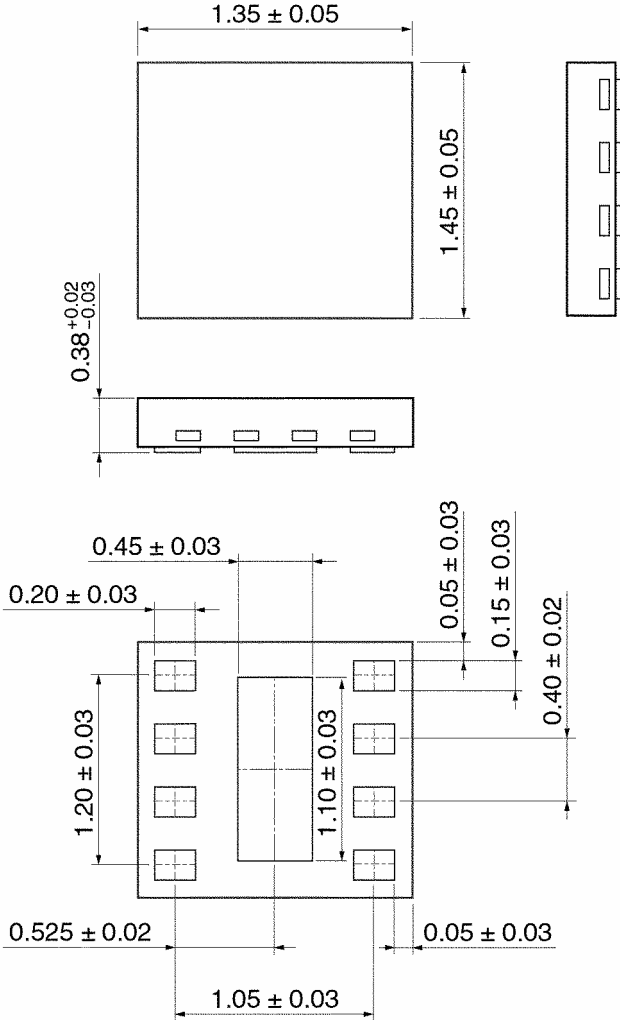
Average operating current can be obtained by the equation:

$$I_{CC (opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

Package Dimensions

CSON8-P-0.4

Unit: mm



Weight : 0.002 g (Typ.)

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20070701-EN GENERAL

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