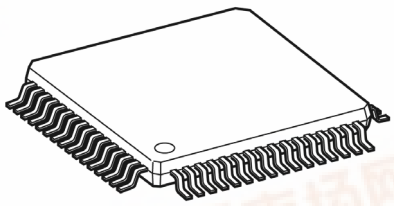
TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC9329AFAG, TC9329AFCG

Portable Audio DTS Controller (DTS-21)

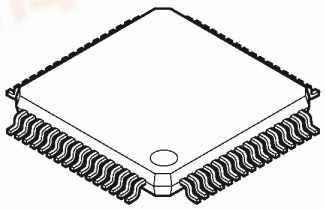
The TC9329AFAG/AFCG is a single-chip DTS microcontroller for portable audio incorporating a 230-MHz prescaler, PLL, and LCD driver. In addition to a 20-bit IF counter, 6-bit A/D converter, serial interface, and buzzer function, the device supports an interrupt function, 8-bit timer/counter, and 8-bit pulse counter. The LCD driver features built-in 1/4 duty, 1/2 bias and a 3-V voltage boosting circuit, implementing stable LCD. The power supply voltage ranges from 0.9 to 1.8 V. Because of its low current consumption (CPU: 80 µA (max)), the device is suitable for use in digital tuning systems in portable equipment such as headphone stereos.

TC9329AFAG



LQFP64-P-1010-0.50E

TC9329AFCG



TQFP64-P-1010-0.50C

Weight
LQFP64-P-1010-0.50E : 0.32 g (typ.)
TQFP64-P-1010-0.50C : 0.26 g (typ.)

Features

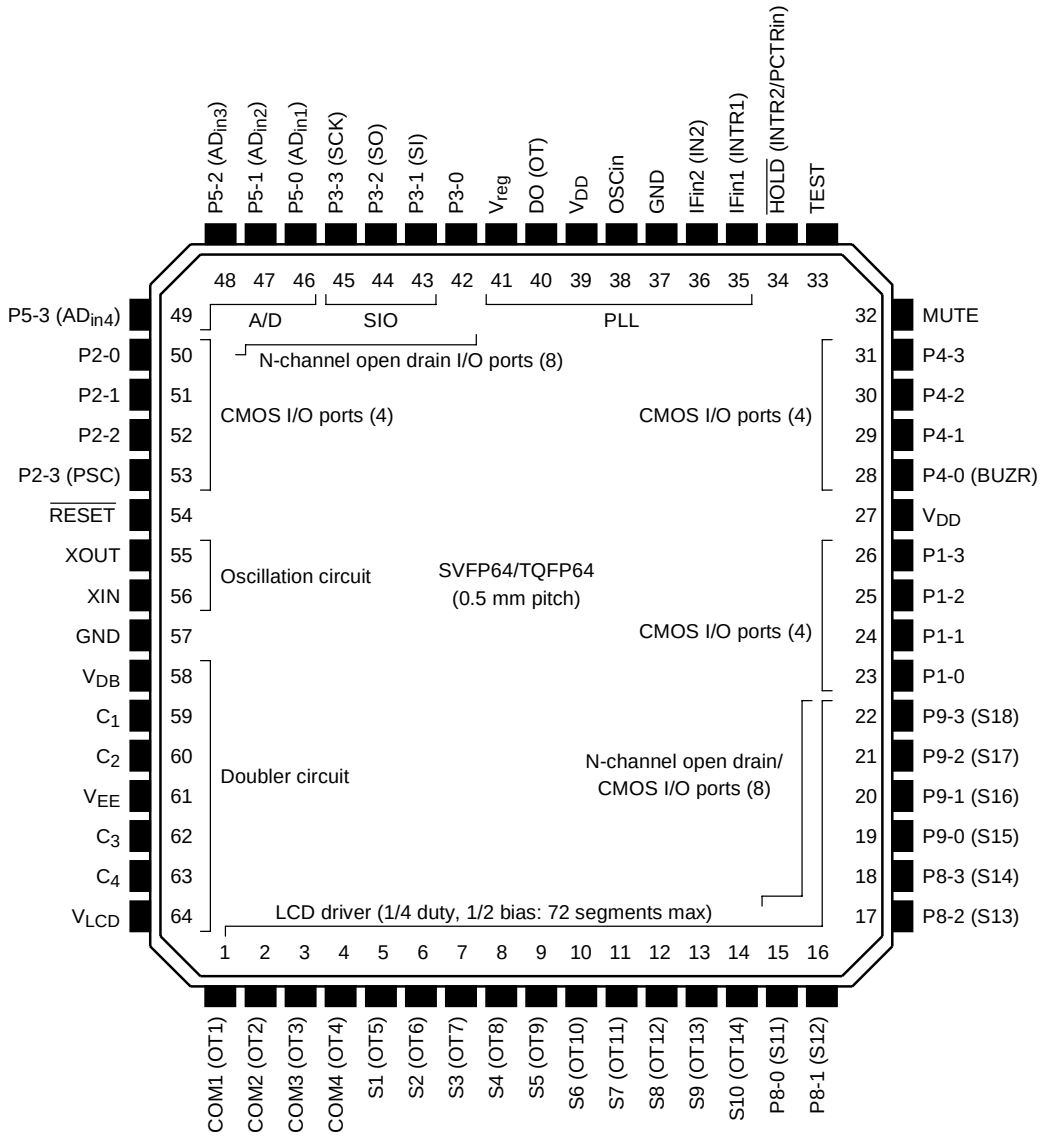
- CMOS DTS microcontroller LSI with built-in 230 MHz prescaler, PLL, and LCD driver
- Operating voltage: V_{DD} = 0.9~1.8 V (typ.: 1.5 V)
- Current dissipation:
  CPU in operation: I_{DD} = 40 µA typ.
  PLL in operation: I_{DD} = 6 mA typ. (VHF mode)
- Operating temperature range: Ta = −10~60°C
- Program memory (ROM): 16 bits × 4096 steps
- Data memory (RAM): 4 bits × 256 words
- Instruction execution time: With crystal oscillator: 40 µs
  With CR oscillator: 6 µs
  (at 1 MHz, V_{DD} = 1.1~1.8 V)
- Crystal oscillator frequency: 75 kHz
- Stack level: 8
- General-purpose IF counter: 20 bit (CMOS input supported)
- A/D converter: 6 bits × 4-channels
- LCD driver: 1/4 duty, 1/2 bias, 72 segments (max)
- I/O port: CMOS I/O ports: 12
  N-channel open drain I/O ports: 16 (max)
  Output-only port: 1
  Input-only ports: 3 (max)
- Timer/counter: 8 bits (as timer clock: INTR1/INTR2; instruction cycle: 1 kHz selectable)
- Pulse counter: 8-bit up/down counter (input via INTR2 pin)

Buzzer: 8 settings, 0.625~3 kHz; 4 built-in modes consisting of continuous, single-shot, 10 Hz intermittent, or 10 Hz intermittent at 1 Hz intervals.

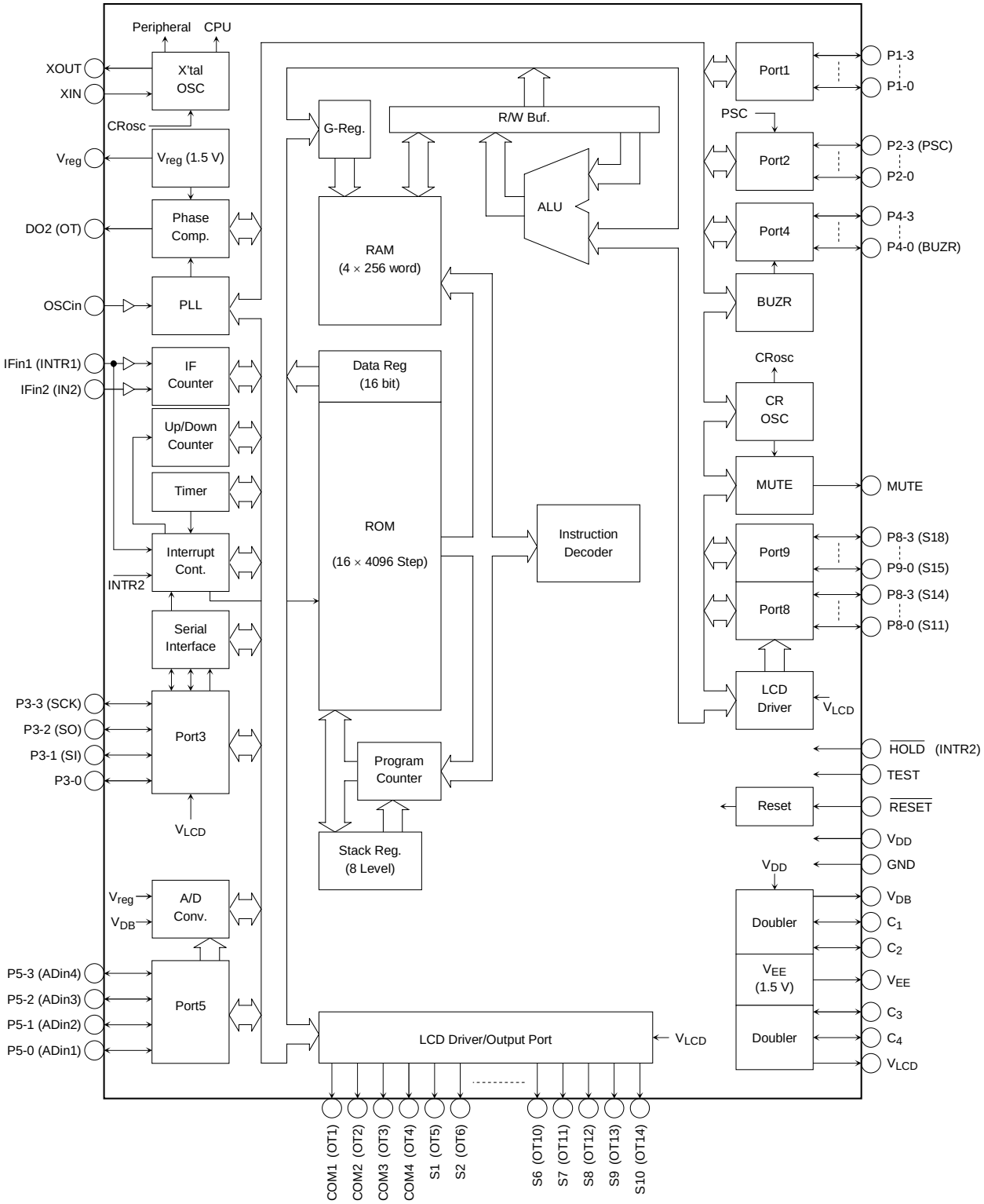
- Interrupts: 2 external, 2 internal (serial interface, 8-bit timer)
- Package: QFP-64 (0.5-mm/0.65-mm pitch, 1.4-mm thickness)

Note: Handle with care to prevent devices from deteriorating due to electrostatic discharge.

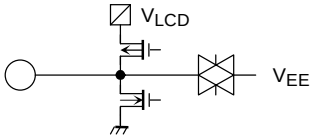
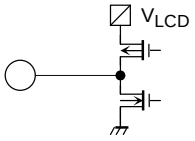
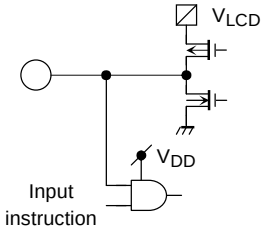
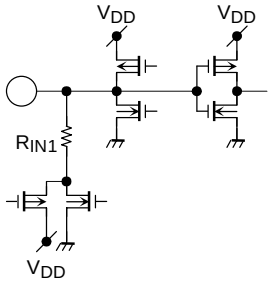
Pin Assignment (top view)



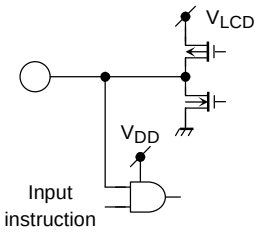
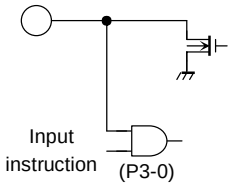
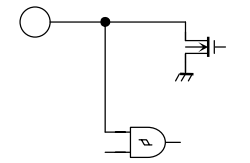
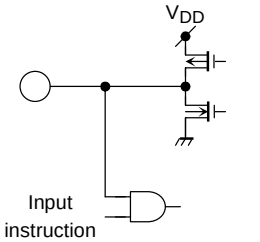
Block Diagram

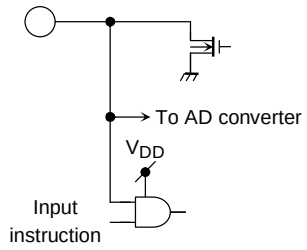
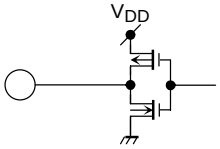
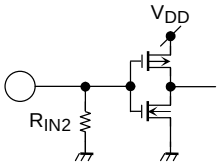


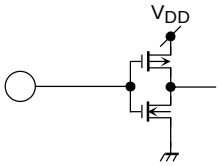
Description of Pin Function

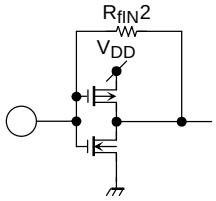
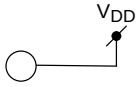
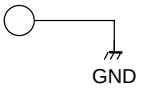
Pin No.	Symbol	Pin Name	Function and Operation	Remarks
1	COM1/OT1	LCD common output/Output port	Outputs common signals to LCD panels. Through a matrix with pins S1 to S18, a maximum of 72 segments can be displayed. Three levels, V_{LCD}, VEE (1/2 V_{LCD}), and GND, are output at 62.5 Hz every 2 ms. V_{EE} is output after system reset and CLOCK STOP are released, and a common signal is output after the DISP OFF bit is set to "0". These pins can be programmed as output ports (Note 1).	
2	COM2/OT2			
3	COM3/OT3			
4	COM4/OT4			
5~14	S1/OT5~ S10/OT14	LCD segment output/Output port	Segment signal output terminals for LCD panel. Together with COM1 to COM4, a matrix is formed that can display a maximum of 72 segments. V_{EE} is output after system reset and CLOCK STOP are released, and a common signal is output after the DISP OFF bit is set to "0". All pins from S1 to S10 can be programmed as output ports (Note 1), and all pins from S11 to S18 as I/O ports, in units of pins.	
15~22	P8-0/S13~ P9-3/S18	LCD segment output/ I/O port 8, 9	When the pins function as output ports, V_{LCD} pin potential and GND potential are output to them. When the pins function as I/O ports, drain output is N-ch open. Because power is supplied from V_{LCD} for the I/O ports, up to V_{LCD} voltage (3 V) can be applied. An instruction increments the data ports (OT1 to OT14) by 1 every time data are accessed. Therefore the ports can be used for external memory address signals, facilitating data access. Note: After system reset, the output port pins are set to LCD output, the I/O port pins to I/O port input.	
23~26	P1-0~P1-3	I/O port 1	The input and output of these 4-bit I/O ports can be programmed in 1-bit units. These pins can be programmed to be pulled up or down. Thus, they can be used as key input pins. By altering the input of I/O ports set to input, the CLOCK STOP mode or the WAIT mode can be released, and the MUTE bit of the MUTE pin can be set to "1".	

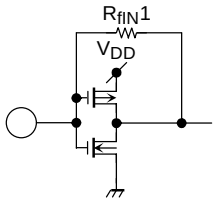
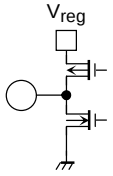
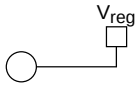
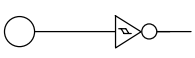
Note 1: When the LCD pin is set as an output port, the "H" level output is the doubled voltage V_{LCD}. Therefore disconnect the voltage boosting capacitor and connect the V_{LCD} pin to the V_{DD} pin.

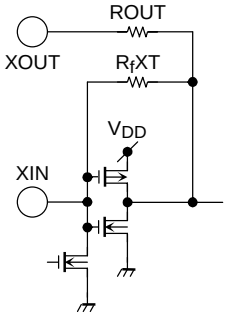
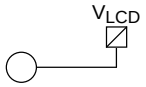
Pin No.	Symbol	Pin Name	Function and Operation	Remarks
50~52	P2-0~P2-2	I/O port 2	The input and output of these 4-bit I/O ports can be programmed in 1-bit units. The P2-3 pin is also used as a PLL prescaler PSC signal output pin. A PLL can be configured using an external prescaler. In such a case, set the pin to I/O port output.	
53	P2-3/PSC	I/O port 2 /Prescaler /PSC output		
42~45	P3-0 P3-1/SI P3-2/SO P3-3/SCK	I/O port 3 /Serial data input /Serial data output /Serial clock I/O	4-bit I/O ports, allowing input and output to be programmed in 1-bit units. The I/O ports are N-ch open drain. Up to 3.6 V can be input. Even at low voltage, N-ch high output current (2 mA typ.) can be obtained. These pins also function as serial interface circuit (SIO) input/output pins. There are two types of serial interface circuit: SIO1 allows 4 or 8-bit input/output and SIO2 allows 26-bit serial data input. SIO1 inputs data of SI pin serially with the edge of the clock of SCK pin, and outputs it to SO pin. Internal (SCK = 37.5 kHz), external, or rising/falling shift can be selected as the clock (SCK) for serial operation. The SO pin can be switched to serial input (SI), facilitating LSI control and communication between controllers. Setting “1” in the SIO2 bit sets the SCK pin to the SIO2 clock input and the SI/SO pin to SIO2 data input. A synchronization circuit is built-in for SIO2. When SIO interrupts are enabled, an interrupt is generated after SIO execution or by SIO2 operating clock input and the program jumps to address 4. All SIO inputs use built-in Schmitt circuits. SIO and all controls are programmable.	 
28	P4-0/BUZR	I/O port 4 /Buzzer output	4-bit I/O ports, allowing input and output to be programmed in 1-bit units. The P4-0 pin is also used for buzzer output. The buzzer output can select 8 kinds of 0.625 to 3-kHz frequencies with 4 modes: continuous output, single-shot output, 10 Hz intermittent output, and 10 Hz intermittent at 1 Hz intervals output. SIO, buzzer, and all associated controls can be programmed.	
29~31	P4-1~P4-3	I/O port 4		

Pin No.	Symbol	Pin Name	Function and Operation	Remarks
46~49	P5-0/AD_{in1}~ P5-3/AD_{in4}	I/O port 5 /AD analog voltage input	4-bit I/O ports, allowing input and output to be programmed in 1-bit units. Pins P5-0 to P5-3 can also be used for analog input to the built-in 6 bit, 4-channel AD converter. The conversion time of the built-in AD converter using the successive comparison method is 280 μs. The necessary pin can be programmed to AD analog input in 1-bit units. Up to the doubled voltage V_{DB} ($V_{DD} \times 2$) can be input as the AD input voltage. I/O ports are N-ch open drain output. Up to the V_{DB} voltage can be applied to the AD input pins. The AD converter and all associated controls are performed via sortware.	
32	MUTE	Muting output port	1-bit output port, normally used for muting control signal output. This pin can set the internal MUTE bit to “1” according to change in the input of I/O port 1 and $\overline{HOLD}$. The MUTE bit output logic can be changed. The internal CR oscillator clock can be output depending on the contents of the test port.	
33	TEST	Test mode control input	Input pin used for controlling TEST mode. “H” (high) level indicates TEST mode, while “L” (low) indicates normal operation. The pin is normally used at low level or in NC (no connection) state. (A pull-down resistor is built in.)	

Pin No.	Symbol	Pin Name	Function and Operation	Remarks
34	$\overline{HOLD}$ /INTR2 /PCTRin	Hold mode control input /External interrupt input /Plus count input	Input pin for request/release hold mode. Normally, this pin is used to input radio mode selection signals or battery detection signals. Hold mode includes CLOCK STOP mode (stops crystal oscillation) and WAIT mode (halts CPU). Setting is implemented with the CKSTP instruction or the WAIT instruction. To request Clock Stop mode, either L-level detection on the $\overline{HOLD}$ pin or forced execution can be programmed. The mode is released by H-level detection on the $\overline{HOLD}$ pin or input change, respectively. Executing the CKSTP instruction stops the clock generator and the CPU, resulting in entry to memory backup state. In memory backup state, current dissipation becomes low (1 μA or less) and the display output/CMOS output ports automatically become L level and N-ch open drain output is set toOff. Regardless of this input state, Wait mode is executed in order to lower power dissipation. Either operation of the crystal oscillator only or CPU suspension can be programmed. For operation of the crystal oscillator only, all displays are at L level and other pins are in hold state. For CPU suspension, the CPU stops and all others retain their states. Wait mode is released by changing $\overline{HOLD}$ input. The P34 pin is also used for external interrupt input. When interrupts are enabled and a 13.3 to 26.7-μA pulse or longer is input to the pin, interrupt INTR1/2 is generated and the program jumps to address 1/2. Input logic or rising/falling edge can be selected for each input interrupt. The internal 8-bit timer clock input can be selected as input to the pins. When the count value reaches the specified value, an interrupt is generated (address 4). The pin is also used for input of an 8-bit pulse counter. Input rising/falling or upcount/downcount can be selected for the counter.	

Pin No.	Symbol	Pin Name	Function and Operation	Remarks
35 36	IFin1/INTR1 IFin2/IN2	IF signal 1 input /External interrupt input IF signal 2 input /Input port	IF signal input pin for the IF counter to count the IF signals of the FM and AM bands and to detect the automatic stop position. The input frequency is between 0.3 to 12 MHz. A built-in input amp. and C coupling allow operation at low-level input. The IF counter is a 20-bit counter with optional gate times of 1, 4, 16 and 64 ms. 20 bits of data can be readily stored in memory. In Manual mode, gate On/Off or CR oscillator clock frequency count can be performed using an instruction. The input pin can be programmed for use as an input port (IN port). In this case, the pins are CMOS input. They can count input clocks using the IF counter. IFin1 also functions as an external interrupt input pin. When interrupts are enabled and a 13.3 to 26.7-μA pulse or longer is input to IFin1, an interrupt is generated and the program jumps to address 1. Input logic or rising/falling edge can be selected for the input interrupt. The internal 8-bit timer clock input can be selected as input to the pin. When the count value reaches the specified value, an interrupt is generated (address 4). Note: When a pin is set to IF input, the input is at high impedance in PLL Off mode or if the pins are not used for input.	
27, 39	V_{DD}	Power-supply pins	Pins to which power is applied. Normally, V_{DD} = 0.9~1.8 V is applied. In backup state (at execution of the CKSTP instruction), current dissipation drops (1 μA or less) and the power supply voltage can be reduced to 0.75 V. Note: To operate the power on reset, the power supply should start up in 10~100 ms.	
37, 57	GND			

Pin No.	Symbol	Pin Name	Function and Operation	Remarks
38	OSCin	local oscillation signal input	For FM input, mode can be switched between 1/2 + Pulse Swallow VHF and FM mode. For AM input, mode can be switched between Pulse Swallow (HF) and Direct Dividing (LF) mode. Normally, local oscillation output (Voltage-Controlled Oscillator: VCO output) of 80 to 230 MHz is input in VHF mode; 60 to 130 MHz in FM mode; 1 to 30 MHz in HF mode; 0.5 to 8 MHz in LF mode. A PLL can be configured using an external prescaler. In such a case, set the pin to LF, and connect the prescaler divider output to the OSCin input pin and the PSC input to the P2-3 (PSC) output pin. With an input amp incorporated, capacitive-coupling, small-amplitude operation is supported. Note: The input is at high impedance in PLL Off mode.	
40	DO/OT	Phase comparator output/output port	PLL phase comparator output pins. Tristate output. When the program counter divider output is higher than the reference frequency, H level is output; when lower, L level; and when they match, high impedance. For the phase comparator power supply, a 1.5-V constant voltage supply (V_{reg} pin) is used. Even if the power supply voltage drops, a stable PLL can be configured. The DO/OT pin can be programmed to high impedance or as an output port (OT). Note: For tristate output, the H-level output uses a constant voltage supply. When H-level output current is required, Toshiba recommend using an external power supply.	
41	V_{reg}	Phase comparator constant voltage supply	Phase comparator constant voltage supply. When the phase comparator output is tristate output, a constant voltage supply of 1.5 V (typ.) is output to the pin. For this output, connect a stabilizing capacitor (0.47 μF typ.). Constant voltage On/Off can be programmed. Because half the voltage potential can be switched to AD converter A/D input, it can be used to detect how much battery remains. At PLL operation, the constant voltage is used for H level phase comparator output. Thus, when H level output current is required, Toshiba recommend using an external power supply. Externally apply 1.8 to 3.6 V to the pin.	
54	$\overline{\text{RESET}}$	Reset input	Input pin for system reset signals. $\overline{\text{RESET}}$ takes place at low level; at high level, the program starts from address “0”.	

Pin No.	Symbol	Pin Name	Function and Operation	Remarks
55	XOUT	Crystal oscillator pin	Crystal oscillator pins. A reference 75 kHz crystal resonator is connected to the XIN and XOUT pins. The oscillator stops oscillating during CKSTP instruction execution. The VXT pin is the power supply for the crystal oscillator. A stabilizing capacitor (0.47 μF typ.) is connected. Usually, the clock of a crystal oscillator is used for the clock for peripheral equipment. Through programming, the built-in VCO can be changed to CPU and CPU only operation can be accelerated.	
56	XIN			
58	V_{DB}	Voltage doubler boosting output pins	Voltage doubler boosting output pins. The V_{DB} pin doubles the V_{DD} pin voltage using the voltage doubler boosting capacitor between C_1 and C_2. The doubled voltage is used for the AD converter and constant voltage circuit (V_{reg}, V_{EE}) power supply. The V_{EE} pin supplies a constant voltage of 1.5 V from the V_{DB} voltage. The voltage is doubled (to 3 V) using the voltage doubler boosting capacitor between C_3 and C_4. The doubled voltage is then supplied to the V_{LCD} pin. The V_{EE} potential and the V_{LCD} potential are used to drive the LCD. Connect a stabilizing capacitor between the V_{DB} pin and GND (0.1 μF, 10 μF typ.), and between the V_{LCD} pin and GND (0.1 μF typ.). Connect a voltage doubler boosting capacitor (0.1 μF typ.) between C_1 and C_2, and between C_3 and C_4. (Note)	
59	C_1			
60	C_2			
61	V_{EE}			
62	C_3			
63	C_4			
64	V_{LCD}			

Note: When the LCD pin is set as an output port, the “H” level output is the doubled voltage V_{LCD}. Therefore disconnect the voltage boosting capacitor and connect the V_{LCD} pin to the V_{DD} pin.

Description of Operations

○ CPU

The CPU consists of a program counter, a stack register, an ALU, a program memory, a data memory, a G-register, a data register, a DAL address register, a carry F/F, a judgment circuit, and an interruption circuit.

1. Program Counter (PC)

The program counter consists of a 14-bit binary up-counter and addresses the program memory (ROM). The counter is cleared when the system is reset and the programs start from the 0 address.

Under normal conditions, the counter is increased in increments of one whenever an instruction is executed, but the address specified in the instruction operand is loaded when a JUMP instruction or CALL instruction is executed.

Also, when an instruction that is equipped with the skip function (AIS, SLTI, TMT, RNS instructions, etc.) is executed, and the result of this includes a skip condition, the program counter is increased in increments of two and the subsequent instruction is skipped. Furthermore, if interruption is received, the vector address corresponding to each interruption is loaded.

Note: Addresses 0000H-0FFFH are reserved for the program memory. For this reason, access to addresses outside this range is prohibited.

Instruction	Contens of Program Counter (PC)													
	PC13	PC12	PC11	PC10	PC9	PC8	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
JUMP ADDR1	← Operand of instruction (ADDR1) →													
JUMP ADDR2	0	0	0	← Operand of instruction (ADDR2) →										
Power on reset RESET by reset pin	0	0	0	0	0	← Operand of instruction (ADDR3) →					← Contents of general register (r) →			
DAL (DA) (DAL bit = 1)	← DAL address register (DA) →													
RN, RNS, RNI	← Contents of stack register →													
At the time of an interruption reception	← Vector address of each interruption →													
Power on reset RESET by reset pin	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Priority	Interruption Factor	Vector Address
1	INTR1 pin	0001H
2	INTR2 pin	0002H
3	Serial inter face	0003H
4	Timer counter	0004H

2. Stack Register

A register consisting of 8 × 14 bits which stores the contents of the program counter +1 (the return address) when a sub-routine call instruction is executed. The contents of the stack register are loaded into the program counter when the return instruction (RN, RNS, RNI instruction) is executed.

There are eight stack levels available and nesting occurs with both levels.

3. ALU

ALU is equipped with binary 4-bit parallel add/subtract functions, logical operation, comparison and multiple bit judgment functions. This CPU is not equipped with an accumulator, and all operations are handled directly within the data memory.

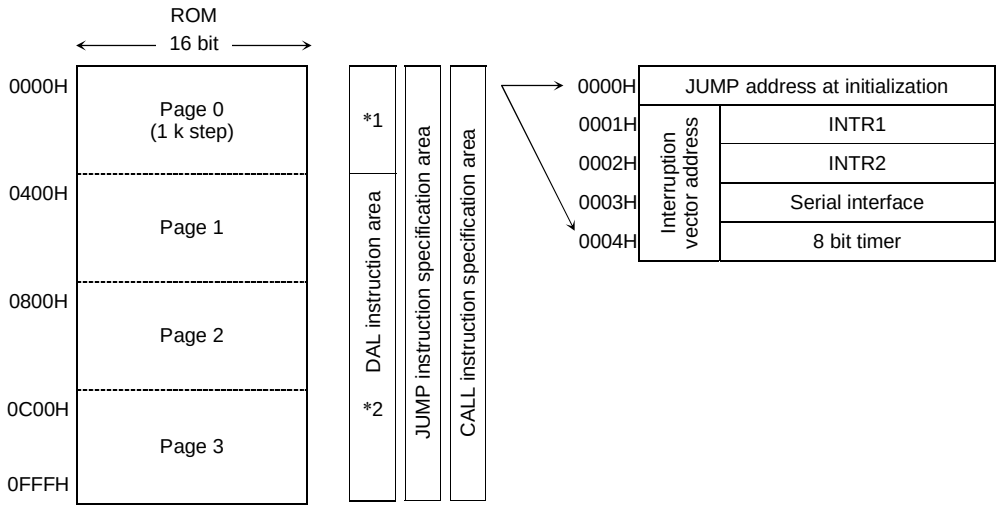
4. Program Memory (ROM)

The program memory consists of 16 bits × 4096 steps and is used for storing programs. The usable address range consists of 4096 steps between address 0000H ~ 0FFFH.

The program memory is divided into 4096 separate steps and consists of page 0 ~ 3. The JUMP instruction and CALL instruction can be freely used throughout all 4096 steps.

In case of setting DAL bit (it arranges on I/O map) "0" (DAL ADDR3, (r) command), the program memory address 0000H ~ 03FFH (page 0) are used as data area and setting DAL bit "1" (DAL (DA) command), the program memory address 0000H to 0FFFH (page 0 ~ 3) are used as data area. The 16 bit contents of this can be loaded into the data register by executing the DAL instruction.

Note: An address outside of the program lop must be set when establishing a data area within the program memory.



*1: DAL bit = DAL access area at setting "0"

*2: DAL bit = DAL access area at setting "1"

Note: DAL bit is arranged on I/O map.

5. Data Memory (RAM)

The data memory consists of 4 bit × 256 words and is used for storing data. These 256 words are expressed in row addresses (4 bits) and column addresses (4 bits). 192 words (row address = address 004H ~ 00FH) within the data memory are addressed indirectly by the G-register. Owing to this, it is necessary to specify the row address with the G-register before the data in this area can be processed.

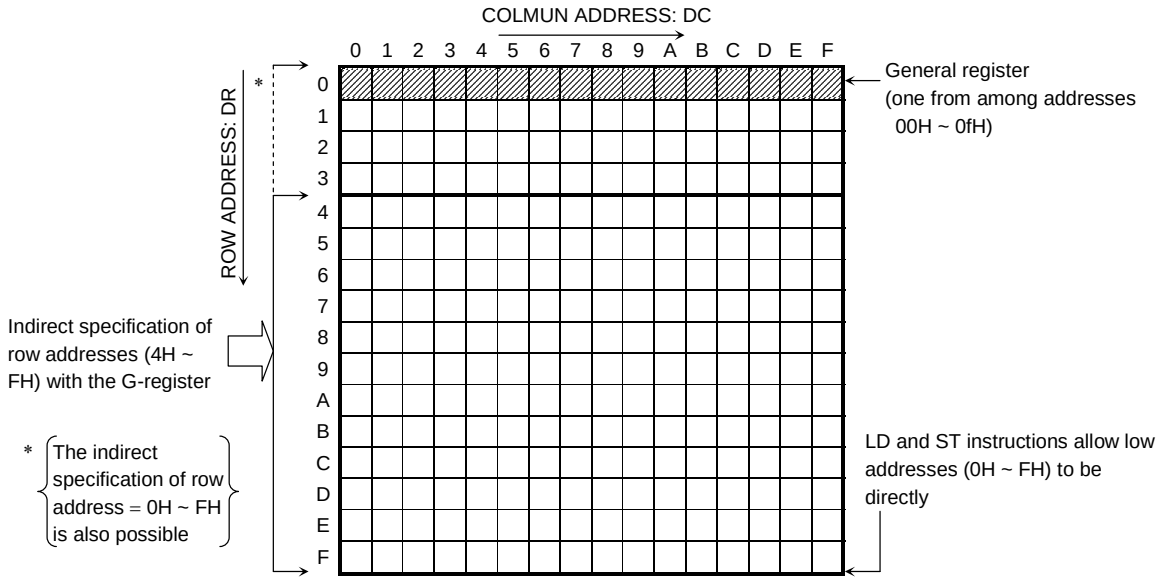
The address 00H ~ 0FH within the data memory are known as general registers, and these can be used simply by specifying the relevant column address (4 bit). These sixteen general registers can be used for operations and transfers with the data memory, and may also be used as normal data memories.

Note: The column address (4 bit) that specifies the general register is the register number of the general register.

Note: All row address (addresses 0H ~ FH) can be specified indirectly with the G-register.

Note: The data memory is 256 words and 2 bits of the 6-bit higher ranks of G-register row address are used “0” (00H ~ 0FH address).

Note: By using LD and ST instructionss, it can be addressed directly in 256 words (row address = 00H ~ 0FH) in a data memory.



6. G-Register (G-REG)

The G-register is a 4 bits register used for addressing the row addresses (D_R = 4H ~ FH addresses) of the data memory's 192 words.

The contents of this register are validated when the MVGD instruction or MVGS instruction are executed, and not affected through the execution of any other instructions. This register is used as one of the ports, and the contents are set when the OUT1 instruction from among the I/O instructions is executed. The 6-bit contents can be directly set by execution of STIG instruction.
(→Refer to the Register Port section.)

7. Data Register (DATA REG)

The data register consists of 1 □ 16 bits and stores 16 bits of optional address data. This register is used as one of the ports, and the contents are loaded into the data memory in units of 4 bits when an IN1 instruction from among the I/O instructions is executed. (□ Refer to the Register Port section.)

Moreover, this register supports writing from the data memory and is used for evacuation/return processing of the data at the time of interruption.

8. DAL Address Register (DA)

The data register consists of 1 × 14 bits.

If a DAL instruction is executed when the DAL bit is set to "1", 16 bits of the data of the free addresses in the program memory specified by this DAL address register are loaded. By the setting (DATA) → DA bit to "1", the contents of data register (DATA REG) can be transmitted to DAL address register (DA).

This register and a control bit are treated as a port, and are accessed by IN3/OUT3 instruction of an input-and-output instruction. (→ Refer to section in Register port item)

9. Carry F/F (Ca Flag)

This is set when either Carry or Borrow are issued in the result of calculation instruction execution and is reset if neither of these are issued.

The contents of carry F/F can only be amended through the execution addition, subtraction, CLT, CLTC instructions and are not affected by the execution of any other instruction.

The carry F/F can be accessed by the IN1/OUT1 instruction of an input-and-output instruction. For this reason, an input-and-output command performs the evacuation and the return at the time of interruption between data memories. (→ Refer to the Register Port section.)

10. Judgment Circuit (J)

This circuit judges the skip conditions when an instruction equipped with the skip function is executed. The program counter is increased in increments of two when the skip conditions are satisfied, and the subsequent instruction is skipped.

There are 15 instructions equipped with a wide variety of skip functions available. (→ Refer to the items marked with a "*" symbol in the Table Instruction Functions and Operational Instructions)

11. Interruption Circuit

An interruption circuit branches to each vector address by the demand from circumference hardware, and performs each interruption processing. (→Refer to the interruption function section.)

12. Instruction Set Table

A total of 57 instruction sets are available, and all of these are single-word instructions.
These instructions are expressed with 6-bit instruction codes.

High order 2 bit / Low order 4 bit		00		01		10	11	
		0		1		2	3	
0000	0	AI	M, I	TMTR	r, M		SLTI	M, I
0001	1	AIC	M, I	TMFR	r, M		SGEI	M, I
0010	2	SI	M, I	SEQ	r, M		SEQI	M, I
0011	3	SIB	M, I	SNE	r, M		SNEI	M, I
0100	4	ORIM	M, I	LD	r, M*	JUMP ADDR1	TMTN	M, N
0101	5	ANIM	M, I				TMT	M, N
0110	6	XORIM	M, I				TMFN	M, N
0111	7	MVIM	M, I				TMF	M, N
1000	8	AD	r, M	ST	M*, r		IN1	M, C
1001	9	AC	r, M				IN2	M, C
1010	A	SU	r, M				IN3	M, C
1011	B	SB	r, M				OUT1	M, C
1100	C	ORR	r, M	CLT	r, M		OUT2	M, C
1101	D	ANDR	r, M	CLTC	r, M		OUT3	M, C
1110	E	XORR	r, M	MVGD	r, M		DAL	ADDR3, r
1111	F	MVSR	M1, M2	MVGS	M, r	CAL ADDR2	SHRC	M
							RORC	M
							STIG	I*
							SKP, SKPN	
							RN, RNS	
							WAIT	P
							CKSTP	
							XCH	M
							DI, EI, RNI	
							NOOP	

13. Table of Instruction Functions and Operational Instructions

(Description of the symbols used in the table)

M : Data memory address.
Generally one of the addresses from among addresses 00H to 3FH in the data memory.
M* : Data memory address (256 words)
One of the addresses from among addresses 000H to 0FFH in the data memory.
(Effective only at the time of ST and LD instruction execution)
r : General register
One of the addresses from among addresses 00H to 00FH in the data memory.
PC : Program Counter (14 bits)
STACK : Stack register (14 bits)
G : G-register (6 bits)
DATA : Data register (16 bits)
I : Immediate data (4 bits)
I* : Immediate data (6 bits, effective only at the time of STIG instruction execution)
N : Bit position (4 bits)
□ : ALL "0"
C : Port code No. (4 bits)
CN : Port code No. (4 bits)
RN : General register No. (4 bits)
ADDR1 : Program memory address (14 bits)
ADDR2 : Program memory address within page 0 to 3 (12 bits)
ADDR3 : High order 6 bits of the program memory address within page 0.
DA : DAL address register
(14 bits, effective only DAL instruction at the time of DAL bits is set to "1")
Ca : Carry
CY : Carry flag
P : Wait condition
b : Borrow
IN1~IN3 : The ports used during the execution of instructions IN1 to IN3
OUT1~OUT3 : The ports used during the execution of instructions OUT1 to OUT3
( ) : Contents of the register or data memory
[ ] C : Contents of the port indicating code No. C (4 bits)
[ ] : Contents of the data memory indicating the contents of the register or data memory
[ ] P : Contents of the program memory (16 bits)
IC : Instruction code (6 bits)
* : Commands equipped with the skip function
DC : Data memory column address (4 bits)
DR : Data memory row address (2 bits)
DR* : Data memory row address
(4 bits, effective only at the time of ST and LD instruction execution)
(M) b0~(M) b3 : Bits data of the contents of a data memory (1 bit)

Instruc-tion Group	Mnemonic		Skip Function	Function Description	Operation Description	Machine Language (16 bits)			
						IC (6 bits)	A (2 bits)	B (4 bits)	C (4 bits)
Addition Instructions	AI	M, I		Add immediate data to memory	M ← (M) + I	000000	DR	DC	I
	AIC	M, I		Add immediate data to memory with carry	M ← (M) + I + ca	000001	DR	DC	I
	AD	r, M		Add memory to general register	r ← (r) + (M)	001000	DR	DC	RN
	AC	r, M		Add memory to general register with carry	r ← (r) + (M) + ca	001001	DR	DC	RN
Subtraction Instructions	SI	M, I		Subtract immediate data from memory	M ← (M) − I	000010	DR	DC	I
	SIB	M, I		Subtract immediate data from memory with borrow	M ← (M) − I − b	000011	DR	DC	I
	SU	r, M		Subtract memory from general register	r ← (r) − (M)	001010	DR	DC	RN
	SB	r, M		Subtract memory from general register with borrow	r ← (r) − (M) − b	001011	DR	DC	RN
Comparison Instructions	SLTI	M, I	*	Skip if memory is less than immediate data	Skip if (M) < I	110000	DR	DC	I
	SGEI	M, I	*	Skip if memory is greater than or equal to immediate data	Skip if (M) ≧ I	110001	DR	DC	I
	SEQI	M, I	*	Skip if memory is equal to immediate data	Skip if (M) = I	110010	DR	DC	I
	SNEI	M, I	*	Skip if memory is not equal to immediate data	Skip if (M) ≠ I	110011	DR	DC	I
	SEQ	r, M	*	Skip if general register is equal to memory	Skip if (r) = (M)	010010	DR	DC	RN
	SNE	r, M	*	Skip if general register is not equal to memory	Skip if (r) ≠ (M)	010011	DR	DC	RN
	CLT	r, M		Set carry flag if general register is less than memory, or reset if not	(CY) ← 1 if (r) < (M) or (CY) ← 0 if (r) ≧ (M)	011100	DR	DC	RN
	CLTC	r, M		Set carry flag if general register is less than memory with carry or reset if not	(CY) ← 1 if (r) < (M) + (ca) or (CY) ← 0 if (r) ≧ (M) + (Ca)	011101	DR	DC	RN

Instruc-tion Group	Mnemonic	Skip Function	Function Description	Operation Description	Machine Language (16 bits)			
					IC (6 bits)	A (2 bits)	B (4 bits)	C (4 bits)
Transfer Instructions	LD r, M*		Load memory to general register	r ← (M*)	0101	DR* (4 bits)	DC	RN
	ST M*, r		Store memory to general register	M* ← (r)	0110	DR* (4 bits)	DC	RN
	MVSR M1, M2		Move memory to memory in same row	(DR, DC1) ← (DR, DC2)	001111	DR	DC1	DC2
	MVIM M, I		Move immediate data to memory	M ← I	000111	DR	DC	I
	MVGD r, M		Move memory to destination memory referring to G-register and general register	[(G), (r)] ← (M)	011110	DR	DC	RN
	MVGS M, r		Move source memory referring to G-register and general register to memory (Note)	(M) ← [(G), (r)]	011111	DR	DC	RN
	STIG I*		Move immediate data to G-register	G ← I*	111111	I*		0010
I/O Instructions	IN1 M, C		Input IN1 port data to memory	M ← [IN1] C	111000	DR	DC	CN
	OUT1 M, C		Output contents of memory to OUT1 port	[OUT1] C ← (M)	111011	DR	DC	CN
	IN2 M, C		Input IN2 port data to memory	M ← [IN2] C	111001	DR	DC	CN
	OUT2 M, C		Output contents of memory to OUT2 port	[OUT2] C ← (M)	111100	DR	DC	CN
	IN3 M, C		Input IN3 port data to memory	M ← [IN3] C	111010	DR	DC	CN
	OUT3 M, C		Output contents of memory to OUT3 port	[OUT3] C ← (M)	111101	DR	DC	CN
Logical Poeration Instructions	ORR r, M		Logical OR of general register and memory	r ← (r) ∨ (M)	001100	DR	DC	RN
	ANDR r, M		Logical AND of general register and memory	r ← (r) ∧ (M)	001101	DR	DC	RN
	ORIM M, I		Logical OR of memory and immediate data	M ← (M) ∨ I	000100	DR	DC	I
	ANIM M, I		Logical AND of memory and immediate data	M ← (M) ∧ I	000101	DR	DC	I
	XORIM M, I		Logical exclusive OR of memory and immediate data	M ← (M) ∀ I	000110	DR	DC	I
	XORR r, M		Logical exclusive OR of general register and memory	r ← (r) ∀ (M)	001110	DR	DC	RN

Note: The execution time for the MVGS instruction is two machine cycles.

Instruc-tion Group	Mnemonic	Skip Function	Function Description	Operation Description	Machine Language (16 bits)			
					IC (6 bits)	A (2 bits)	B (4 bits)	C (4 bits)
Bit Judgement Instruction	TMTR r, M	*	Test general register bits by memory bits, then skip if all bits specified are true	Skip if r [N (M)] = all "1"	010000	DR	DC	RN
	TMFR r, M	*	Test general register bits by memory bits, then skip if all bits specified are false	Skip if r [N (M)] = all "0"	010001	DR	DC	RN
	TMT M, N	*	Test memory bits, then skip if all bits specified are true	Skip if M (N) = all "1"	110101	DR	DC	N
	TMF M, N	*	Test memory bits, then not skip if all bits specified are false	Skip if M (N) = all "0"	110111	DR	DC	N
	TMTN M, N	*	Test memory bits, then not skip if all bits specified are true	Skip if M (N) = not all "1"	110100	DR	DC	N
	TMFN M, N	*	Test memory bits, then not skip if all bits specified are false	Skip if M (N) = not all "0"	110110	DR	DC	N
	SKP	*	Skip if carry flag is true	Skip if (CY) = 1	111111	00	—	0011
	SKPN	*	Skip if carry flag is false	Skip if (CY) = 0	111111	01	—	0011
SUB = Routne Instructions	CAL ADDR2		Call subroutine	STACK ← (PC) + 1 and PC ← ADDR2	1011	ADDR2 (12 bits)		
	RN		Return to main routine	PC ← (STACK)	111111	10	—	0011
	RNS		Return to main routine and skip unconditionally	PC ← (STACK) and skip	111111	11	—	0011
JUMP Instructions	JUMP ADDR1		Jump to address specified	PC ← ADDR1	10	ADDR1 (14 bits)		
Intruption Instruction	DI		Reset IMF (Note)	IMF ← 0	111111	00	—	0111
	EI		Set IMF (Note)	IMF ← 1	111111	01	—	0111
	RNI		Return to main routine and set IMF (Note)	PC ← (STACK) IMF ← 1	111111	11	—	0111

Note: The IMF bit is an interruption master permission flag and is arranged on I/O map.
(→ Refer to the interruption function section.)

Instruc-tion Group	Mnemonic	Skip Function	Function Description	Operation Description	Machine Language (16 bits)			
					IC (6 bits)	A (2 bits)	B (4 bits)	C (4 bits)
Other Instructions	SHRC M		Shift memory bits to right direction with carry	0 → (M) b3 → (M) b2 → (M) b1 → (M) b0→ (CY)	111111	DR	DC	0000
	RORC M		Rotate memory bits to right direction with carry	┌→ (M) b3 → (M) b2 → (M) b1→ (M) b0 → └ (CY)	111111	DR	DC	0001
	XCH M		Exchange memory bits mutually	(M) b3 ↔ (M) b0, (M) b2 ↔ (M) b1	111111	DR	DC	0110
	DAL ADDR3, r		IF DAL bit = 0 then load program in page 0 to DATA register IF DAL bit = 1 then load program memory referring to DAL address register to DATA register (Note)	DATA ← [ADDR3 + (r)] p in page 0	111110	ADDR3 (6 bits)		RN
	WAIT P		At P = "0" H, the condition is CPU waiting (soft wait mode)	Wait at condition P	111111	P	—	0100
			At P = "1" H, expect for clock generator, all function is waiting (hard wait mode)					
	CKSTP		Clock generator stop	Stop clock generator to MODE condition	111111	—	—	0101
	NOOP		No operation	—	111111	—	—	1111

Note: The four low order bits of the program memory's 10-bit address specified with the DAL instruction are addressed indirectly with the contents of the general registerer.

Note: The excution time for the DALinstruction is two machine cycles.

Note: DALbitsand DAL address register (DA) are arrenged on the I/O map.
(→ Refer to the Register Port section)

Note: When "1" is set to DAL bit and the DAL instruction is executed, all the operand part becomes invalid and the reference addresses are used for the DAL address register.

I/O Map (IN1 (M, C), IN2 (M, C), IN3 (M, C), OUT1 (M, C), OUT2 (M, C), OUT3 (M, C))

I/O / Code	φL1				φL2				φL3				φK1				φK2				φK3			
	OUT1				OUT2				OUT3				IN1				IN2				IN3			
	Y1	Y2	Y4	Y8	Y1	Y2	Y4	Y8	Y1	Y2	Y4	Y8	Y1	Y2	Y4	Y8	Y1	Y2	Y4	Y8	Y1	Y2	Y4	Y8
0	HF	Power control		FM	I/O port 1 pull-down				I/O port 1				IF monitor			0	A/D data				I/O port 1			
		PW0	PW1		PD0	K1	PD2	PD3	-0	-1	-2	-3	BUSY	MANUAL	OVER		AD0	AD1	AD2	AD3	-0	-1	-2	-3
1	Programmable counter 1				A/D control				I/O port 2				IF data 1				A/D data				I/O port 2			
	P0	P1	P2	P16	AD SEL0	AD SEL1	AD SEL2	STA	-0	-1	-2	-3	F0	F1	F2	F3	AD4	AD5	BUSY	0	-0	-1	-2	-3
2	Programmable counter 2				Serial interface control 1				I/O port 3				IF data 2								I/O port 3			
	P4	P5	P6	P7	edge	$\overline{SCK}$-INV	$\overline{SCK}$-I/O	SIO-ON	-0	-1	-2	-3	F4	F5	F6	F7					-0	-1	-2	-3
3	Programmable counter 3				Serial interface control 2				I/O port 4				IF data 3				Serial interface monitor			0	I/O port 4			
	P8	P9	P10	P11	STA	SO-I/$\overline{O}$	8/$\overline{4}$bit	SIO Select	-0	-1	-2	-3	F8	F9	F10	F11	BUSY	COUNT	SIO F/F		-0	-1	-2	-3
4	Programmable counter 4				Serial interface output data 1				I/O port 5				IF data 4				Serial interface input data 1				I/O port 5			
	P12	P13	P14	P15	SO0	SO1	SO2	SO3	-0	-1	-2	-3	F12	F13	F14	F15	SI0	SI1	SI2	SI3	-0	-1	-2	-3
5	Reference select			Programmable counter	Serial interface output data 2								IF data 5				Serial interface input data 2							
	R0	R1	R2	P16	SO4	SO5	SO6	SO7					F16	F17	F18	F19	SI4	SI5	SI6	SI7				
6	IF counter control 1				Timer reset		CKSTP mode	Test port 2									Timer							
	IF1/$\overline{2}$	PW	IF1/$\overline{INTR1}$	IF2/$\overline{IN2}$	2 Hz F/F	Clock		#4									2 Hz F/F	10 Hz	100 Hz	0				
7	IF counter control 2				Interrupt control				I/O port 8				$\overline{HOLD}$	INTR1	INTR2	0	Interrupt master flag	0	0	0	I/O port 8			
	STA/$\overline{STP}$	MANIAL	G0	G1	POL1 (INTR1)	POL2 (INTR2)	IE	*	-0	-1	-2	-3					IMF				-0	-1	-2	-3
8	MUTE	MUTE control			Interrupt permission flag				I/O port 9				MUTE	MUTE control			Interrupt permission flag				I/O port 9			
		I/O-1	POL	HOLD	EF1 (INTR1)	EF2 (INTR2)	EF3 (SIO)	FE4 (Timer)	-0	-1	-2	-3		I/O	POL	HOLD	EF1	EF2	EF3	EF4	-0	-1	-2	-3
9	UNLOCK Detection	DO2 control			Interrupt latch reset				HOLD PLL off control	IF counter Split	Prescaller IN	PSC ENA	Unlock detection		Input port		Interrupt latch							
	RESET	PN	M0	M1	ILR1 (INTR1)	ILR2 (INTR2)	ILR3 (SIO)	ILR4 (Timer)					F/F	ENA	(INTR1)	IN2	IL1	IL2	IL3	IL4				
A	BUZZR output control 1				Timer counter Interrupt detection data1				DAL	(DATA) → DA	OT Count Up	port 1 Pull-up					Timer counter data 1				DAL	0	0	0
	BF0	BF1	BF2	BEN	ID0	ID1	ID2	ID3									CT0	CT1	CT2	CT3				
B	BUZZR output control 2				Timer counter Interrupt detection data2				DAL address								Timer counter data 2				DAL address			
	BM0	BM1	BUZR ON	POL	ID4	ID5	ID6	ID7	DA0	DA1	DA2	DA3					CT4	CT5	CT6	CT7	DA0	DA1	DA2	DA3
C	CA Flag	*	*	*	Timer counter control				Data register 1				CA flag	0	0	0					Data register 1			
					CK0	CK1	GT	CR	d0	d1	d2	d3									d0	d1	d2	d3
D	G register 1				Data select				Data register 2				G register 1				Data select				Data register 2			
	G0	G1	G2	G3	SEL1	SEL2	SEL4	SEL8	d4	d5	d6	d7	G0	G1	G2	G3	S1	S2	S3	S4	d4	d5	d6	d7
E	G register 2				Segment data 1/ General purpose output data				Data register 3				G register 2								Data register 3			
	G4	G5	*	*	COM1/OT	COM2/OT	COM3/OT	COM4/OT	d8	d9	d10	d11	G4	G5	0	0					d8	d9	d10	d11
F	Test port 1				Segment data2/ Segment IO control				Data register 4												Data register 4			
	#0	#1	#2	#3	COM1	COM2	COM3	COM4	d12	d13	d14	d15									d12	d13	d14	d15

Refer to next page

ϕKL2D

Data Select			
S1	S2	S4	S8

I/O / ϕL2D	ϕL2E				ϕL2F			
	OUT2				OUT2			
	Y1	Y2	Y4	Y8	Y1	Y2	Y4	Y8
0	S1/OT1~OT4				S13			
	COM1 /OT1	COM2 /OT2	COM3 /OT3	COM4 /OT4	COM1	COM2	COM3	COM4
1	S2/OT5~OT8				S14			
	COM1 /OT5	COM2 /OT6	COM3 /OT7	COM4 /OT8	COM1	COM2	COM3	COM4
2	S3/OT9~OT12				S15			
	COM1 /OT9	COM2 /OT10	COM3 /OT11	COM4 /OT12	COM1	COM2	COM3	COM4
3	S4/OT13~OT14				S16			
	COM1 /OT13	COM2 /OT14	COM3	COM4	COM1	COM2	COM3	COM4
4	S5				S17			
	COM1	COM2	COM3	COM4	COM1	COM2	COM3	COM4
5	S6				S18			
	COM1	COM2	COM3	COM4	COM1	COM2	COM3	COM4
6	S7				Segment/IO select			
	COM1	COM2	COM3	COM4	S11	S12	S13	S14
7	S8				Segment/IO select			
	COM1	COM2	COM3	COM4	S15	S16	S17	S18
8	S9				I/O control 1			
	COM1	COM2	COM3	COM4	-0	-1	-2	-3
9	S10				I/O control 2			
	COM1	COM2	COM3	COM4	-0	-1	-2	-3
A	S11				I/O control 4			
	COM1	COM2	COM3	COM4	-0	-1	-2	-3
B	S12							
	COM1	COM2	COM3	COM4				
C								
D								
E								
F					LCD control			*
					DISP OFF	LCD OFF	OTB-UP	

ϕL3B				ϕK3B			
OUT3				IN3			
Y1	Y2	Y4	Y8	Y1	Y2	Y4	Y8
DAL address 1				DAL address 1			
DA0	DA1	DA2	DA3	DA0	DA1	DA2	DA3
DAL address 2				DAL address 2			
DA4	DA5	DA6	DA7	DA4	DA5	DA6	DA7
DAL address 3				DAL address 3			
DA8	DA9	DA10	DA11	DA8	DA9	DA10	DA11
DAL address 4				DAL address 4			
DA12	DA13	*	*	DA12	DA13	0	0
Pulse counter control				Pulse counter data			
DOWN	POL	*	*	PC0	PC1	PC2	PC3
Pulse counter control				Pulse counter data			
CTR RESET	OVER RESET	*	*	PC4	PC5	PC6	PC7
OSC control				Pulse counter data			
IFin	CPU Select	OSC on	Freq Select	OVER	0	0	0
OSC data				SIO2 decode data			
OSC0	OSC1	OSC2	OSC3	DEC0	DEC1	DEC2	DEC3
SIO2 data select	*			SIO2 information data 1			
				INF0	INF1	INF2	INF3
				SIO2 information data 2			
				INF4	INF5	INF6	INF7
Vreg ON	*	*	*	SIO2 information data 3			
				INF8	INF9	INF110	INF11
				SIO2 information data 4			
				INF12	INF13	INF14	INF15
0: Offset data 1: Check data				SIO2 offset/Check data 1			
				OFS0 /CHK0	OFS1 /CHK1	OFS2 /CHK2	OFS3 /CHK3
				SIO2 offset/Check data 2			
				OFS4 /CHK4	OFS5 /CHK5	OFS6 /CHK6	OFS7 /CHK7
				SIO2 offset/Check data 3			
				OFS8 /CHK8	OFS9 /CHK9	0	0

○ I/O map

All of the ports within the device are expressed with a matrix of six I/O instructions (OUT 1 ~ 3 instructions and IN 1 ~ 3 instructions) and a 4-bit code number.
The allocation of these ports is shown on the following page in the form of an I/O map. The ports used in the execution of the various I/O instructions on the horizontal axis of the I/O map are allocated to the port code numbers indicated on the vertical axis. The G-register, data register and DAL bits are also used as ports.
The OUT1 ~ 3 instructions are specified as output ports and the IN 1 ~ 3 instructions are specified as input ports.

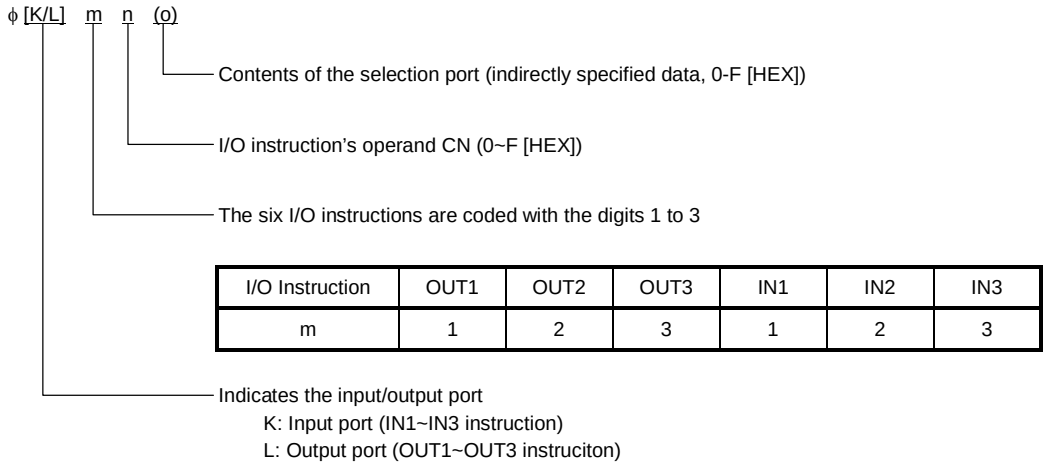
Note: The ports indicated by the angled lines on the I/O map do not actually exist within the device.

The contents of other ports and data memories are not affected when data is output to a non-existent output port with the execution of the output instruction. The data loaded from data memories when a non-existent input port has been specified with the execution of an input instruction becomes "1".

Note: The outout ports marked with an asterisk (*) on the I/O map are not used. Data output to these ports assume the don't care status.

Note: The Y1 contents of the ports expressed in 4 bits correspond to the data memory's low order bits and the Y8 contents correspond to the high order bits.

The ports specified with the six I/O instructions and code No. C are coded in the following manner:



I/O Instruction	OUT1	OUT2	OUT3	IN1	IN2	IN3
m	1	2	3	1	2	3

(Example) The setting for the G-register is allocated to code "D" and "E" in the OUT1 instruction.
The encoded expression at this time becomes "ϕL1D"and "ϕL1E".

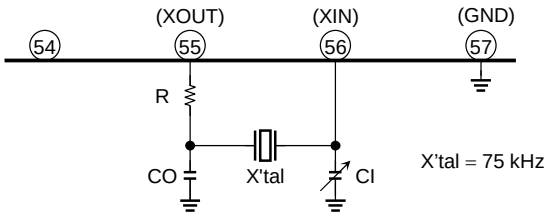
○ Clock Generator

The clock generator generates the standard clock used as the standard of the system clock supplied to a core-based CPU and circumference hardware.

Through the program, it is possible to switch between an external crystal oscillation circuit and the built-in CR oscillation circuit as the CPU operation clock.

1. Crystal Oscillation Circuit

75 kHz crystal resonator is connected to the device's crystal resonator terminal (XN, XOUT) as indicated below. During normal operation, the oscillation signal is supplied to the clock generator, the reference frequency divider and other elements, and generates the various CPU timing signals and reference frequency.



Note: It is necessary to use a crystal resonator with a low CI value and favorable start-up characteristics. Be sure to adjust and set the external resistance and capacitor constant to the crystal resonator actually used.

2. CR VCO

Through the use of the built-in CR VCO, it is possible to raise the CPU processing speed. This will be utilized for high-speed processing in the required system. The OSCon bit controls the ON/OFF operation of the CR oscillation circuit; and if this bit is set to "1", the CR VCO starts operating.

If the setting of the CPU Select bits is "0", the CPU operates on the 75 kHz for the crystal oscillator clock; if the setting is "1", the CPU operates on the CR VCO clock. The oscillation frequency of CR VCO (fCR) is 1 MHz (typ.); and a clock that divides this frequency by 1/2 or 1/4 can be used as the CPU operation clock.

The CR VCO frequency serves as a system that can control the resistance of the CR VCO through the program so that factors, such as power supply voltage and the variations in the built-in capacitor and resistance can be changed. For this reason, it is possible to calculate the CR oscillation frequency using the IF counter.

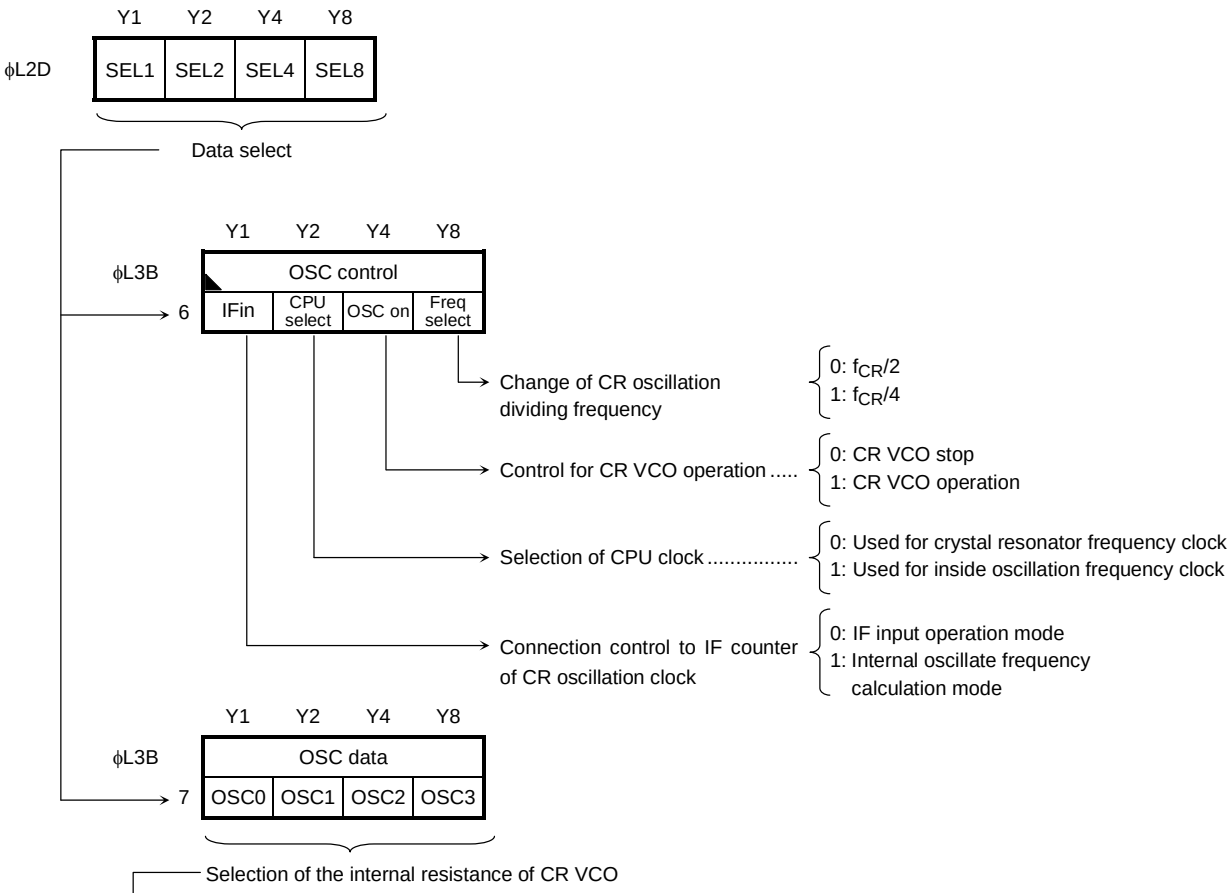
If used for the CPU clock, the frequency of the CR VCO is changed to the CPU operation clock after the CR VCO resistance is controlled and adjusted to the set-up frequency and the CR oscillation frequency is calculated using the IF counter. Moreover, the frequency changes with the change in power supply voltage from −15% to +10% of the set value, V_{DD} = 1.5 V (i.e., from V_{DD} = 1.1 V to V_{DD} = 1.8 V). If a setting frequency with an accuracy greater than this range is required, be sure always to adjust the CR VCO frequency using the IF counter. The frequency setting range of CR VCO can be freely set up in the range 0.8 to 1.2 MHz.

The resistance of the CR VCO, which has a standard value of 36 kΩ (1 MHz), can be programmed to 16 levels, from 20 kΩ to 50 kΩ (in 2 kΩ steps) and the value set using the data of 3 bits of OSC0-OSC3. The Freq Select bit sets the division value of the CR oscillation frequency. The frequency is fCR/2 if this bit is set to "0", and fCR/4 if the bit is set to "1". When the frequency is set to f_{CR} = 1 MHz, the instruction executing time is compared with the 40 μs for when the crystal oscillator clock is used. The instruction execution time is accelerated to 3/500 kHz = 6 μs for 1/2 division mode, and to 3/250 kHz = 12 μs for 1/4 division mode. Although the processing speed of the CPU is accelerated, other timing functions (such as that for the Timer, etc.) operate on the crystal oscillation frequency.

The Ifin bit is a control bit for changing the CR oscillation frequency clock to the IF counter. If "0" is set, the IF counter starts calculating the IF (etc.); if "1" is set, the CR VCO frequency can be selected as the clock input of the IF counter. To calculate the CR VCO frequency, it is necessary to set the Prescaler IN bit to "1". (→ Refer to IF counter item.)

Moreover, the CR oscillation frequency clock can be output from the MUTE terminal, and used for external IC clocks and monitoring of the CR oscillation clock monitor. If the Test port 1 (ϕL1F) is set to "5H", the CR VCO clock outputs from MUTE terminal.

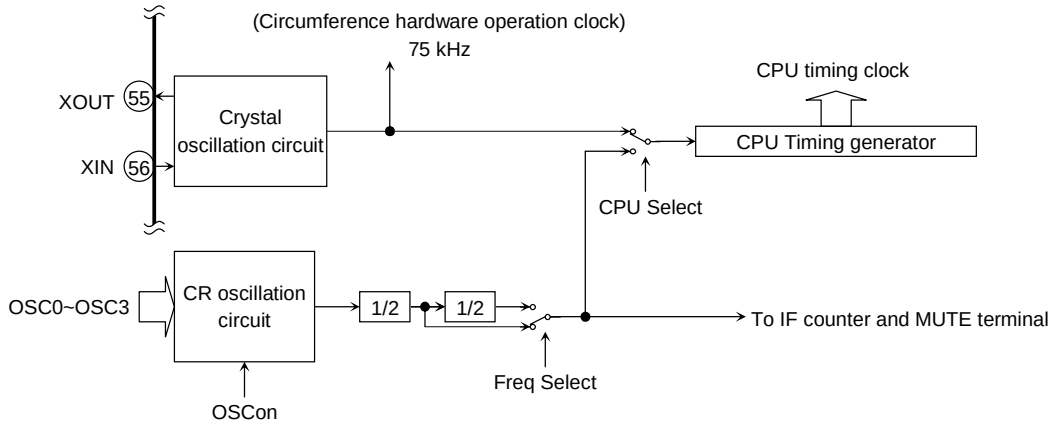
The setup and control of the frequency of the CR VCO is set using an OUT3 instruction for which [CN = 6~7H] has been specified in the operand



OSC0	OSC1	OSC2	OSC3	Resistance (Typ.)	Oscillation Frequency (Typ.)
0	0	0	0	20 kΩ	f_{CR} = 1.8 MHz
↓	↓	↓	↓	(2 kΩ interval)	↓
1	0	0	0	36 kΩ	f_{CR} = 1.0 MHz
↓	↓	↓	↓	(2 kΩ interval)	↓
1	1	1	1	50 kΩ	f_{CR} = 0.64 MHz

Note: The oscillation frequency is the frequency of a standard product and this frequency varies with the power supply voltage and the product. The frequency range in which settings be made is from 0.8~ 1.2 MHz.

3. Composition of a Clock Generator



○ System Reset

The device's system will be reset when the $\overline{\text{RESET}}$ terminal is subject to the "L" level. The program will start from 0 address after about 100 ms of stand-by time have elapsed following system reset.

Note: The LCD common output and the segment output will be fixed at their "L" level during system reset and during the subsequent stand-by period.

Note: It is necessary to initialize through the program any of the internal ports shown in the above-mentioned I/O map that were not initialized after system reset. The ◤ mark on the I/O map after system reset indicates a port or bit set to "0" after system reset, while the ◣ mark indicates a port or bit set to "1". A port or bit with no mark is unfixed..

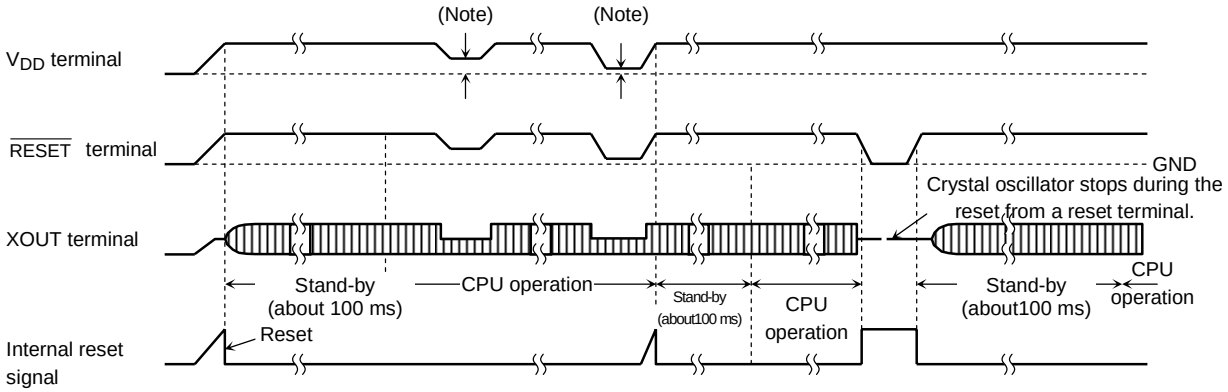
I/O \ ϕL2D	ϕL2F			
	OUT2			
	Y1	Y2	Y4	Y8
8	I/O control 1			
	-0	-1	-2	-3

After system reset, this port is set to "0".

I/O \ Code	ϕL1			
	OUT1			
	Y1	Y2	Y4	Y8
5	Reference select			Programmable counter
	R0	R1	R2	P16

After system reset, this port is set to "1".

After system reset, this bit is unfixed.



<Timing of operation >

Note: If there is a possibility that the power supply voltage will drop to 0.9 V or less, set to clock stop mode or activate the reset operation.

○ Back-up Mode

By executing the CKSTP instruction or WAIT instruction, three kinds of back-up mode can be activated.

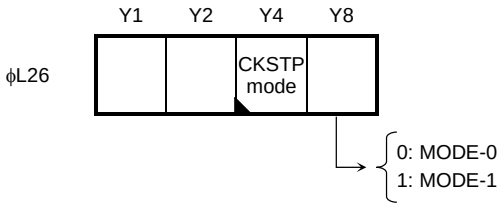
1. Clock Stop Mode

Clock stop mode is a function that suspends system operations and maintains the internal status immediately prior to suspension at a low level of current consumption (under 1 μA). Crystal oscillations suspended simultaneously and CMOS output ports and output terminals for LCD display purposes are automatically set at "L" level, and N-channel open-drain terminals are set to off status (high impedances) automatically. The supply voltage can be reduced to 0.75 V with clock stop mode.

Suspension is activated at the CKSTP instruction execution address when the CKSTP instruction is executed. The next address is executed after approximately 100 ms of stand-by time when clock stop mode is cancelled.

(1) Clock stop mode setting

There are two types of mode setting for clock stop mode. The required setting is selected with the CKSTP MODE bit. This bit is accessed with the OUT2 instruction for which [CN = 6H] has been specified in the operand.



① MODE-0

Wtih this mode set, the clock stop mode is assumed if the CKSTP instruction is executed when the $\overline{\text{HOLD}}$ terminal is at "L" level. The same operations as the NOOP instruction will be assumed if the CKSTP instruction is executed when the $\overline{\text{HOLD}}$ terminal is at "H" level.

② MODE-1

With this mode set, the clock stop mode is assumed when the CKSTP instruction is executed regardless of the $\overline{\text{HOLD}}$ terminal level.

Note: The PLL will assume off status during execution of the CKSTPinstruction.

Note: Before the execution of the clock stop instruction, be sure to access the $\overline{\text{HOLD}}$ input terminal and I/O port 1 input port and rest the 2 HzF/F. Without execution of this instruction, it may not be possible to enter clock mode even if clock mode is executed.

(2) Canceling clock stop mode

① MODE-0

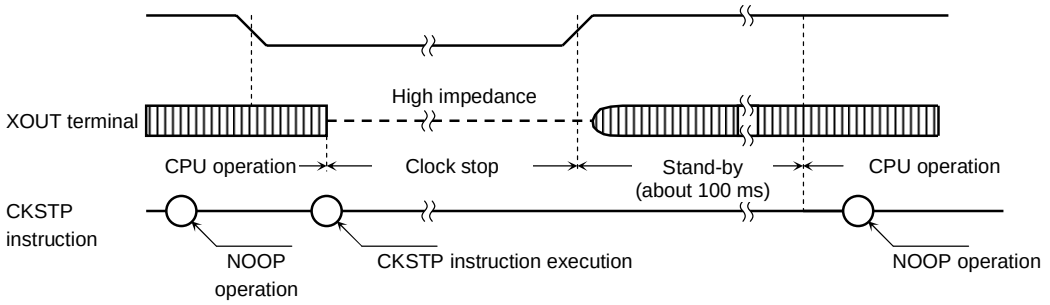
Clock stop mode is cancelled when specified in this mode by changing the "H" level of the $\overline{\text{HOLD}}$ terminal or the input status of the I/O port (P1-0~3) specified in the input port.

② MODE-1

Clock stop mode is cancelled when specified in this mode by changing the $\overline{\text{HOLD}}$ terminal or the input status of the I/O port (P1-0~3) specified in the input port.

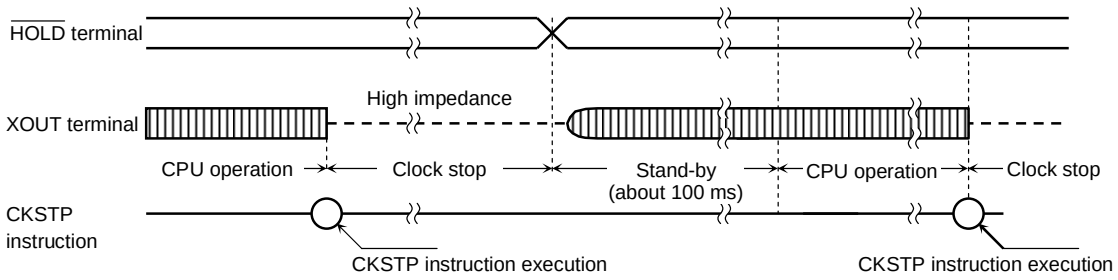
(3) Clock stop mode timing

① MODE-0



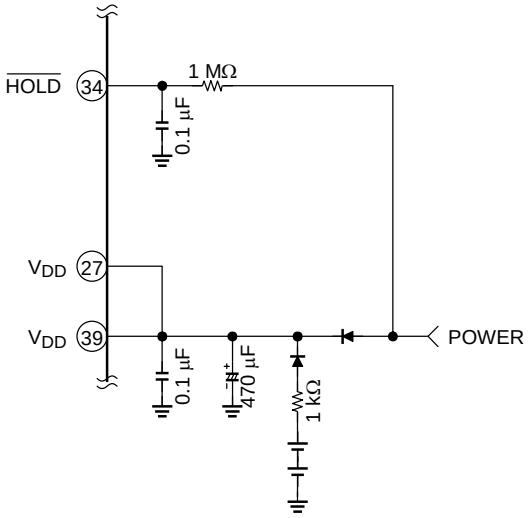
(The clock stop mode is assumed if the CKSTP instruction is executed when the $\overline{\text{HOLD}}$ input is at "L" level.)

② MODE-1

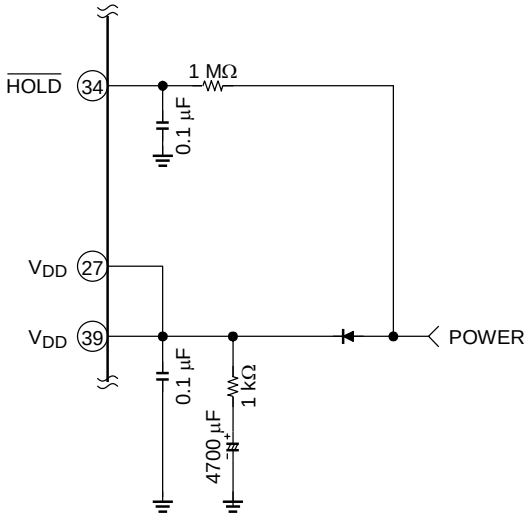


(The clock stop mode is assumed whenever the CKSTP instruction is executed.)

(4) Example of a circuit (example of a MODE-0 circuit)



Example of battery back-up circuit



Example of a condenser back-up circuit

2. Wait Mode

Wait mode suspends system operations, maintains the internal status immediately prior to suspension and reduces current consumption. There are two types of wait mode: SOFT WAIT mode and HARD WAIT mode. Operations are suspended at the address where the WAIT instruction was executed when the wait mode is activated. The next address is executed immediately after the wait mode is cancelled without entry to stand-by status.

(1) SOFT WAIT mode

Only the CPU operations within the device are suspended on execution of a WAIT instruction in which [P = 0H] has been specified in the operand. The crystal resonator and other elements will continue to operate normally at this time. The SOFT WAIT mode is efficient in reducing current consumption during clock operations when used in programs that include clock functions.

Note: Current consumption will differ in accordance with execution time of CPU operation.

(2) HARD WAIT mode

The operations of all elements, with the exception of the crystal resonator, can be suspended by the execution of a WAIT instruction in which [P = 1H] has been specified in the operand. This enables even greater levels of current consumption reduction than the SOFT WAIT mode. It suspends the CPU operation.

Note: The output port is maintained during HARD WAIT mode. All LCD display output terminals are fixed at "L" level and the voltage doubler circuit (V_{DB}), LCD voltage regulator ciicuit (V_{EE}) and LCD voltage doubler circuit (V_{LCD}) operate.

(3) Wait mode setting

The wait status is assumed whenever the WAIT instruction is executed.

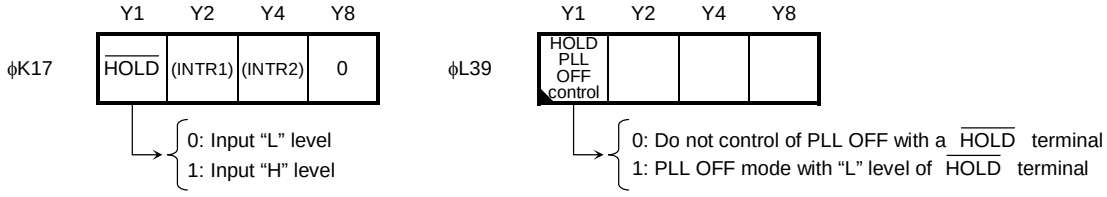
Note: The PLL OFF status will be assumed during the wait mode.

(4) Wait mode cancellation conditions

Wait mode is cancelled when the following conditions are satisfied:

① When the input status of the $\overline{\text{HOLD}}$ terminal changes.
② When the input status of the I/O port specified in the input port (P1-0~3) changes.
③ When the 2 Hz Timer F/F is set as "1" (only with the SOFT WAIT mode)

3. $\overline{\text{HOLD}}$ Input Port



The $\overline{\text{HOLD}}$ terminal can be used as an input port. This bit loads into the data memory data input using the IN1 instruction for which [CN = 7H] has been specified in the operand. It is necessary to access this port prior to the execution of the CKSTP instruction when clock stop mode or wait mode is set. Note that, without accessing this port it may not be possible to enter clock stop mode even if this instruction is executed.

While HOLD PLL off control bit is set to "1", PLL off mode result if $\overline{\text{HOLD}}$ terminal input goes to "L" level. Therefore setting to PLL off-mode can be done quickly during battery replacement.

The bit is accessed with the OUT3 instruction for which [CN = 9H] has been specified in the operand. PLL off mode becomes active even if all reference ports are "1". (→ Refer to the reference frequency divider item)

Note: The $\overline{\text{HOLD}}$ input terminal is used as an INTR2 terminal. The same as data is output at the $\overline{\text{HOLD}}$ and INTR2 input ports.

○ Interrupt Function

The peripheral hardware that can use the Interrupt function has an INTR1 terminal, INTR2 terminal, Timer counter, and Serial interface.

If this peripheral hardware fulfills the conditions, the interrupt request signal from the peripheral hardware is output, and the interrupt request is issued. On being received, each interrupt branches to a vector address determined by the interrupt factor, and the processing routine for the interrupt begins. Pretreatment and post-processing are necessary in the interrupt routine, before and after the normal Interrupt processing, to restore the same state that was in effect at the time the interrupt occurred. It is necessary to perform shunting and return of the register and indestructible data memory used by ALU to the data memory for Interrupt use.. When interrupt processing ends, the program is restored using the Return command for the Interrupt function.

The INTR1 and INTR2 terminals are serve as IFin1 and $\overline{\text{HOLD}}$ terminals.

1. Interrupt Control Circuit

The Interrupt Control Circuit consists of an interrupt permission flag, an interrupt latch, and an interrupt priority circuit block. This control performs setup and control through the OUT2/IN2 instructions.

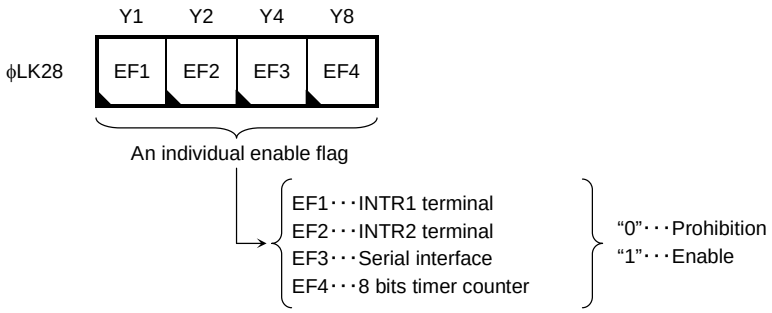
(1) Interrupt enable flag

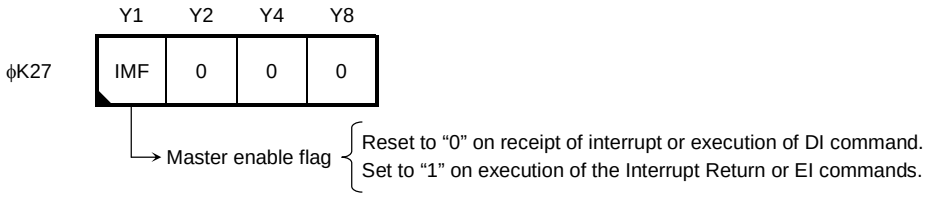
The interrupt enable flag has a master permission flag and individual permission flags corresponding to each interrupt factor. An individual enable flag sets the interrupt prohibition/permission according to the interrupt factor. A master enable flag is a flag for prohibiting or permitting all Interrupts. If these enable registers are set to "1", permission takes effect; if they are set to "0", prohibition takes effect..

An individual enable flag is accessed through the OUT2/IN2 instructions for which [CN □ 8H] has been specified in the operand. A master enable flag can perform permission/prohibition by execution of an EI/DI instruction.

Interrupt is prohibited by execution of a DI command, and enabled by execution of an EI command. At this time, interrupt is enabled during execution of the EI command and DI command in the program.

If an interrupt request is received, the master enable flag is reset to "0" and all interrupts are prohibited. On execution of the interrupt return command, the flag is set to "1". A master enable flag is read into the data memory using an IN2 command for which [CN = 7H] has been specified.



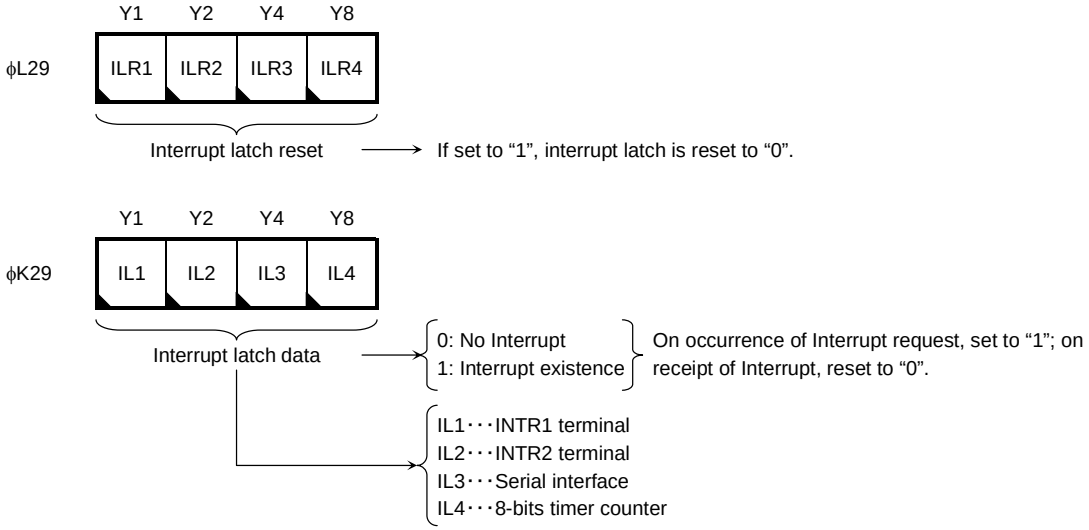


(2) Interrupt latch

If an Interrupt request generates, the interrupt latch is set to "1".

If Interrupt is enabled, the CPU will be requested to receive the Interrupt, and the process will branch to the Interrupt routine. If the Interrupt is received at this time, the Interrupt latch is reset by data "0" automatically.

Interrupt latch data can read by the program and the existence or nonexistence of an Interrupt occurrence can be determined on an individual basis. In accordance with the Interrupt request, the Interrupt latch that was set to "1" is reset to "0"; in this way, it is possible to cancel or initialize the Interrupt request.



(3) Interrupt priority circuit block

Interrupt priority circuit is a circuit that determines the order in which Interrupts are processed if Interrupts occur simultaneously or if two or more Interrupts have been permitted.. Vector addresses for the interrupt routine are also generated in this block.

Priority	Interrupt Factor	Vector Address
1	INTR1 terminal	0001H
2	INTR2 terminal	0002H
3	Serial interface	0003H
4	Timer counter	0004H

2. Interrupt Reception Processing

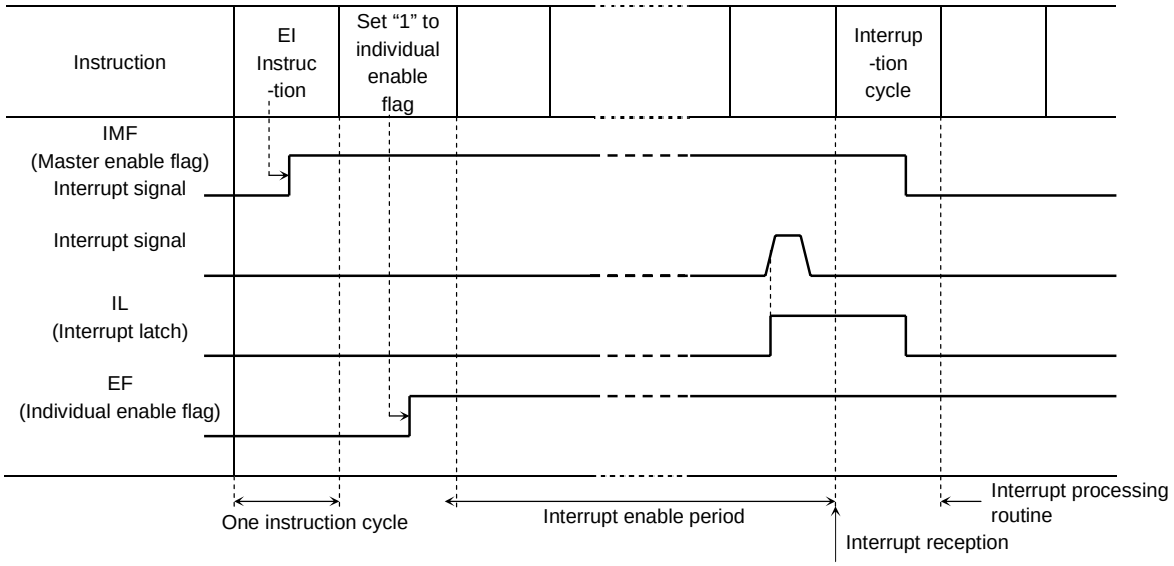
The interrupt request is retained until the interrupt is received or the interrupt latch is reset to "0" by system reset operation or by the program. The interrupt reception operation is as shown below.

① If the interrupt conditions are fulfilled, each item of peripheral hardware outputs each interrupt request signal and sets the Interrupt latch to "1".
② The Interrupt latch of the interrupt factor received resets to "0" if the interrupt enable flag corresponding to each interrupt factor and the master enable flag are set to "1".
③ The interrupt master enable flag resets to "0" and interrupt is prohibited.
④ The contents of a stack pointer are made -1.
⑤ The contents of the program counter (PC) are shunted to the stack register. In this case, the contents of the program change to the next address after the point at which the interrupt was received, or the next address after the point at which the interrupt was permitted.
⑥ The contents of the vector address corresponding to the received interrupt are transferred to the program counter.
⑦ The contents of the vector address are executed.

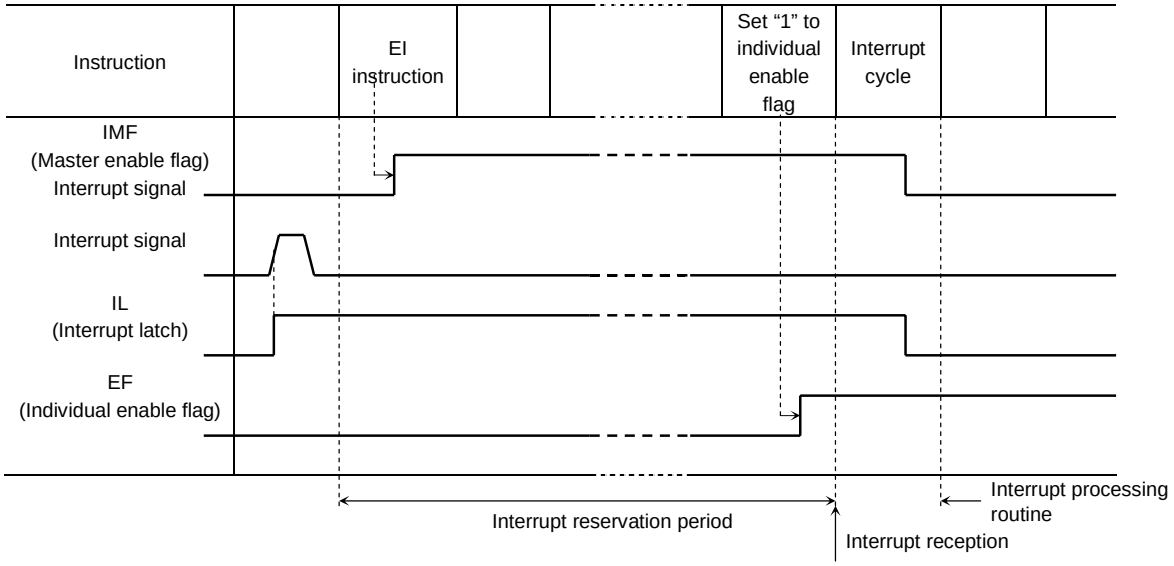
Steps ①~⑥ are executed within one instruction cycle. This instruction cycle is called the "Interrupt Cycle"

Note: The stack pointer is a pointer for which an 8-level stack register is specified.

Interrupt enable period



Interrupt holed period



3. Return Processing from Interrupt Processing Routine

A special command, the RNI instruction, is used to return to the processing state that was in effect before the interrupt was received.

With execution of the RNI instruction, the following processing is executed step-by-step automatically.

① The contents of the address stack, specified by the stack pointer, are returned to the program counter.
② Set the Interrupt Master Enable Flag to "1" to activate the enable state.
③ +1 is applied to the contents to the stack pointer.

The above-mentioned RNI instruction processing is performed in one instruction cycle.

4. Interrupt Processing Routine

The interruption is received regardless of the program being run when the interrupt request is issued if this is the program area where the interrupt is enabled. Therefore, to restore the base program after the interrupt processing is completed, it is necessary to return to the state in which interrupt processing was not being performed. For this reason, it is necessary to perform the shunting and return operations within the interrupt processing routine, at least for those items such as the register and data memory that can be operated within the interrupt processing routine.

(1) Shunting processing

In the execution of the shunting processing, it is essential that a carry flag be shunted. If interruption is received during the execution of arithmetic or similar operations, the contents of the carry flag (CY), etc., will change, resulting in the program making incorrect decisions. For this reason, the contents of the carry flag are shunted in the data memory once through the IN1 instruction in the data of the carry flag of the I/O map.

The contents of the data memory used by the interruption processing routine and the contents of a general register are also made to shunt if needed. Furthermore, when MVGD, MVGS or DAL instruction is used in the interrupt routine, it is necessary to shunt the contents of the G-register or the DAL address register.

(2) Return processing

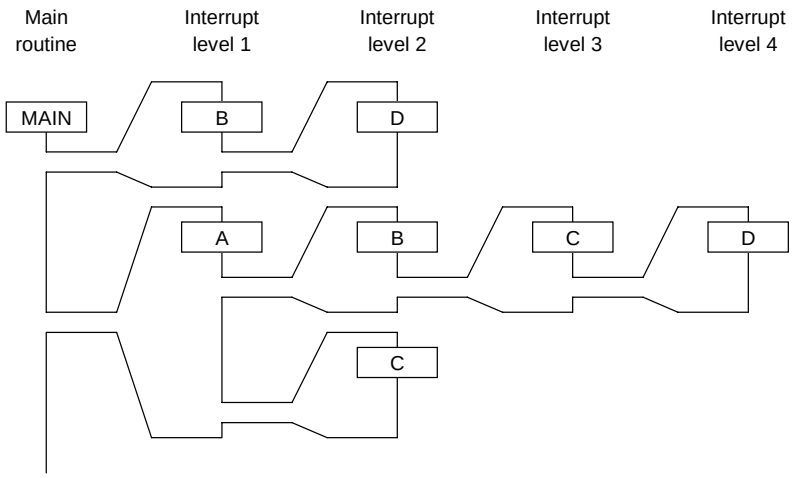
Return processing should do the opposite to the above-mentioned shunting processing.

Since, when the interrupt is received, the interrupt master enable flag is reset to "0", it follows that before receiving the interrupt, the interrupt master enable flag must have been "1".

For this reason, the RNI instruction is executed and a master enable flag is returned.

5. Multiplex Interrupt

Multiplex Interrupt is a method of processing others interrupt during interrupt processing.
As shown in the figure, the other interrupt factor C or D is processed during the interrupt processing of interrupt factors A and B. In this process, the depth of the interrupt is called the interrupt level.



The example of multiplex interrupt

Caution is required for the following points when using multiplex interrupt.

① The priority of interrupt factors
② Restriction of the address stack level used at the time of interrupt request issue
③ Shunting processing of the carry flag, the data memory, etc.

(1) Priority of interrupt factor

In this priority ranking, the processing of interrupt C must be given priority even if the interrupt processing of A or B is in progress; and the processing of D must be given priority even if the interrupt processing of C is in progress.

The necessity of determining priority in the handling of multiple interruptions can be illustrated as follows. Suppose, for example, there are the interruption factors A and B. For factor A, a request is generated about every 10 ms and the interrupt processing time is 4 ms; for factor B, a request is generated about every 2 ms and the interrupt processing time is 1 ms. If no priority were applied to A and B, then a request for interrupt A that came in during the processing of interrupt B could lead to interrupt A being processed, resulting in the processing of interrupt B being repeatedly stopped. Such a case requires a program that establishes the priority A □ B, not only prohibiting interrupt A during the processing of interrupt B but also enabling the reception of interrupt B during the processing of interrupt A.

As explained in the item on the interrupt priority circuit block, when all individual enable flags are set to "1" (enable state), the priority of the hardware can be changed by manipulating the individual enable flags in the program.

As a rule, received interrupts and low-priority interrupts are prohibited, and high-priority interrupts are enabled in the interrupt processing routine.

(2) Restriction of address stack level

As explained in the item on interrupt reception processing, when an interrupt request is issued, the return address is shunted automatically to the address stack. As explained in the item on registers, an address stack is also used for execution of sub-routine call instructions on eight levels. For this reason, if the interrupt level and sub routine call level exceed eight levels, the contents of the return address recorded from the first address stack are destroyed. Therefore restriction is necessary.

(3) Shunting processing

When using the Multiplex Interrupt function, it is necessary to secure a shunting area for shunting processing separately for each interrupt factor.

○ External Interrupt and Timer Counter Function

There are two types of external interrupt: that using the INTR1 terminal and that using the INTR2 terminal. Interrupt requests are issued by the rising or falling edge of a signal applied to these terminals.

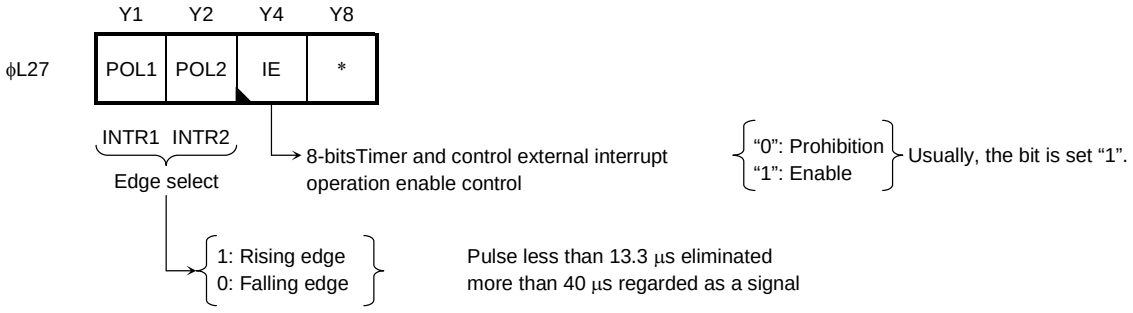
The timer counter is an 8-bit binary counter and has the function of timer and external clock timer. The input of the external clock timer function is used as an external interrupt terminal (INTR1, INTR2).

1. External Interrupt Function

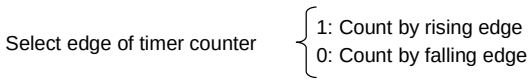
There are two input terminals for external interrupt, INTR1 and INTR2; and an interrupt request is issued on detection of the edge of these inputs. There is a noise canceller for the input: a noise removal clock uses a frequency of 75 kHz, and any pulse under this frequency is removed as noise. The IE bit is an enable bit which permits 8-bit timer counter operation, and interrupt and external interrupt requests. It is possible to select either the rising or falling edge as the input edge for each terminal. Usually, this bit is set to "1".

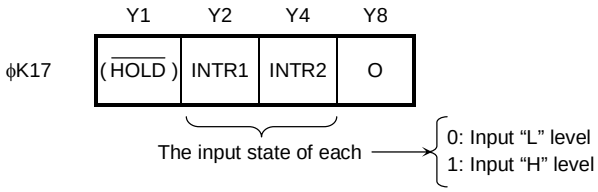
These controls are accessed using an OUT2 instruction for which [CN □ 7H] has been specified in the operand. The program will branch to address 0001H on receipt of an INTR1 interrupt, and to address 0002H on receipt of an INTR2 interrupt.

These terminals are used as input ports and the input status can be read into the data memory by execution of an IN2 instruction for which [CN □ 7H] has been specified in the operand.



Note: The edge of the external clock of the timer counter is also controlled. No noise cancel function is used for the input to the timer counter. Therefore, even if no interrupt occurs, caution is necessary regarding the input of a clock pulse of less than 40 s into the clock pulse counter.





Note: An interrupt request may be issued if an edge is changed using POL bits. For this reason, when changing an edge, be sure to prohibit interruption beforehand. After making the change, reset the interrupt latch and return to normal operation.

Note: The INTR1 terminal and INTR2 terminal are used as IFin1 terminal and $\overline{\text{HOLD}}$ terminal respectively. If using only the INTR1 terminal be sure to set IF1/$\overline{\text{INTR}}$ bits (φL16) to "0". Also, the same data is output at the $\overline{\text{HOLD}}$ input and INTR2 input port.

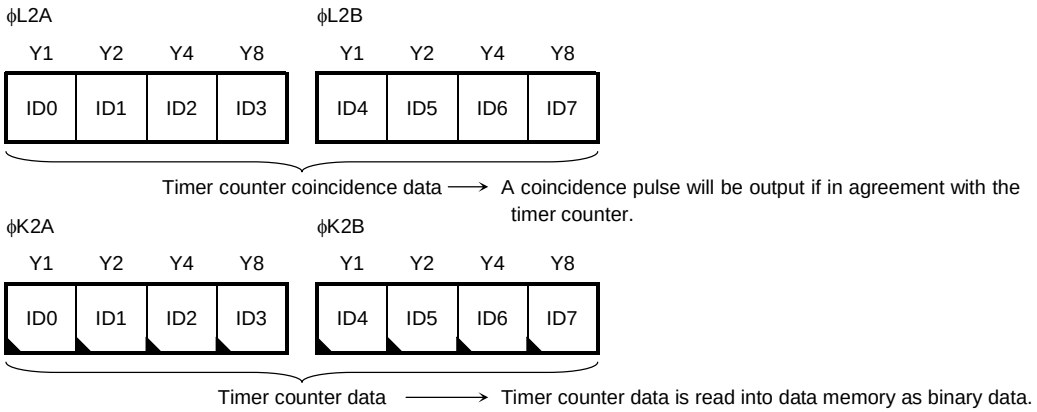
2. Timer Counter Function

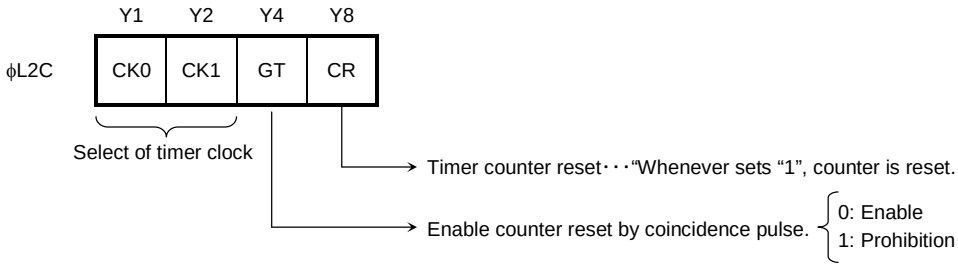
Timer counter are consists of 8-bit binary counter, counter coincidence register, digital comparator and controlled the control circuit.

If timer counter is coincided with the contents of counter coincidence register, timer counter is outputted a coincidence signal pulse and interrupt request is done by inputting timer clock to 8-bit binary counter timer clock. Reset of Timer counter is possible with a coincidence pulse and a program, and it can perform enable and prohibition of reset by the coincidence pulse. As a clock of timer, it can be selected INTR1/2 input and an instruction cycle and 1 kHz.

(1) Timer counter register configuration

The timer counter register consists of a counter data, coincidence register and a control register.





CK1	CK0	Timer clock
0	0	INTR1 terminal input
0	1	INTR2 terminal input
1	0	Instruction cycle clock (40 μs)
1	1	1 kHz

Select clock edge by POL bit
0: Count by raising edge
1: Count by falling edge

Note: To use the timer counter, it is necessary to set the IE bit to "1".

Note: Set the IF1/$\overline{\text{INTR}}$ bits (ϕL16) to "0" when the INTR1 terminal is used as a timer clock.

(2) Timer mode

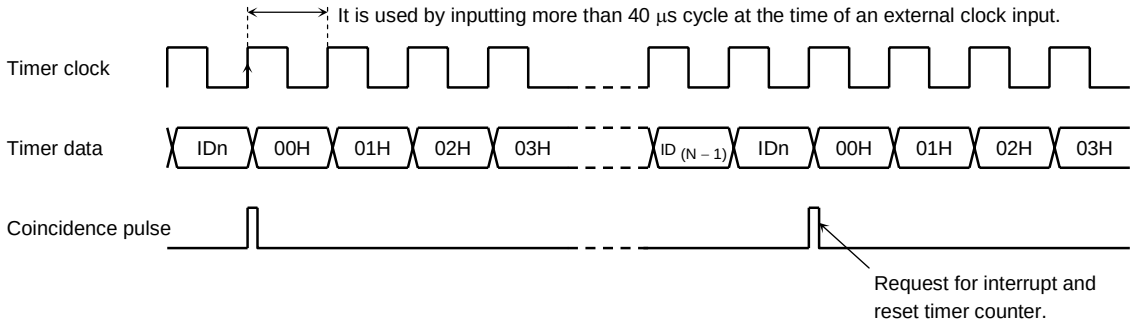
Timer mode is detected fixed time. Interrupt request is done and reset to counter whenever it detects fixed time. At this time, control bit is set to 1 kHz or an instruction as timer clock, "0" to GT bit and "0" (it does not reset) to CR bit.

Timer coincidence data is

Timer time = IDn (coincidence data) × Timer clock cycle

It sets up the data which corresponding to time.

In addition, although an external terminal can be used for Timer clock, a clock frequency should use the frequency below 25 kHz. If GT bit is setup "1", it can be also be integrated of an external clock.



○ Internal Interrupt and Interrupt Function

Interrupt has two types of timer counter and serial interface.

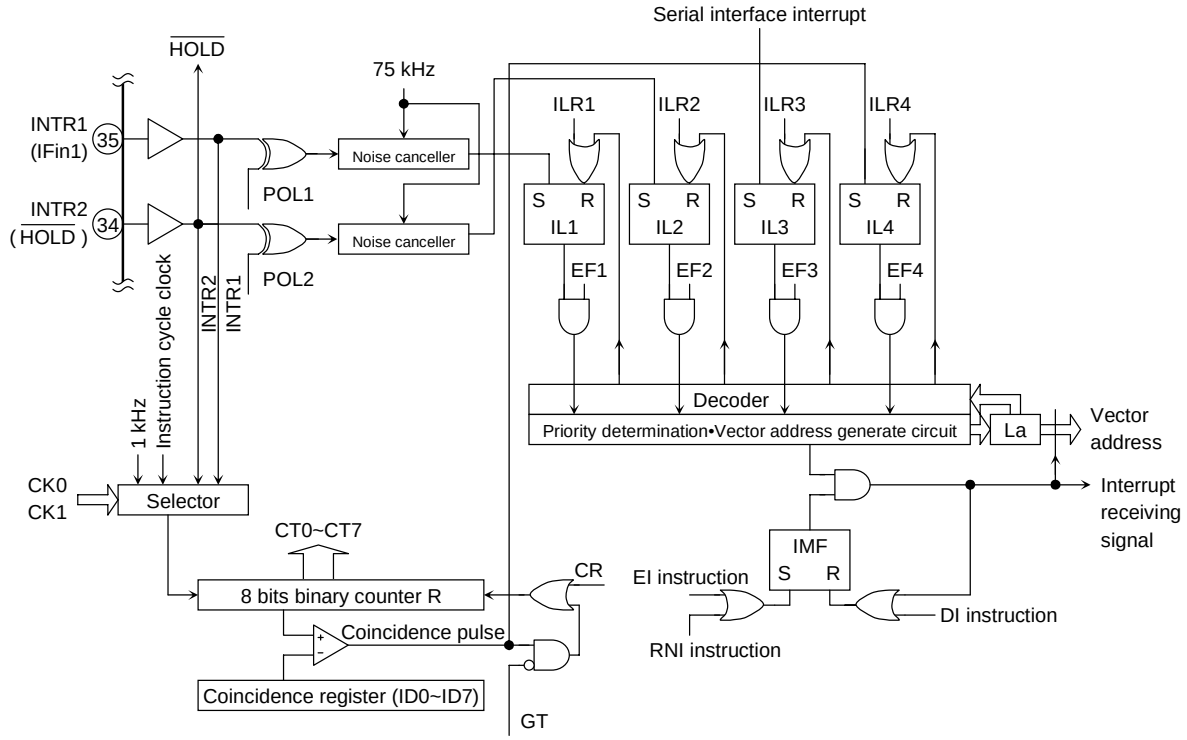
1. Interrupt of Timer Counter

If timer counter value is same as coincidence register value, interrupt of timer counter is occurred interruption. Refer to the item of timer counter function in detail.

2. Interrupt of Serial Interface

Interrupt of serial interface is occurred interruption at the time of finishing operation of serial interface. Refer to the item of serial interface function in detail.

3. Interruption Block Configuration



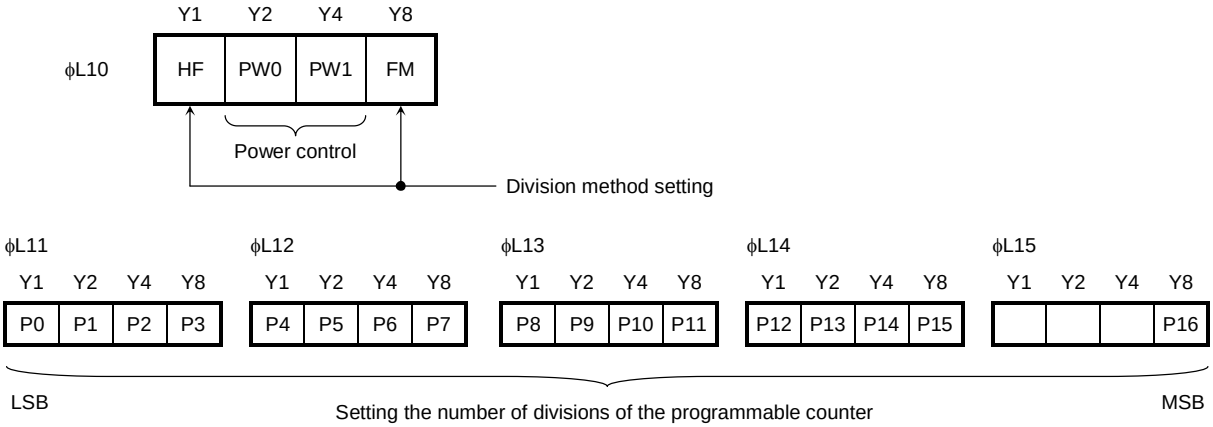
○ Programmable Counter

The programmable counter consists of two modulus prescalers, a 4-bit + 13 bit programmable counter and a port to control these elements.

The programmable counter controls the ON/OFF functions for the contents of the reference port and $\overline{\text{HOLD}}$ input status. By using external prescaler (TD6134AF/TD7101/04F) or 1 chip tuner IC that is built-in for 1/16 prescaler (TA2142FN), it's possible to reduce the emission from the tuner portion and consumption current.

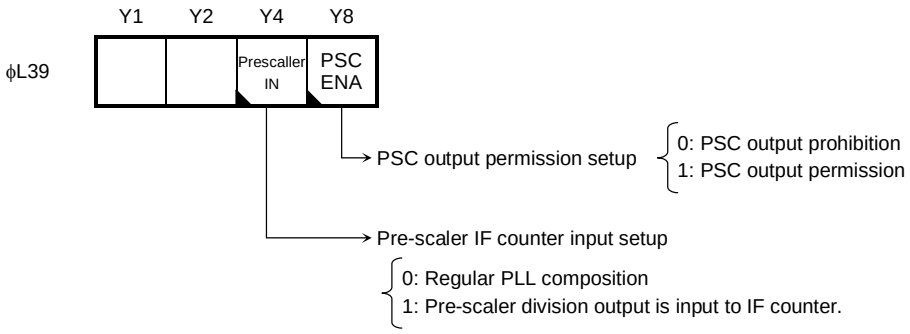
1. Programmable Counter Control Port

This port is controlling for division frequency, division method and operating current and gain of prescaler.



The division method and power control of the prescaler are accessed using an OUT1 instruction for which [CN = 0H] has been specified in the operand.

The division frequency setting is accessed using an OUT1 instruction for which [CN = 1~5H] has been specified and the setting is made by writing in the P16 bits (ϕL15). All data between P0 to P16 are updated when P16 is set. It is therefore necessary to access P16 without fail even when updating only certain items of data and to perform setting as the final process.



PSC output permission setup is used at the time of connection of external prescaler.

In the setup to prescaler IF input, if the bit is set to "1", a programmable counter stops and prescaler 1/15 and 16 are fixed to 16 division. Usually, consisting of PLL, the bit is set to "0".

(→ Refer to the IF counter item)

2. Division Method Setting

The pulse swallow method or direct method are selected using the HF and FM bit.

The power control bits (PW0/1) control the gain of the amplifier and prescaler (1/2, 1/15・16). Although the power bit in each mode has five methods, set it up as shown in a table.

By using the single-chip tuner IC that is built-in for the 1/16 prescaler (TA2142FN), set the LF mode and set the division value after the 1/16 division frequency.

Mode	HF	PW0	PW1	FM	Division Method	Example of Receiving Band	Operation Frequency Range	Division Number (Note)
LF	0	1	0	0	Direct division method	MW/LW	0.5~8 MHz	n
HF1	1	1	0	0	Pulse swallow method (1/15•16)	SW	3~30 MHz	
HF2	1	0	1	0			1~10 MHz	
FM	1	1	0	1	Pulse swallow method (1/2 + 1/15•16)	FM	60~130 MHz	2•n
VHF	1	0	1	1		TV (1 ch~12 ch)	80~230 MHz	

Note: "n" represents the number of divisions programmed.

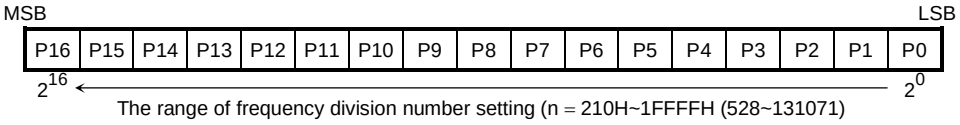
Note: Do not perform a setup except for the above-mentioned power control setup.
There are not normal operation such as flowing over-current or unlocked PLL etc..

Note: A local oscillation input is common to each mode, and is altogether input into OSCin terminal.

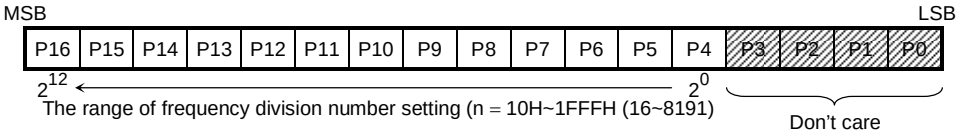
3. Frequency Division Number Setting

The frequency division number for the programmable counter is set in bits P0 to P16 in binary.

- Pulse swallow method (17 bit)

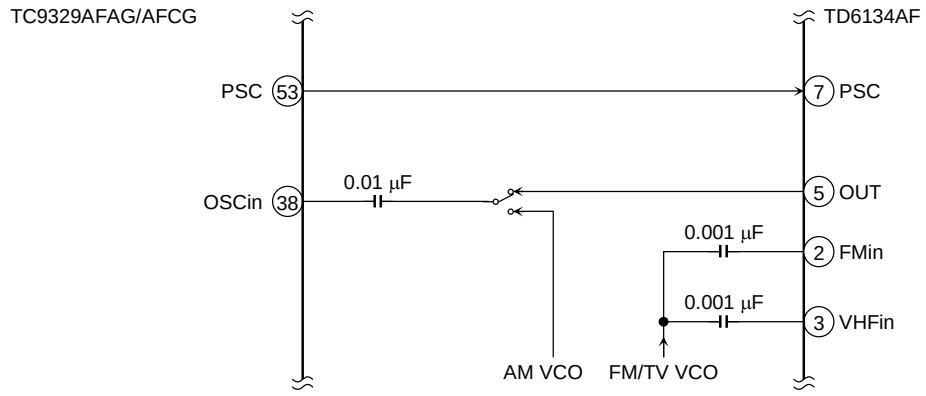


- Direct division method (13 bit)



4. PSC Output Permission Setting

In case of using the external pre-sccaler (TD6134AF/TD7101/04F), PSC output permission bit is setup to "1". At this time, a swallow counter will be operating and prescaler will be in a stop state, and PSC output is outpu P2-3 terminal. A division method is set as LF mode, and AM VCO input and an external prescaler output are changed and input into AMin input terminal. P3 terminal is used by setting it as an output port.

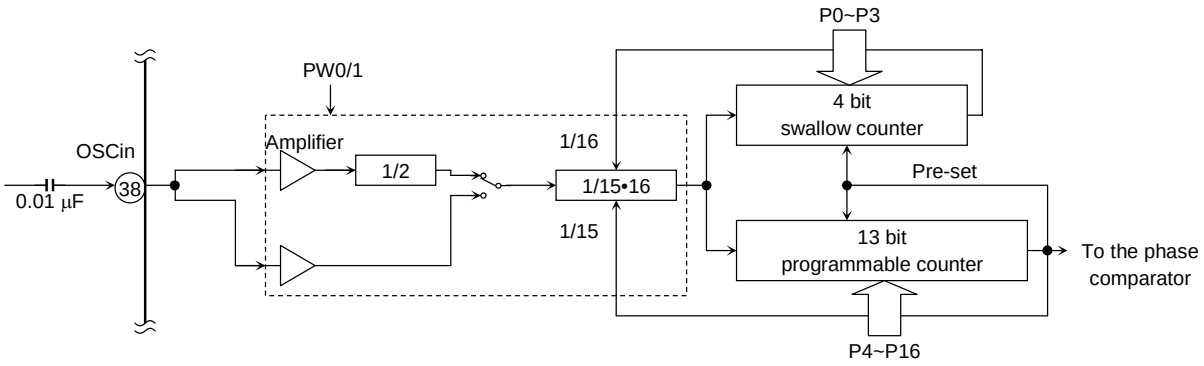


The example of an external pre-scaler connection circuit

5. Programmable Counter Circuit Configuration

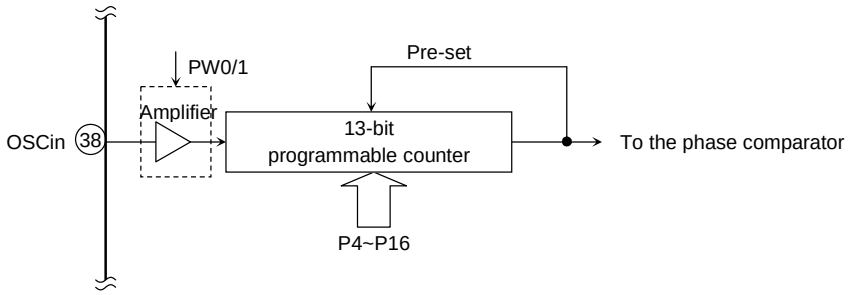
- Pulse swallow method circuit configuration

This circuit consists of amplifier, two 1/15・16 modulus prescalers, the 4-bit swallow counter and a 13-bit binary programmable counter. A 1/2 frequency divider is added to the front stage of the prescaler when in the VHF/FM mode.



- Direct division method circuit configuration

  The prescaler is not required if this is selected; instead, the13-bit programmable counter is used.



Note: OSCin terminal has been fitted into the amplifier, and small amplitue possible by linking them to a condenser. The input is high impedance when PLL is in the off mode. VCO input serves as each of operation mode common terminal.

Note: If it becomes PLL off-mode, all programmable counter parts will be stopped. The contents of each control port are held at this time.

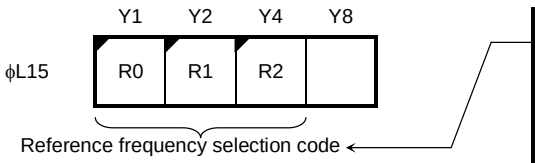
○ Reference Frequency Divider

The reference frequency divider divides the oscillation frequency of the external 75 kHz crystal and generates the following seven types of PLL reference frequency signals; 1 kHz, 3 kHz, 3.125 kHz, 5 kHz, 6.25 kHz, 12.5 kHz and 25 kHz. These signals are selected with reference port data.

The selected signal is supplied as a reference frequency for the phase comparator as described below. Also, the PLL is switched on and off with the contents of the reference port.

1. Reference Port

The reference port is an internal port for selecting the seven reference frequency signals. This port is accessed using an OUT1 instruction for which [CN □ 5H] has been specified in the operand (□L15). Operations for the programmable counter, the IF counter and reference counter are suspended; and the PLL assumes the off mode when the contents of the reference port are all "1". As the frequency division setting data for the programmable counter is updated when the reference port is set, it is necessary to set the frequency division number of the programmable counter prior to setting the reference port.



R2	R1	R0		Reference Frequency
0	0	0	0	1 kHz
0	0	1	1	3 kHz
0	1	0	2	3.125 kHz
0	1	1	3	5 kHz
1	0	0	4	6.25 kHz
1	0	1	5	12.5 kHz
1	1	0	6	25 kHz
1	1	1	7	PLL off mode

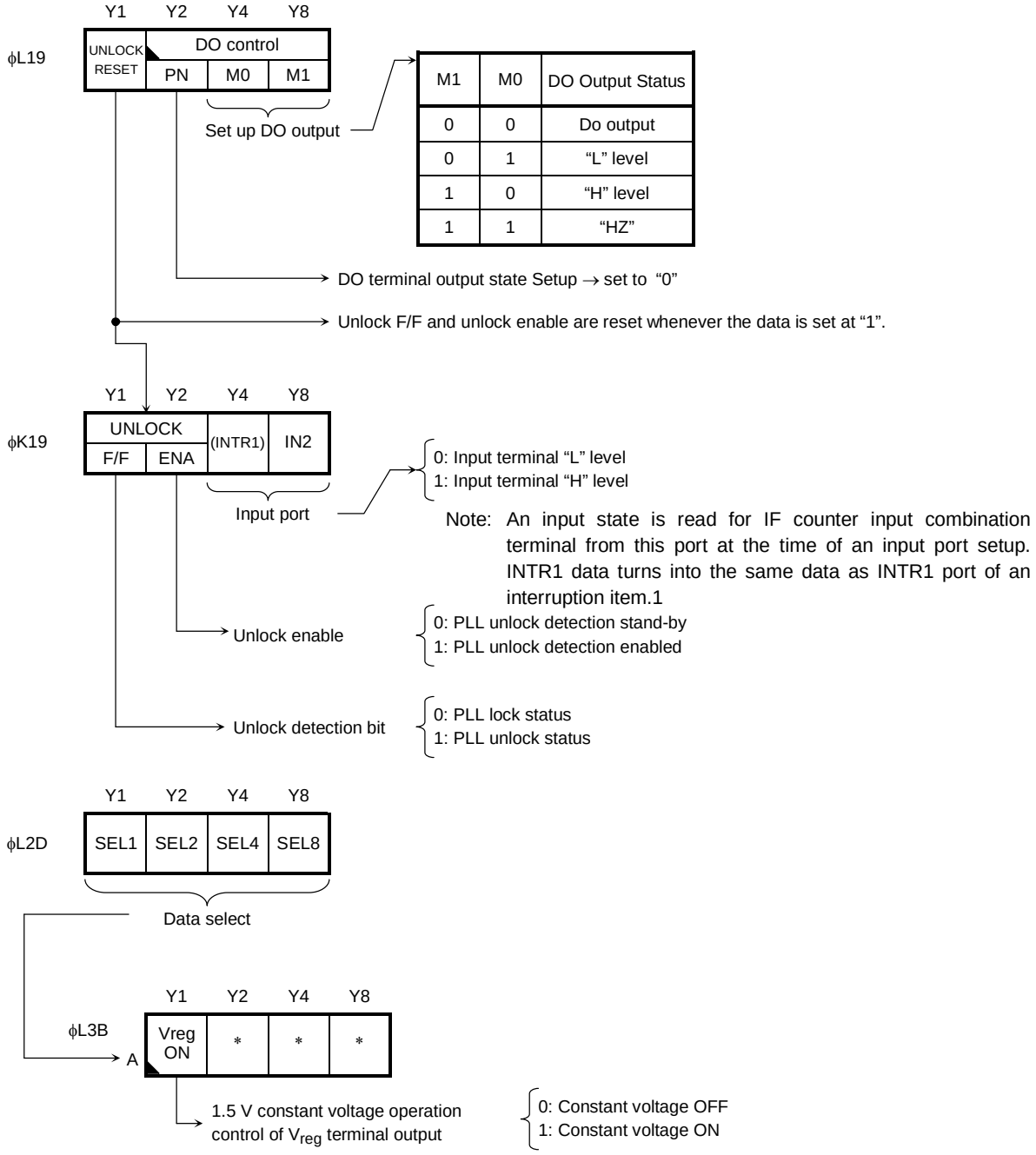
○ Phase Comparator and Lock Detection Port

The phase comparator compares the difference in phasing between the reference frequency signal supplied from the reference frequency divider and frequency division output of the programmable counter and outputs the result. It then controls the VCO (voltage control oscillator) via a low pass filter in order to ensure that the two frequency signals and the phase difference match.

In order to use a phase comparator and a charge pump output are constant voltage Vreg potential (1.5 V), it is possible to stabilized phase comparison even if VDD potential was set to 0.9 V.

The DO terminal can also be used as a general-purpose output with the Do control port.

1. Do control Port and the Unlock Detection Port



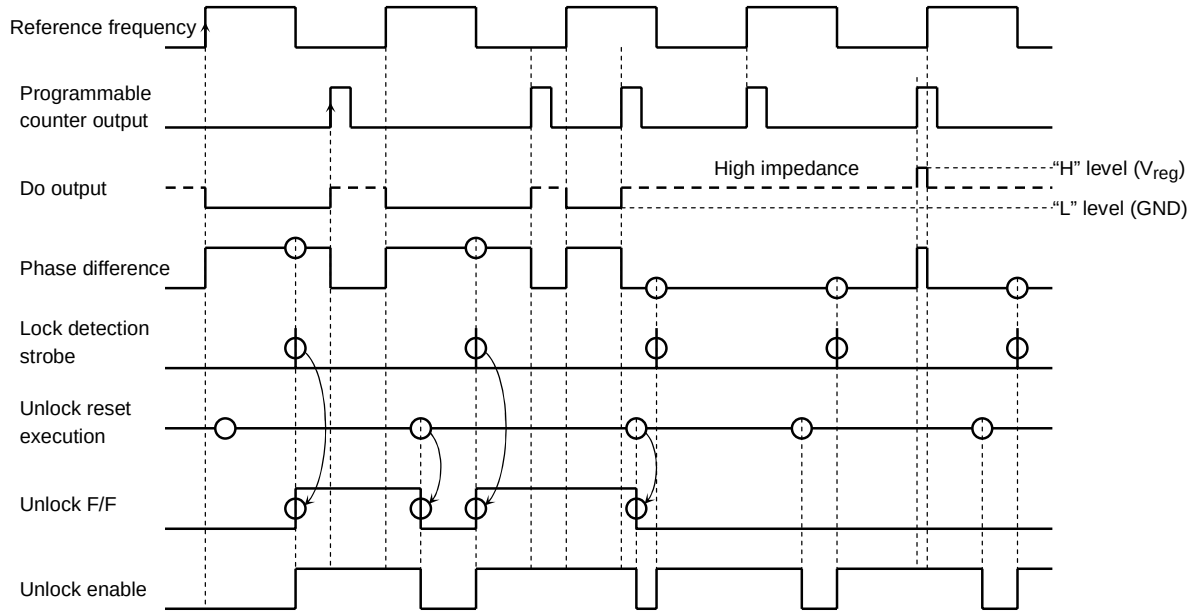
M0 and M1 bit of DO control ports are perform a general-purpose output port setup of DO output, and a setup of high impedance.

The power supply of a phase comparison and a charge pump output circuit is using V_{reg} terminal. The V_{reg} terminal is output constant voltage of 1.5 V and "H" level of charge pump output is output V_{reg} terminal. For a reason, phase comparison operation power supply voltage was stabilized by 0.9 V is possible. The operation control of V_{reg} Constant voltage is controlled by V_{reg} ON bit (ϕL3BA), if the bit is set "0", the V_{reg} terminal potential is output V_{DD} level and set "1", it becomes 1.5 V Constant voltage potential For this reason, it is set "1" at the time of PLL on mode and set "0" at the time of PLL off-mode. Unlock F/F detects the phase difference of a programmable counter division output and reference frequency to the timing from which about 180 degrees of phases shifted. When a phase does not suit at this time (that is unlock status), unlock F/F is set. The unlock F/F status is reset whenever the UNLOCK RESET bit is set as "1".

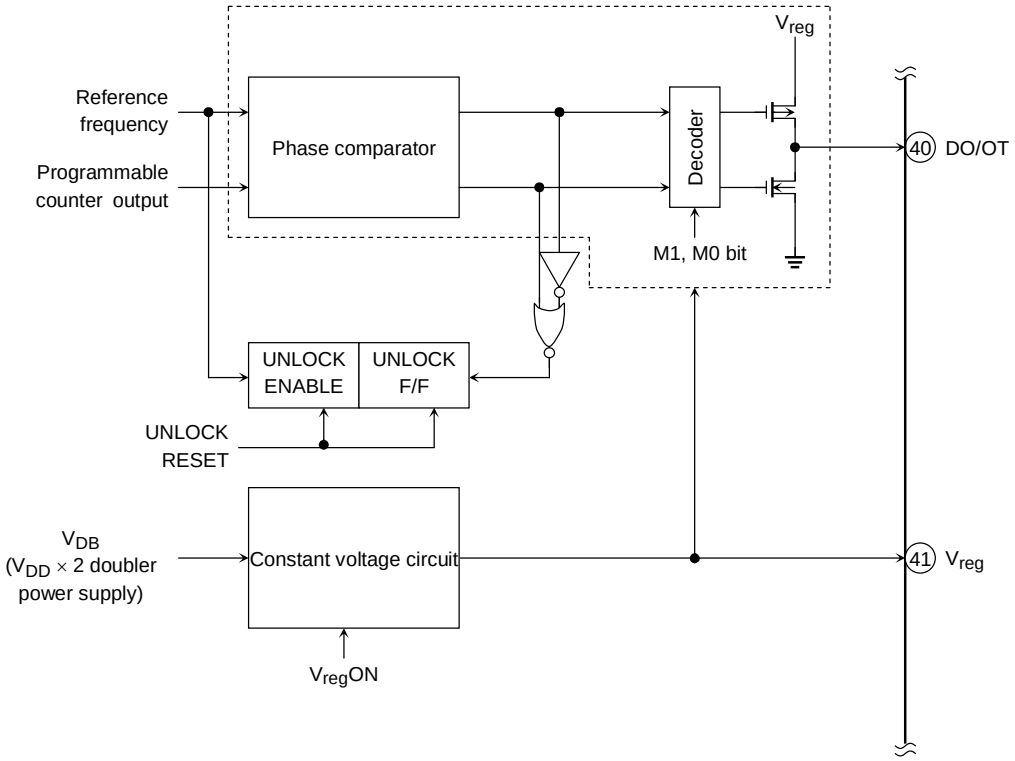
It is necessary to access to UNLOCK F/F after establishing more time than is required for the reference frequency cycle after the unlock F/F has been reset in order to detect the phase difference with the reference frequency cycle. It is for this purpose that the enable bit has been made available, but the unlock F/F must not be accessed until after it has been confirmed that the unlock enable has been set at "1".

Note: When PLL off mode is set during the DO output setup, the output of this terminal becomes as high impedance. In DO terminal, when PLL off-mode or the clock stop mode is set up at the time of a general-purpose output port setup, this output state is held.

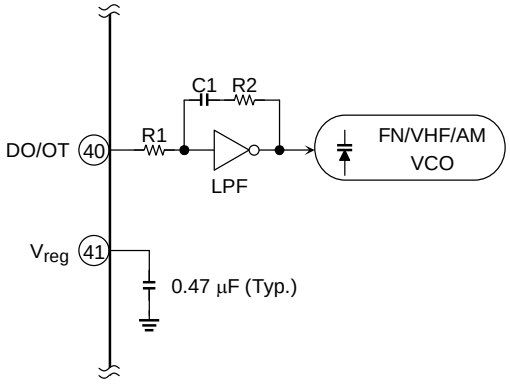
2. Phase Comparator and Unlock Port timing



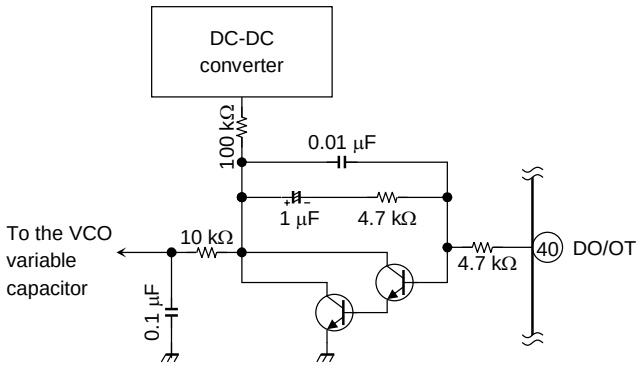
3. Phase Comparator and the Unlock Port Circuit Configuration



Note: At the time of PLL on mode, V_{reg}ON bit is setup “1” and PLL off mode, set up “0”.



Example of low pass filter circuit (for reference)



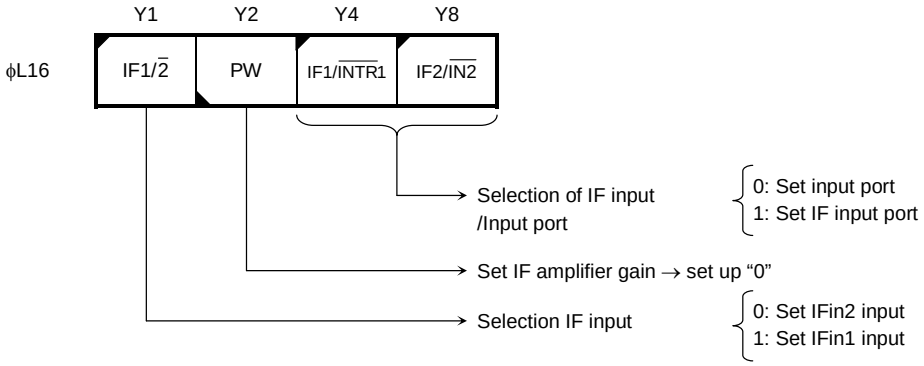
Example of an active low pass filter circuit (for reference)

Note: The filter circuits illustrated in the above diagrams are for reference purposes only. Be sure to design the actual circuits taking into account the band configuration of the system and required characteristics.

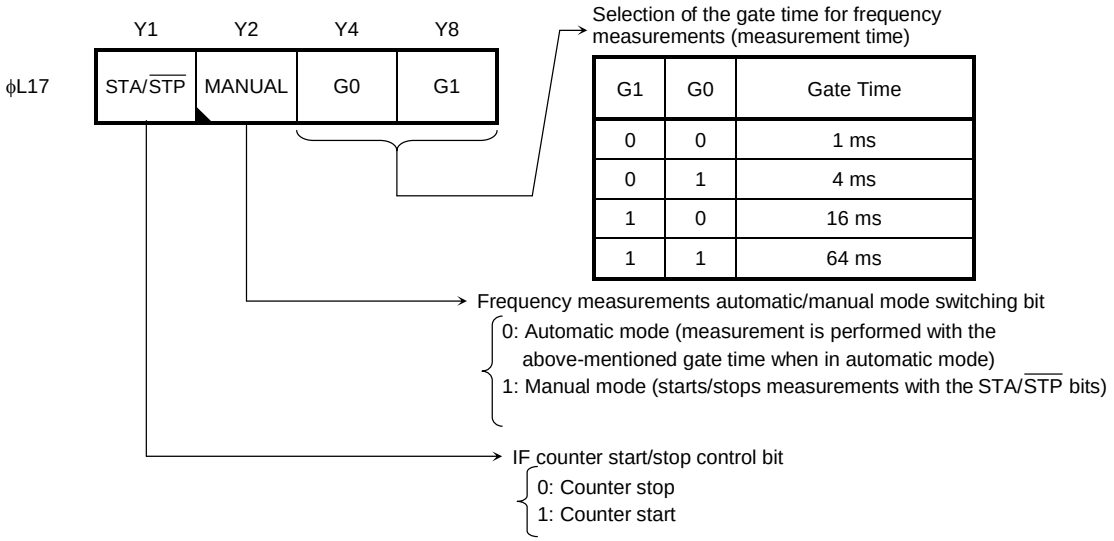
○ IF Counter

The IF counter is a 20-bit general-purpose IF counter that calculates Fm and AM intermediate frequencies (IF) during auto-tuning and can be used for detecting auto-stop signals, etc. The VCO of an analog tuner is measured, and detection of the received frequency and detection of the CR oscillation frequency can be performed.

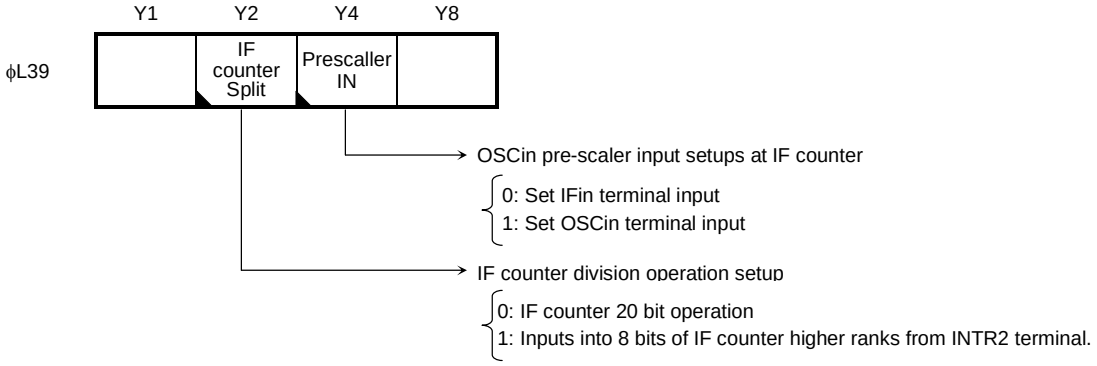
1. IF Counter Control Port and Data Port



Note: At the time of an input port setup, the terminal becomes CMOS input type and be able to detect frequency by IF counter.

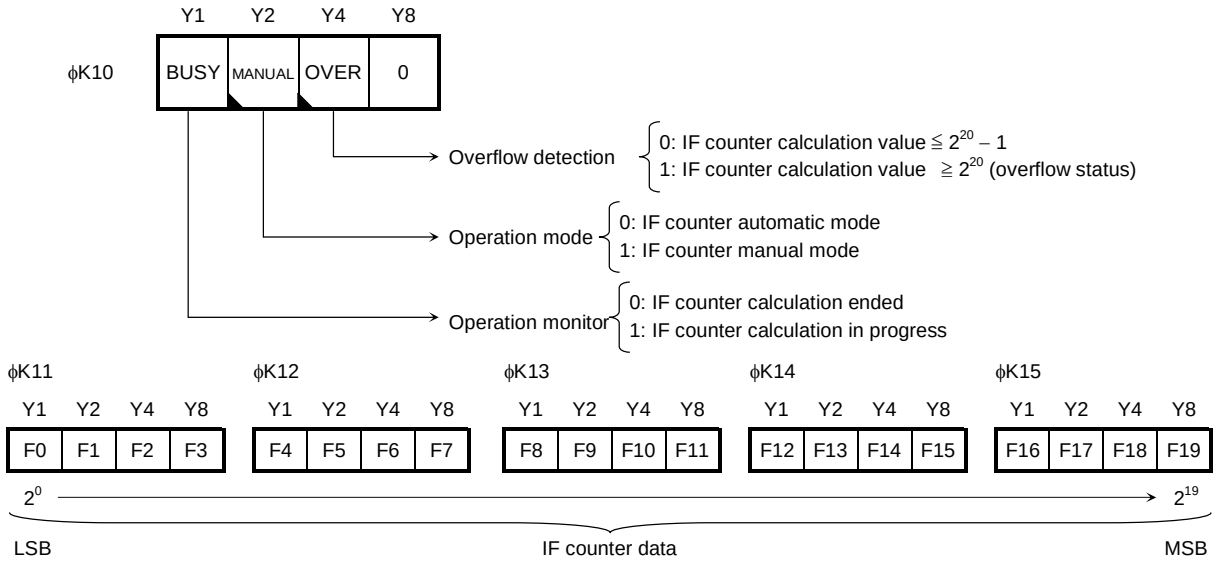


G1	G0	Gate Time
0	0	1 ms
0	1	4 ms
1	0	16 ms
1	1	64 ms



Note: When a prescaler input is set as IF counter input, at the time of a setup of a pulse-swallow system, prescsler;1/15•16 are fixed to 16 division, and this frequency is input into IF counter.

Note: When a division operation setup of the IF counter is carried out, the counter of 8 bits of higher ranks is input from INTR2 terminal. However, only 8 bits of this higher rank cannot perform a gate setup by the auto mode. Reset of this counter is reset by setting up "1" to STA/STP bit.



Note: When it is set as IF input, in PLL off-mode, IF input amplifier is turned off in PLL-off mode. In using IF counter in PLL off-mode, it sets it as an input port (CMOS input).

Note: The input amplifier un-chosen by IF1/$\overline{2}$ bit. If input amplifier turns off, this input will serve as high impedance.

(3) IF counter automatic mode

A setup in the auto mode of IF counter is set "0" to MANUAL bit and gate time is set up according to the frequency band to measure. If the STA/$\overline{\text{STP}}$ is set "1", operation of IF counter will be started and the set-up clock in gate time will be input, and this number of input pulses is counted and it ends. An end of the calculation of IF counter can be judged by referring to BUSY bit. When more 2^{20} pulses are input for a total numerical value, OVER bit is set to "1". BUSY bit and OVER bit are judged "0" and the frequency input can be measured by taking in IF data of F0-F19.

(4) IF counter manual mode

By internal time base (10 Hz etc.), it is used when gate time is controlled and it measures frequency. The manual mode is set "1" to MANUAL bit. At this time, a gate time setup serves as don't care. In STA/$\overline{\text{STP}}$ bit is set to "1", it starts calculation. In STA/$\overline{\text{STP}}$ bit is set to "0", it will end and calculation will take in data by the binary.

(5) An input setup and division setup of IF counter

Usually, intermediate frequency (IF) Measurement is input into IFin1 or IFin2 terminal input, and measures this frequency. These terminals contain input amplifier and small-size width operation is possible. In addition, the following setup is possible to the input to IF counter, and use it for it according to specification.

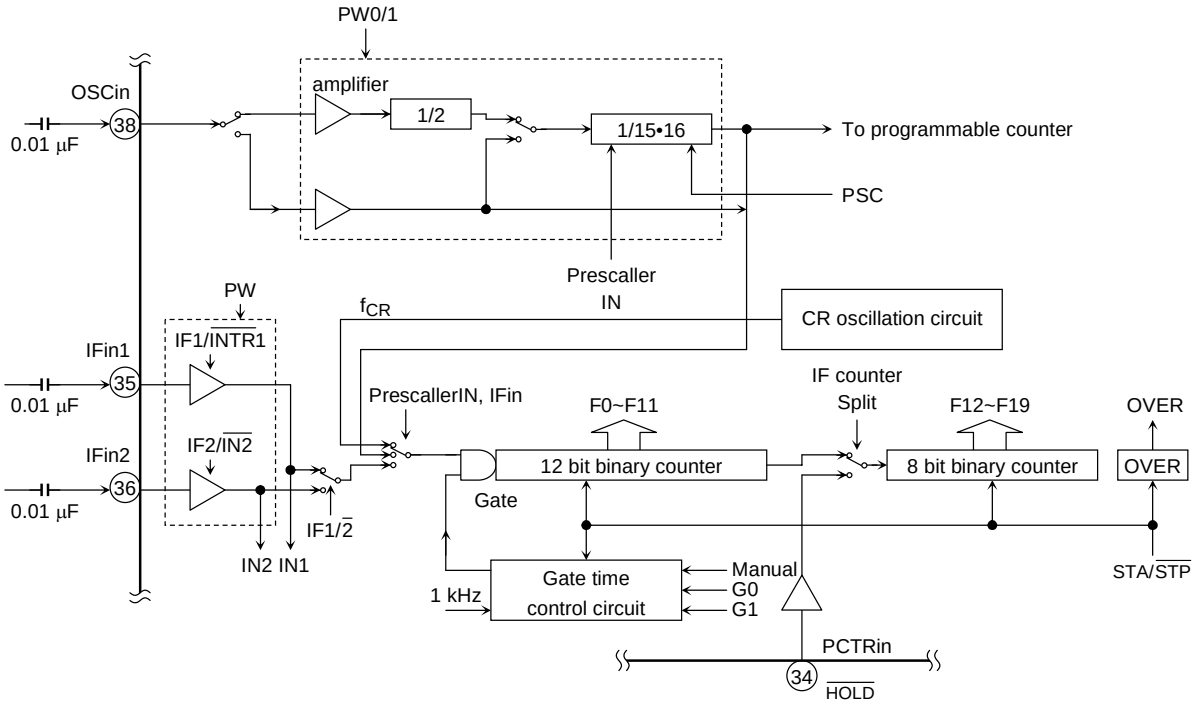
IF1/$\overline{2}$	IF1/$\overline{\text{INTR1}}$	IF2/$\overline{\text{IN2}}$	IF counter Split	Prescaller IN	Ifin (ϕL3B6:Y1)	IF Input Setup		
1	1	*	0	0	0	IFin1 input (amplifier operation)		
1	0	*	0	0	0	INTR1 (IFin1) input (CMOS input)		
0	*	1	0	0	0	IFin2 input (amplifier operation)		
0	*	0	0	0	0	IN2 (IFin2) input (CMOS input)		
*	*	*	0	1	0	OSCin input	VHF mode (32 divided frequency)	(Note)
							FM mode (32 divided frequency)	(Note)
							HF1/2 mode (16divided frequency)	(Note)
							LF mode (input frequency)	(Note)
*	*	*	0	1	1	CR Oscillation frequency (f_{CR})		
*	*	*	1	*	*	Input from PCTRin ($\overline{\text{HOLD}}$) terminal only 8 bits only of higher ranks.		

Note: Refer to the programmable counter item for the input frequency range at the time of prescaler input setup.

2. IF Counter Circuit Configuration

The IF counter circuit consists of an input amplifier, a gate time control circuit and a 12. 8 bit binary counter.

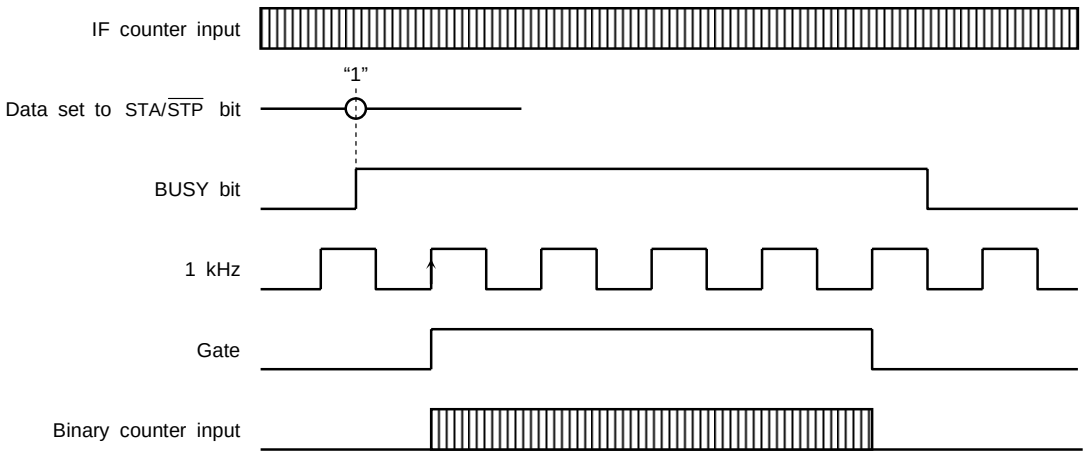
The OSCin prescaler and CR oscillation clocks can be input as IF counters.



Note: All the binary counters of the IF counter operate in a standup.

Note: During input of the OSCin into the IF counter, the 1/15･16 of the prescaler is fixed to a dividing frequency of 1/16.

This dividing frequency becomes 1/32 in VHF/FM mode and 1/16 in HF mode. In LF mode, the OSC frequency can be input directly.



An example of IF counter auto mode operation timing

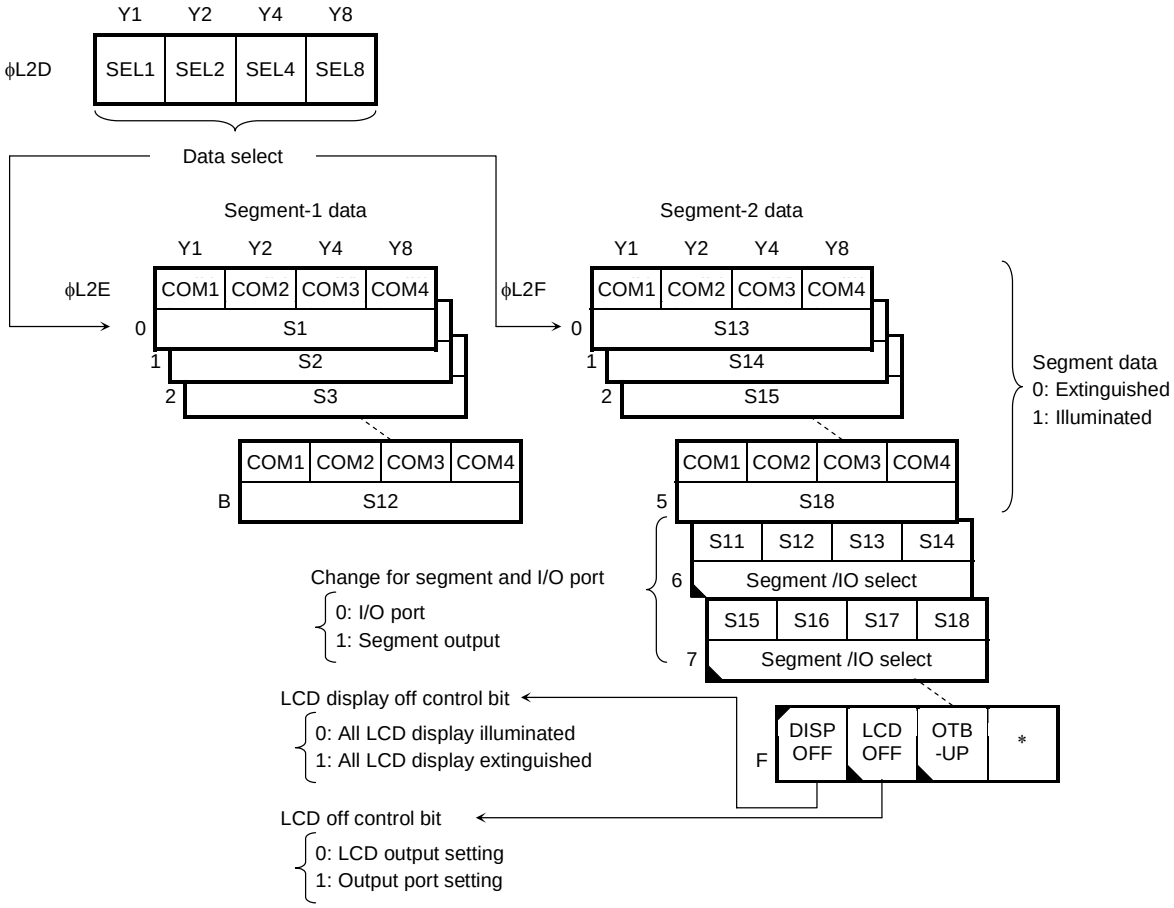
○ LCD Driver

The LCD driver uses a 1/4 duty and 1/2 bias drive method (62.5 Hz frame frequency).

The common output outputs the V_{LCD}, $V_{LCD}/2$ (V_{EE}) and the GND electrical potential, and the segment output outputs the V_{LCD} and GND electrical potential.

A combination of four common outputs and 18 segment outputs enables a maximum of 72 segments to be illuminated. The S11 to S18 segment output pins for the LCD driver can also be used as I/O ports on being set to function as I/O ports after system reset. The I/O port and segment output can be changed using bit units. All LCD output pins (COM1-S14) can be changed to output ports. The LCD driver is incorporates a constant voltage circuit (V_{EE} = 1.5 V) for display purposes and a voltage doubler circuit (V_{LCD} = 3.0 V). The voltage doubler (V_{DB}), which raises the power supply voltage to twice its level, is used for the constant voltage circuit for the display (V_{EE}). For this reason, it is even possible to stabilize the LCD display at a power supply voltage of 0.9 V.

1. LCD Driver Port



Note: If the DISP off-bit is set to “1”, common output and a segment output.are output at “L” level.

Note: The segment data controls the illumination and extinguishing of segment lighting corresponding to the common output and segment output..

Note: During clock stop mode and about 100 ms after system reset, all the common and segment outputs are fixed at “L” level..

The LCD driver control port consists of the segment data selection port and the segment data port. These ports are accessed using an OUT2 instruction for which [CN = DH~FH] has been specified in the operand. The segment data for the LCD driver is set through the segment data ports (ϕL2E, ϕL2F). The LCD display will be extinguished when the segment data port is set to "0", and will be illuminated when the port is set at "1". Also, the segment-2 data (ϕL2FF) specified with FH in the segment selection port becomes the DISP OFF bit and LCD OFF bit without setting of the segment data.

It is possible to extinguish the entire LCD display using the DISP OFF bit without setting the segment data. If this bit is set to "1", the common output and segment output are fixed to "L" level and the entire LCD display is extinguished. The segment data is retained at this point, and the previous display appears on the LCD if the DISP off bit is set to "0". In addition, rewriting of segment data is possible during DISP OFF. Moreover, after reset and CKSTP instruction execution, the DISP off bit is set to "1".

The LCD off bit can set all LCD output terminals to serve as output ports. For the LCD display, this bit is set "0".

(→ Refer to the output port item)

The terminals S11 to S18 terminal are used as I/O Ports. This control is done a segment/IO port select port (ϕL2F6, ϕL2F7).

Set to "1", the port will become segment output port and set to "0", it will become an I/O Port.

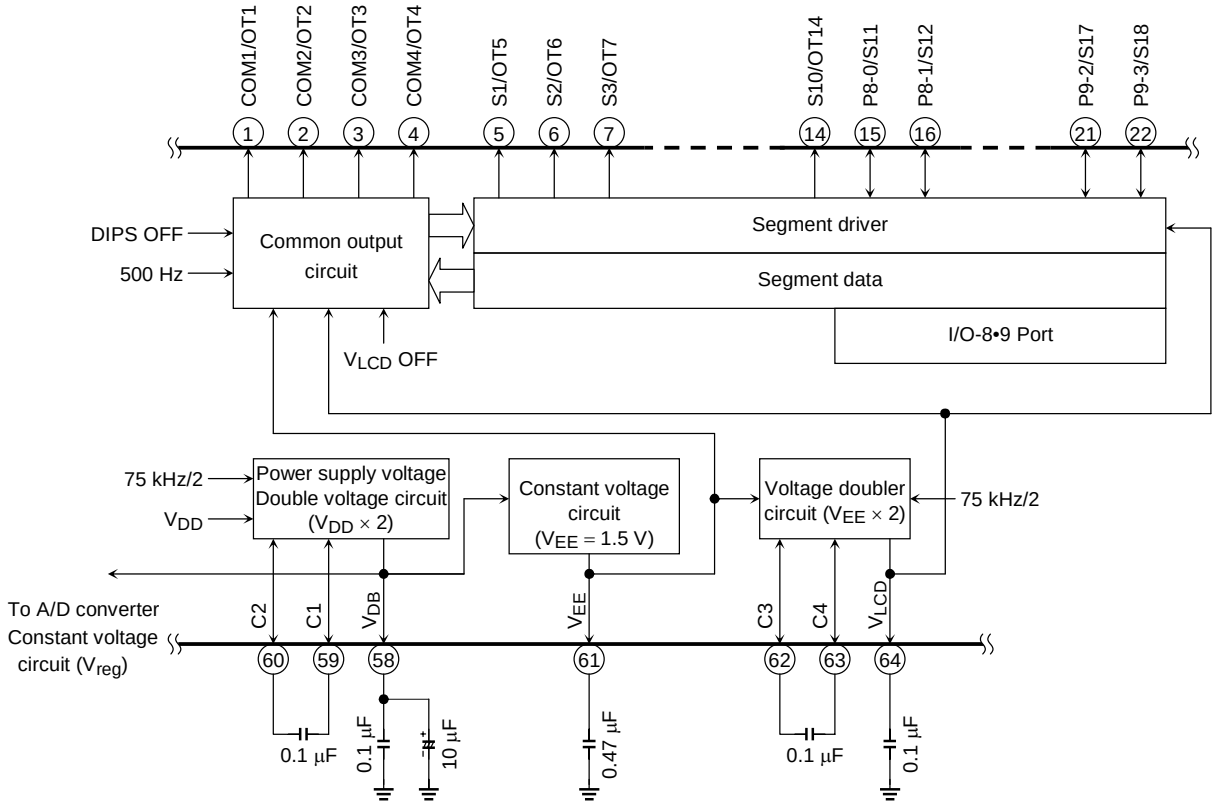
(→ Refer to the output port item)

These data is divided and undirected setting by data selects port (ϕL2D). The data of a specification port to set a segment data port to beforehand is set, and the data port corresponding to it is accessed.

A data select port is +1 increment whenever accessing data port (ϕL2E, ϕL2F). For this reason, after setting up a data selection port, it can set up continuously.

Note: The data select port is +1 increment automatically by accessing ϕL2E, ϕL2F, ϕL3B, ϕK3B on I/O map.

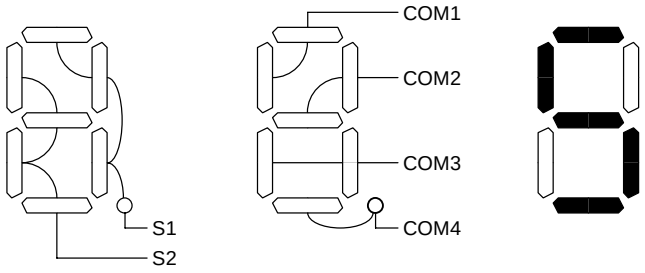
2. LCD Driver Circuit Configuration



Note: If set to serve as an I/O port, this output port is Nch open drain.

Note: In case of setting segment output as output port in setup "1" to V_{LCD} OFF bit ,"H" level of all output becomses V_{LCD} potential output. When "H" output is made into V_{DD} remove the capacitor between C3/C4, and connect V_{LCD} and V_{DD}.

Note: During clock stop mode and reset, the potential of $V_{LCD}/V_{EE}/V_{DB}$ becomes as V_{DD} level.



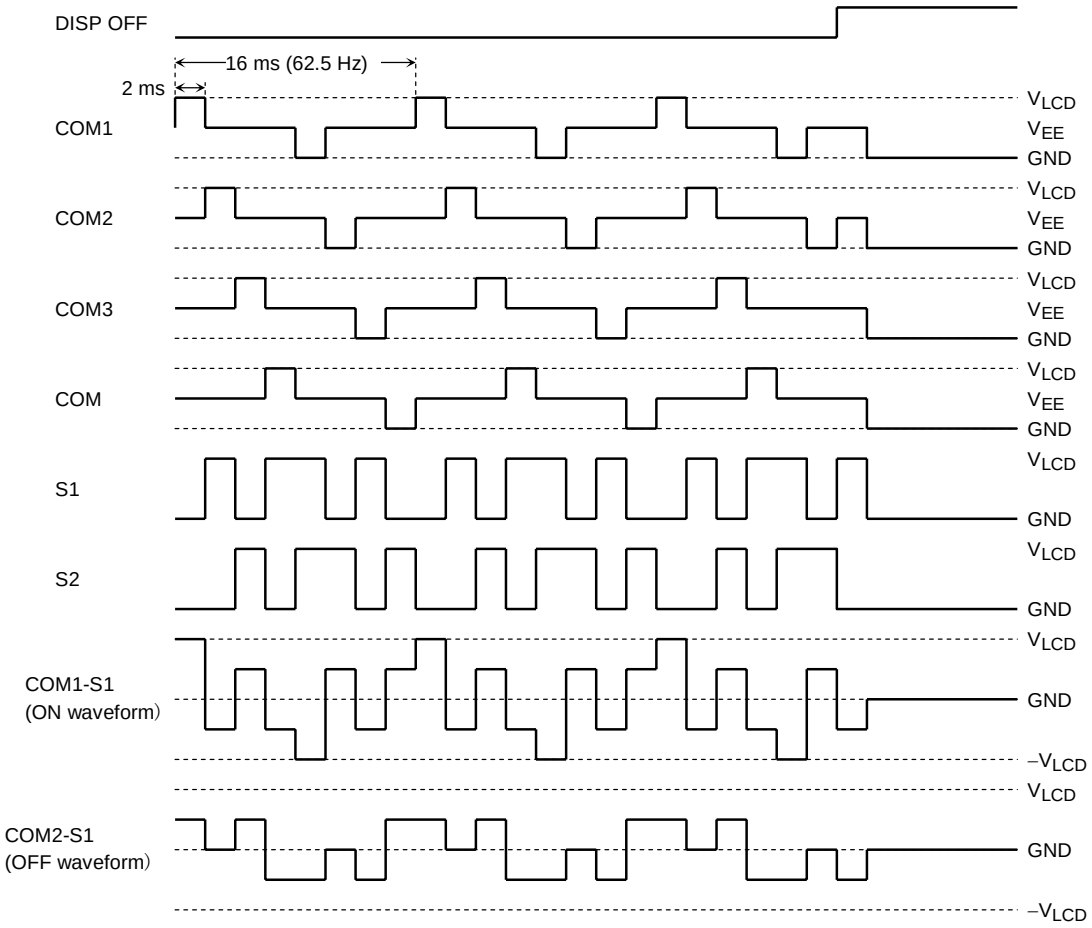
Example of segment data

Segment data -1 (ϕL2E)

	Y1	Y2	Y4	Y8
0	COM1	COM2	COM3	COM4
(S1)	1	0	1	0

	Y1	Y2	Y4	Y8
1	COM1	COM2	COM3	COM4
(S2)	1	1	0	1

Segment data selection (ϕL2D)



The potential of the LCD driver waveform outputs the potential of the V_{LCD} and GND, and the middle potential level that is 1/2 these values.

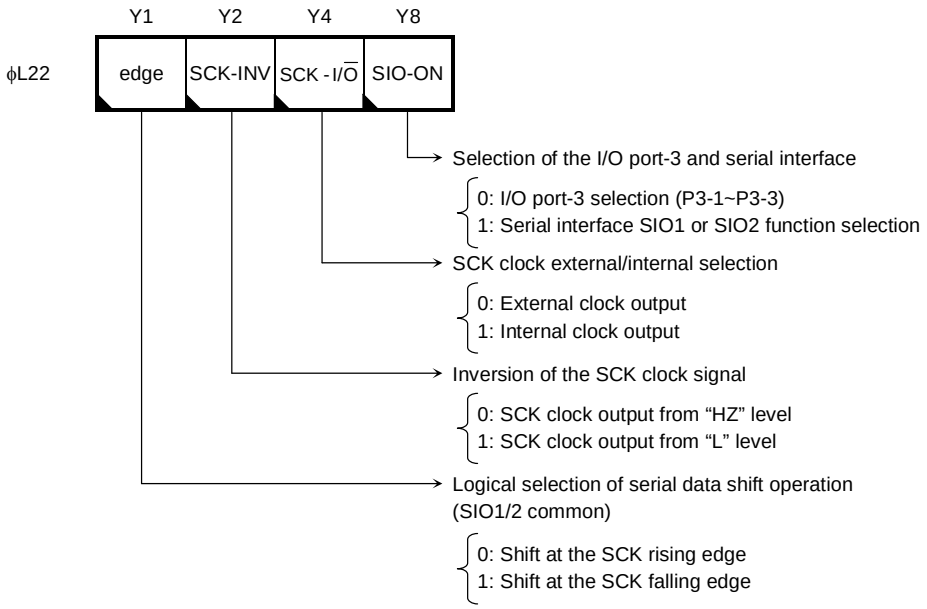
○ Serial Interface (SIO1/2)

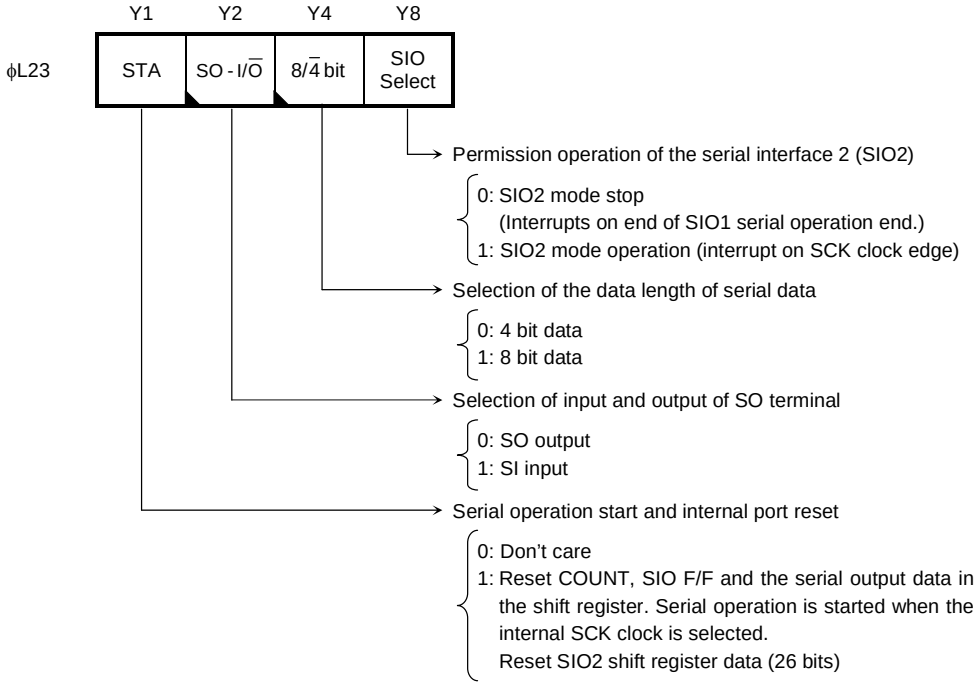
There are two kinds of serial interface: SIO1 and SIO2. SIO1 is the serial I/O port, which transmits and receives data (4 bits or 8 bits) in synchronization with an internal or external serial clock. The SI, SO, and SCK terminals transmit and receive together with the extension LSI and microcomputer, etc. Interruption is issued when the serial interface stops operating. All outputs are Nch open drain outputs.

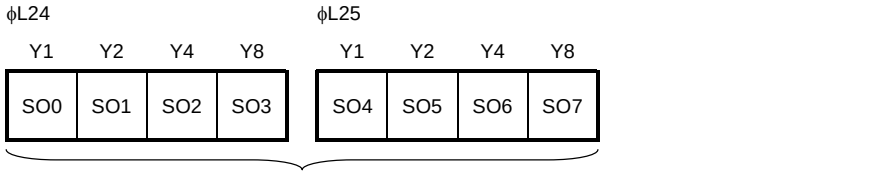
SIO2 inputs 26-bit data serially in synchronization with an external serial clock.

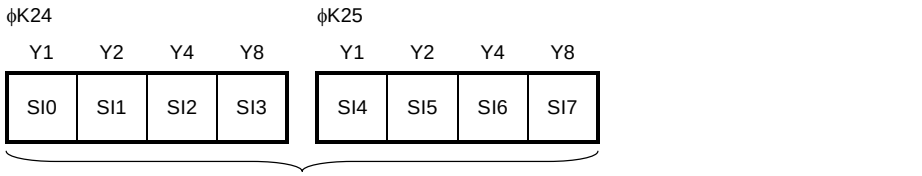
SIO2 has a function for decoding the input serial data, and interruption is issued for every input serial clock edge.

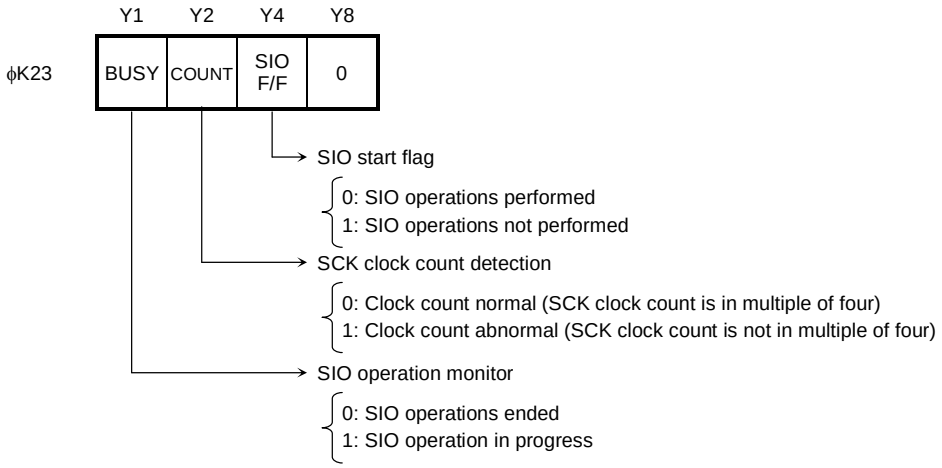
1. Control Port and Data Port of the Serial Interface











Serial interface control and data are accessed with an OUT2 and IN2 instruction for which [CN = 2H~5H] has been specified in the operand.

The serial interface terminal is used together with the I/O-3 P3-1, P3-2, and P3-3 terminals, and each of the I/O port-3 terminals are switched to operate as SI, SO and SCK terminals by setting the SIO ON bit to "1".

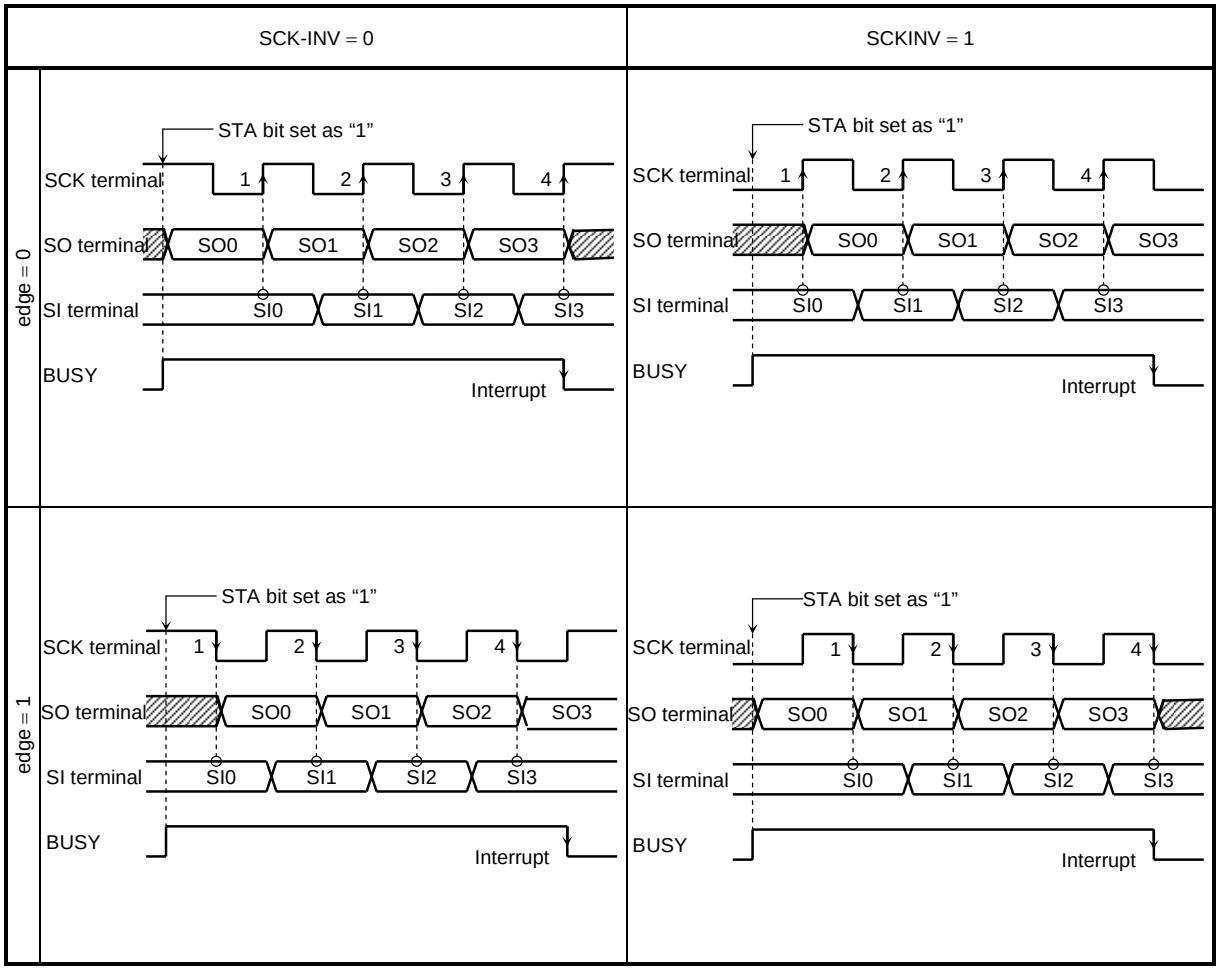
Note: All the serial interface inputs incorporate Schmidt circuits.

Note: Since the SI (P3-1) terminal can be used as an I/O port even when the serial interface function is selected, it can be used for the SIO strobe signal, etc.
If this terminal is used for serial input, be sure to enter "1" for the setting of the P3-1 output data and change it to the input state.

① edge, SCK-INV, SCK-I/O bits

The edge bit is setup the edge of a shift and the SCK-INV bit set up the input-and-output waveform of a shift clock. Serial clock (SCK) shift operation is performed on the rising edge if the edge bit is set to “0”, and on the falling edge if the edge bit is set to “1”. SCK-INV bit is set the bit of serial clock output from “H” or L”. In case of setting "0", it starts shift operation from “H” output, and setting “1”, it starts shift operation from “L” output. These bits perform serial operation in accordance with the settings as shown in the following table. Make the settings in accordance with the controlling serial format.

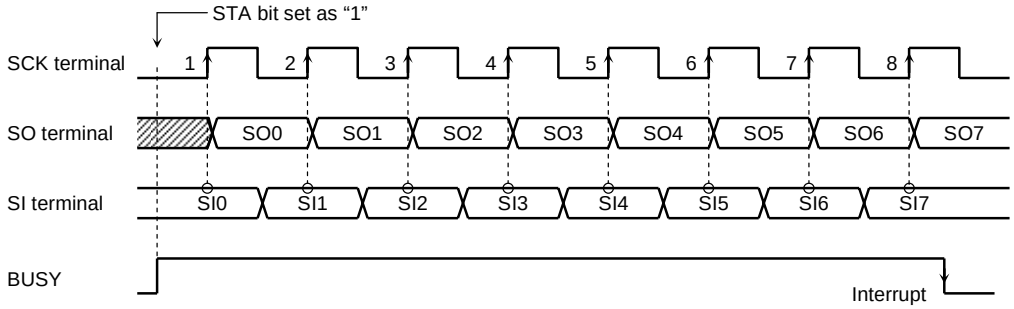
SCK-I/O bit is setup the input-output of serial clock. Usually, when this product is used as a master, t “1” to SCK-I/O bit and then it used as serial clock output and in the case of a slave, set to “0” and then it used as serial input.



Note: The “H” level of the SCK/SO terminal indicates its pull-up status. In this period this status will be “HZ”.

② 8/4 bit

The 8/4 bit selects the length of the serial data. The length of the serial data is set at 4 bits when this bit is "0" and at 8 bits when this bit is "1". If SIO is started when a serial clock is set as an internal clock, a clock (4 bits or 8 bits) will be continuously output by the state of this bit.

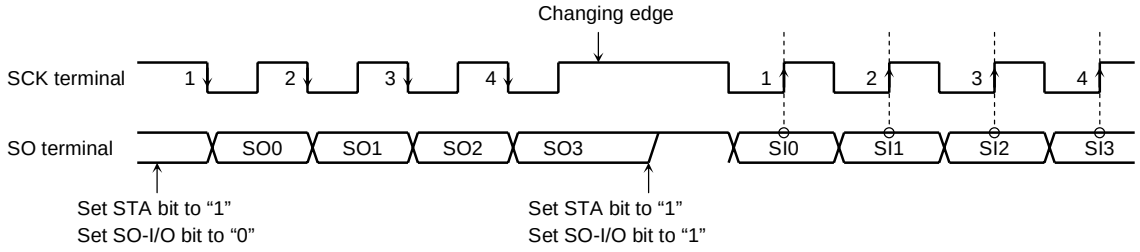


Example of serial operation for an 8 bit setting

③ SO-I/$\overline{O}$ bit

This bit sets the serial I/O for the SO terminal.

The SO terminal outputs serial data when the bit is set at "0", and is used for serial data input when this bit is set at "1". This control is used as a serial bus system for outputting and inputting serial data through one terminal.



Example for serial input-output operation

④ Serial interface operation monitor

The operational status of the serial interface is determined by referencing the BUSY, COUNT, and SIO F/F bits.

As the BUSY bit becomes "1" during SIO operations, control data switching and serial data access is performed when the BUSY bit is "0". It interrupts in falling of BUSY bit and a demand is published.

The COUNT bit determines whether the sending/receiving of data has been performed in multiples of four. The bit is set to "0" if shift operation was performed in multiples of four, and to "1" if not. .

The SIO F/F bit is set to "1" when the SCK terminal starts shift operation.

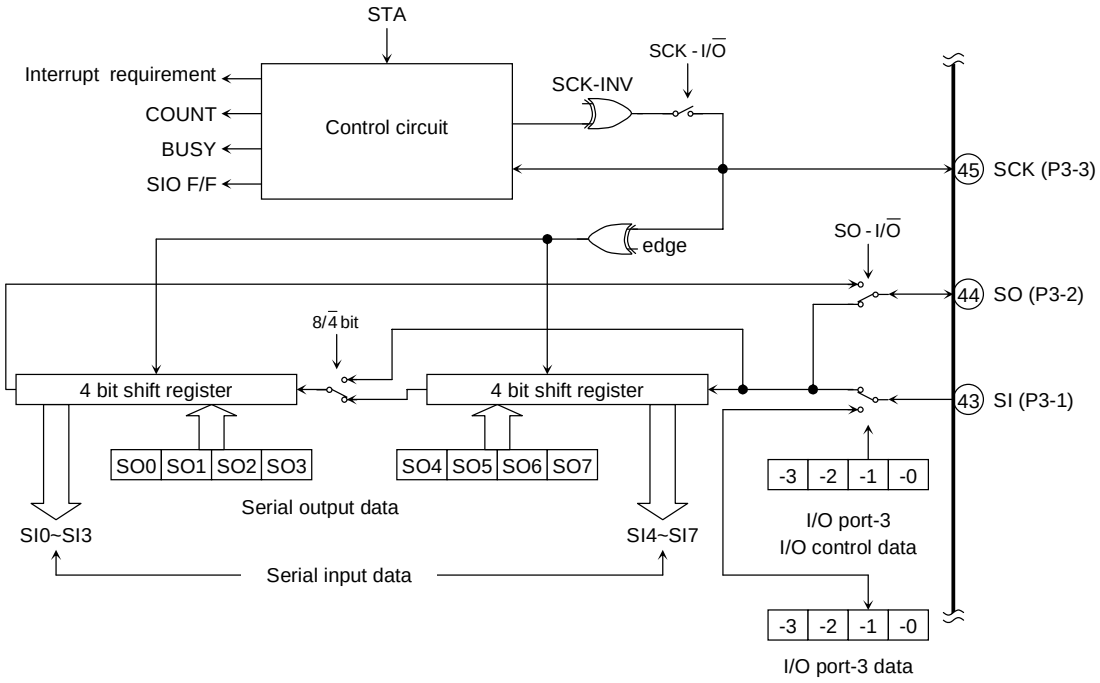
Both COUNT bb it and SIO F/F bits are reset to "0" when "1" is set in the STA bit. These two bits are mostly used when the SCK terminal sets external clocks (slave mode). An external clock is input and it can be judged to be the information that serial data was transmitted and received whether operation was performed normally.

Usually, since interruption is published, interruption processing performs a serial interface end.

⑤ STA bit

STA bit is used to start serial interface operation. Serial operation is started whenever the STA bit is set to "1". If the STA bit is set to "1", serial output data will be transmitted to a shift register, and the COUNT bit and SIO F/F bit will be reset. A serial clock is output for an internal SCK setting; and a state of waiting for the serial clock input will take effect in the case of an external setting.

2. Composition of the Serial Interface 1 (SIO1)



Srial interface 1 consists of a control circuit, a shift register, and an I/O Port.

Note: The erminal can be used as I/O Port -3 (P3-1).

Note: The shift memory contents for the data and serial input data are stored by the data memory.

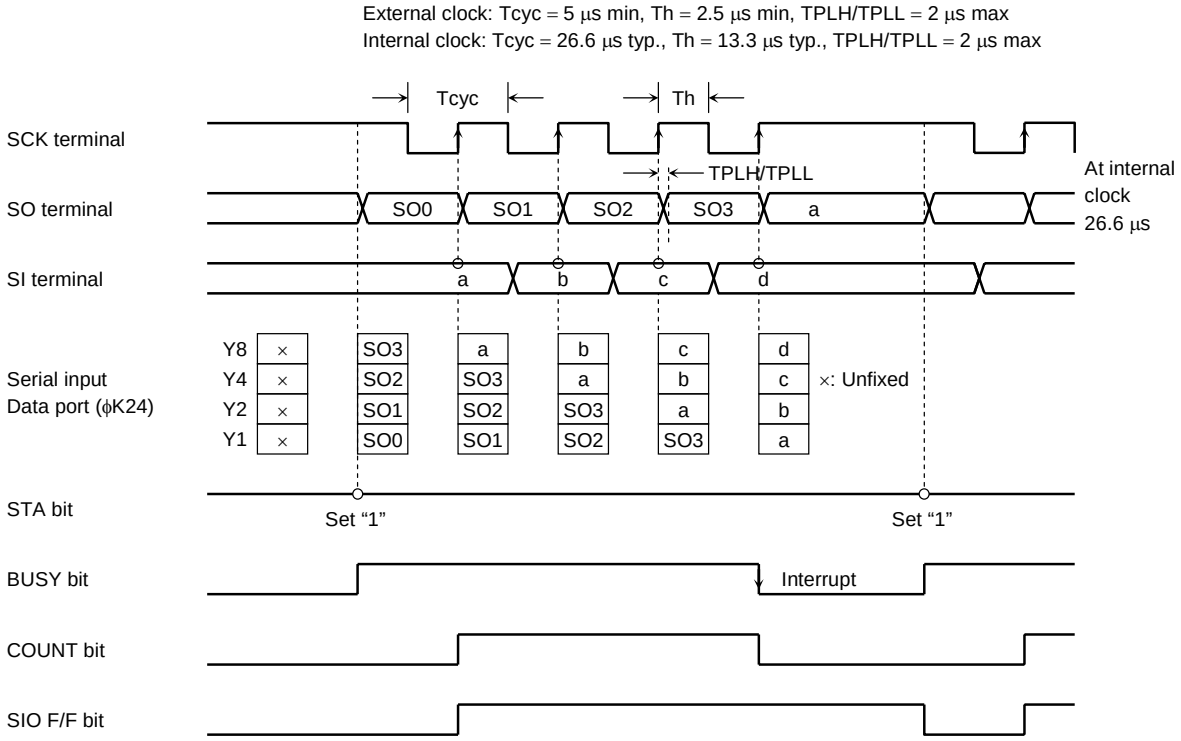
For this reason, the contents of the data set to serial output data and those of the serial input data are not in agreement.

Note: All serial input terminals are the Schmitt input type.

Note: The output of the SO terminal and the serial clock output of SCK terminal are Nch open drain outputs. For this reason, connect pull-up resistance. In addition, be sure to use a pull-up potential of 3.6 V or less.

3. Serial Interface Timing of SIO1 Circuit

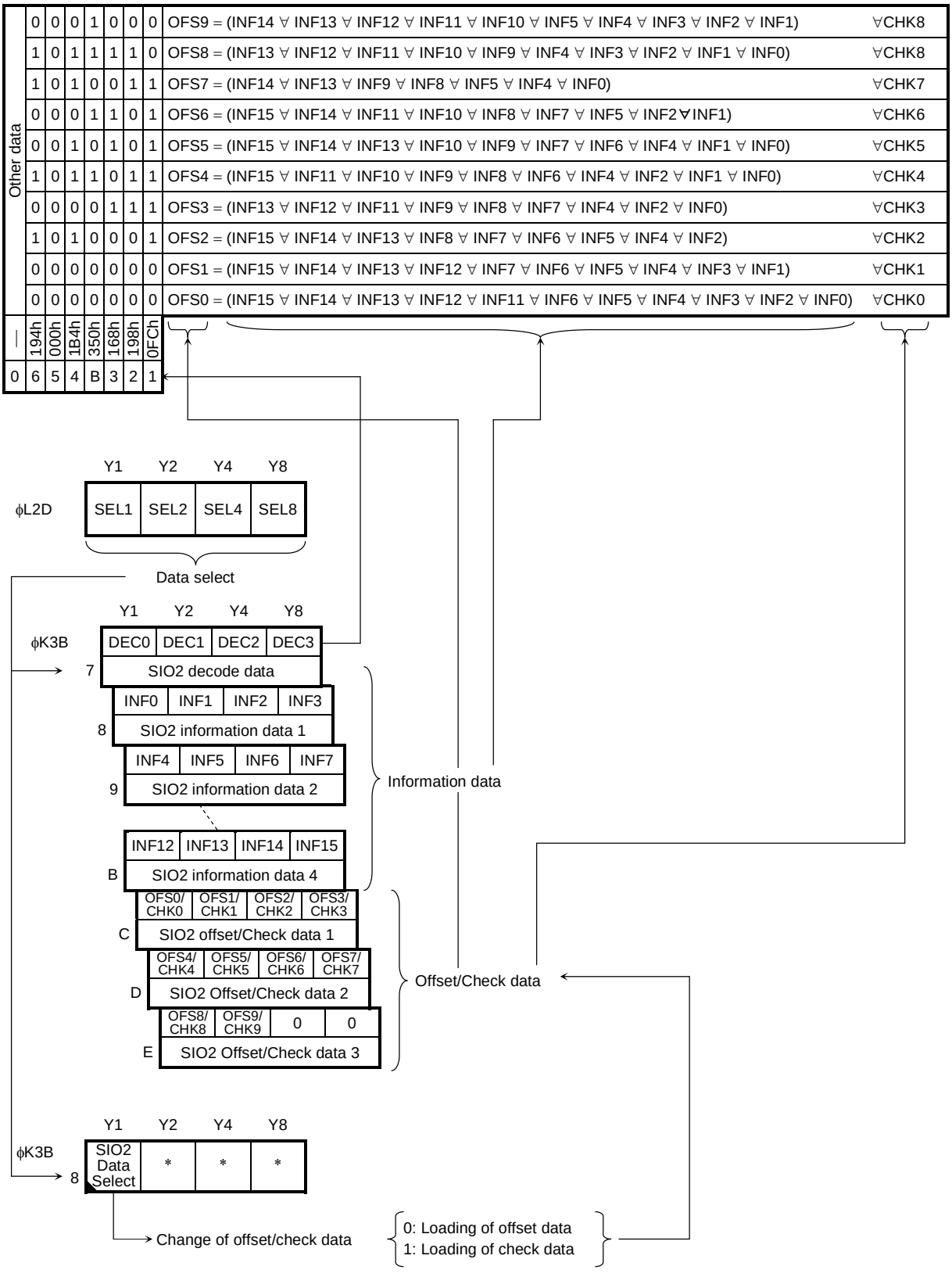
The clock frequency output from the SCK terminal when the SCK clock is set as an internal clock is 37.5 kHz (Duty. = 50%). When the SCK clock is as an external input, a clock of a maximum of 200 kHz can be input.



4. Serial Interface 2 (SIO2) control and Data Ports

Note: ∀: EXOR (exclusive logic sum)

Other data	0	0	0	1	0	0	0	OFS9 = (INF14 ∀ INF13 ∀ INF12 ∀ INF11 ∀ INF10 ∀ INF5 ∀ INF4 ∀ INF3 ∀ INF2 ∀ INF1)	∀CHK8
	1	0	1	1	1	1	0	OFS8 = (INF13 ∀ INF12 ∀ INF11 ∀ INF10 ∀ INF9 ∀ INF4 ∀ INF3 ∀ INF2 ∀ INF1 ∀ INF0)	∀CHK8
	1	0	1	0	0	1	1	OFS7 = (INF14 ∀ INF13 ∀ INF9 ∀ INF8 ∀ INF5 ∀ INF4 ∀ INF0)	∀CHK7
	0	0	0	1	1	0	1	OFS6 = (INF15 ∀ INF14 ∀ INF11 ∀ INF10 ∀ INF8 ∀ INF7 ∀ INF5 ∀ INF2 ∀ INF1)	∀CHK6
	0	0	1	0	1	0	1	OFS5 = (INF15 ∀ INF14 ∀ INF13 ∀ INF10 ∀ INF9 ∀ INF7 ∀ INF6 ∀ INF4 ∀ INF1 ∀ INF0)	∀CHK5
	1	0	1	1	0	1	1	OFS4 = (INF15 ∀ INF11 ∀ INF10 ∀ INF9 ∀ INF8 ∀ INF6 ∀ INF4 ∀ INF2 ∀ INF1 ∀ INF0)	∀CHK4
	0	0	0	0	1	1	1	OFS3 = (INF13 ∀ INF12 ∀ INF11 ∀ INF9 ∀ INF8 ∀ INF7 ∀ INF4 ∀ INF2 ∀ INF0)	∀CHK3
	1	0	1	0	0	0	1	OFS2 = (INF15 ∀ INF14 ∀ INF13 ∀ INF8 ∀ INF7 ∀ INF6 ∀ INF5 ∀ INF4 ∀ INF2)	∀CHK2
	0	0	0	0	0	0	0	OFS1 = (INF15 ∀ INF14 ∀ INF13 ∀ INF12 ∀ INF7 ∀ INF6 ∀ INF5 ∀ INF4 ∀ INF3 ∀ INF1)	∀CHK1
	0	0	0	0	0	0	0	OFS0 = (INF15 ∀ INF14 ∀ INF13 ∀ INF12 ∀ INF11 ∀ INF6 ∀ INF5 ∀ INF4 ∀ INF3 ∀ INF2 ∀ INF0)	∀CHK0
—	194h	000h	1B4h	350h	168h	198h	0FCh		
0	6	5	4	B	3	2	1		



The data port of the serial interface 2 (SIO2) is constituted of 16-bit information data (ϕK3B8~B), 10-bit check data, 10-bit offset data and 4-bit decoding data (ϕK3B7). In 26-bit serial data, serial data of 16-bit are information data and 10-bit are check data. As shown in the above-mentioned table, the data that took the exclusive logic sum of each bit of 26-bit data turns into offset data. Furthermore, when the offset data is specialized in the above –mentioned, the data of 1~6h and Bh are output as 4-bit decoding data. Loading port of check data and offset data (ϕK3BC~E) are common and selection of loading is SIO2 data Select bit (ϕL3B8). If the bit is set to "0", the offset data will be loaded and set to "1", the check data will be loaded.

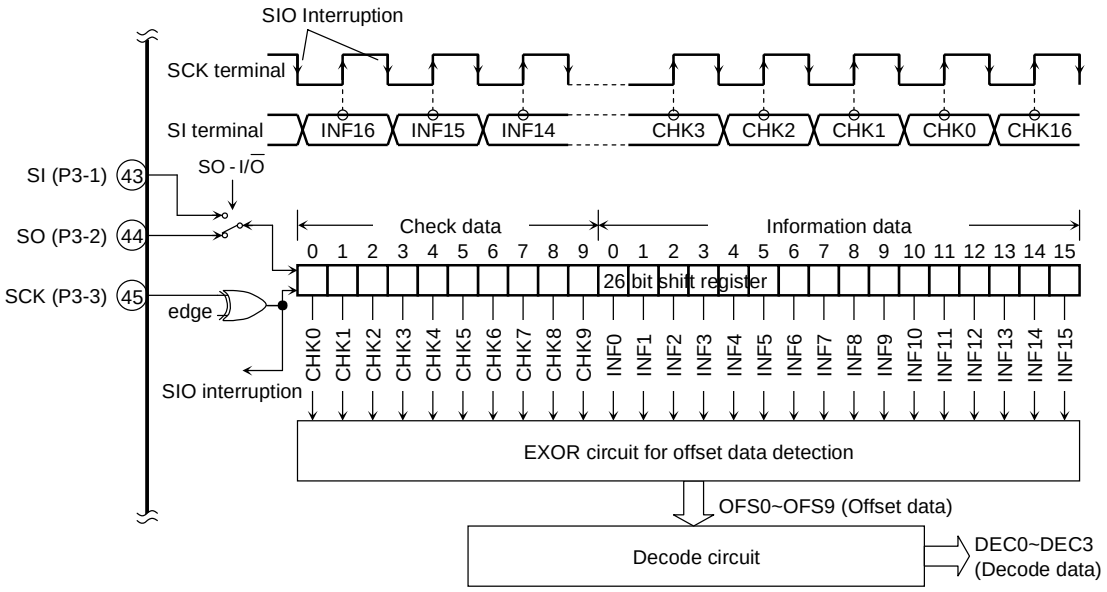
If the data "1" is set to SIOon bit (ϕL22) and SIO Select bit (ϕL23), SIO2 will be in a permission state of operation. If the data "1" is set to STA bit (ϕL23), 26-bit shift registers are all reset and SI terminal input state will be serially input one by one by the shift register with the shift clock of SCK terminal clock. If SIO interruption is permitted at this time, interruption will be published with edge contrary to the shift edge of a shift clock. SI terminal and SO terminal can be changed to a serial input terminal by the SO-I/O bit, if the data "0" is set up, SI terminal will serve as a serial data and "1" will be set up, SO terminal will serve as a serial data input. If SI terminal is selected as a serial input, since SO terminal turns into a SIO1 serial output terminal, we recommend use of SO terminal to a serial input.

These data is divided and indirect specified set up by the data select port (ϕL2D). The data of a specification port to set DAL address port to beforehand is set, and the data port corresponding to it is accessed. A data selection port is +1 increment by accessing of DAL address port (ϕKL3B). For this reason, after setting up a data selection port, it can set up continuously.

Note: The data select port is +1 increment automatically by accessing ϕL2E, ϕL2F, ϕL3B and ϕK3B on I/O map.

Control and serial data of the serial interface-2 is accessed using an OUT2 instruction for which [CN = 3H] has been specified in the operand.

5. Control and Serial Data of the Serial Interface 2



Note: If the SI terminal is used for serial input, the SO terminal will serve as an SIO1 serial output.

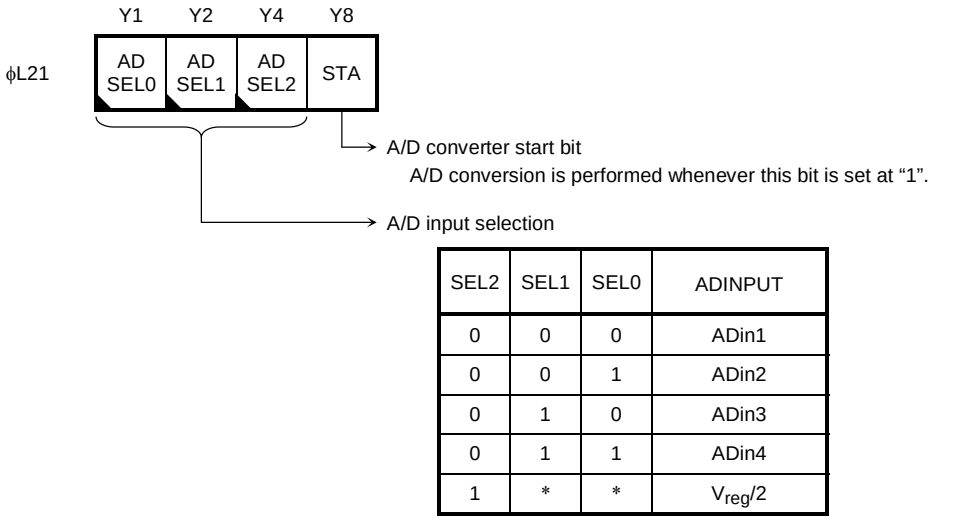
When using the SI terminal as a serial input, be sure to set the P3-1 output data to "1" and change it to the input state.

Note: Serial input is inputt and shifted also SIO1 at the same time.

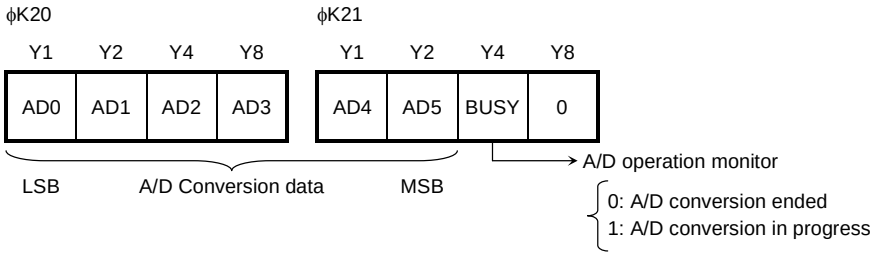
○ A/D Converter

The A/D converter is used for measuring the strength of electric fields and the voltage of batteries with 4-channel 6-bit resolution.

1. A/D Converter Control Port and Data Port



SEL2	SEL1	SEL0	ADINPUT
0	0	0	ADin1
0	0	1	ADin2
0	1	0	ADin3
0	1	1	ADin4
1	*	*	$V_{reg}/2$



A/D converter is the serial comparison systems of 6 bit decomposition ability.

An internal power supply (V_{DD}) is used for the standard voltage of A/D conversion. The voltage dividing this power supply by 64 and the A/D input voltage are compared, and the data is output to the A/D conversion data port. The A/D conversion input follows the multiplex method for the four channels of the external input terminals (ADin1~ADin4 terminal) and the 1/2 potential of the Vreg terminal voltage, and is selected using bits AD SEL0 to AD SEL2.

The A/D converter performs A/D conversion whenever the STA bit is set at "1", and this ends after seven machine cycles (280 μs). The completion of A/D conversion is determined by reference to the BUSY bit, and the A/D conversion data is loaded into the data memory after conversion has finished.

The result of A/D conversion is obtained through the following calculation.

$$V_{DD} \times \frac{n - 0.5}{64} \ (63 \geqq n \geqq 1) \ \leqq \text{A/D input voltage} \ \leqq V_{DD} \times \frac{n + 0.5}{64} \ (62 \geqq n \geqq 0)$$

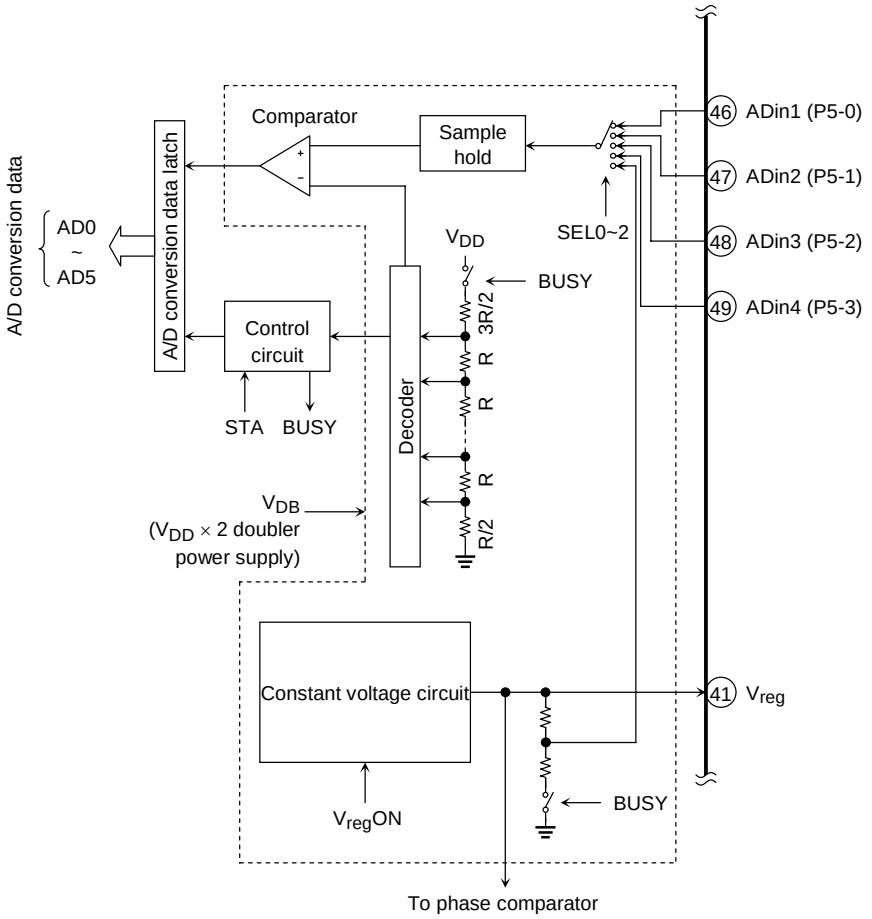
(n is the A/D conversion data value. [decimal])

The $V_{reg}/2$ to the A/D input is used for battery detection. The V_{reg} potential is 1.5 V ± 0.15 V and 1/2 potential: 0.75 V ± 0.075 V of V_{reg} terminal voltage is chosen as A/D input, and V_{DD} potential which is standard potential can be detected by carrying out A/D conversion of this potential. When V_{DD} potential is 1.5 V, A/D conversion data is set to 20H, and if A/D data goes up and V_{DD} potential serves as 0.75 V as V_{DD} potential falls, it will serve as 3FH. If this function is used, the V_{reg}ON bit is set to "1".

These controls are accessed with an OUT2/IN2 instruction for which [CN = 0H, 1H] has been specified in the operand.

Note: If the V_{reg}ON bit is set to "1" , the CPU operating consumption current is increased. The Vreg terminal also supplies power to the phase comparator.

2. A/D Converter Circuit Configuration



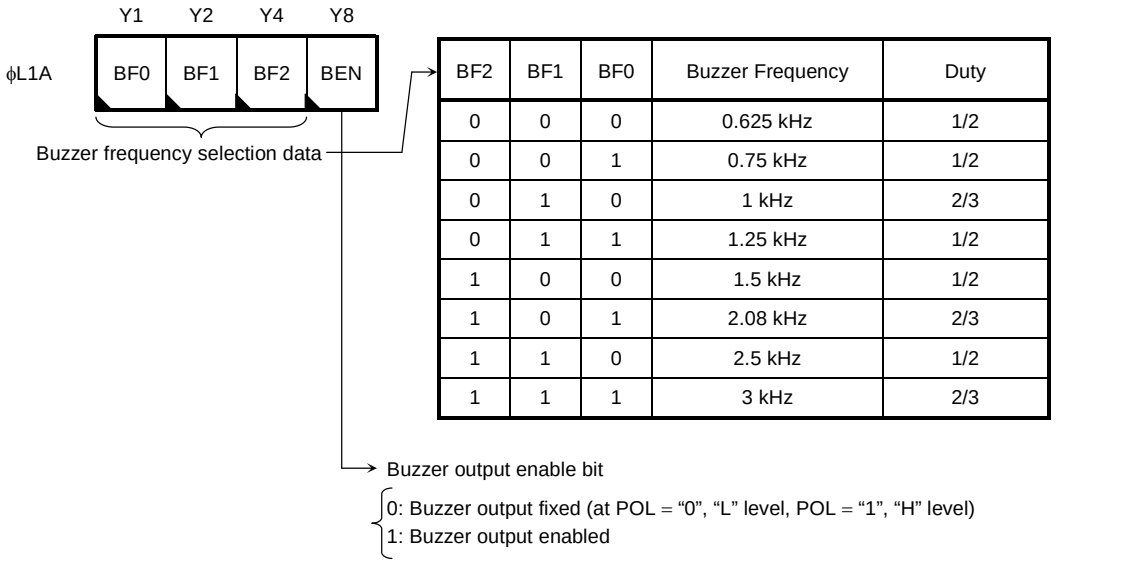
The A/D converter consists of a 6-bit D/A converter, a comparator, an A/D conversion latch and control circuit. Since the 6-bit D/A converter and comparator part operate only when the BUSY bit is "1", there is no A/D converter power when the A/D converter is inoperative. The doubler voltage (twice that of V_{DD}) is used to drive the A/D converter part.

Note: To the output data of I/O Port -5 (Nch open drain) corresponding to A/D input terminal to use set up "1" and use it by changing into an input state.

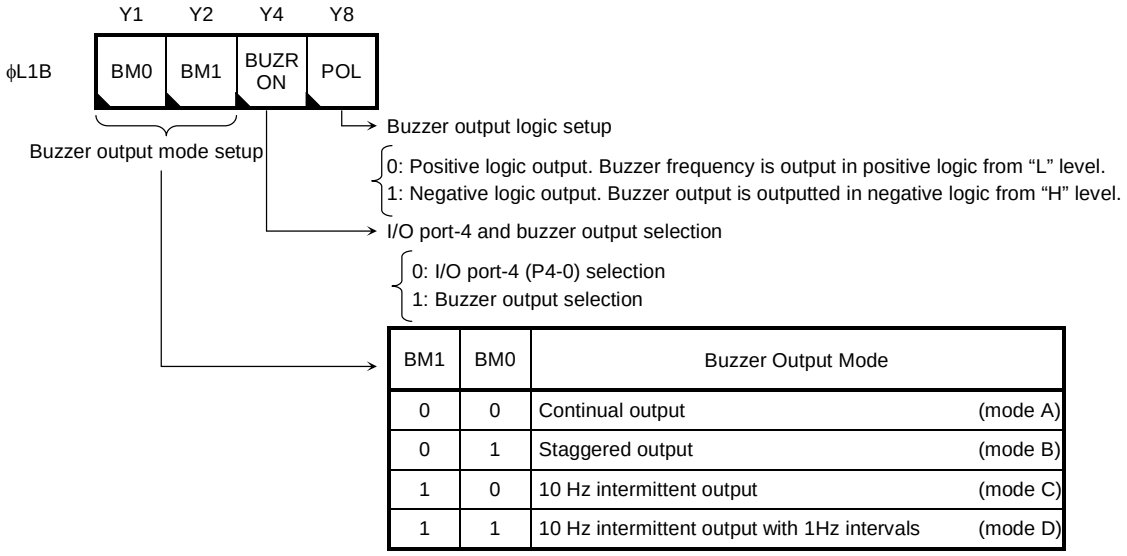
○ Buzzer Output

The buzzer output can be used to output tones and alarm tones to confirm key operations and the tuning scan mode. The buzzer type can be selected from a combination of four output modes and eight different frequencies.

1. Buzzer Control Port



BF2	BF1	BF0	Buzzer Frequency	Duty
0	0	0	0.625 kHz	1/2
0	0	1	0.75 kHz	1/2
0	1	0	1 kHz	2/3
0	1	1	1.25 kHz	1/2
1	0	0	1.5 kHz	1/2
1	0	1	2.08 kHz	2/3
1	1	0	2.5 kHz	1/2
1	1	1	3 kHz	2/3



BM1	BM0	Buzzer Output Mode	
0	0	Continual output	(mode A)
0	1	Staggered output	(mode B)
1	0	10 Hz intermittent output	(mode C)
1	1	10 Hz intermittent output with 1Hz intervals	(mode D)

Ports P4-0 I/O are also used for buzzer output. In order to set it as a buzzer output, BUZR ON bit is set up "1" and it changes to a buzzer output by setting it as an output by the P4-0 I/O control port. After logic setting up of buzzer frequency, mode setup and a logic setup, buzzer enable bit is set up "1", it outputs buzzer. At the time of condition setup, buzzer enable bit is setup "0".

In continual output mode (mode A), if the buzzer enable bit is set to "1", the buzzer frequency will be output continuously; if "0" is set, the buzzer output will stop. In staggered output mode, whenever the buzzer enable bit is set to "1", the buzzer is output and stopped at 50-ms intervals.

Under a buzzer output (50 ms), if buzzer enable bit is set to "1" again, the buzzer is extended to 50 ms, being output for 100 ms.

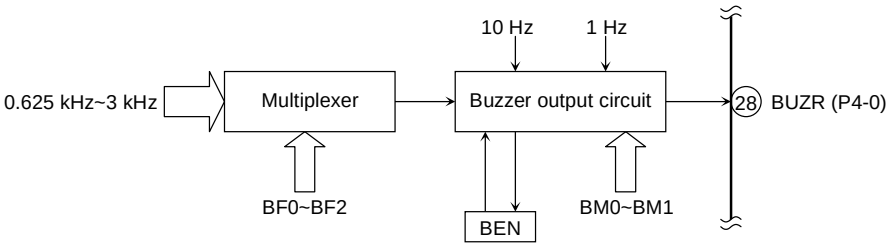
Given that a further extension of 50 ms to 150 ms is possible, the buzzer time can be set up easily.

In the 10-Hz intermittent output mode (mode C), if the buzzer enable bit is set to "1", a 50-ms buzzer output and 50-ms buzzer pause are carried out continuously. A setting of "0" stops the buzzer output.

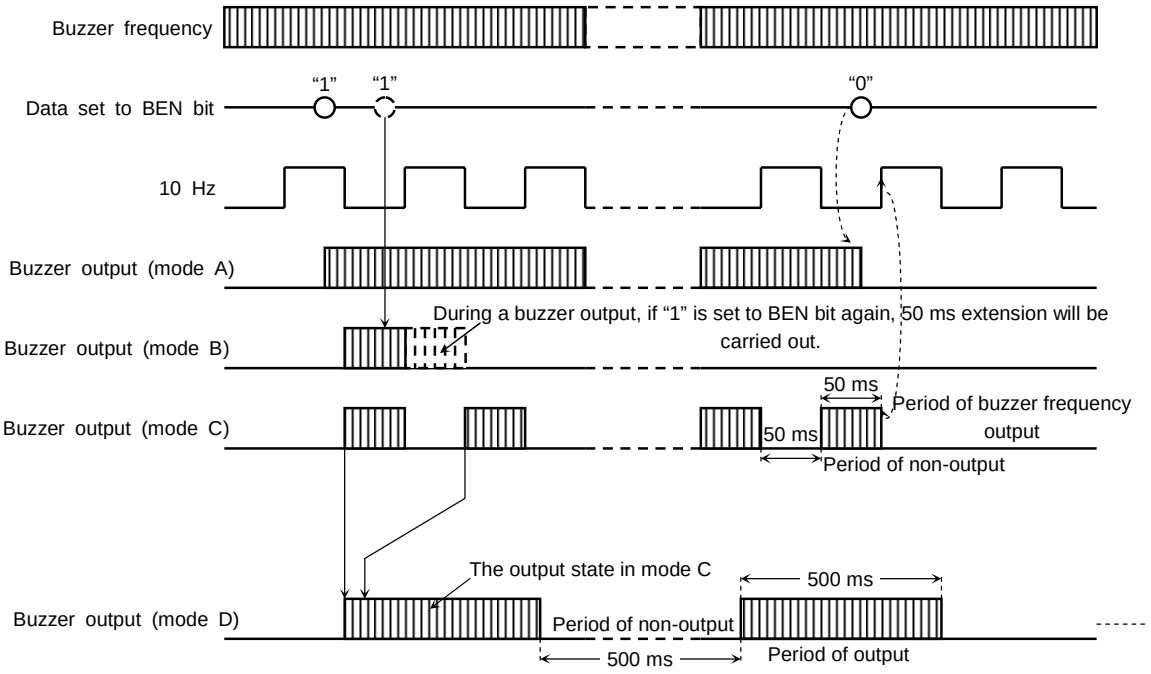
10 Hz intermittent output with 1 Hz intervals mode (mode D), if buzzer enable bit is set "1", 50 ms buzzer output and 50 ms buzzer pause will carry out 500 ms output, after that 500 ms pause output of 50 ms buzzer output and the 50 ms buzzer pause is carried out again, and this operation is repeated. A set of "0" stops a buzzer output. At mode B, C, and D, a buzzer is in an output state, even if it sets "0" to buzzer enable bit and it makes it stop, the buzzer of 50 ms is output and stops. In addition, a buzzer output state can be judged according to the contents of a timer port. The timer port 10 Hz bit is "0", buzzer is an output state and it is in a pause state at the time of "1".

The control of buzzer is accessed by an OUT 1 instruction for which [CN = AH, BH] has been specified in the operand.

2. Buzzer Circuit Configuration



3. Buzzer Output Timing



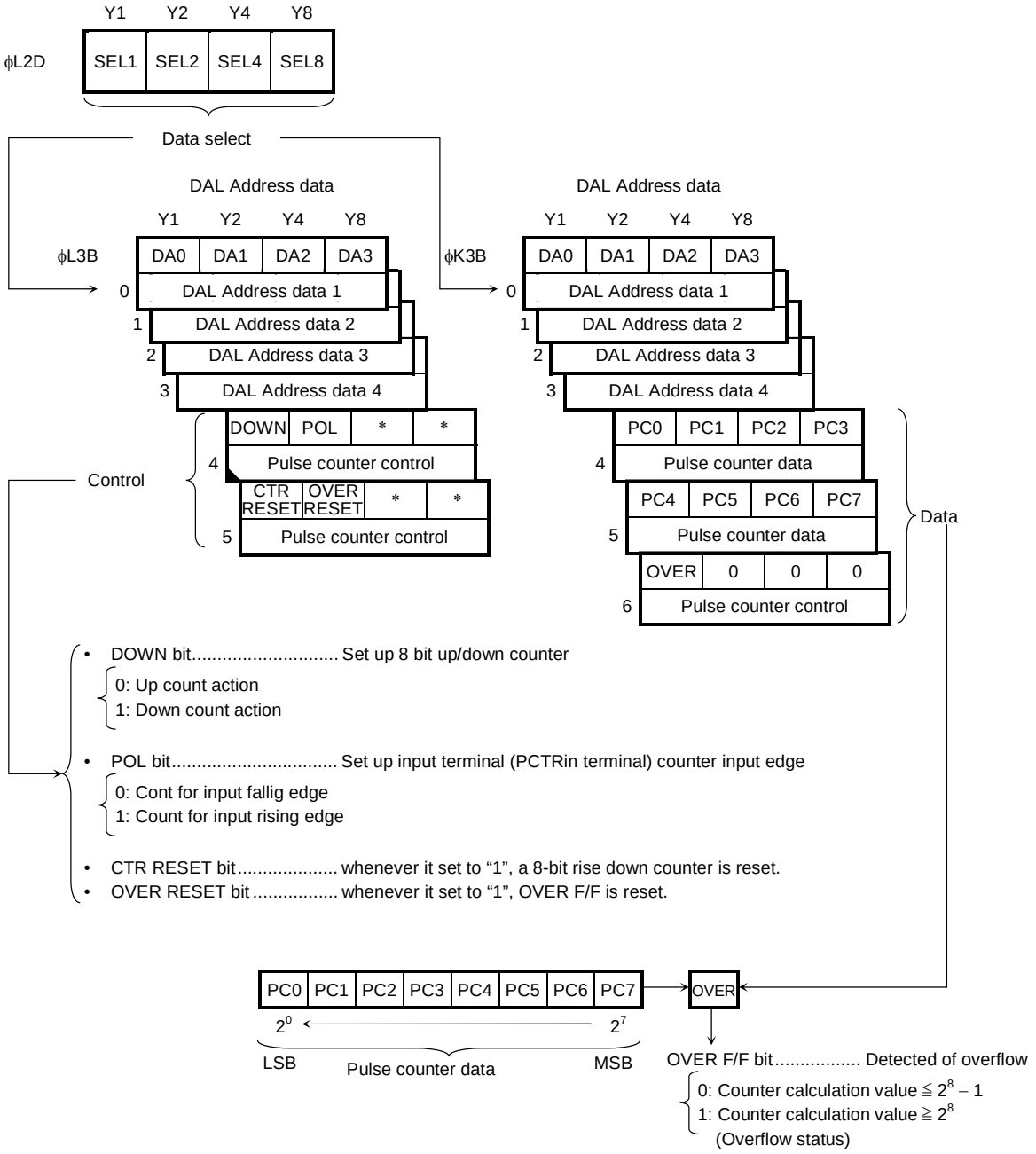
Note: When making the buzzer output function active, be sure to set P4-0 to the input state (by setting the I/O control port to "1").

Note: The change of buzzer frequency is updated in modifications of 10 Hz.

○ Pulse Counter

The pulse counter is an 8-bit up/down counter and detection of the number of clocks can be performed with PCTRin terminal (CMOS input type) used also $\overline{\text{HOLD}}$ terminal. It can use for the count and detection of a tape run.

1. Pulse Counter Control Port, Data Port



The pulse counter measures the number of pulses in the PCTRin input terminal.

POL bit set up the clock edge of input terminal. If "0" is set, it will count in the falling of an input and it will set to "1", it will count in the rising of an input. Usually, this bit is used fixed.

DOWN bit sets up a up/down of 8-bit counter. If it sets to "0" and it will set to rise count operation and "1", down count operation will be done. A change of a rise/down can be performed freely. However, if a clock pulse is input during change command execution, since it is canceled, be careful of this count.

When 2^8 or more pulses are input, OVER F/F bit is set to "1". When performing count operation of 8-bits or more, this OVER F/F are detected, and on a data memory, only the number of times of overflow is added and subtracted, and can correspond. After detection by this bit, and OVER RESET bit is set "1" and OVER F/F is reset. The CTR RESET bit resets only the 8-bit counter. The counter is reset whenever this bit is set to "1".

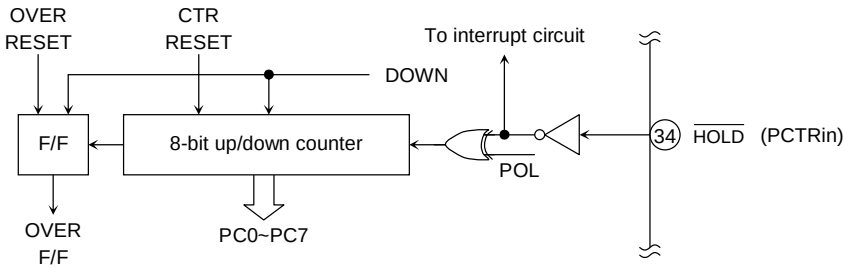
Counter data loaded data in a data memory by the binary.

The control of pulse counter and data loading is accessed using the OUT3/IN3 instructions for which [CN = BH] have been specified in the operand and arranges in DAL address register port. This port is set up by data select port (ϕL2D), which specified the division. The data of a specification port to set beforehand is set and the data port corresponding to it can be accessed. The data select port is +1 increments whenever it accesses DAL address port (ϕL3B, ϕK3B). For this reason, after setting up a data selection port, it can set up continuously.

Note: If POL bit is changed, a clock pulse may enter. Reset data by the reset bit after changing.

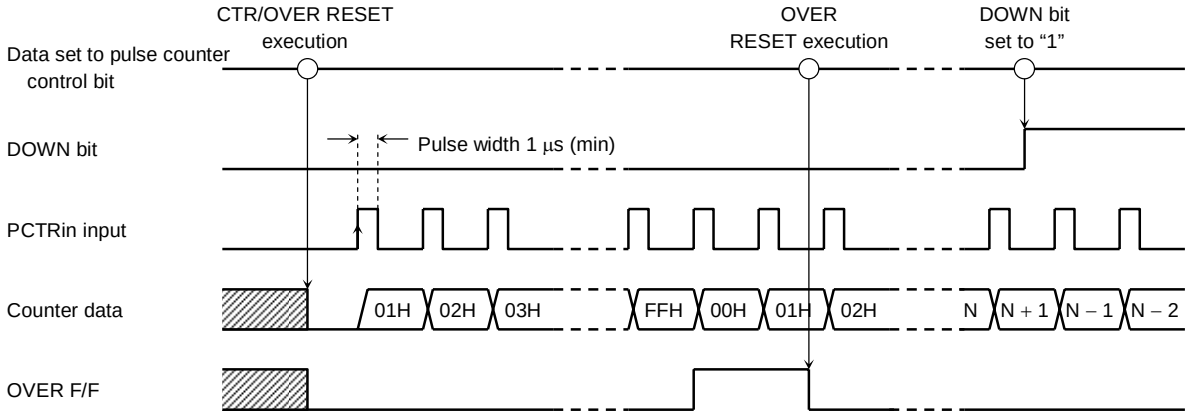
Note: If data select port is +1 increments whenever it accesses ϕL2E, ϕL2F, ϕL3B, ϕK3B on the I/O map.

2. Pulse Counter Circuit Configuration



Note: It can be used together as pulse counter and interrupt function ($\overline{\text{HOLD}}$ terminal input).

3. Example for Pulse Counter Timing



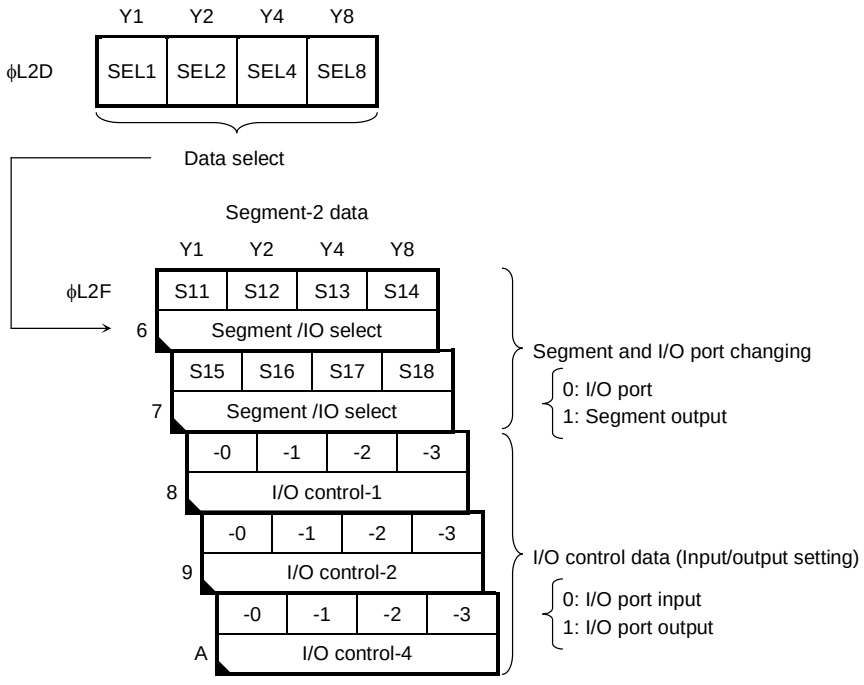
○ Input and Output Port (I/O Port)

There are 28 I/O ports available between I/O ports 1~5, 8-9 of which are used to input and output control signals. Of these 28 I/O ports, 12 I/O ports are CMOS type and 16 I/O ports are Nch open drain type. The combination function and the functional features of each I/O port are as follows.

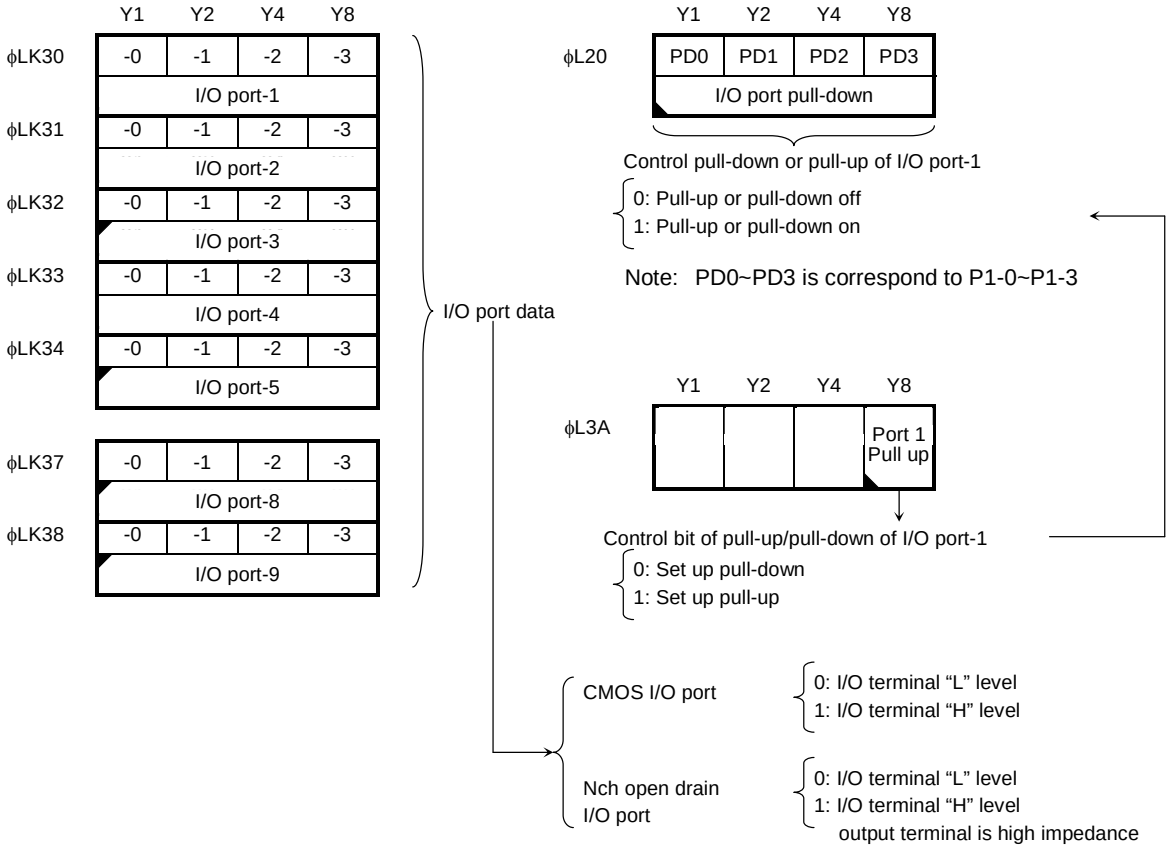
I/O Port		Combination and Additional Function	Structure
I/O port-1		It is possible to set pull-up/pull-down. But, a combination of pull-up pull down is not available.	CMOS
I/O port-2	P2-0~-2	—	
	P2-3	Prescaller PSC output	
I/O port-3*	P3-0	—	Nch open drain
	P3-1~3	Serial interface input/output port	
I/O port-4	P4-0	Buzzer output	CMOS
	P4-1~3	I/O port	
I/O port-5		6-bit A/D converter analog input The potential to V_{DB} ($V_{DD} \times 2$) can be input.	Nch open drain
I/O port-8		The potential to V_{LCD} (3 V) can be input.	
I/O port-9			

Note: I/O port-3 terminal of * markis Nch high output buffer output and output-proof is 3.6 V (max).

1. I/O Port Control, I/O Port Data



Note: I/O-1, I/O-2, - - - - - is correspond to the name of P1-0~-3, P2-0~-3, - - - - - terminal.



The I/O port for the I/O ports is set with the contents of the I/O control data port. "0" is set in the I/O control data port bit which corresponds to the relevant port when setting the input port, and "1" is set when setting the output port.

I/O control data port is arranged segment-2 data port and set up by data select port (ϕL2D), which specified the division. The data of a specification port to set beforehand is set and the data port corresponding to it can be accessed. The data select port is +1 increments whenever it accesses DAL address port (ϕL2F). For this reason, after setting up a data selection port, it can set up continuously.

The output status of the I/O port is controlled by executing the OUT3 instruction for which corresponds to each I/O port during output port setting. The contents of the data currently output can also be loaded into the data memory by executing the IN3 instruction. In addition, the data read by the IN3 command is not surely in agreement with the data output by the OUT3 instruction and, in order to read the state of a terminal.

The data input in the I/O port is loaded into the data memory by executing the IN3 instruction which corresponds to each I/O port during input port setting. The contents of the output latch will have absolutely no effect on the input data at this point.

Nch open drain I/O ports have not I/O control data. When it makes an input, it is set "1" in I/O data port, the status becomes high impedance and read the input status into data memory by IN3 instruction. When output state becomes "L" level, it set "0" in I/O data port by OUT3 command.

The execution of the WAIT instruction and CKSTP instruction is cancelled and CPU operations are re-started when the status of the I/O port input specified in the input port changes with I/O port-1. Also, the MUTE port and MUTE bit are forcibly set to "1" during changes in the input status when the MUTE port's I/O bit is set at "1". By control port of I/O port-1 pull-down, it sets up pull-down or pull-up status. It can set up a pull-down or pull-up for every terminal and if the port is set up "1", it will become a pull-up or a pull-down. The pull-up/pull down control bit of I/O Port -1 perform a change of a pull-up and a pull down.

The status is pull-down if the bit is set to "0", and pull-up if the bit is set to "1"

Set up the pull-up and pull-down is used for key matrix configuration. I/O Port -1 with a pull down or a pull-up is considered for a usual I/O Port output as an input as an output of a key matrix, and a key matrix is constituted. It is able to constitute of the key matrix of a low noise by the following methods. In setting pull-down to I/O port-1, the output side of a key matrix is usually high impedance (input state), output and scan to "H" level on key loaded line, detected key input or non by loading input status of I/O port-1. In the case of a pull-up, "L" level is output and it detected on a key loading line. During executing of CKSTP instruction and WAIT instruction, the existence of this key input can also be judged and re-started. When re-starting at the time of CKSTP command execution, I/O Port -1 is used by changing into a pull-up state. For the clock stop mode, since the outputs of an I/O Port are output all "L" level, I/O Port -1 stands by in the state of a pull-up, and if a key is input, I/O Port -1 input will change and re-start. In this case, since the standby time of about 100 ms occurs as time lag after being canceled of a clock stop. Since release of WAIT instruction holds the output state, re-starting is possible by the method of both a pull-up and a pull down, and since there is no time lag from release, detection and operation of a key are quickly possible. Using these backup modes together can reduce consumption current.

Since the input of I/O Port -1 is an inverter input, the usage that serves as middle potential cannot be done to this input. But, only at the time of execution of the input instruction, since an input will be in an ON state, even if middle potential is input, as for other I/O Port inputs, unusual consumption current does not occur. For this reason, use of the pull-up in potential lower than VDD potential, the three value output of an output level, etc. is possible.

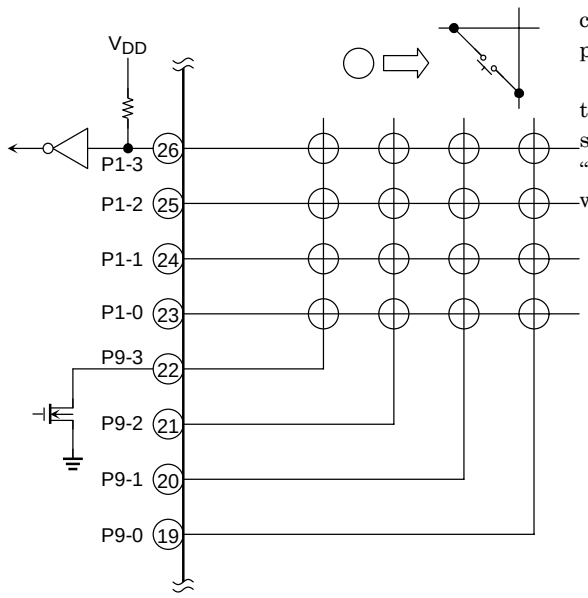
I/O Port -2, -4 terminals are the I/O Ports of CMOS structure, P2-3 terminal is the prescaler PSC output, P4-0 terminal is the buzzer output and P3-1-3 terminals are the serial interface serve a double purpose, respectively. I/O port-3, -5, -8~-9 are Nch open drain I/O port.

I/O Port -3 uses V_{LCD} (3 V) for the gate potential of Nch output buffer. For this reason, the output current by which power supply voltage was stabilized also in the time of low voltage can be obtained. This port can perform the input and output to 3.6 V.

I/O port-5 is used as 6-bit A/D converter input. This port is able to input V_{DB} potential (the potential to $V_{DD} \times 2$).

I/O Port -8, -9 are using also LCD driver. V_{LCD} (3 V) is used for the gate potential of an Nch open output buffer. For this reason, the output current by which power supply voltage was stabilized also in the time of low voltage can be obtained. These terminals can perform the input and output to V_{LCD} (3 V). These terminals are set as the input of an I/O Port after reset.

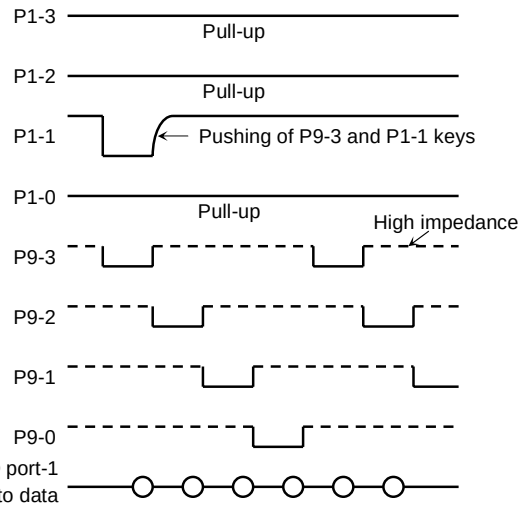
Note: The data select port is +1 increments automatically when it accesses ϕL2E, ϕL2F, ϕL3B, ϕK3B on the I/Omap.



Example for key input matrix circuit

The following is an example of key input matrix circuit configuration. Without key input, it pulled-up and key is pushed, it input "L" level from souce side(I/O port-9).

It is necessary to take into consideration the shift time to the pull-up of a key input from "L". They are all about a key souce side at the time of WAIT instruction execution and "L" WAIT instruction can be lifted, whenever a key input will be pushed, if it stands by on the level.



○ Register Port

The G-register and data register outlined in the explanation on the CPU are also used as a single internal port.

1. G-register (ϕKL1D, ϕKL1E)

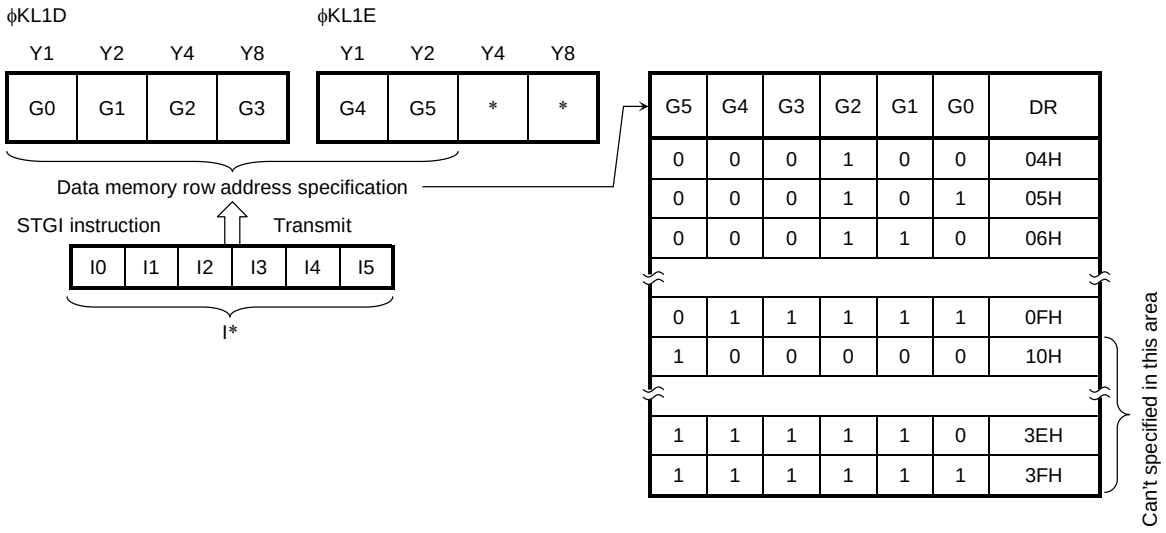
This register addresses the data memory's row addresses (DR = 04H~3FH) during execution of the MVGD instruction and MVGS instruction. The register is accessed using an OUT1/IN1 instruction for which [CN = DH~EH] has been specified in the operand. Moreover, if STGI instruction is used, data can be set to this register using a single instruction.

Note: The contents of this register are only valid when the MVGD instruction and MVGS instruction are executed and are ineffective when any other instruciton is executed. Moreover, this register is not affected by MVGD instruction and MVGS instruction.

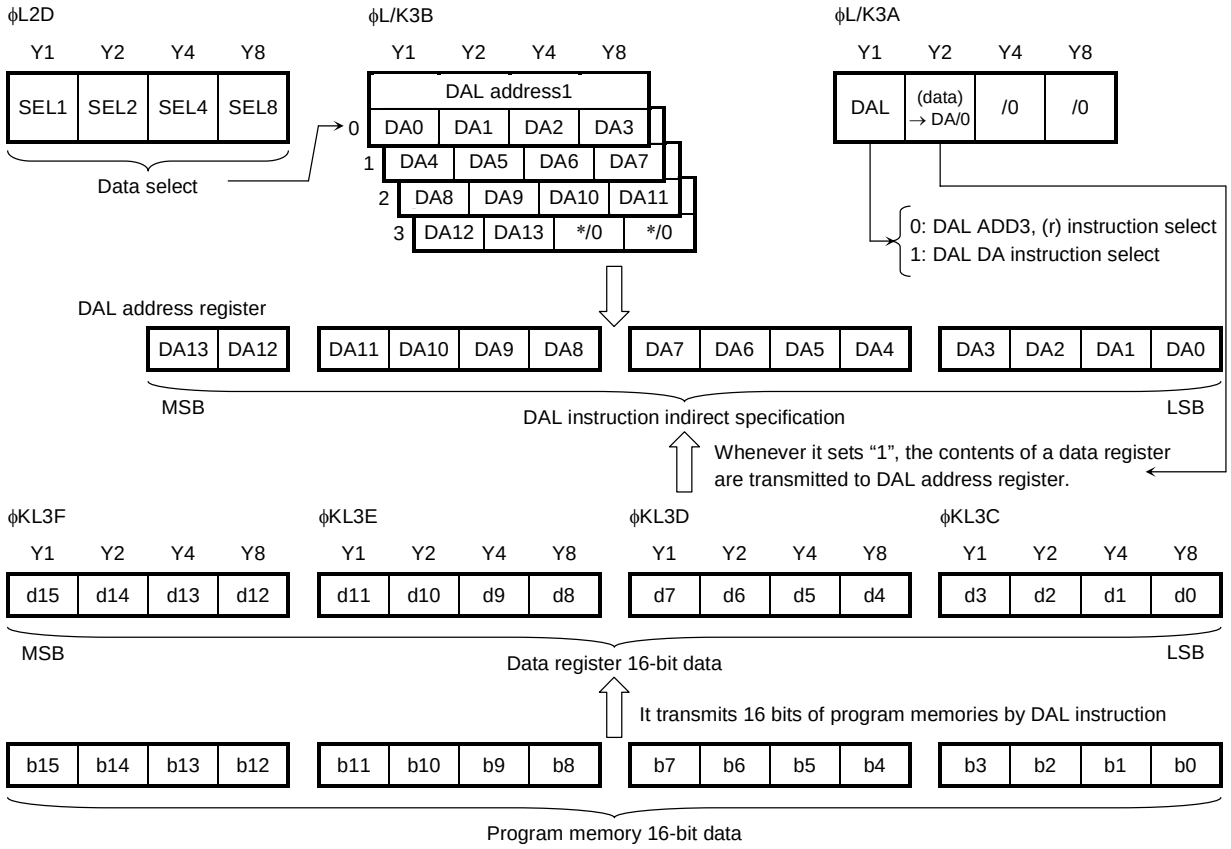
Note: All of the data memory row addresses can be specified indirectly by setting data 00H to 3FH in the G-register. (DR = 00H~3FH)

Note: For a reason with a RAM capacity of 256 words, this product will become unfixed if 10H-3FH is specified to be G-register.

Note: Writing and read-out are possible for this register. Please evacuate and return in a data memory if needed at the time of interruption.



2. Data Register (ϕKL3C~ϕKL3F), DAL Address Register (ϕKL3B0~ϕKL3B3) and Control Bit



The data register is 16-bit register for which load the program memory data when the DAL instruction is executed. The contents of this register are loaded into the data memory in 4-bit units with the execution of the OUT1/IN1 instructions for which [CN = CH~FH] has been specified in the operand. This register can be used for loading LCD segment decoding operations, radio band edge data and the data related to binary to BCD conversion.

The DAL address register (DA) is 14-bit register for which specified the program memory indirectly when the DAL instruction is executed. There are 2 kinds of operation methods of DAL instruction. The control is selected by DAL bit. When DAL bit is set "0", ADDR3 (6 bit) of the operand and contents of general register (r) becomes the reference address of program memory and when DAL bit is set "1", 14 bit of DAL address register becomes reference address. At the time of setting DAL bit is "0" and execution of DAL instruction, only program memory area (0000H~03FFH) becomes reference area and DAL bit is set "1" and execution of DAL instruction, all program memory area (0000H~3FFFH) becomes reference area.

If (DATA) → DA bit is set to "1", it can transfer from the contents of data register to 14 bit DAL address register by executing of single instruction.

The contents of DAL address register are accessed the data in 4-bit units with the execution of the OUT3/IN3 instruction for which [CN = BH] have been specified in the operand. DAL address register port is setup by data select port (ϕL2D) for which divides and indirect specified. The data of a specification port to set beforehand is set and the data port corresponding to it is accessed. Data select port is +1 incremented whenever is accessed this port(ϕL3B, ϕK3B). For this reason, after setting up a data selection port, it can access continuously.

DAL bit and (DATA) → DA bit are accessed with the execution of OUT3/IN3 instruction for which [CN = AH] has been specified in the operand.

Note: DAL address register becomes effective only execution of DAL instruction when setting "1" and becomes unrelated at the time of other instruction execution. It does not have the influence on this register by DAL instruction.

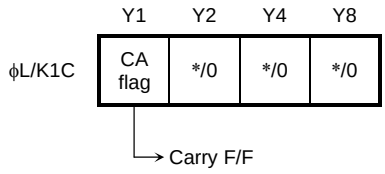
Note: For this product have 4 k step of ROM Capacity, If 1000H - 3FFFH is specified to be DAL address register and DAL instructiion is executed, the contents of a data register will become unfixed.

Note: It's possible to write in and read out for data register and DAL address register. Please evacuate and return in a data memory if needed at the time of interruption.

Note: It's no action when (DATA) → DA bit is set "0" . When it accesses to ϕK3A, it only read out only the DAL bit. (The other bit is "0".)

3. Carry F/F (Ca flag, ϕKL1C)

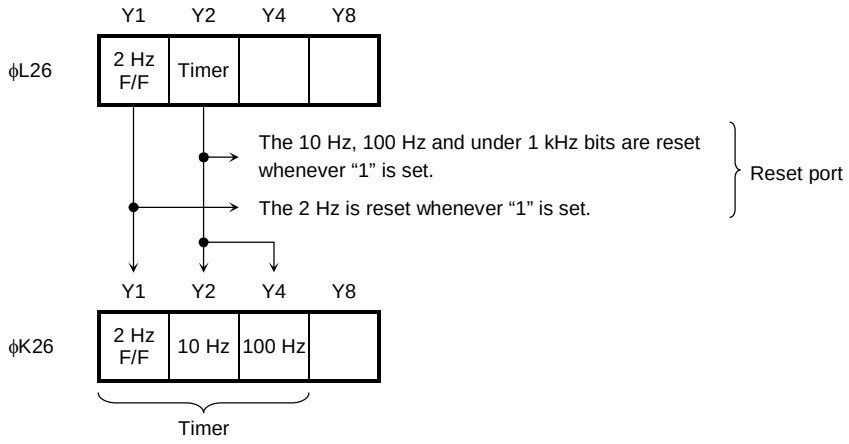
This is set when either Carry or Borrow are issued in the result of calculation instruction execution and is reset if neither of these is issued. The carry F/F is accessed with OUT1/IN1 instructions for which [CN = CH] have been specified. For this reason, evacuation and a return of the carry F/F at the time of interruption can be performed easily. Carry F/F is written in a data memory by IN1 instruction at the time of evacuation, it is evacuated, and the data evacuated by OUT1 instruction is transmitted to carry F/F from a data memory at the time of a return.



○ Timer Port

The timer is equipped with 100 Hz, 10 Hz and 2 Hz F/F bits and is used for counting clock operations and tuning scan mode, etc.

1. Timer Port

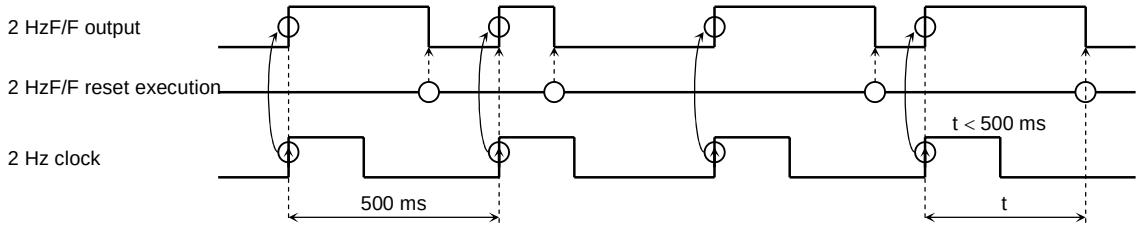


The timer ports are accessedusing an OUT2 instruction for which [CN = 6H] has been specified in the operand.

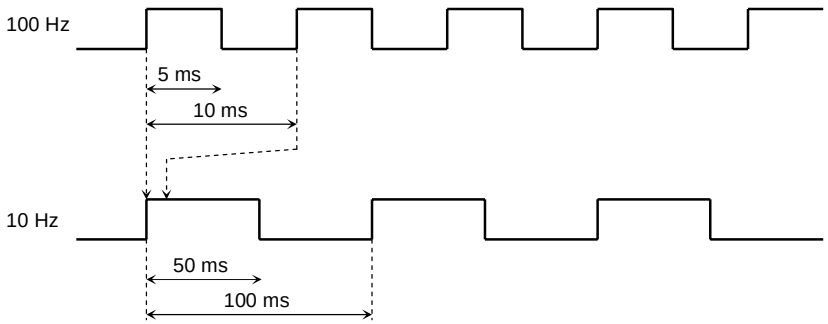
2. Timer Port Timing

The 2-Hz timer F/F is set with the 2 Hz (500 ms) signal and is reset by setting "1" in the 2-Hz F/F of the reset port. This bit is usually used as a clock counter.

The 2-Hz timer F/F can only by reset with the 2-Hz F/F of the reset port, and incorrect counts will be output and correct timers not acquired if not reset within a 500 ms cycle.



The 10 Hz and 100 Hz timers are output to 10 Hz and 100 Hz bits will respective cycles of 100 ms and 10 ms and a pulse of duty 50%. Counters at 1 kHz or below will be reset whenever the reset port's timer bit is set at "1".



○ Output Port (Both as LCD Driver Terminal)

There are 14-output ports of 14 CMOS type. These output ports are used as LCD driver and changed output port by V_{LCD} OFF bit. If V_{LCD} OFF bit is set to "1", this port becomes output port. The output data to output port is used as segment data port-1 (ϕL2E). This data is accessed with OUT2 instruction for which [CN = EH] is specified and is setup by data select port (ϕL2D) for which divides and indirect specified as same as segment data. The data of a specification port to set a segment data port to beforehand is set, and the data port corresponding to it is accessed. The data select port is +1 incremented whenever is accessed segment data port-1 (ϕL2E). For this reason, after setting up a data selection port, it can set up continuously.

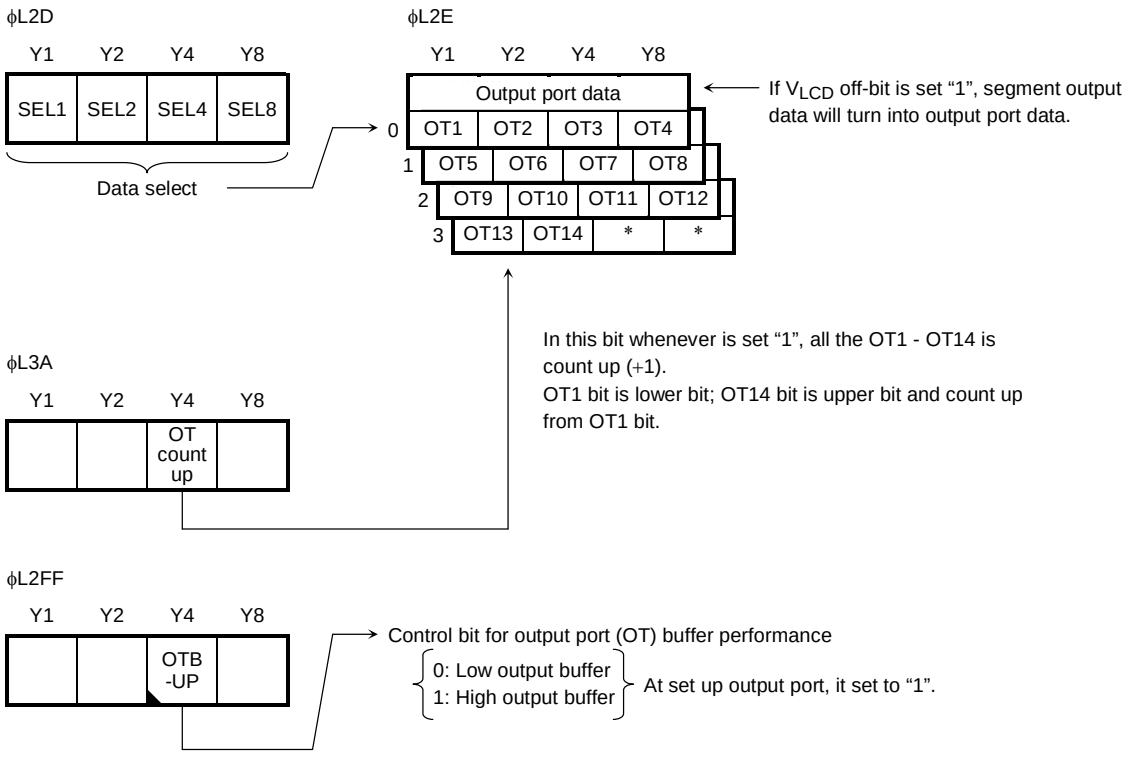
Output data is +1 increment with OT count UP bit by executing one instruction. For this reason, it can be used as an address signal output when using an external memory etc. Output buffer capability can be changed at the time of an output setup. If OTB-UP bit is set "0", it becomes low output buffer (same performance of LCD output driver) and set "1", it becomes high output buffer. During output port setup, this bit is usually set to "1".

The power supply of this output port is used V_{LCD} doubler potential, when using it as an output port, remove for the capacitor of V_{LCD} doubler potential (between C3-C4) and connect with V_{DD} terminal and use V_{LCD} terminal.

Note: Data select port is +1 increment automatically whenever is accessed ϕL2E, ϕL2F, ϕL3B, ϕK3B on I/O map.

Note: If set "0" to OT count UP bit, it's not performed count-up.

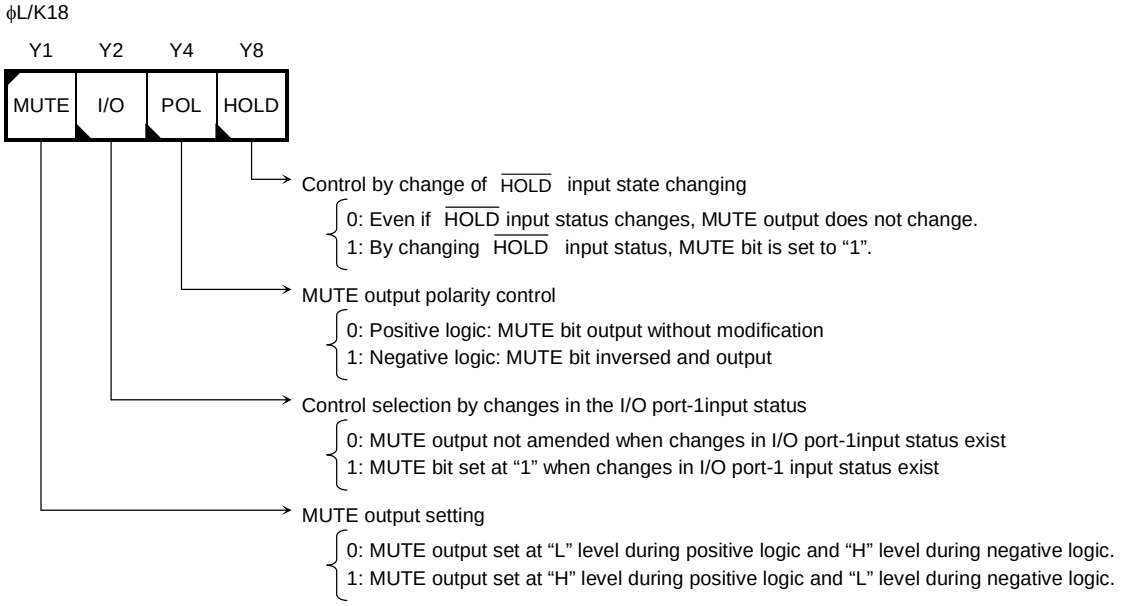
Note: Refer to LCD driver item.



○ MUTE Output

This is a dedicated 1-bit CMOS output port for muting control purposes.

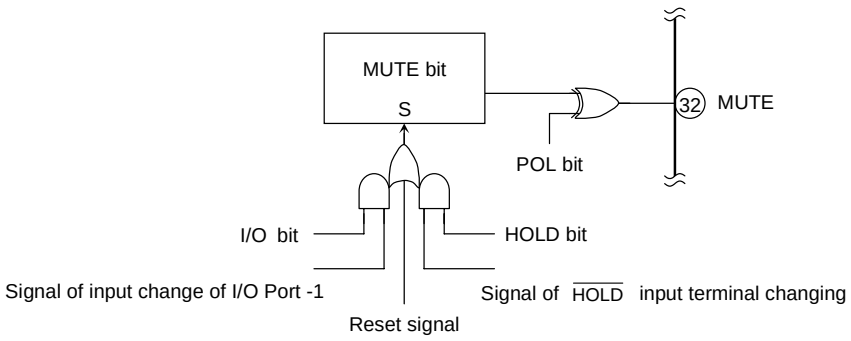
1. MUTE Port



This port is accessed using an OUT1/IN1 instruction for which [CN = 8H] has been specified in the operand. The MUTE output is used for muting control. This function prevents noise from being generated during linear circuit switching when band is performed with the I/O port-1 or $\overline{\text{HOLD}}$ input. This control is set up according to the contents of I/O bit and HOLD bit. POL bit sets up the logic of MUTE output.

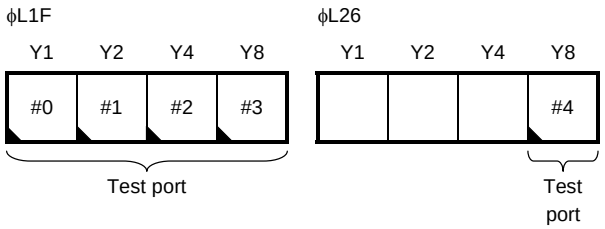
Please set up according to specification.

2. Circuit Composition of MUTE Output



○ Test Port

Access is performed using an OUT1 instruction for which [CN = FH] has been specified in the operand, and an OUT2 instruction for which [CN = 6H] has been specified in the operand. "0" is usually set with the program.



If the following data is set as test port from #3 to #0, various signals can be made to output from MUTE terminal.

#3	#2	#1	#0	Data	MUTE Terminal Output
0	0	0	0	0	MUTE output
0	0	0	1	1	Programmable counter frequency
0	0	1	0	2	Reference frequency
~	~	~	~	~	Prohibition
0	1	0	1	5	CR VCO frequency
~	~	~	~	~	Prohibition
1	1	1	1	F	

○ Application to an Emulator Chip

If TEST terminal is supplied "H" level (test mode), the device operates as an emulator chip. Three kinds of test modes are abailable and can constitute a soft development tool by using three devices.

Radio operation can be checked by the connection between this soft development tool and IC for tuners, performing soft development.

Please refer to TC932AFAG/AFCG software development tool specifications of a development tool.

Absolute Maximum Ratings (Ta = 25°C)

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{DD}	−0.3~4.0	V
Voltage doubler boosting voltage	V_{DB}	−0.3~4.0	V
Output voltage 1 (N-channel open drain)	V_{O1} (*)	−0.3~4.0	V
Output voltage 2 (N-channel open drain)	V_{O2} (*)	−0.3~V_{DB} + 0.3	V
Output voltage 3 (N-channel open drain)	V_{O3} (*)	−0.3~V_{LCD} + 0.3	V
Input voltage	V_{IN}	−0.3~V_{DD} + 0.3	V
Power dissipation	P_D	100	mW
Operating temperature	T_{opr}	−10~60	°C
Storage temperature	T_{stg}	−65~150	°C

*: V_{O1}: P3-0~P3-3 pin
V_{O2}: P5-0~P5-3 pin
V_{O3}: P8-0~P8-3, P9-0~P9-3 pin

Electrical Characteristics (unless otherwise specified, Ta = 25°C, V_{DD} = 1.5 V)

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Range of operating supply voltage	V_{DD1}	—	Under CPU operation (*)	0.9	~	1.8	V
	V_{DD2}	—	Under PLL operation (*)	0.9	~	1.8	
Range of memory retention voltage	V_{HD}	—	Crystal oscillation stopped (CKSTP instruction executed) (*)	0.75	~	1.8	V
Operating current	I_{DD1}	—	PLL operation (VHF mode), at input FMin = 230 MHz	—	6	10	mA
	I_{DD2}	—	Under CPU operation only (PLL off, display turned on, V_{reg} Off)	—	40	80	μA
	I_{DD3}	—	Under CPU operation only (PLL off, display turned on, V_{reg} On)	—	50	—	
	I_{DD4}	—	In Hard wait mode, (PLL off, crystal oscillator operating only)	—	20	40	
	I_{DD5}	—	At Soft wait executed, (PLL off, CPU stopped)	—	30	—	
	I_{DD6}	—	Under CPU accelerated operation, (CR oscillator operation, PLL off, display on)	—	250	500	
Memory retention current	I_{HD}	—	Crystal oscillation stopped (CKSTP instruction executed)	—	0.1	1.0	μA
Crystal oscillation frequency	f_{XT}	—	(*)	—	75	—	kHz
Crystal oscillation start-up time	t_{st}	—	Crystal oscillation f_{XT} = 75 kHz	—	—	1.0	s
CR oscillation frequency	f_{CRW}	—	V_{DD} = 1.1~1.8 V, Ta = −10~60°C	0.8	1.0	1.2	MHz

*: Guaranteed when V_{DD} = 0.9~1.8 V, Ta = −10~60°C

Voltage Doubler Boosting Circuit

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Doubled voltage	V_{DB}	—	GND reference (V_{DB})	—	$V_{DD} \times 2$	—	V
Doubled voltage output current	I_{DB}	—	$V_{OH} = V_{DB} - 0.1$ V (V_{DB})	−50	−200	—	μA
Doubled voltage reference voltage	V_{EE}	—	GND reference (V_{EE})	1.35	1.50	1.65	V
Constant voltage for phase comparator	V_{reg}	—	GND reference (V_{reg}) (*)	1.35	1.50	1.65	V
Constant voltage temperature characteristic	Dv	—	GND reference (V_{EE})	—	−5	—	mV/°C
Power supply output current for phase comparator	I_{reg}	—	$V_{OH} = V_{reg} - 0.1$ V (V_{reg}) (Note 1)	−50	−200	—	μA
Doubled voltage	V_{LCD}	—	GND reference (V_{LCD})	2.7	3.0	3.3	V
Doubled voltage output current	I_{LCD}	—	$V_{OH} = V_{LCD} - 0.1$ V (V_{LCD}) (Note 1)	−50	−200	—	μA

*: Guaranteed when V_{DD} = 0.9~1.8 V, Ta = −10~60°C

Note 1: The “H” level output current of the pin using the V_{reg}/V_{LCD} power supply must not exceed the power supply (doubled voltage: V_{DB}) output current.

Programmable Counter/IF Counter Operating Frequency Range

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
OSCin (VHF mode)	f VHF	—	V_{IN} = 0.1 V_{p-p}, V_{DD} = 0.9~1.8 V (*)	80	~	230	MHz
OSCin (FM mode)	f FM	—	V_{IN} = 0.1 V_{p-p}, V_{DD} = 0.9~1.8 V (*)	60	~	130	MHz
OSCin (HF mode)	f HF1	—	V_{IN} = 0.1 V_{p-p}, V_{DD} = 0.9~1.8 V (*)	3.0	~	30	MHz
	f HF2	—	V_{IN} = 0.1 V_{p-p}, V_{DD} = 0.9~1.8 V (*)	1.0	~	10	
OSCin (LF mode)	f LF	—	V_{IN} = 0.1 V_{p-p}, V_{DD} = 0.9~1.8 V (*)	0.5	~	8	MHz
IFin1, IFin2	f IF	—	V_{IN} = 0.1 V_{p-p}, V_{DD} = 0.9~1.8 V (*)	0.3	~	12	MHz
PSC transfer delay time	tpd	—	C_L = 15 pF, V_{DD} = 1.1~1.8 V (PSC) (*)	—	—	400	ns

*: Guaranteed when V_{DD} = 0.9~1.8 V, Ta = −10~60°C

Programmable Counter/IF Counter Input Amplitude Range

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
OSCin (VHF mode)	V VHF	—	Same as for f VHF (*)	0.1	~	0.6	V_{p-p}
OSCin (FM mode)	V FM	—	Same as for f FM (*)	0.1	~	0.6	V_{p-p}
OSCin (HF mode)	V HF	—	Same as for f HF1~2 (*)	0.1	~	0.6	V_{p-p}
OSCin (LF mode)	V LF	—	Same as for f LF (*)	0.1	~	0.6	V_{p-p}
IFin1, IFin2	V IF	—	Same as for f IF (*)	0.1	~	0.6	V_{p-p}

*: Guaranteed when V_{DD} = 0.9~1.8 V, Ta = −10~60°C

LCD Common Output/Segment Output (COM1~COM4, S1~S18)

Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Output current	"H" level	IOH1	—	V_{LCD} = 3 V, $V_{OH} = V_{LCD} - 0.3$ V (COM1~COM4)	−0.10	−0.20	—	mA
		IOH2	—	V_{LCD} = 3 V, $V_{OH} = V_{LCD} - 0.3$ V (S_1~S_{18})	−0.05	−0.10	—	
	"L" level	IOL1	—	V_{LCD} = 3 V, V_{OL} = 0.3 V (COM1~COM4)	0.10	0.30	—	
		IOL2	—	V_{LCD} = 3 V, V_{OL} = 0.3 V (S_1~S_{18})	0.05	0.15	—	
Output voltage 1/2 level		VBS	—	No load (COM1~COM4)	1.35	1.5	1.65	V

Output Port, I/O Port (OT1~OT14, P8-0~P8-3, P9-0~P9-3)

Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Output current	"H" level	IOH3	—	V_{LCD} = 3 V, $V_{OH} = V_{LCD} - 0.3$ V (Note 2, except I/O port)	−1.5	−3.0	—	mA
	"L" level	IOL3	—	V_{LCD} = 3 V, V_{OL} = 0.3 V	1.5	3.0	—	
Input leak current		ILI	—	$V_{IH} = V_{LCD}$, V_{IL} = 0 V (P8-0~P8-3, P9-0~P9-3)	—	—	±1.0	μA
Input voltage	"H" level	V_{IH1}	—	(P8-0~P8-3, P9-0~P9-3)	$V_{DD} \times 0.8$	~	V_{DD}	V
	"L" level	V_{IL1}	—	(P8-0~P8-3, P9-0~P9-3)	0	~	$V_{DD} \times 0.2$	

Note 2: The "H" level output current is the current when the pin power supply is fixed.
Make sure that pins using the V_{reg}/V_{LCD} power supply do not exceed the power supply (doubled voltage: V_{DB}) output current.

I/O Port (P1-0~P5-3)

Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Output current	"H" level	IOH4	—	V_{DD} = 1.5 V, V_{OH} = V_{DD} − 0.2 V (I/O port P2, P4)	−0.4	−0.8	—	mA
		IOH5	—	V_{DD} = 0.9 V, V_{OH} = V_{DD} − 0.2 V (I/O port P2, P4)	−0.04	−0.2	—	
	"L" level	IOL4	—	V_{DD} = 1.5 V, V_{OL} = 0.2 V (except I/O port P3)	0.5	1.0	—	
		IOL5	—	V_{DD} = 0.9 V, V_{OL} = 0.2 V (except I/O port P3)	0.1	0.3	—	
		IOL6	—	V_{DD} = 0.9~1.8 V, V_{OL} = 0.2 V (I/O port P3)	1.0	2.0	—	
Input leak current		ILI	—	V_{IH} = V_{DD}, V_{IL} = 0 V (I/O port P1, P2, P4)	—	—	±1.0	μA
			—	V_{IH} = 3.6 V, V_{IL} = 0 V (I/O port P3)	—	—	±1.0	
			—	V_{IH} = V_{DB}, V_{IL} = 0 V (I/O port P5)	—	—	±1.0	
Input voltage	"H" level	V_{IH2}	—	except I/O port 3	V_{DD} × 0.8	~	V_{DD}	V
		V_{IH4}	—	I/O port 3	V_{DD} × 0.8	~	3.6	
	"L" level	V_{IL2}	—	—	0	~	V_{DD} × 0.2	
Input pull-down resistor		RIN1	—	When P1-0~P1-3 are set to pull-down or pull-up	30	60	120	kΩ
SCK clock external input frequency		f_{SIO}	—	When I/O port P3-3 are set to serial clock input	—	—	200	kHz

MUTE Output

Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Output current	"H" level	IOH4	—	V_{DD} = 1.5 V, V_{OH} = V_{DD} − 0.2 V	−0.4	−0.8	—	mA
		IOH5	—	V_{DD} = 0.9 V, V_{OH} = V_{DD} − 0.2 V	−0.04	−0.2	—	
	"L" level	IOL4	—	V_{DD} = 1.5 V, V_{OL} = 0.2 V	0.5	1.0	—	
		IOL5	—	V_{DD} = 0.9 V, V_{OL} = 0.2 V	0.1	0.3	—	

$\overline{\text{HOLD}}$, INTR1/2, IN1/2 Input Port, $\overline{\text{RESET}}$ Input

Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Input leak current		ILI	—	V_{IH} = V_{DD}, V_{IL} = 0 V	—	—	±1.0	μA
Input voltage	"H" level	V_{IH3}	—	—	VDD × 0.8	~	V_{DD}	V
	"L" level	V_{IL3}	—	—	0	~	V_{DD} × 0.2	

Note 2: The "H" level output current is the current when the pin power supply is fixed.
Make sure that pins using V_{reg}/V_{LCD} power supply do not exceed the power supply (doubled voltage: V_{DB}) output current.

A/D Converter (ADin1~ADin4)

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Analog input voltage range	VAD	—	—	0	~	V_{DB}	V
Resolution	VRES	—	—	—	6	—	bit
Conversion total error	—	—	—	—	±0.5	±1.0	LSB
Analog input leak	ILI	—	$V_{DD} = V_{DB}$, $V_{IH} = V_{DB}$, $V_{IL} = 0$ V	—	—	±1.0	μA

DO Output

Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Output current	"H" level	IOH4	—	$V_{reg} = 1.5$ V, $V_{OH} = V_{reg} - 0.2$ V (Note 2)	−0.4	−0.8	—	mA
	"L" level	IOL4	—	$V_{reg} = 1.5$ V, $V_{OL} = 0.2$ V	0.5	1.0	—	
Output off leak current		ITL	—	$V_{DD} = 1.5$ V, $V_{TLH} = 1.5$ V, $V_{TLL} = 0$ V	—	—	±100	nA

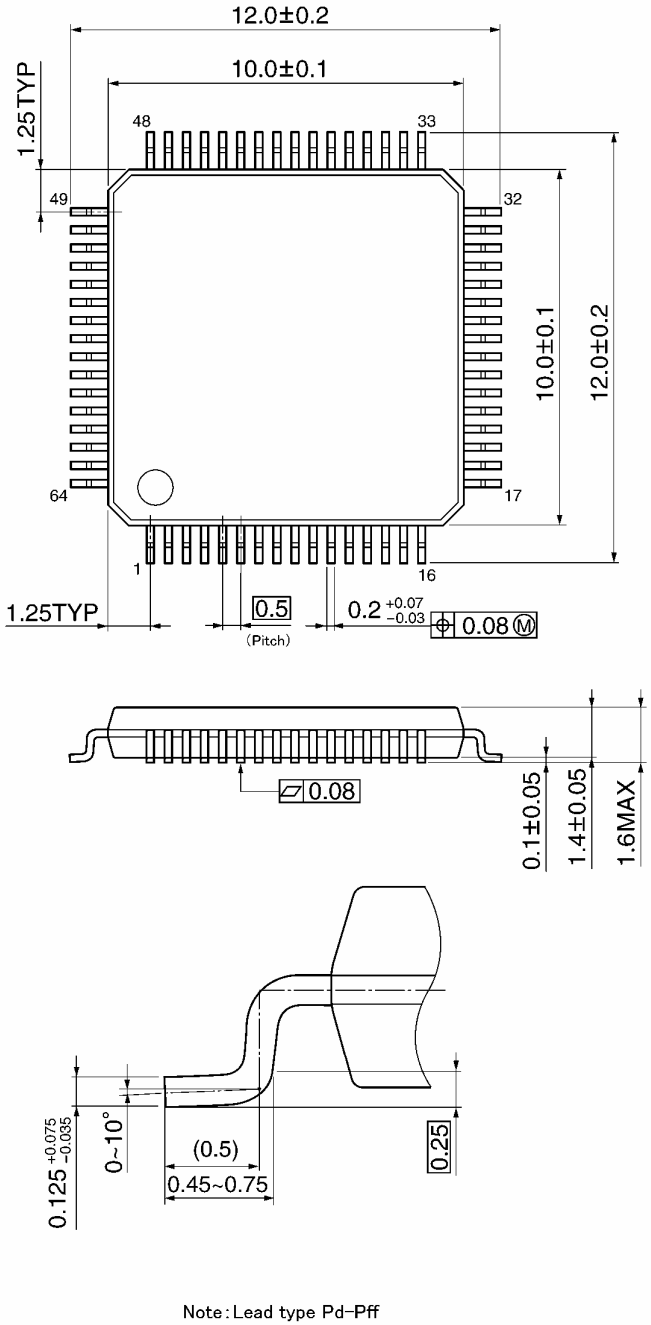
Others

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Input pull-down resistance	RIN2	—	(TEST)	5	10	30	kΩ
XIN amp. feedback resistance	RfXT	—	(XIN-XOUT)	—	20	—	MΩ
XOUT output resistance	ROUT	—	(XOUT)	—	4	—	kΩ
Input amp. feedback resistance	Rf_{IN1}	—	VHF mode, FM mode (OSCin)	100	200	400	kΩ
		—	HF mode, LF mode (OSCin)	300	600	1200	
	Rf_{IN2}	—	(IFin1, IFin2)	300	600	1200	

Note 2: The "H" level output current is the current when the pin power supply is fixed.
Make sure that pins using V_{reg}/V_{LCD} power supply do not exceed the power supply (doubled voltage: V_{DB}) output current.

Package Dimensions

LQFP64-P-1010-0.50E Unit: mm

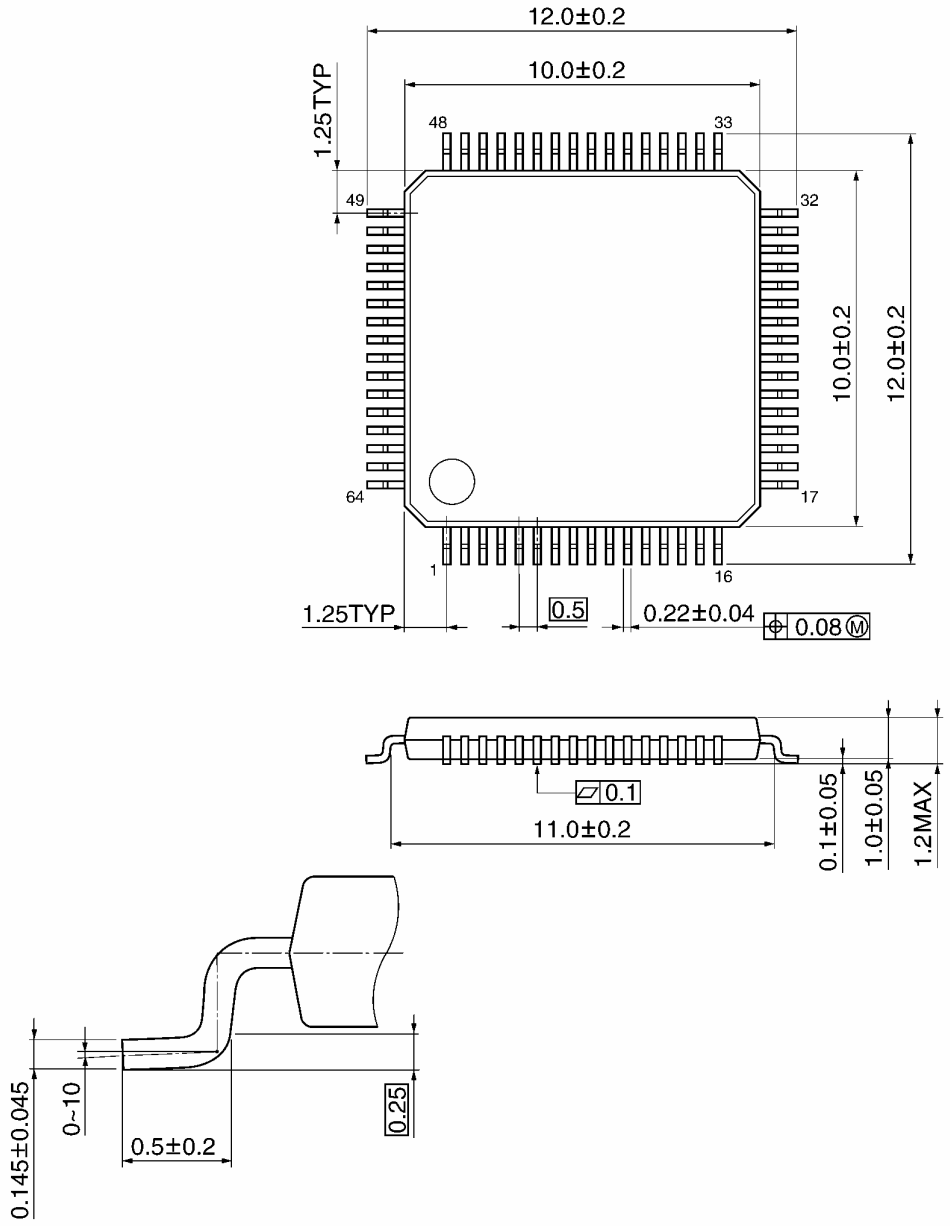


Note : Lead type Pd-Pff

Weight: 0.32 g (typ.)

Package Dimensions

TQFP64-P-1010-0.50C Unit: mm



Note: Lead type SN-Ag

Weight: 0.26 g (typ.)

About solderability, following conditions were confirmed

- Solderability

  (1) Use of Sn-37Pb solder Bath
  - solder bath temperature = 230°C
  - dipping time = 5 seconds
  - the number of times = once
  - use of R-type flux

  (2) Use of Sn-3.0Ag-0.5Cu solder Bath
  - solder bath temperature = 245°C
  - dipping time = 5 seconds
  - the number of times = once
  - use of R-type flux

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060116EBA

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