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TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

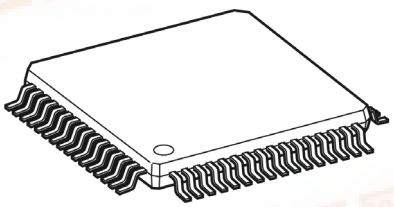
TC9349AFG

Single-Chip DTS Microcontroller (DTS-21)

The TC9349AFG is a single-chip DTS microcontroller for portable audio incorporating a 30 MHz prescaler, PLL, and LCD driver. In addition to an IF counter, serial interface and buzzer function, the device incorporates an interrupt function, timer counter, pulse counter, electronic volume function and A/D converter

The device also supports selection of 1/4-duty 1/2 bias or 1/4-duty 1/3 bias for the LCD driver, while a built-in 3 V voltage doubler boosting circuit implements stable operation of the LCD monitor.

The power supply voltage ranges from 0.9 V to 1.8 V. Due to its low-current consumption, the device is suitable for use in digital tuning systems in portable equipment such as headphone stereos.



LQFP64-P-1010-0.50E

Weight: 0.32 g (typ.)

Features

- CMOS DTS microcontroller LSI with built-in prescaler PLL and LCD driver
- Operating voltage range: VDD = 0.9 to 1.8 V (typ.: 1.5 V)
- Current dissipation: With CPU in operation: IDD = 150 μA (typ.)
  With PLL in operation: IDD = 1 mA (typ. At inputting OSCin = 30 MHz)
- Operating temperature range: Ta = –10 to 60°C
- Program memory (ROM): 16-bit × 8192 steps
- Data memory (RAM): 4-bit × 512 words
- Oscillator frequency: Crystal oscillator: 75 kHz (crystal oscillator)
  High-speed oscillator: 300 to 600 kHz (ceramic oscillator or crystal oscillator)
- Instruction execution time: Crystal oscillator: 40 μs
  High-speed oscillator: 5 to 10 μs
- Interrupt: External: 2 system (INTR1, INTR2 pin)
  Internal: 4 system (serial-interface, timer-port, timer-counter, decreased voltage detection)
- Interrupt stack: 4 level × 26 bit G-register, Data select, Carry flag, Data register
- Address stack: 16 level × 13 bit (program counter)
- I/O port: CMOS I/O port: 36 (max)
  N-ch open-drain I/O port: 9 (max)
  Exclusive output port: 2 (max), exclusive input port: 1 (max)
- LCD driver: 1/4 duty, 1/2 bias or 1/4 duty, 1/3 bias: 72 segments (max)
- Serial Interface: 1 system, 2 channel (N-ch open-drain, CMOS I/O port), 3 kinds (3-wired, 2-wired, UART)
- Buzzer: 4 kinds of frequency (1 kHz, 1.56 kHz, 2.08 kHz, 3 kHz),
  4 modes (continuous, single-shot, 10 Hz intermittent, 10 Hz intermittent 1 Hz interval)
- Timer counter: 8 bit, 2 kinds of timer clock (25 kHz, 1 kHz),
  2 modes (timer counter, pulse width measure (INTR1 pin))
- Pulse counter: 8 bit up/down counter
- Electronic volume: 2 channel, 32 step (0 dB to –78 dB, –∞dB)
- A/D converter: 6 bit, 4 channel, conversion time: 240 μs
- Amplifier for LPF: 5.5 V output max. (Tout, Tin)
- DC/DC converter of VT: 2 stage (0.75 V, 1.0 V) voltage detected (VDET)
  15 kinds of doubler clock, 2 types of doubler clock output
  (CMOS output: DDCK2, N-ch output: DDCK1)

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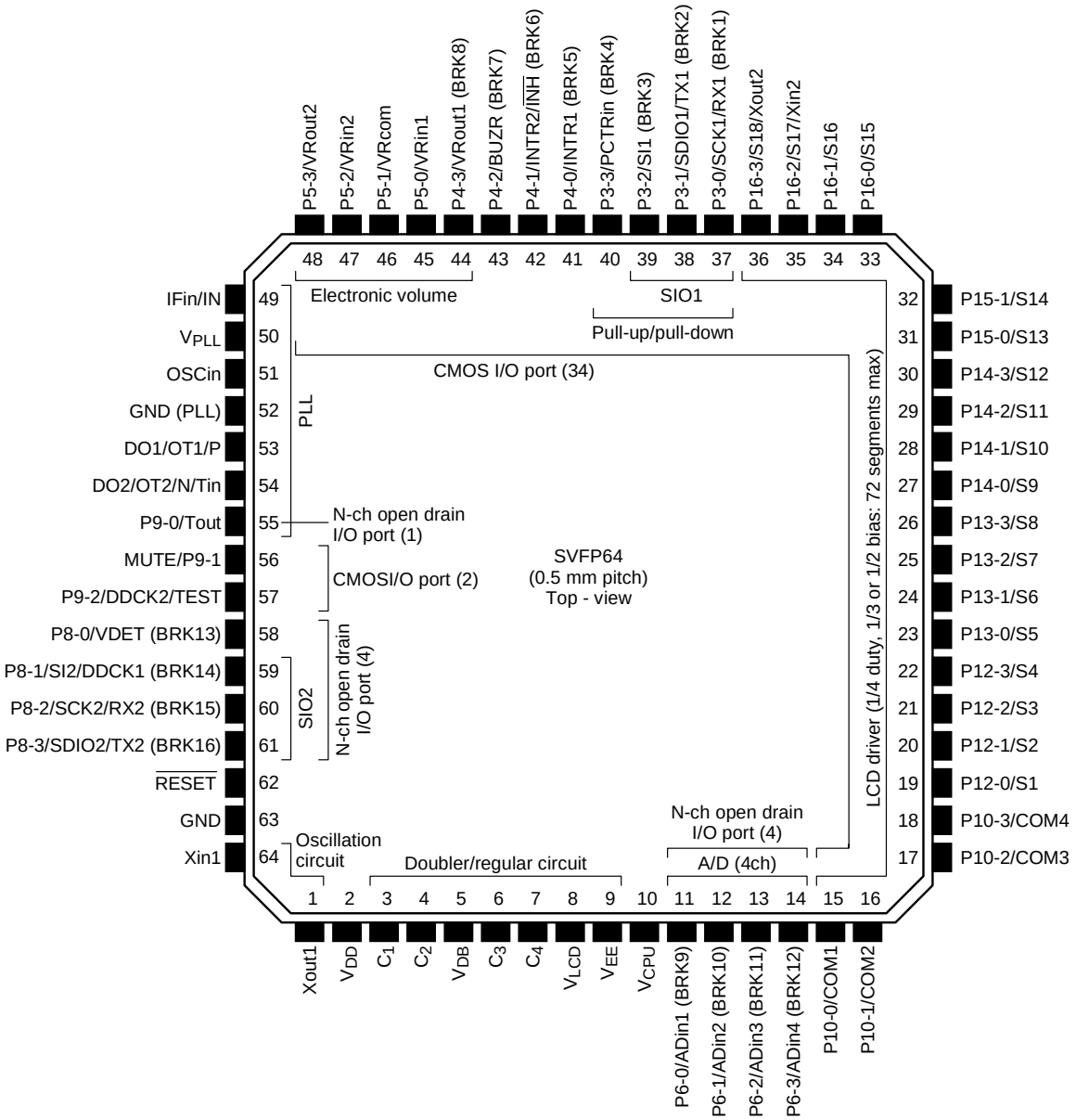
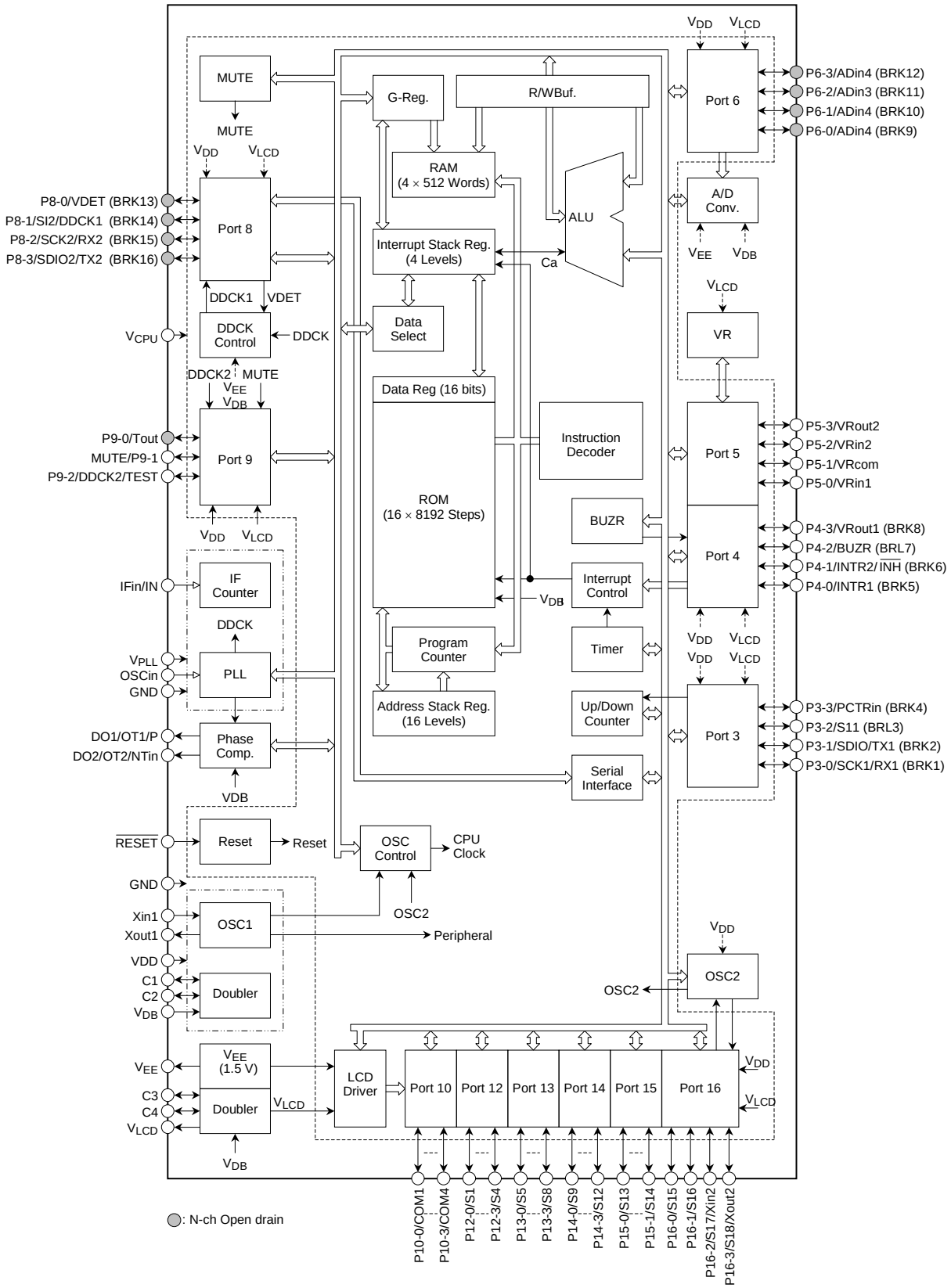
- DC/DC converter for CPU: Charge-pump type
  Two kinds of doubler clock: 75 kHz crystal oscillator,
  high-speed oscillator clock (300 to 600 kHz),
  setting doubler voltage for 3 stages (2.0 V, 2.5 V, 3.0 V)
- Programmable counter: 16-bit HF mode: 1/15 or 16-pulse swallow-type (1 to 30 MHz, Vin = 0.1Vp-p (min))
  LF mode: 12 bit direct divider type (0.5 to 4 MHz, Vin = 0.1Vp-p (min))
- Reference frequency: 10 kinds (1 kHz, 1.3889 kHz, 1.5625 kHz, 2.7778 kHz, 3 kHz, 3.125 kHz, 5 kHz, 6.25 kHz, 12.5 kHz, 25 kHz)
- Phase comparator: 2 (max), setting for “H”/“L” level, High-impedance and built-in output resistor by program. two units (max); “H”/“L” level-setting, high-impedance setting, and built-in output resistor setting (0 kΩ, 5 kΩ, 50 kΩ, 100 kΩ) possible through programming (DO1/DO2); automatic change of output resistor according to phase difference is possible through programming. (DO2)
- General-purpose IF counter: 20 bits, 0.03 to 12 MHz, Vin = 0.1Vp-p (min)
- Backup function: three modes: clock stop (stoppage of crystal oscillator); hard wait, (crystal oscillator operation only); soft wait (CPU intermittent operation)
- Reset function: Built-in power-on reset circuit
- Decreased voltage detection function: Voltage detection is possible in 25 mV steps in the range VDD = 0.850 V to 1.225 V. Decreased voltage detection enables selection of the CPU stop function.
- Package: QFP-64 (0.5 mm in pitch, 1.4 mm thick)
- EEPROM product: TC93E49FG

Note: This product is sensitive to electrostatic discharge. Handle with care.

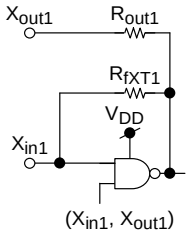
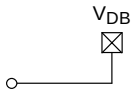
Pin Assignment

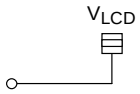
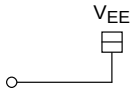
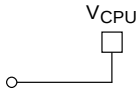
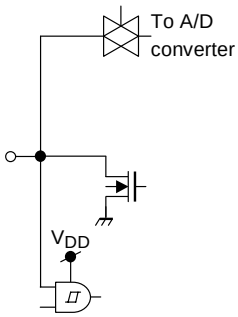


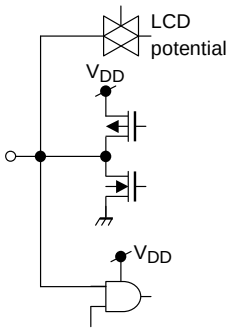
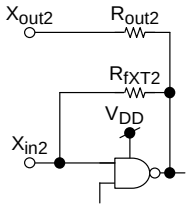
Block Diagram

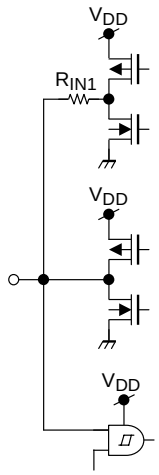


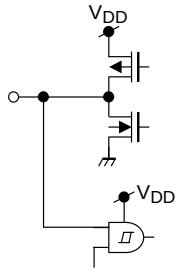
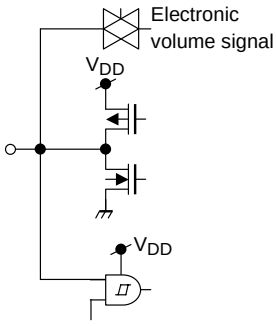
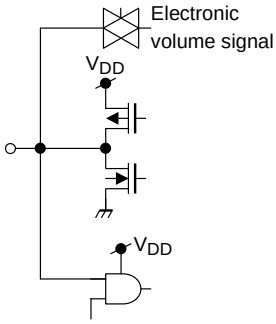
Description of Pin Functions

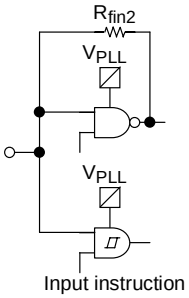
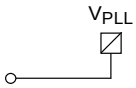
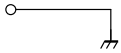
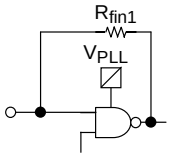
PIN No.	Symbol	Pin Name	Function and Operation	Remarks
64	Xin1	Crystal oscillator pin	Crystal oscillator pins. A reference 75 kHz crystal resonator is connected to the Xin1 and Xout1 pins.	
1	Xout1			
68	GND	Power-supply pins	Power supply pin for the crystal oscillator and doubler circuit for the CPU (V_{DB}). Normally, V_{DD} = 0.9 to 1.8 V is applied. V_{DD} potential is detected in the 0.850 V to 1.225 V range in 25 mV steps using the decreased voltage detection circuit. If V_{DD} potential falls below the voltage being set, the CPU can be stopped to prevent incorrect operation. Note: After reset, the voltage set for the decreased voltage detection is V_{DD} = 0.85 V. CPU stop function is enabled.	
2	VDD			
3	C1	Doubler output pins for CPU	Doubler output pins for CPU. The doubler system is the charge-pump system. When a doubler clamp is permitted, a voltage of 2.0 V, 2.5 V or 3.0 V can be selected. A doubler clock can select either one of 75 kHz, 37.5 kHz or high-speed oscillator clock. Usually, the V_{DB} pin connected to the capacitor for stabilization (0.1 μF, 10 μF typ.) supplies voltage for the power supply of the CPU only (V_{CPU}). The V_{DB} potential is supplied to the power supply of the A/D converter, and a 1.5 V constant-voltage circuit (V_{EE}). The voltage is doubled by the doubler capacitor between C1 and C2 (0.47 μF typ.). When the doubler clamp is enabled, the voltage is doubled below the voltage being set. Note: During reset or execution of the clock stop instruction, the V_{DB} pin is set to V_{DD} level. The LX pin is L level for CMOS output, and at high impedance for open-drain output.	—
4	C2			—
5	VDB			

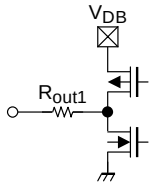
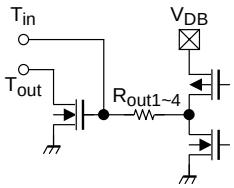
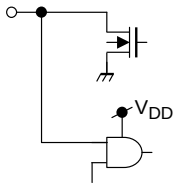
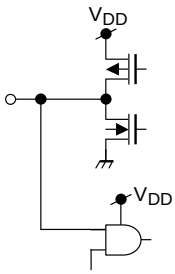
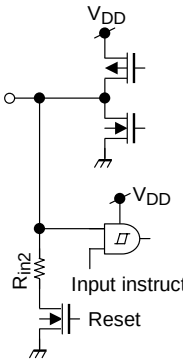
PIN No.	Symbol	Pin Name	Function and Operation	Remarks
6	C3	Doubler output pin for LCD driver	Doubler output pin for the LCD driver. The VLCD pin doubles the VEE pin voltage to 3 V using the voltage doubler capacitance between C3 and C4. The doubled VLCD voltage is supplied to the I/O port, the power supply of the LCD driver, and the electronic volume power supply. Usually, the stabilizing capacitor (0.1 μF typ.) is connected between the VLCD pin and GND. The voltage doubler capacitor (0.1 μF typ.) is connected between C3 and C4. Note: During reset or execution of a clock stop instruction, the VLCD pin is set to the VCPU power supply level.	—
7	C4			—
8	VLCD			
9	VEE	Constant-voltage output pin	Constant-voltage output pin. The VEE pin outputs 1.5 V (typ.) constant-voltage power supply. The VEE potential is used for the voltage doubler for the CPU, the clamp function of the DC/DC converter and the reference voltage of the A/D converter. The stabilizing capacitor (0.47 μF typ.) is connected to the VEE pin. Note: During reset or execution of the clock stop instruction, the VEE pin is at high impedance.	
10	VCPU	CPU power supply pin	CPU power supply pin. Normally, 1.2 to 3.6 V is applied. When memory backup is required, VDB potential is applied to this pin and this pin's potential is held. In backup state (at execution of the CKSTP instruction), current dissipation drops (0.5 μA or less), and the power supply voltage can be reduced to 0.75 V. If voltage is applied to this pin, the device system is reset and the program starts from address "0" (power-on reset). Note: To operate the power-on reset, the power supply should start up in 10 to 100 ms. Note: To be used with VCPU ≤ VLCD.	
11~14	P6-0/ADin1 (BRK9) ~ P6-3/ADin4 (BRK12)	I/O port 6 /AD analog input	4-bit N-ch open-drain I/O ports, allowing input and output to be programmed in 1-bit units. If the ports are set as the input state of an I/O port, these can be set to break pins. The backup mode can be released by changing the input state of the break pin in the backup mode. I/O ports are N-ch open-drain output. Up to the V_{DB} voltage can be applied to the AD input pins. Pins P6-0 to P6-3 can also be used for analog input to the built-in 6-bit, 4-channel A/D converter. The conversion time of the built-in A/D converter using the successive comparison method is 240 μs. The necessary pin can be programmed to A/D analog input in 1-bit units. Up to the doubled voltage VDB (VDD × 2) can be input as the A/D input voltage.	

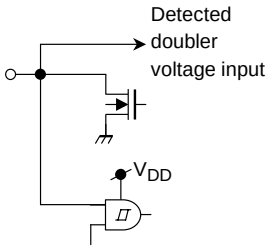
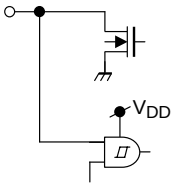
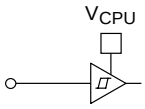
PIN No.	Symbol	Pin Name	Function and Operation	Remarks
15 ~ 18	P10-0/COM1 ~ P10-3/COM4	I/O port 10 /LCD common output	22-bit CMOS I/O ports, allowing input and output to be programmed in 1-bit units. It can be set as LCD driver output through programming. Through a matrix with pins COM1 to COM4 and S1 to S18, a maximum of 72 segments can be displayed. When the LCD OFF bit is set to “0”, all of 8 pins of P10-0 to P12-3 become the LCD output of COM1 to COM4 and S1 to S4. Other LCD driver pins (S5 to S18) can be set to the LCD driver output for every pin. Either of two drive systems can be selected: 1/4 duty1/2 bias system (frame frequency: 62.5 kHz) or 1/4 duty 1/3 bias system (frame frequency: 125 kHz). When 1/2 bias system is set, common output is VLCD, 1/2 VLCD and GND, and segment output is VLCD and GND. When 1/3 bias system is set, common output and segment output are VLCD, 1/3 VLCD, 2/3 VLCD and GND. If “1” is set to DISP OFF bit, common output is non-selected waveform and LCD display are all switched off.	 Input instruction
19 ~ 22	P12-0/S1 ~ P12-3/S4	I/O port 12 /LCD segment output		
23 ~ 26	P13-0/S6 ~ P13-3/S8	I/O port 13 /LCD segment output		
27 ~ 30	P14-0/S9 ~ P14-3/S12	I/O port 14 /LCD segment output		
31 ~ 32	P15-0/S13 / P15-1/S14	I/O port 15 /LCD segment output	Pins P16-2 and P16-3 can be set to the high-speed oscillation pins Xin2 and Xout2 through programming. A 300-600 kHz ceramic or crystal oscillator is connected to Xin2 and Xout2 pins. This oscillation clock can be changed to CPU operation clock for high-speed CPU operation. During execution of the clock stop instruction, oscillation stops. Note: When changing the CPU clock to a high-speed oscillator clock, do so 100 ms or more after the high-speed oscillator is enabled.	 (X_{in2}, X_{out2})
33 ~ 36	P16-0/S15 /Xin2 ~ P16-3/S18 /Xout2	I/O port 16 /LCD segment output /High speed oscillator		

PIN No.	Symbol	Pin Name	Function and Operation	Remarks
37 38 39 40	P3-0/SCK1 /RX1 (BRK1) P3-1/SDIO1 /TX1 (BRK2) P3-2/SI1 (BRK3) P3-3/PCTin (BRK4)	I/O port 3 /Serial clock input/ output 1/UART input 1 /Serial data input/ output 1/UART output 1 /Serial data input 1 /Pulse counter input	4-bit CMOS I/O Port, allowing input and output to be programmed in 1-bit units. When the I/O port is set as input, the pull-up/pull-down state can be programmed in 1-bit units. If set as the input state of an I/O port and a backup release enable state, the backup state can be released by changing input state in the clock stop and the wait modes. Pins P3-0 to P3-2 are used as input/output pins of a serial interface circuit. The serial interface circuit corresponds to 2-wired, 3-wired and UART types. Serial clock edge, serial clock input/output and clock frequency are selectable, facilitating the control of various LSIs and communication between controllers. When interruption of a serial interface circuit is permitted, interruption occurs and a program is jumped to the 3rd address after the serial interface operation is completed. The P3-3 pin is used as 8-bit pulse counter input PCTRin. Since it is possible to select either or both of the rising edge and falling edge of the input pin, as well as count-up or count-down, the pin can be used as an input to a tape count.	 Input instruction Release enables

PIN No.	Symbol	Pin Name	Function and Operation	Remarks
41 42 43	P4-0/INTR1 (BRK5) P4-1/INTR2 $\overline{\text{INH}}$ (BRK6) P4-2/BUZR (BRK7)	I/O port 4 /External interrupt input 1 /External interrupt input 2 /PLL inhibit input /Buzzer output	8-bit CMOS I/O Port, allowing input and output to be programmed in 1-bit units. When P4-0 to P4-3 ports are set as the input and backup release enable states, the backup state in the clock stop and wait modes can be released by changing input state. Pins P4-0 and P4-1 are also used as external interrupt input INTR1 and INTR2. When external interrupt is enabled and a 3-clock pulse of CPU (40 μs: using 75 kHz oscillator) or longer is input to the INTR1 or INTR2 pin, an interrupt is generated and a program jumps to the 1st or 2nd address. For input interrupt, input logic or rising/falling edge can be selected for each pin. The signal input from the INTR1 pin can measure the pulse width using the 8-bit internal timer. The signal can be used to detect a remote control signal. The P4-1 pin is used as the PLL inhibit input $\overline{\text{INH}}$. If the $\overline{\text{INH}}$ pin is set to the PLL inhibit enable state, the PLL is stopped during "L" level of the $\overline{\text{INH}}$ pin. The P4-2 pin is used as the buzzer output. For the buzzer output it is possible to select 4 frequencies, 1/1.56/2.08/3 kHz, with 4 modes: continuous output, single-shot output, 10-Hz intermittent output, and 10-Hz intermittent 1-Hz interval output. Pins P4-3 and P5-0 to P5-3 are used as input/output pins for electronic volume. There are two electronic volume channels. An I/O port or electronic volume is selectable for every channel. Attenuation can be controlled from 0 dB to –78 dB and ∞ dB in 32 steps.	 Input instruction Release enables (P4-0 to P4-2)
44	P4-3/VRout1 (BRK8)	I/O port 4 /Electronic volume output1		 Input instruction Release enables (P4-3)
45 46 47 48	P5-0/VRin1 P5-1/VRcom P5-2/VRin2 P5-3/VRout2	I/O port 5 /Electronic volume input1 /Electronic volume reference voltage input /Electronic volume input 2 /Electronic volume output 2		 Input instruction (P5-0 to P5-3)

PIN No.	Symbol	Pin Name	Function and Operation	Remarks
49	IFin/IN	IF signal input /Input port	IF signal input pin. The input frequency is between 0.03 and 12 MHz. A built-in input amp and C coupling allow small-amplitude operation. The IF counter can store 20-bit data in memory. In Manual mode, gate On/Off control can be performed using an instruction. The input pin is used as an input port (IN port). In this case, the pin is for CMOS input, so that input clocks can be counted using the IF counter. Note: When a pin is set to IF input, the input is at high impedance in PLL-off mode. Note: Since the V_{PLL} power supply is used in this circuit, an input state cannot be read when the V_{PLL} power supply is in the OFF state.	
50	VPLL	PLL Power supply pin	Pin to which power is applied for the PLL prescaler. Normally, the supply voltage to be applied is from 0.9 to 1.8 V. Current dissipation becomes low in PLL-off mode. Usually, the pin is connected to the VDD	
52	GND (PLL)			
51	OSCin	Local oscillation signal input	Programmable counter input pin. It is possible to select the pulse-swallow type (HF mode) or the direct divide type (LF mode) through programming. The local oscillation output of 1 to 30 MHz is input in the HF mode; 0.5 to 4 MHz in the LF mode. A built-in input amp and C coupling allow small-amplitude operation. Note: The input is at high impedance in PLL-off mode.	

PIN No.	Symbol	Pin Name	Function and Operation	Remarks
53 54	DO1/OT1/P DO2/OT2/N /Tin	Phase comparator output /output port /P output /Tr. Input for LPF	PLL phase comparator output pins. Tristate output: When the program counter divider output is higher than the reference frequency, High level is output; when the output is lower, Low level; and when they match, high impedance. The doubler voltage V_{DB} is used for phase comparator power supply. The V_{DB} power supply potential is output for High level. The DO1 and DO2 pins incorporate 3 types of output resistance (5 kΩ, 50 kΩ, 100 kΩ), which can be changed for each pin. The DO2 pin can change output resistance automatically according to the phase difference of the PLL. Therefore, lock-up time is improved. The DO2 pin can be programmed to high-impedance or as an output port (OT1, OT2). The phase comparator charge pump control signal (P/N), which is used to configure an external charge pump, can be output from the DO1/2 pin. If the phase comparator charge pump control signal (P/N) is set, when the program counter divider output is higher than the reference frequency, P/N is output at H/L level; when the output is lower, L/H level; and when they match, L/L level.	 (DO1/OT1/P, DO2/OT2)  (T_{in}, T_{out}) Note: T_{in}/T_{out} setting  Input instruction (P9-0)
55 56 57	P9-0/Tout MUTE/P9-1 P9-2/DDCK2 /TEST	I/O port 9 /Tr. Output for LPF /Mute output /Clock output 2 for doubler /TEST mode input	Pins P9-1 to P9-2 is 2-bit CMOS I/O ports. The P9-0 pin is a 1-bit N-ch open-drain I/O, allowing input and output to be programmed in 1-bit units. The P9-1 pin is used as the MUTE output. The MUTE output is usually used for muting control signal output. The MUTE bit can be set to "1" through change in the input of the I/O port input release (BRK) pin. The MUTE output logic can be set through programming. During system reset ($\overline{RESET}$ = "L"), the P9-2 pin is pulled down and becomes the test mode input. Therefore, the pin is normally used at Low level or in open state during the reset condition. Through programming, it is possible to use the N-ch FET transistor for low path filter amplifiers (5.5 V voltage). As for FET transistors, Tin pin is set as gate input and Tout pin is set as drain output.	 Input instruction (MUTE/P9-1)  Input instruction, Reset (P9-2/DDCK2/TEST)

PIN No.	Symbol	Pin Name	Function and Operation	Remarks
58 ~ 61	P8-0/VDET (BRK13) P8-1/SI2 /DDCK1 (BRK14) P8-2/SCK2 /RX2 (BRK15) P8-3/SDIO2 /TX2 (BRK16)	I/O port 8 /Detected doubler voltage input /Serial data input 2 /Doubler clock output 1 /Serial clock input/ output 2 /UART input 2 /Serial clock input/ output 2 /UART output 2	The port 8 is a 4-bit N-ch open-drain I/O port, allowing control of ON/OFF for an output transistor to be programmed in 1-bit units When an output is set as OFF, the pin can be used as an input port. When the backup release enable state is set, the backup state in the clock stop and wait modes can be released by a change in the input or output pin. The I/O port is N-ch open-drain I/O. Up to 5.5 V can be input to or output from the I/O port. This pin is used to configure the switching regulator for VT. The voltage is doubled by the doubler clock output DDCK1 (P8-1) or DDCK2 (P9-2). The divided voltage is input to the detected doubler voltage VDET pin (P8-0) to control the doubler clock. The DDCK1 output is 5.5V N-ch output. The VT doubled voltage is doubled to 5 V through the use of an external transistor. The DDCK2 output is CMOS output The voltage can be doubled through the use of an external transistor. For the doubler clock, it is possible to select from three types of dividing frequency: crystal oscillator, high-speed oscillator and OSCin input. It is also possible to select through programming the comparator reference potential of the VDET input: either 0.75 V or 1.0 V. Pins P8-1 to P8-3 are used as serial interface circuit (SIO) input/output pins. The serial interface circuit corresponds to 2-wired type, 3-wired type, and UART. Serial clock edge, serial clock input/output, and clock frequency can be selected, facilitating the control of various LSIs and communication between controllers. When interrupts of a serial interface circuit are enabled, an interrupt is generated after serial interface and the program jumps to the 3rd address.	 Input instruction Release enables (P8-0)  Input instruction Release enables (P8-1, P8-3)
62	$\overline{\text{RESET}}$	Reset input	Input pin for system reset signals. The input uses built-in Schmitt circuit. $\overline{\text{RESET}}$ takes place while at Low level; at High level, the program starts from address “0” after 100 ms standby. Normally, if voltage is applied to the VCPU pin, the system is reset (power-on reset).Therefore, this pin should be set to High level during operation.	

Description of Operations

○ CPU

The CPU consists of a program counter, a stack register, an ALU, program memory, data memory, a G-register, a data register, a DAL address register, a carry flip-flop (F/F), a judge circuit, interrupt stack register and an interrupt circuit.

1. Program Counter (PC)

The program counter is a 14-bit binary up-counter used to address program memory (ROM). The program counter is cleared by a system reset and starts from address 0.

The PC is normally incremented by 1 at the execution of each instruction. However, executing a Jump or Call instruction loads the address specified in the operand of the instruction to the PC.

When an instruction with a skip function (the AIS, SLTI, TMT, RNS instructions, etc.) is executed and the result of the instruction satisfies the skip condition, the PC is incremented by 2 and the next instruction is skipped.

When an interrupt is received, the system loads the vector address corresponding to the interrupt.

Note: The program memory (ROM) uses the address range 0000H to 1FFFH. Access to addresses outside this range is prohibited.

Instruction	Contents of program counter (PC)													
	PC13	PC12	PC11	PC10	PC9	PC8	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
JUMP ADDR1	0	← Instruction operand (ADDR1) →												
CALL ADDR2	0	← Instruction operand (ADDR2) →												
DAL ADDR3, (r) (DAL bit = 0)	0	0	0	0	← Instruction operand (ADDR3) →						← Contents of general register (r) →			
DAL (DA) (DAL bit = 1)	← DAL address register (AR) →													
RN, RNS, RNI	← Contents of stack register →													
When interrupt received	← Vector addresses for interrupt →													
Power-on reset, reset by RESET pin	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Interrupt source	Vector address
INTR1 pin	0001H
INTR2 pin / Timer port	0002H
Serial interface / timer port / decreased voltage detection	0003H
Timer counter	0004H

2. Address Stack Register (ASR)

The address stack register consists of 16 × 14 bits. When the subroutine call instruction is executed or an interrupt is processed, this register stores a value equal to the contents of the program counter + 1 (that is, the return address). Executing the return instruction (RN, RNS, RNI) loads the contents of the address stack register to the program counter.

There are 16 stack levels available and nesting occurs for up to 16 levels. The address stack register is mapped to I/O and can be read/written by the input and output instructions.

3. ALU

The arithmetic and logic unit (ALU) has binary 4-bit parallel addition/subtraction functions, logical operation, comparison and multiple bit judge functions. The CPU does not include an accumulator; all operations use the contents of the data memory directly.

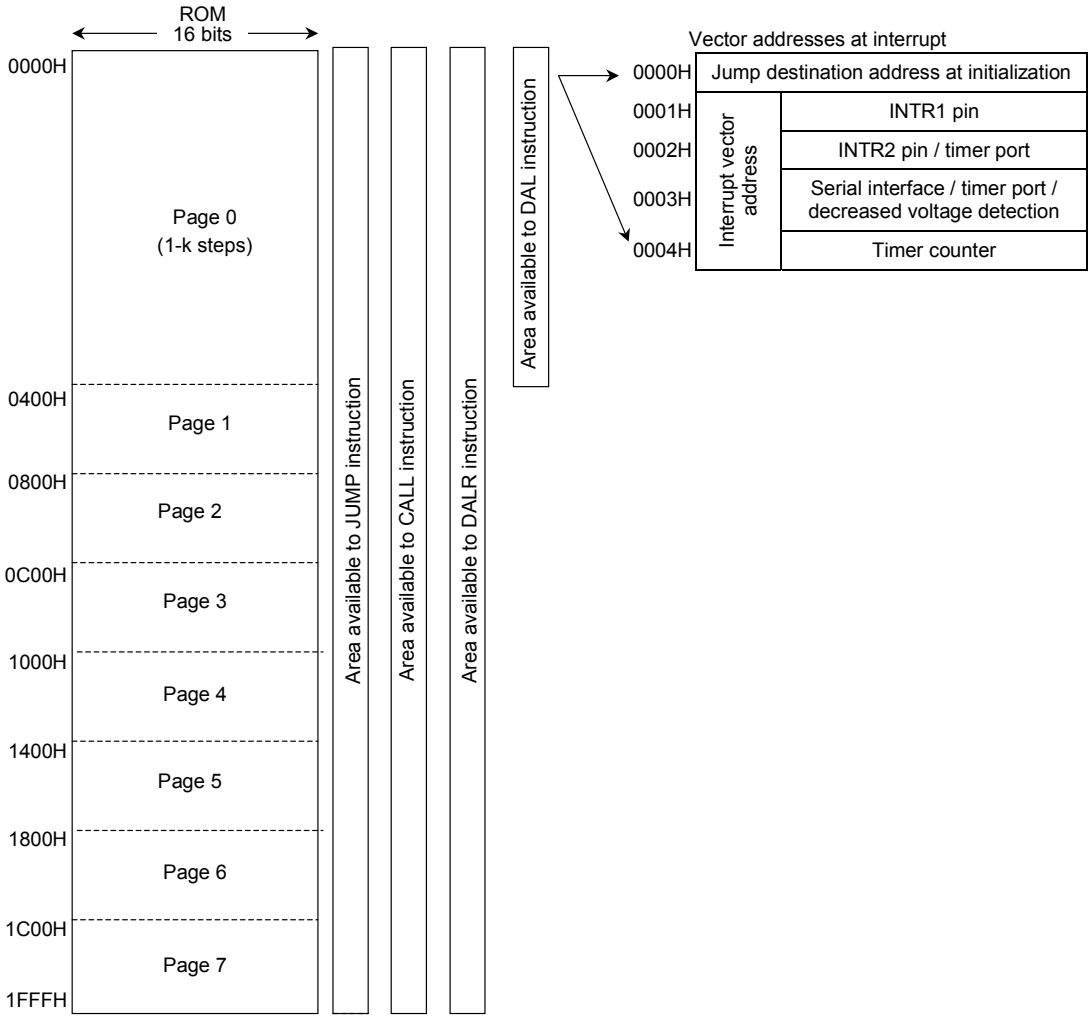
4. Program Memory (ROM)

The program memory consists of 16 bits × 8192 steps and is used for storing programs. The usable address range consists of 8192 steps between addresses 0000H and 1FFFH.

The program memory divides the 8192 into eight separate steps and consists of pages 0 to 7. The JUMP and CALL instructions can be freely used throughout all 8192 steps. When the data refer DAL (DAL instruction) is executed, the program memory addresses 0000H to 03FFH (page 0) are used as data areas; when the indirect refer DAL instruction (DALR instruction) is executed, the program memory addresses 0000H to 0FFFFH (pages 0 to 3) are used as data areas. Execution of these instructions enables their 16-bit contents to be loaded into the data register.

Note: Set the data area in program memory to addresses outside the program loop.

Note: The program counter used to set the program memory has 14 bits and can specify a program memory up to address 3FFF. Do not specify non-existing addresses from 2000H to 3FFFH.



5. Data Memory (RAM)

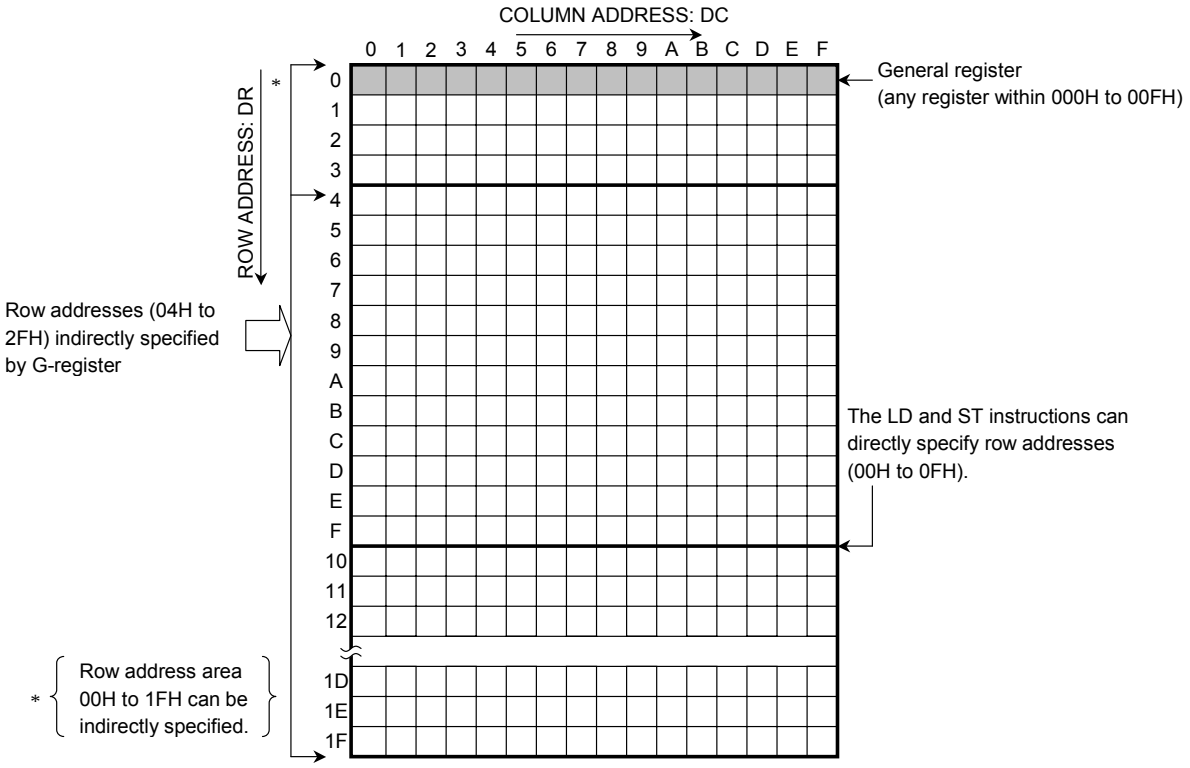
The data memory consisting of 4 bits × 512 words is used to store data. These 512 words are expressed in a row address (4 bits) and column address (4 bits). 348 words (row address = 04H to 1FH) within the data memory are addressed indirectly by the G-register. Therefore it is necessary to specify the row address with the G-register before the data in this area can be processed.

The addresses 00H to 0FH within the data memory are known as general registers, and can be used simply by specifying the relevant column address (4 bit). These sixteen general registers can be used for operations and transfers with the data memory, and may also be used as normal data memories.

Note: The column address (4 bits) that specifies the general register is the register number of the general register.

Note: All row addresses (00H to 1FH) can be specified indirectly with the G-register.

Note: The LD and ST instructions can directly address 256 words of data memory (row address area 00H to 0FH).



6. G-register (G-REG)

The G-register is a 5-bit register used for addressing the row address (DR = 00H to 1FH) of the data memory's 512 words. This register is located on the I/O map and accessed by input-and-output instruction. The 5-bit contents can be directly set by execution of the STIG instruction. (Refer to Register Ports.)

The contents of this register are effective when the MVGD or MVGS instruction is executed, and are not affected through execution of any other instructions. The contents of the G-register are evacuated to the interrupt stack register when an interrupt request is generated, and returned to the G-register during execution of the RNI instruction. (Refer to Interrupt Stack Register.)

7. Data Register (DATA REG)

The data register consists of 16 bits and loads 16 bits of data from any address in the program memory on execution of the DAL instruction. This register is used as one of the ports. The contents of the register are loaded into the data memory in 4-bit units when the IN1 instruction among the I/O instructions is executed. (Refer to Register Ports.) The contents of data register are evacuated to the interrupt stack register when an interrupt request is generated, and returned to the data register during execution of the RNI instruction. (Refer to Interrupt Stack Register.)

8. DAL Address Register (AR)

The DAL address register consists of 14 bits. When the DALR instruction is executed, 16 bits of the data of the program memory on the address specified by the DAL address register is loaded to the data register. The contents in the DAL address register are automatically increased by one whenever the DALR instruction is executed.

The contents of the data register can be transferred to the DAL address register by execution of the MVAR instruction. The DAL address register is located on the I/O map and accessed by input and output instructions.
(Refer to Register Ports.)

9. Carry Flag (Ca Flag)

The carry flag register is set when either Carry or Borrow is issued in the result of calculation instruction execution, and is reset if neither of these is issued. The flag is located on the I/O map and can be accessed by the input and output instructions. (Refer to Register Port.)

The contents of a carry flag are changed by execution of only the addition, subtraction, CLT, CLTC, SHRC or RORC instruction and are not affected by execution of other instructions. The contents of carry flag are evacuated to the interrupt stack register when an interrupt request is generated, and returned to the carry flag during execution of the RNI instruction.
(Refer to Stack Register.)

10. Interrupt Stack Register (ISR)

This register consists of 4 levels and 26 bits. When an interrupt occurs, the contents of the G-register (5 bits), data select (4 bits), carry flag (1 bit) and data register (16 bits) are automatically evacuated to the interrupt stack register. After interrupt processing has been completed, these contents are returned to each register by the RIN instruction. Four levels of stack and nesting are allowed in the interrupt stack register. (Refer to Interrupt Stack Register.)

11. Judge Circuit (J)

This circuit judges the skip conditions when an instruction with the skip function is executed. The program counter is increased by two when the skip conditions are satisfied, and the subsequent instruction is skipped. There are 15 instructions with a wide variety of skip functions available. (Refer to the items marked with a "*" symbol in Instruction Function and Operation Table.)

12. Interrupt Circuit

An interrupt circuit branches to the various vector addresses according to the demands from peripheral hardware and performs different types of interrupt processing. (Refer to Interrupt Function.)

13. Instruction Set Table

A total of 59 instruction sets are available, and all of these are single-word instructions. These instructions are expressed with a 6-bit instruction code.

Upper 2 bits / Lower 4 bits		00		01		10	11	
		0		1		2	3	
0000	0	AI	M, I	TMTR	r, M	JUMP ADDR1	SLTI	M, I
0001	1	AIC	M, I	TMFR	r, M		SGEI	M, I
0010	2	SI	M, I	SEQ	r, M		SEQI	M, I
0011	3	SIB	M, I	SNE	r, M		SNEI	M, I
0100	4	ORIM	M, I	LD	r, M*		TMTN	M, N
0101	5	ANIM	M, I				TMT	M, N
0110	6	XORIM	M, I				TMFN	M, N
0111	7	MVIM	M, I				TMF	M, N
1000	8	AD	r, M	ST	M*, r	CAL ADDR2	IN1	M, C
1001	9	AC	r, M				IN2	M, C
1010	A	SU	r, M				IN3	M, C
1011	B	SB	r, M				OUT1	M, C
1100	C	ORR	r, M	CLT	r, M		OUT2	M, C
1101	D	ANDR	r, M	CLTC	r, M		OUT3	M, C
1110	E	XORR	r, M	MVGD	r, M		DAL	ADDR3, r
1111	F	MVSR	M1, M2	MVGS	M, r		SHRC	M
							RORC	M
							STIG	I*
							SKP, SKPN	
							RN, RNS	
							WAIT	P
							CKSTP	
							XCH	M
							DI, EI, RNI	
							DALR	
							MVAR	
							NOOP	

14. Instruction Function and Operation Table

(Description of the symbols used in the table)

M	Data memory address Normally, an address within 000H to 03FH in the data memory.
M*	Data memory address (256 words) An address within 000H to 0FFH in the data memory. (Effective only during execution of the ST or LD instruction)
r	General register An address within 000H to 00FH in the data memory.
PC	Program counter (14 bits)
ASP	Address stack pointer (14 bits)
ASR	Address stack register (14 bits)
ISP	Interrupt stack pointer (2 bits)
ISR	Interrupt stack register (26 bits)
G	G-register (5 bits)
DATA	Data register (16 bits)
I	Immediate data (4 bits)
I*	Immediate data (6 bits, effective only during execution of the STIG instruction)
N	Bit position (4 bits)
–	All “0”
C	Port code number (4 bits)
CN	Port code number (4 bits)
RN	General register number (4 bits)
ADDR1	Program memory address (13 bits)
ADDR2	Upper 6 bits of program memory address within page 0
AR	DAL address register (14 bit)
Ca	Carry
CY	Carry flag
P	Wait condition
b	Borrow
IN1~IN3	Ports used during execution of the IN1 to IN3 instructions
OUT1 ~ OUT3	Ports used during execution of the OUT1 to OUT3 instructions
( )	Contents of registers or data memory
[ ] C	Contents of the port indicated by the code number C (4 bits)
[ ]	Contents of data memory indicated by the register or data memory
[ ] P	Contents of program memory (16 bits)
IC	Instruction code (6 bits)
*	Command with skip function
DC	Data memory column address (4 bits)
DR	Data memory row address (2 bits)
DR*	Data memory row address (4 bits, effective only during execution of the ST or LD instruction)
(M) b0 ~ (M) b3	Bit data of data memory contents (1 bit)

Instruction Set	Mnemonic	Skip Function	Function	Operation	Machine Language (16 Bits)			
					IC (6 Bits)	A (2 Bits)	B (4 Bits)	C (4 Bits)
Addition instruction	AI M, I		Add immediate data to memory	M ← (M) + I	000000	DR	DC	I
	AIC M, I		Add immediate data to memory with carry	M ← (M) + I + ca	000001	DR	DC	I
	AD r, M		Add memory to general register	r ← (r) + (M)	001000	DR	DC	RN
	AC r, M		Add memory to general register with carry	r ← (r) + (M) + ca	001001	DR	DC	RN
Subtraction instruction	SI M, I		Subtract immediate data from memory	M ← (M) − I	000010	DR	DC	I
	SIB M, I		Subtract immediate data from memory with borrow	M ← (M) − I − b	000011	DR	DC	I
	SU r, M		Subtract memory from general register	r ← (r) − (M)	001010	DR	DC	RN
	SB r, M		Subtract memory from general register with borrow	r ← (r) − (M) − b	001011	DR	DC	RN
Compare instruction	SLTI M, I	*	Skip if memory is less than immediate data	Skip if (M) < I	110000	DR	DC	I
	SGEI M, I	*	Skip if memory is greater than or equal to immediate data	Skip if (M) ≧ I	110001	DR	DC	I
	SEQI M, I	*	Skip if memory is equal to immediate data	Skip if (M) = I	110010	DR	DC	I
	SNEI M, I	*	Skip if memory is not equal to immediate data	Skip if (M) ≠ I	110011	DR	DC	I
	SEQ r, M	*	Skip if general register is equal to memory	Skip if (r) = (M)	010010	DR	DC	RN
	SNE r, M	*	Skip if general register is not equal to memory	Skip if (r) ≠ (M)	010011	DR	DC	RN
	CLT r, M		Set carry flag if general register is less than memory, or reset if not	(CY) ← 1 if (r) < (M) or (CY) ← 0 if (r) ≧ (M)	011100	DR	DC	RN
	CLTC r, M		Set carry flag if general register is less than memory with carry or reset if not	(CY) ← 1 if (r) < (M) + (ca) or (CY) ← 0 if (r) ≧ (M) + (Ca)	011101	DR	DC	RN

Instruction Set	Mnemonic	Skip Function	Function	Operation	Machine Language (16 Bits)			
					IC (6 Bits)	A (2 Bits)	B (4 Bits)	C (4 Bits)
Transfer instruction	LD r, M*		Load memory to general register	r ← (M*)	0101	DR* (4 bits)	DC	RN
	ST M*, r		Store memory to general register	M* ← (r)	0110	DR* (4 bits)	DC	RN
	MVSR M1, M2		Move memory to memory in same row	(DR, DC1) ← (DR, DC2)	001111	DR	DC1	DC2
	MVIM M, I		Move immediate data to memory	M ← I	000111	DR	DC	I
	MVGD r, M		Move memory to destination memory referring to G-register and general register	[(G), (r)] ← (M)	011110	DR	DC	RN
	MVGS M, r		Move source memory referring to G-register and general register to memory	(M) ← [(G), (r)]	011111	DR	DC	RN
	STIG I*		Move immediate data to G-register	G ← I*	111111	I*		0010
	MVAR		Move DATA register data to DAL address register	AR← (DATA)	111111	—	—	1001
I/O instruction	IN1 M, C		Input IN1 port data to memory	M ← [IN1] C	111000	DR	DC	CN
	OUT1 M, C		Output contents of memory to OUT1 port	[OUT1] C ← (M)	111011	DR	DC	CN
	IN2 M, C		Input IN2 port data to memory	M ← [IN2] C	111001	DR	DC	CN
	OUT2 M, C		Output contents of memory to OUT2 port	[OUT2] C ← (M)	111100	DR	DC	CN
	IN3 M, C		Input IN3 port data to memory	M ← [IN3] C	111010	DR	DC	CN
	OUT3 M, C		Output contents of memory to OUT3 port	[OUT3] C ← (M)	111101	DR	DC	CN
Logical Operation instruction	ORR r, M		Logical OR of general register and memory	r ← (r) ∨ (M)	001100	DR	DC	RN
	ANDR r, M		Logical AND of general register and memory	r ← (r) ∧ (M)	001101	DR	DC	RN
	ORIM M, I		Logical OR of memory and immediate data	M ← (M) ∨ I	000100	DR	DC	I
	ANIM M, I		Logical AND of memory and immediate data	M ← (M) ∧ I	000101	DR	DC	I
	XORIM M, I		Logical exclusive OR of memory and immediate data	M ← (M) ∀ I	000110	DR	DC	I
	XORR r, M		Logical exclusive OR of general register and memory	r ← (r) ∀ (M)	001110	DR	DC	RN

Instruction Set	Mnemonic	Skip Function	Function	Operation	Machine Language (16 Bits)			
					IC (6 Bits)	A (2 Bits)	B (4 Bits)	C (4 Bits)
Bit judge instruction	TMTR r, M	*	Test general register bits by memory bits, then skip if all bits specified are true	Skip if r [N (M)] = all "1"	010000	DR	DC	RN
	TMFR r, M	*	Test general register bits by memory bits, then skip if all bits specified are false	Skip if r [N (M)] = all "0"	010001	DR	DC	RN
	TMT M, N	*	Test memory bits, then skip if all bits specified are true	Skip if M (N) = all "1"	110101	DR	DC	N
	TMF M, N	*	Test memory bits, then not skip if all bits specified are false	Skip if M (N) = all "0"	110111	DR	DC	N
	TMTN M, N	*	Test memory bits, then skip if all bits specified are true	Skip if M (N) = not all "1"	110100	DR	DC	N
	TMFN M, N	*	Test memory bits, then not skip if all bits specified are false	Skip if M (N) = not all "0"	110110	DR	DC	N
	SKP	*	Skip if carry flag is true	Skip if (CY) = 1	111111	00	—	0011
	SKPN	*	Skip if carry flag is false	Skip if (CY) = 0	111111	01	—	0011
Subroutine instruction	CALL ADDR2		Call subroutine	ASR ← (PC) 1 and PC ← ADDR2 ASP ←(ASP) + 1	101	ADDR2 (13 bits)		
	RN		Return to main routine	PC ← (ASR) ASP ←(ASR) - 1	111111	10	—	0011
	RNS	*	Return to main routine and skip unconditionally	PC ← (ASR) and skip ASP ←(ASR) - 1	111111	11	—	0011
Jump instruction	JUMP ADDR1		Jump to address specified	PC ← ADDR1	10	ADDR1 (13 bits)		
Interrupt instruction	DI		Reset IMF (Note)	IMF ← 0	111111	00	—	0111
	EI		Set IMF (Note)	IMF ← 1	111111	01	—	0111
	RNI		Return to main routine and set IMF (Note)	PC ← (ASR) PC ← (ASR) – 1 Ca, G, DATA, DATA SELECT ← (ISR) ISP ← (ISP) – 1 IMF ← 1	111111	11	—	0111

Note: The IMF bit is an interrupt master enable flag located on the I/O map. (Refer to Interrupt Functions.)

Instruction Set	Mnemonic	Skip Function	Function	Operation	Machine Language (16 Bits)			
					IC (6 Bits)	A (2 Bits)	B (4 Bits)	C (4 Bits)
Other instructions	SHRC M		Shift memory bits to right direction with carry	0 → (M) b3 → (M) b2 → (M) b1 → (M) b0→ (CY)	111111	DR	DC	0000
	RORC M		Rotate memory bits to right direction with carry	(M) b3 → (M) b2 → (M) b1→ (M) b0 → (CY)	111111	DR	DC	0001
	XCH M		Exchange memory bits mutually	(M) b3 ↔ (M) b0, (M) b2 ↔ (M) b1	111111	DR	DC	0110
	DAL ADDR3, r		Load program in page 0 to DATA register (Note)	DATA ← [ADDR3 + (r)] P in page 0	111110	ADDR3 (6 bits)		RN
	DALR		Load program memory to DATA register referring to DAL address register, and increment DAL address register	DATA ← [(AR)]P AR ← (AR) + 1	111111	—	—	1000
	WAIT P		At P = "0" H, the condition is CPU waiting (soft wait mode) At P = "1" H, all functions except for clock generator enter the waiting state (hard wait mode)	Wait at condition P	111111	P	—	0100
	CKSTP		Clock generator stop	Stop clock generator to MODE condition	111111	—	—	0101
	NOOP		No operation	—	111111	—	—	1111

Note: The lower 4 bits of the 10 bits of program memory specified by the DAL instruction (DAL ADDR2, r) are addressed indirectly by the contents of the general register. The 13 bits of program memory specified by DALR instruction are used for indirect addressing.

Note: The DAL address register (AR) is located on the I/O map. (Refer to Register Ports.)

Note: The DAL or DALR instruction run-time is two machine cycles.

○ I/O Map, Data Select Port (ϕL/K1A)

All the ports within the device are expressed with a matrix of six I/O instructions (OUT1 to 3 instructions and IN1 to 3 instructions) and 4-bit code numbers.

The allocation of these ports is shown on the following page in the form of an I/O map. The ports used in the execution of the various I/O instructions on the horizontal axis of the I/O map are allocated to the port code numbers indicated on the vertical axis. The G-register, data register and DAL bits are also used as ports.

The OUT1 to 3 instructions are specified as output ports, and the IN 1 to 3 instructions are specified as input ports.

Note: The ports indicated by the angled lines on the I/O map do not actually exist within the device. When data is output to a non-existing output port by execution of the output instruction, the contents of other ports and data memories are not affected. When a non-existing input port is specified by execution of an input instruction, the data loaded from the data memory assumes "don't care" status.

Note: The output ports marked with an asterisk (*) on the I/O map are not used. Data output to these ports assumes "don't care" status.

Note: The Y1 contents of the ports expressed in 4 bits correspond to the LSB and the Y8 contents correspond to the MSB in the data memory.

The ports specified with the six I/O instructions and code number C are coded in the following manner.

ϕ [K/L] m n (o) (Pp)

- (Pp): Pages (1 to 3)
- (o): Contents of selected port (indirectly specified data, 0 to F (HEX))
- n: I/O instruction operand CN (0 to F (HEX))
- m: The six I/O instructions are coded with digits 1 to 3

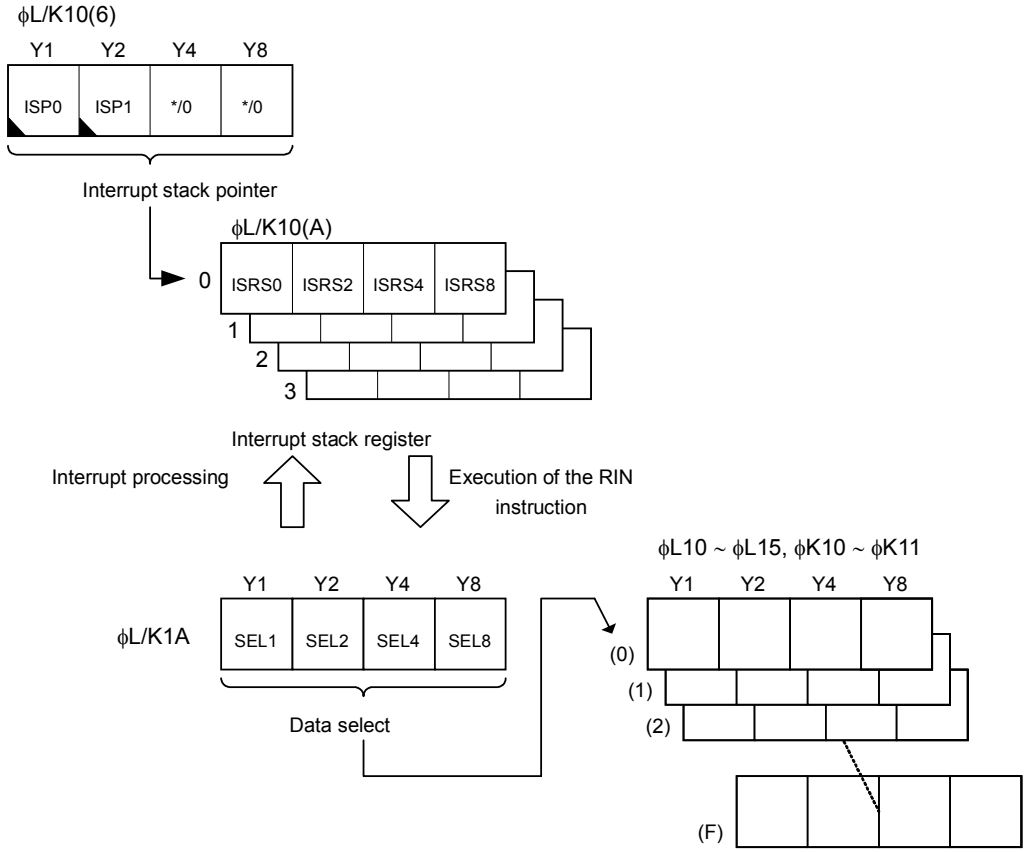
I/O instruction	OUT1	OUT2	OUT3	IN1	IN2	IN3
m	1	2	3	1	2	3

- [K/L]: Indicates input/output ports.
  - K: Input port (instructions IN1 to 3)
  - L: Output port (instructions OUT1 to 3)

Example: The setting for the G-register is allocated to code 8 and 9 in the OUT1 instruction. The encoded expression at this time becomes ϕL18 and ϕL19.

Data port (ϕL10 to 16, ϕK10 to 11) on the I/O map is divided into 16 and indirectly specified by the contents of the data select port (ϕL/K1A). The indirectly specified port is accessed by the OUT1 instruction with the operand [CN = 0 to 6H] or IN1 instruction with the operand [CN = 0 to 1H]. Whenever the data select port accesses the data port, it is automatically incremented by 1.

The data select port has a 4-bit interrupt stack register. When an interrupt request is generated, the 4 bits in the data select port are evacuated to the interrupt stack register specified by the interrupt stack pointer, and returned to the data select port during execution of the RNI instruction.



< Indirect specification by the data selection port >

I/O Map (IN1 (M, C), IN2 (M, C), IN3 (M, C), OUT1 (M, C), OUT2 (M, C), OUT3 (M, C))

Page 1	ϕL1				ϕL2				ϕL3				ϕK1				ϕK2				ϕK3			
	OUT1				OUT2				OUT3				IN1				IN2				IN3			
	Y1	Y2	Y4	Y8	Y1	Y2	Y4	Y8	Y1	Y2	Y4	Y8	Y1	Y2	Y4	Y8	Y1	Y2	Y4	Y8	Y1	Y2	Y4	Y8
0	Data port 1				Interrupt enable flag								Data port 1				Interrupt enable flag							
					EF1 (INTR1)	EF2 (INTR2/TM)	EF3 (SIO/TP/W)	EF4 (TIMER)									EF1 (INTR1)	EF2 (INTR2/TM)	EF3 (SIO)	EF4 (TIMER)				
1	Data port 2				Interrupt latch reset								Data port 2				Interrupt latch							
					ILR1 (INTR1)	ILR2 (INTR2/TM)	ILR3 (SIOTP/W)	ILR4 (TIMER)									ILR1 (INTR1)	ILR2 (INTR2/TM)	ILR3 (SIOTP/W)	ILR4 (TIMER)				
2	Data port 3				INTR1 control		INTR2 control		I/O port 3 output data				IF data 1				Interrupt master flag				I/O port 3 input data			
					POS1	NEG1	POS2	NEG2	-0	-1	-2	-3	F0	F1	F2	F3	IMF	0	0	0	-0	-1	-2	-3
3	Data port 4				A/D converter control				I/O port 4 output data				IF data 2				A/D converter data				I/O port 4 input data			
					AS SEL0	AS SEL1	AS SEL2	STA	-0	-1	-2	-3	F4	F5	F6	F7	AD0	AD1	AD2	AD3	-0	-1	-2	-3
4	Data port 5				DO1 control				I/O port 5 output data				IF data 3				A/D converter data				I/O port 5 input data			
					R0	R1	M0	M1	-0	-1	-2	-3	F8	F9	F10	F11	AD4	AD5	Busy	0	-0	-1	-2	-3
5	Data port 6				DO2 control 1				I/O port 6 output data				IF data 4								I/O port 6 input data			
					R0	R1	M0	M1	-0	-1	-2	-3	F12	F13	F14	F15					-0	-1	-2	-3
6	Data port 7				DO2 control 2								IF data 5				STOP F/F	BUZER 10 Hz	VDO OFF F/F	0				
					AUTO1	ENA	CK0	CK1					F16	F17	F18	F19								
7	LCD driver control				UNLOCK RESET	PN	POL	LPFON	I/O port 8 output data				IF monitor				Unlock detect				I/O port 8 input data			
	DISP OFF	LCD OFF	BIAS	*					-0	-1	-2	-3	Busy	MANUAL	OVER	0	UNLOCK	ENA	Unknown	Unknown	-0	-1	-2	-3
8	G-register 1				MUTE	MUTE control							G-register 1				MUTE	MUTE control			I/O port 9 input data			IN
	G0	G1	G2	G3		POL	Break	MUTE ENA					G0	G1	G2	G3		IO1	POL	0	-0	-1	-2	
9	G-register 2												G-register 2								I/O port 10 input data			
	G4	*	*	*									G4	0	0	0					-0	-1	-2	-3
A	Data select				Timer reset		Timer port interrupt control		I/O port 3 control				Data select				Timer							
	S1	S2	S4	S8	2 Hz F/F	Clock	CK SEL	ENA	-0	-1	-2	-3	SEL1	SEL2	SEL4	SEL8	2 Hz F/F	10 Hz	100 Hz	200 Hz				
B	CA flag	*	*	*	Pulse counter control 1				I/O port 4 control				CA flag	0	0	0	Pulse counter data				I/O port 12 input data			
					POS	NEG	DOWN	*	-0	-1	-2	-3					PC0	PC1	PC2	PC3	-0	-1	-2	-3
C	Data-register 1 (DATA)				Pulse counter control 2				I/O port 5 control				Data-register 1 (DATA)				Pulse counter data				I/O port 13 input data			
	d0	d1	d2	d3	CTR RESET	OVER RESET	*	*	-0	-1	-2	-3	d0	d1	d2	d3	PC4	PC5	PC6	PC7	-0	-1	-2	-3
D	Data-register 2 (DATA)				Timer counter control				I/O port 16 control				Data-register 2 (DATA)				Pulse counter data				I/O port 14 input data			
	d4	d5	d6	d7	CK	PW	CR Disable	CR	-0	-1	-2	-3	d4	d5	d6	d7	OVER	0	0	0	-0	-1	-2	-3
E	Data-register 3 (DATA)				Timer counter interrupt detect data 1								Data-register 3 (DATA)				Timer counter data 1				I/O port 15 input data		0	0
	d8	d9	d10	d11	ID0	ID1	ID2	ID3					d8	d9	d10	d11	CT0	CT1	CT2	CT3	-0	-1		
F	Data-register 4 (DATA)				Timer counter interrupt detect data 2				I/O port 16 data				Data-register 4 (DATA)				Timer counter data 2				I/O port 16 input data			
	d12	d13	d14	d15	ID4	ID5	ID6	ID7	-0	-1	-2	-3	d12	d13	d14	d15	CT4	CT5	CT6	CT7	-0	-1	-2	-3

Refer to the next page

ϕL/K1A

Data select			
SEL1	SEL2	SEL4	SEL8

I/O / ϕL/K1A	ϕL10				ϕK10			
	OUT1				IN1			
	Y1	Y2	Y4	Y8	Y1	Y2	Y4	Y8
0	Address stack pointer (ASP)				Address stack pointer (ASP)			
	ASP0	ASP1	ASP2	ASP3	ASP0	ASP1	ASP2	ASP3
1	Address stack select				Address stack select			
	ASS0	ASS1	ASS2	ASS3	STKS0	STKS1	STKS2	STKS3
2	Address stack register 1 (ASR)				Address stack register 1 (ASR)			
	ASR0	ASR1	ASR2	ASR3	ASR0	ASR1	ASR2	ASR3
3	Address stack register 2 (ASR)				Address stack register 2 (ASR)			
	ASR4	ASR5	ASR6	ASR7	ASR4	ASR5	ASR6	ASR7
4	Address stack register 3 (ASR)				Address stack register 3 (ASR)			
	ASR8	ASR9	ASR10	ASR11	ASR8	ASR9	ASR10	ASR11
5	Address stack register 4 (ASR)				Address stack register 4 (ASR)			
	ASR12	ASR13	*	*	ASR12	ASR13	0	0
6	Interrupt stack pointer (ISP)				Interrupt stack pointer (ISP)			
	ISP0	ISP1	*	*	ISP0	ISP1	0	0
7	Interrupt stack select				Interrupt stack select			
	ISS0	ISS1	*	*	ISS0	ISS1	0	0
8	Interrupt stack register (ISR)				Interrupt stack register (ISR)			
	ISRG0	ISRG1	ISRG2	ISRG3	ISRG0	ISRG1	ISRG2	ISRG3
9	Interrupt stack register (ISR)				Interrupt stack register (ISR)			
	ISRG4	*	*	*	ISRG4	0	0	0
A	Interrupt stack register (ISR)				Interrupt stack register (ISR)			
	ISRdS0	ISRdS1	ISRdS2	ISRdS3	ISRdS0	ISRdS1	ISRdS2	ISRdS3
B	Interrupt stack register (ISR)				Interrupt stack register (ISR)			
	ISRCA	*	*	*	ISRCA	0	0	0
C	Interrupt stack register (ISR)				Interrupt stack register (ISR)			
	ISRd0	ISRd1	ISRd2	ISRd3	ISRd0	ISRd1	ISRd2	ISRd3
D	Interrupt stack register (ISR)				Interrupt stack register (ISR)			
	ISRd4	ISRd5	ISRd6	ISRd7	ISRd4	ISRd5	ISRd6	ISRd7
E	Interrupt stack register (ISR)				Interrupt stack register (ISR)			
	ISRd8	ISRd9	ISRd10	ISRd11	ISRd8	ISRd9	ISRd10	ISRd11
F	Interrupt stack register (ISR)				Interrupt stack register (ISR)			
	ISRd12	ISRd13	ISRd14	ISRd15	ISRd12	ISRd13	ISRd14	ISRd15

ϕL11				ϕK11			
OUT1				IN1			
Y1	Y2	Y4	Y8	Y1	Y2	Y4	Y8
DAL address 1 (AR)				DAL address 1 (AR)			
AR0	AR1	AR2	AR3	DA0	DA1	DA2	DA3
DAL address 2 (AR)				DAL address 2 (AR)			
AR4	AR5	AR6	AR7	DA4	DA5	DA6	DA7
DAL address 3 (AR)				DAL address 3 (AR)			
AR8	AR9	AR10	AR11	DA8	DA9	DA10	DA11
DAL address 4 (AR)				DAL address 4 (AR)			
AR12	AR13	TROM	*	DA12	DA13	TROM	0
Serial interface output data 1				Serial interface input data 1			
SO0	SO1	SO2	SO3	SI0	SI1	SI2	SI3
Serial interface output data 2				Serial interface input data 2			
SO4	SO5	SO6	SO7	SI4	SI5	SI6	SI7
Serial interface output data 3				Serial interface input data 3			
SO8	SO9	SOE	SOF	SI8	SI9	SIE	SIF
Serial interface control 1				Serial interface monitor 1			
M0	M1	PORT SEL	SIO	BUSY1	SOERR	RX F/F	BUSY2
Serial interface control 2				Serial interface monitor 2			
CK0	CK1	OSC0	OSC1	OCT0	OCT1	OCT2	OCT3
Serial interface control 3				Serial interface monitor 3			
MASTER	POL	N-chS	SIS	ICT0	ICT1	ICT2	ICT3
Serial interface control 4							
STPS	SWENA	MSB	SOS				
Serial interface control 5							
STA0	STA1	STA2	STA3				
Serial interface control 6							
STP0	STP1	STP2	STP3				
Serial interface control 7				Decreased voltage detection voltage trimming register			
TSTA1	TSTA2	STP	F/F RESET	TR0	TR1	TR2	TR3
Decreased voltage detection control 1				Constant-voltage trimming register			
WAIT ENA	INH ENA	VSTOP ENA	*	TT0	TT1	TT2	TT3
Decreased voltage detection control 2				PLL amplifier trimming register			
STOP F/F RESET	INT LB SEL	TIM SEL	BREAK ENA	TA0	TA1	TA2	TA3

ϕL/K1A

Data select			
S1	S2	S4	S8

I/O \ ϕL/K1A	ϕL12				ϕL13				ϕL14				ϕL15				ϕL16			
	OUT1				OUT1				OUT1				OUT1				OUT1			
	Y1	Y2	Y4	Y8	Y1	Y2	Y4	Y8	Y1	Y2	Y4	Y8	Y1	Y2	Y4	Y8	Y1	Y2	Y4	Y8
0	I/O port 9 output data								S13				Buzzer output control 1				IF counter control 1			
	-0	-1	-2	*					COM1	COM2	COM3	COM4	BF0	BF1	*	BEN	NC	IFin	Prescaller IN	0
1	I/O port 10 output data								S14				Buzzer output control 2				IF counter control 2			
	-0	-1	-2	-3					COM1	COM2	COM3	COM4	BM0	BM1	BUZR ON	POL	STA/$\overline{\text{STP}}$	MANUAL	G0	G1
2	I/O port 11 output data								S15				Electric volume data 1				TEST port 1			
	-0	-1	-2	-3					COM1	COM2	COM3	COM4	VR0	VR1	VR2	VR3	#0	#1	#2	#3
3	I/O port 12 output data								S16				Electric volume data 2				TEST port 2			
	-0	-1	-2	-3					COM1	COM2	COM3	COM4	VR4	*	*	*	#4	*	*	*
4	I/O port 13 output data				S1				S17				Electric volume control							
	-0	-1	-2	-3	COM1	COM2	COM3	COM4	COM1	COM2	COM3	COM4	CH1	CH2	VR MUTE	-∞dB				
5	I/O port 14 output data				S2				S18				DC/DC converter control 1							
	-0	-1	-2	-3	COM1	COM2	COM3	COM4	COM1	COM2	COM3	COM4	VDET SEL	0	VDET ENA	*				
6	I/O port 15 output data				S3				Interrupt priority 1		Interrupt priority 2		DC/DC converter control 2							
	-0	-1	*	*	COM1	COM2	COM3	COM4	PRI1-0	PRI1-1	PRI2-0	PRI2-1	DD0	DD1	DD2	DD3				
7					S4				Interrupt priority 3		Interrupt priority 4		DC/DC converter control 3							
					COM1	COM2	COM3	COM4	PRI3-0	PRI3-1	PRI4-0	PRI4-1	DDCK1/2	DDCK ENA	POL	*				
8	I/O port 9 control				S5				Doubler voltage control for CPU				PLL mode select							
	*	-1	-2	*	COM1	COM2	COM3	COM4	VC0	VC1	CLAMP	OSC2	HF	*	*	0				
9	I/O port 10 control				S6				I/O port 2 brake permit				0	0	0	$\overline{\text{INH}}$ ENA				
	-0	-1	-2	-3	COM1	COM2	COM3	COM4	BP3	BP4	BP6	BP8								
A					S7				I/O port 3 pull-up				Programmable counter 1							
					COM1	COM2	COM3	COM4	PU30	PU31	PU32	PU33	P0	P1	P2	P3				
B	I/O port 12 control				S8				I/O port 3 pull-down				Programmable counter 2							
	-0	-1	-2	-3	COM1	COM2	COM3	COM4	PD30	PD31	PD32	PD33	P4	P5	P6	P7				
C	I/O port 13 control				S9				I/O port 13 / Segment select				Programmable counter 3							
	-0	-1	-2	-3	COM1	COM2	COM3	COM4	S5	S6	S7	S8	P8	P9	P10	P11				
D	I/O port 14 control				S10				I/O port 14 / Segment select				Programmable counter 4				Decreased voltage detection voltage trimming register			
	-0	-1	-2	-3	COM1	COM2	COM3	COM4	S9	S10	S11	S12	P12	P13	P14	P15	TR0	TR1	TR2	TR3
E	I/O port 15 control				S11				I/O port 15 / Segment select				Reference select				Constant-voltage trimming register			
	-0	-1	*	*	COM1	COM2	COM3	COM4	S13	S14	*	*	R0	R1	R2	R3	TT0	TT1	TT2	TT3
F					S12				I/O port 16 / segment select				Clock generator control				PLL amplifier trimming register			
					COM1	COM2	COM3	COM4	S15	S16	S17	S18	INV ON	OSC2 ON	CK SEL	*	TA0	TA1	TA2	TA3

○ System Reset

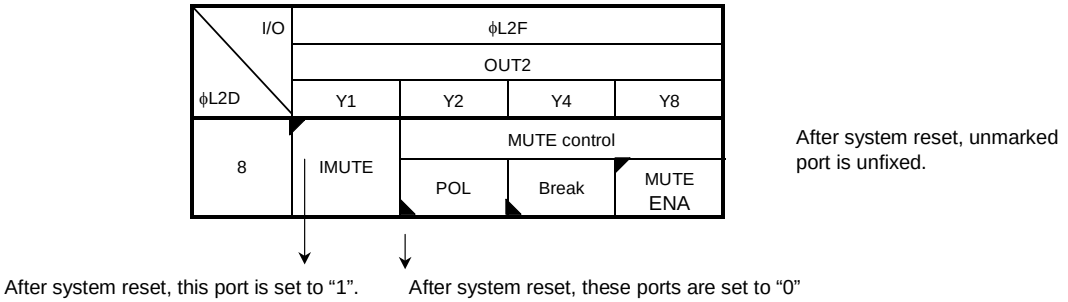
The device system will be reset when the $\overline{\text{RESET}}$ pin is subject to the "L" level or when a voltage of 0 V → 1.2 V to 3.6 V is supplied to the V_{CPU} pin (power-on reset). On system reset, the program will start from "0" address immediately after a standby time of 100 ms following the startup of the low-speed oscillator. Since the power-on reset function is being used, the $\overline{\text{RESET}}$ terminal should be fixed at "H" level under normal conditions.

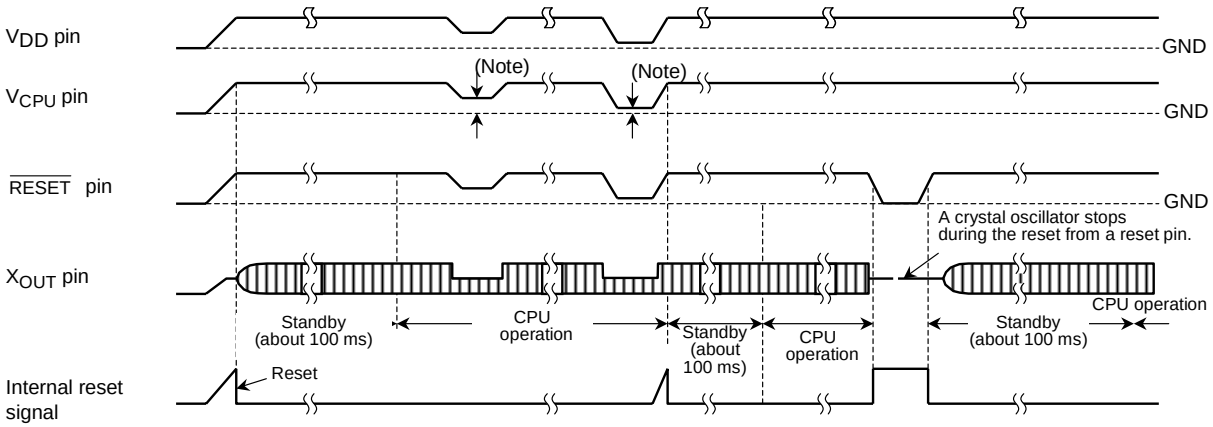
Note: The input circuit of the $\overline{\text{RESET}}$ pin operates on a V_{CPU} power supply, and the input voltage level is 0 V~V_{CPU}.

Note: The power-on reset circuit operates on power startup of the V_{CPU} power supply.

Note: The LCD common output and the segment output will be fixed at "L" level during system reset and during the subsequent standby period.

Note: It is necessary to initialize any internal port shown in the above-mentioned I/O map that has not been initialized after system reset. The ◣ mark on the I/O map shows a port or bit that is set to "0" after system reset, while the ◤ mark shows a port or bit that is set to "1". No mark shows a port or bit that is unfixed.





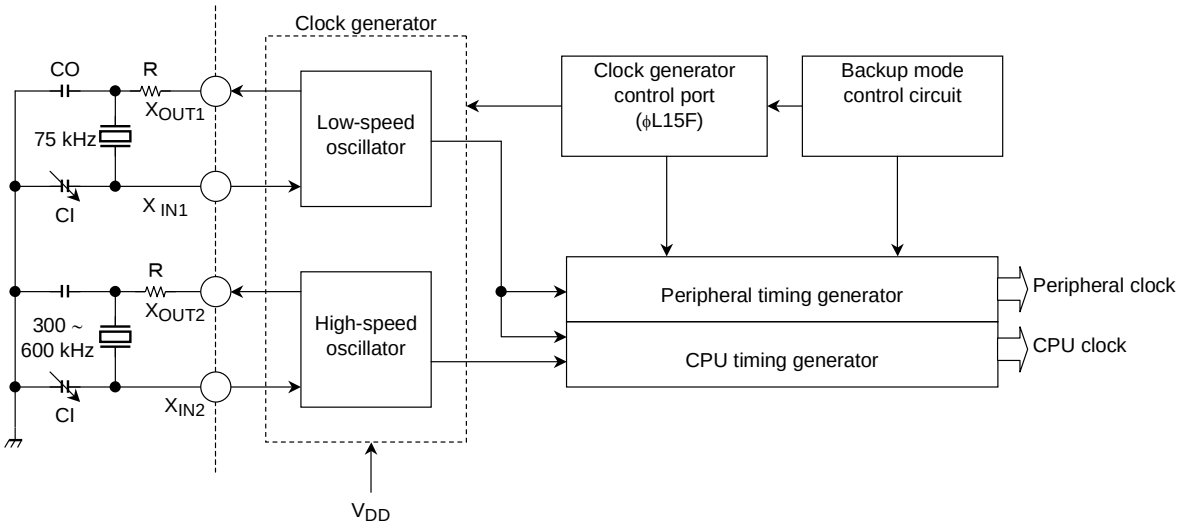
< Timing of Operation >

Note: If the V_{DD} power supply voltage falls below 0.9 V or the V_{CPU} power supply voltage falls below 1.2 V, set to clock stop mode and operate the reset function. The V_{CPU} power supply voltage will be reset when the power supply is restarted (power-on reset).

Note: V_{CPU} pins are usually supplied from doubler voltage V_{DB} pins. Refer to the backup mode item.

○ System clock control circuit

The system clock control circuit consists of a clock generator, clock generator control port, timing generator and backup mode control circuit.



Note: It is necessary to use a crystal resonator with a low CI value and favorable startup characteristics.

Note: Adjust and determine the external resistance and capacitor constant to match the crystal resonator actually used.

Note: The low-speed oscillator and high-speed oscillator are equipped with a built-in Schmitt circuit.

Note: The power supply of the low-speed oscillator and high-speed oscillator uses a V_{DD} pin.

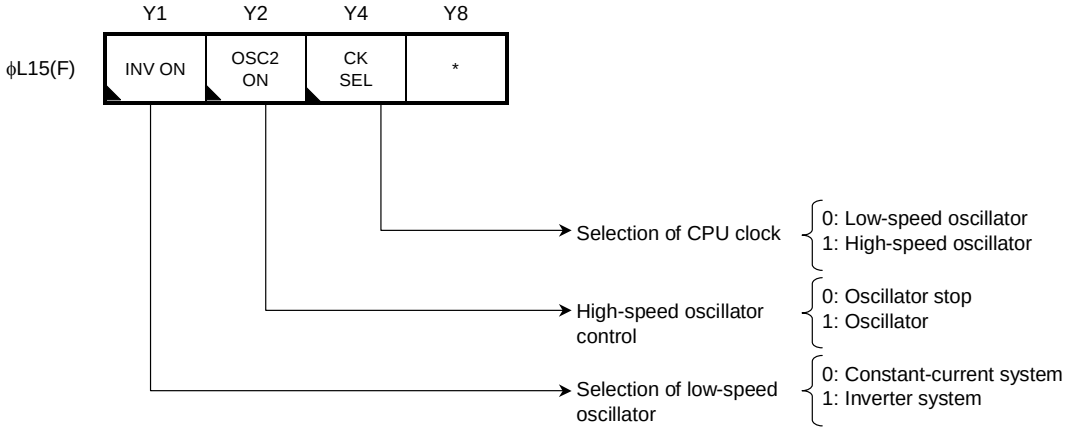
1. Clock generator

The clock generator circuit generates the basic clock used as the standard for the system clock supplied to a core-based CPU and peripheral hardware. The circuit incorporates low-speed and high-speed oscillators, with a 75 kHz crystal resonator connected to the X_{IN1} and X_{OUT1} pin and a 300 to 600 kHz ceramic resonator or a crystal resonator connected to the X_{IN2} to X_{OUT2} pin.

The CPU clock and doubler clock (V_{DB} doubler or doubler for VT) can be converted to a high-speed oscillation clock through programming. Since items such as the timer and reference frequency utilize the 75 kHz clock during this time, the timer duration measurement and PLL are unaffected.

2. Clock generator control port

The clock generator control port controls the low-speed and high-speed oscillators.



The $OSC2_{ON}$ bit controls the on/off setting of the high-speed oscillator. If this bit is set to “1”, the high-speed oscillator is enabled and oscillation is started.

The CK SEL bit converts the CPU operation clock to a low-speed or high-speed oscillator clock. After reset, the CPU operates with a 75 kHz low-speed clock. When the high-speed clock is to be used, conversion to the high-speed clock takes place after the $OSC2_{ON}$ bit is set to “1” and the high-speed oscillator frequency is stabilized. The INV ON bit can be used to change the circuit type of the 75 kHz low-speed oscillator. This is usually set to a constant-current type.

Note: The high-speed oscillator clock can be used as the doubler clock for the V_{DB} pin or doubler clock for the VT (DDCK1/DDCK2).

Note: CK SEL bit control is restricted to conversion of the CPU operation clock and does not affect items such as PLLs and timers.

Note: The circuit type of the 75 kHz low-speed oscillator is used for the constant-current system. If the crystal oscillator circuit is set to an inverter type, its output level rises. This circuit type should only be used to investigate whether or not the tuner characteristic of the crystal oscillator has been affected.

○ DC/DC converter for CPU

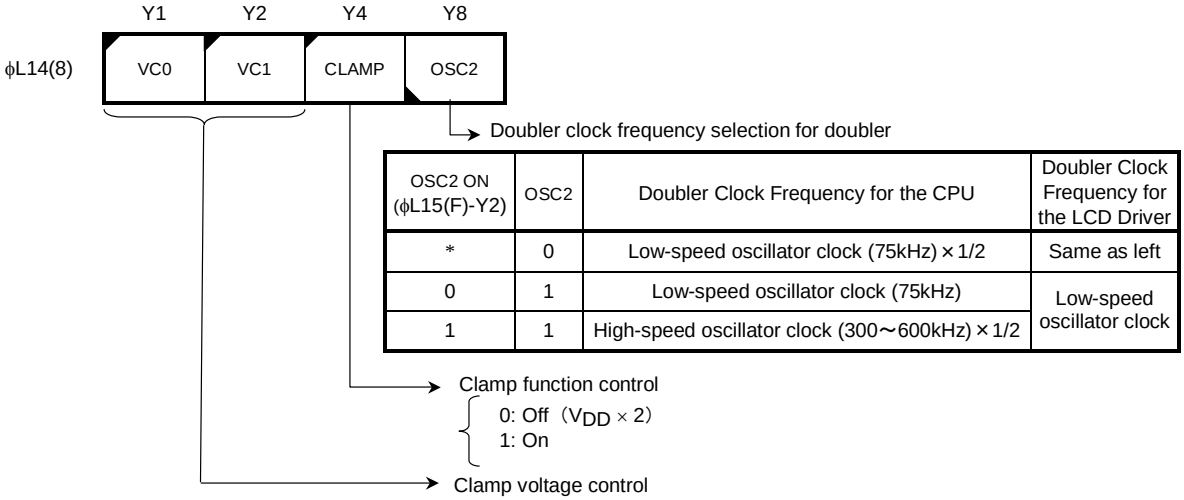
The device incorporates a DC/DC converter for the CPU power supply. The CPU doubler circuit comprises a charge pump system utilizing a capacitor.

There is a built-in clamp control function, for which an electrical potential of 2.0, 2.5 and 3.0 V can be set through programming.

The capacitor-utilizing charge pump system supplies a V_{DD} level charge between the C1 and C2 pins, and a doubler potential twice the V_{DD} potential is output to the V_{DB} pin. Note that, if twice the voltage of the V_{DD} pin decreases following clamp setting using this method, the doubler potential also decreases.

Three types of 1/2 frequency can be selected for the doubler clock: 37.5 kHz, 75 kHz, and a high-speed oscillation clock. After reset, a frequency of 37.5 kHz is output. Set the doubler clock to the required doubler capability.

The doubled V_{DB} potential is supplied to the A/D converter and the V_{EE} constant-voltage circuit. The V_{DB} potential is usually supplied to the V_{CPU} pin through a Schottky diode.

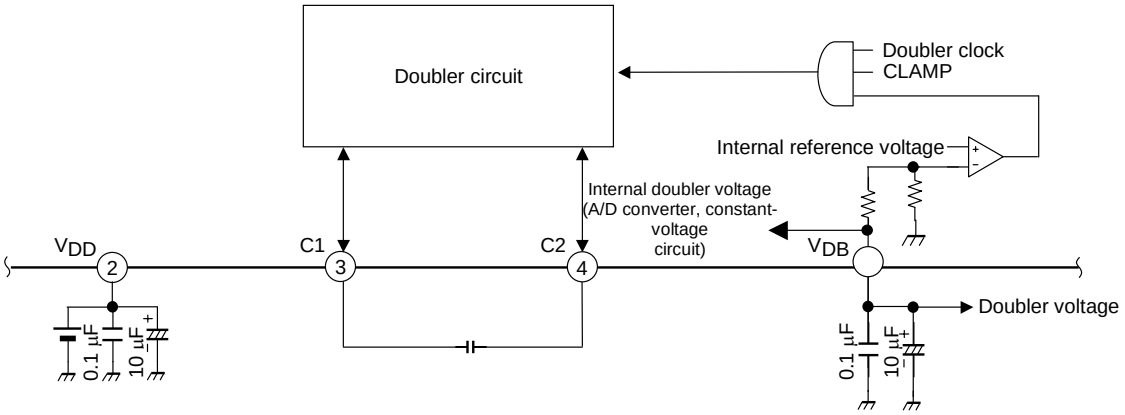


Note: This becomes effective only when the clamp function is ON.

OSC2 ON (ϕL15(F)-Y2)	OSC2	Doubler Clock Frequency for the CPU	Doubler Clock Frequency for the LCD Driver
*	0	Low-speed oscillator clock (75kHz) × 1/2	Same as left
0	1	Low-speed oscillator clock (75kHz)	Low-speed oscillator clock
1	1	High-speed oscillator clock (300～600kHz) × 1/2	

VC0	VC1	Clamp voltage
0	0	Prohibition
0	1	2.0V
1	0	2.5V
1	1	3.0V

Note: If the OSC2 bit is set to “1”, the doubler clock for the LCD driver is also changed simultaneously.

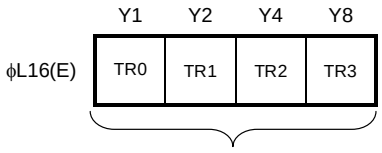


Example of an Application Circuit for a Charge Pump Doubler System Utilizing a Capacitor

Note: The V_{DB} pin is fixed at the V_{DD} pin level while the clock stop instruction is being executed.

○ Constant-voltage circuit (V_{EE})

There is a built-in constant-voltage circuit (V_{EE}) to provide the reference voltage of the LCD driver and DC/DC converter for the VT and for the CPU and A/D converter. The constant-voltage circuit utilizes the doubler V_{DB} pin power supply for the CPU and outputs a constant voltage of 1.5 V from the V_{EE} pin. There is a constant-voltage compensation data port for rectifying the constant-voltage value V_{EE}, and voltage can be rectified per 20 mV. Do not set this port through programming as correction data is usually determined at the time of shipment.



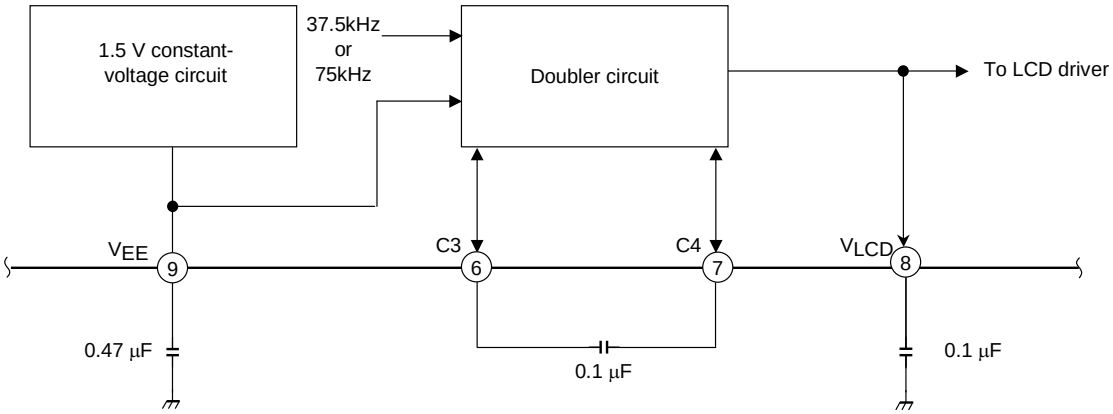
The constant-voltage rectify data

Note: After system reset, this serves as the port for data rectification so that V_{EE} is set to 1.5 V at the time of shipment. For this reason, do not access this port.

Note: During reset or a clock stop, the V_{EE} pin becomes high impedance.

○ LCD driver doubler circuit (V_{LCD})

There is a built-in doubler circuit for LCD drivers (V_{LCD}) that acts as an LCD driver power supply.
The doubler circuit for LCD drivers outputs a 3 V constant voltage doubled from a 1.5 V constant voltage through the capacitor-utilizing charge pump system doubler.



Note: During reset or a clock stop, the V_{LCD} pin outputs the V_{CPU} level.

Note: The V_{LCD} doubler potential is used for the power supply in the I/O port, etc.

Note: The doubler clock can use 37.5 kHz or 75 kHz (OSC2 bit).

○ Backup mode

Backup mode decreases the operating current and holds data memory and other registers. Backup mode can be implemented through programming-based backup or hardware-based backup.

For programming-based backup, three types of backup mode are possible through the executing of CKSTP or WAIT instructions.

For hardware-based backup there are two types of function: a decreased voltage detection function and a power-off backup function. When the V_{DD} pin power supply falls to the decreased voltage detection setting potential (V_{DD} = 0.85 V - 1.225 V), a decrease voltage detection function stops the CPU temporarily and prevents incorrect operation of the CPU. During this time, the operational status of such items as the LCD driver, I/O ports, and PLL is held. If the V_{DD} pin level is set to approximately 0.5 V or less, the power-off backup function will stop functions such as LCD driver, I/O port, and PLL operations; reduce the only power supply for the CPU (V_{CPU} pin) to a low consumption current (0.5 μA or less); and hold memory contents and the status of other registers.

1. Clock stop mode

Execution of the CKSTP instruction actuates clock stop mode.

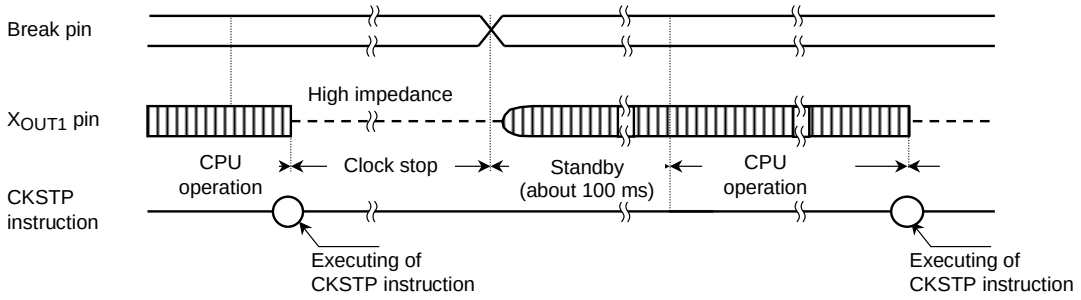
Clock stop mode suspends system operations while maintaining the internal status immediately prior to suspension. At this time, the V_{DD}, V_{PLL} and V_{CPU} pin power supplies change to low consumption current (10 or less μA); crystal oscillation stops; the LCD indication output pin and CMOS output port are fixed to the "L" level; and the N-ch open drain pins are all set to the OFF (high-impedance) state automatically. The power supply of the V_{DD} and V_{PLL} pins can be lowered to the OFF state, and the power supply of the V_{CPU} pin power supply can be lowered to 0.75 V.

Clock stop is released under the following conditions:

1) If there is a change in the input state of an I/O port (I/O ports 3, 4, 6, and 8) that has been set as a break pin and to input. (Refer to the section on I/O ports.)
2) If the V_{DD} power supply pin is changed from the off to the on state (at approximately 0.5 V or more) when the VDD power supply break is enabled (BRAEK ENA bit (ϕL11(F)) = "1").

Release of clock stop mode causes the next address to be executed after 100 ms of standby time have elapsed.

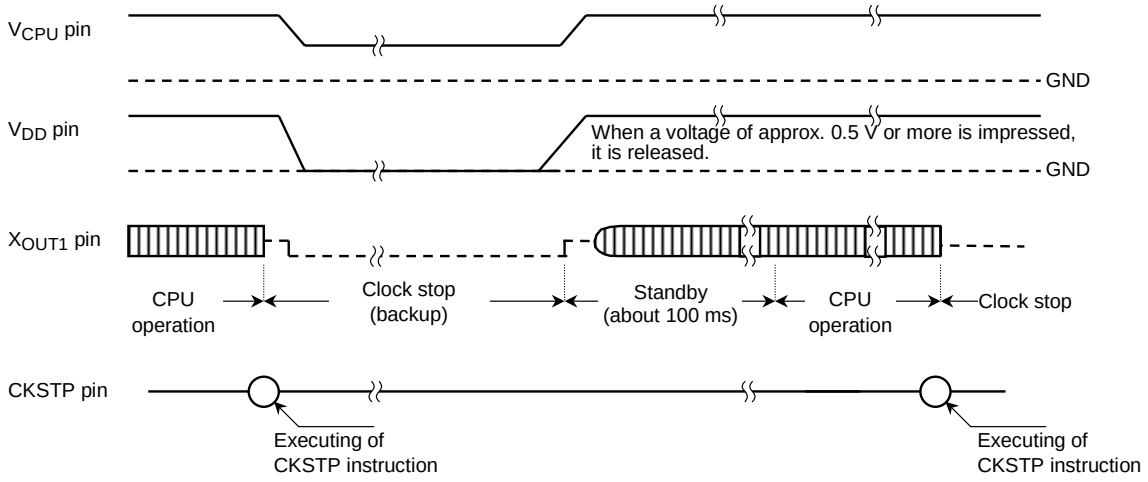
Note: The PLL changes to the off state during execution of the CKSTP instruction.



Example of Operation Timing Using a Break Pin

Note: Clock stop mode is actuated on execution of the CKSTP instruction.

Note: When break pin input is set, it is necessary to read this input state before execution of the CKSTP instruction.



Example for Operating Timing by Power Supply Pin

Note: Release of the CKSTP instruction through on/off of the V_{DD} power supply pin requires the BREAK ENA bit (ϕL11(F)) to be set to "1". When this function is enabled, about 10 μA will be consumed in the V_{CPU} pin if voltage is applied through the V_{DD} pin during CKSTP instruction execution. For this reason, this function should be prohibited if voltage is always impressed through the V_{DD} pin power supply.

Note: It is necessary to retain the potential of the V_{CPU} pin. Provide backup using a capacitor or similar means.

Note: Reset occurs if the V_{CPU} pin level (typ: 0.3 V) falls to 0.75 V or below and the voltage is then applied (power-on reset).

2. Wait mode

Wait mode suspends system operations, maintains the internal status immediately prior to suspension and decreases current consumption. This mode stops at the address for the execution of the WAIT instruction on execution of hard and soft wait. On cancellation of wait mode, the next address is executed immediately, with no standby interval.

(1) SOFT WAIT mode

Only CPU operations within the device are suspended when a WAIT instruction is executed in which [P = 0H] has been specified in the operand. The crystal resonator and other elements will continue to operate normally at this time. SOFT WAIT mode is efficient in reducing current consumption during clock operations when used in programs that include clock functions.

The wait status applies whenever the WAIT instruction is executed. Wait mode is canceled on the following conditions:

1) If there is a change in the input state of an I/O port (I/O ports 3, 4, 6, and 8) that has been set as a break pin and to input. (Refer to the section on I/O ports.)
2) When the 2 Hz Timer F/F is set as “1”

Note: The backup state applies if the V_{DD} power supply pin goes off in wait mode when the V_{DD} power supply is enabled (BRAEK ENA bit (ϕL11(F)) = "1"). The state is released when the power supply is turned on (at approximately 0.5 V or more). At this time, the CPU starts up after 100 ms of standby time have elapsed.

Note: Current consumption will vary depending on the execution time of the CPU operation.

(2) HARD WAIT mode

The operations of all elements, with the exception of the crystal resonator and doubler operating (V_{DB} / V_{LCD} pin), can be suspended by execution of a WAIT instruction in which [P = 1H] has been specified in the operand. This enables even greater levels of current consumption reduction than SOFT WAIT mode. This suspends the CPU operation.

During hard wait mode, the state of the output port is maintained and all LCD output pins are fixed at the “L" level. The wait status is assumed whenever the WAIT instruction is executed. Wait mode is canceled on the following conditions:

1) If there is a change in the input state of an I/O port (I/O ports 3, 4, 6, and 8) that has been set as a break pin and to input. (Refer to the section on I/O ports.)
2) If the V_{DD} power supply pin is changed from the off to the on state (at approximately 0.5 V or more) when the VDD power supply break is enabled (BRAEK ENA bit (ϕL11(F)) = "1").

Note: Wait mode is also released when the V_{DD} power supply pin in wait mode is changed from the off to the on state (at approximately 0.5 V or more) when the V_{DD} power supply break has been enabled (BRAEK ENA bit (ϕL11(F)) = "1").

Note: The PLL OFF status will be assumed during wait mode.

Note: During wait mode, the power supply doubler circuit (V_{DB} pin), the constant-voltage supply circuit for the LCD (V_{EE} pin) and the doubler circuit for the LCD (V_{LCD} pin) continue to operate.

3. Backup mode by hardware

The backup mode by hardware detects the power supply voltage level of a V_{DD} pin and actuates backup mode. There are two types of backup function by hardware: a decreased voltage detection function and a power supply off detection function.

(1) Decreased voltage detection function

The decreased voltage detection function detects the V_{DD} pin level, suspends the operation of the CPU and prevents incorrect operation of the CPU. If the V_{DD} pin level falls below the decreased voltage detection setting (V_{DD} = 0.85V - 1.225V) potential when the detected decrease voltage function is enabled, CPU operation will be suspended; and if the V_{DD} pin again rises above the set voltage, the CPU will restart. Although the CPU stops, other functions continue to operate normally.

Decreased voltage detection operation is performed at intervals. The frequency of detection can be selected through programming, with detection being performed at a rate of once every two instructions or 16 instruction cycles. Select according to power consumption and speed of power supply variation.

The detection voltage can be set to an interval of 25 mV within the range of V_{DD} = 0.85 V ~ 1.225 V. Set according to the specification. Since suspension of CPU operation can be prohibited, it is also possible to detect residual battery level between 0.85 V and 1.225 V by varying the detection setting voltage and detecting the detection flag. In this case, execute a backup instruction after detection of the minimum voltage level to prevent incorrect operation of the CPU.

Where interrupt is permitted, the interrupt will be issued if the VSTOP F/F bit is set to “1”. If interrupt is received, the program will branch to 0003H address.

Moreover, PLL off-mode can be actuated during decreased voltage detection. Therefore the PLL can be quickly suspended should the voltage drop.

The VSTOP F/F bit enables detection of suspension or of a fall below the detection voltage. Upon detection this bit is set to "1" and will be reset by execution of flag reset (STOP F/F Reset = "1").

Through programming, therefore, it is possible to make various operation settings for when a decrease in the V_{DD} potential (battery voltage) occurs.

Note: Both serial interface and timer port are used for the interrupt function of the decreased voltage detection circuit. When this interrupt is used, the interrupt function of the serial interface and the timer port cannot be used.

(2) Detected power supply OFF function

Detected power supply OFF function detects the fact that the power supply is off during battery exchange or similar procedures and actuates the backup state of the CPU circuit (V_{CPU} pin) to keep it on hold.

If the detected power supply off function is enabled (BRAEK ENA bit (ϕL11(F)) = "1"), the V_{DD} pin level is about 0.5 V or less and all functions stop. At this time, the V_{CPU} pin power supply changes to low current consumption (0.5 μA or less); the LCD output pin and CMOS output port change to “L” level; the N-channel open-drain pins are all automatically fixed to the off (high-impedance) state; and the PLL changes to off mode. If the power supply is switched on again, the CPU will operate after a standby interval of 100 ms. The V_{DD} OFF F/F bit enables detection of whether the power supply has been switched off.

Note: Set the V_{DD} pin level to GND level during power supply off. If V_{DD} level potential remains, current will be consumed by the V_{CPU} pin.

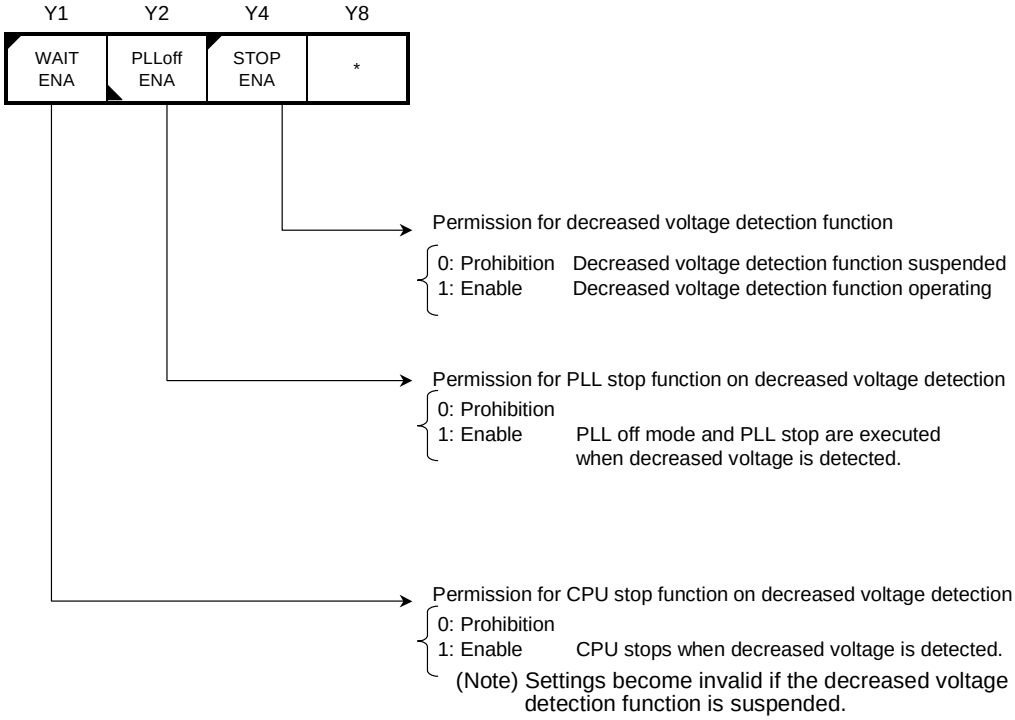
Note: The BRAEK ENA bit (ϕL11(F)) permits VDD power supply break and power supply off detection function.

Note: Use this function together with the decreased voltage detection function.

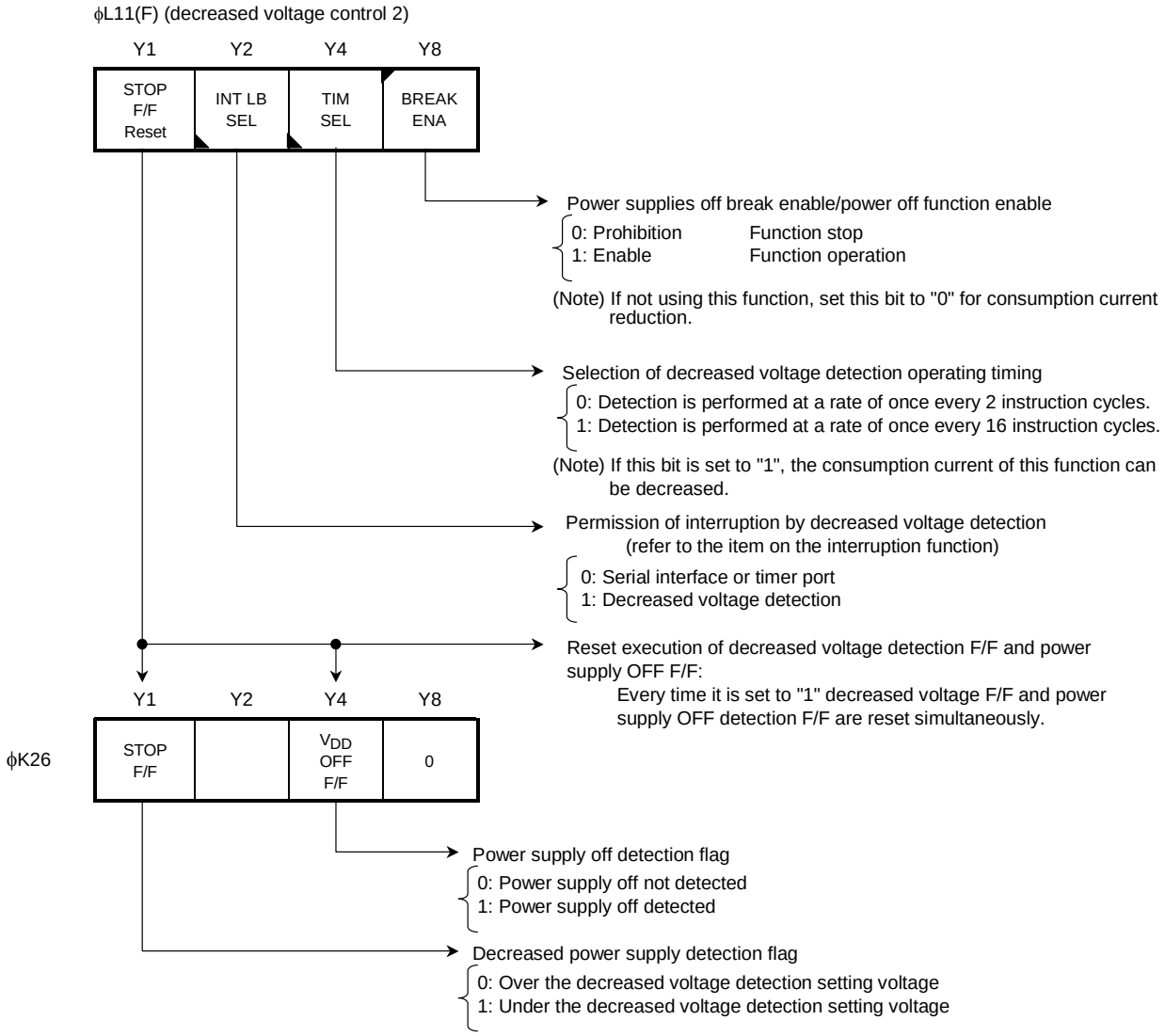
(3) Backup control register by hardware

Decreased voltage detection and power supply off detection function control are accomplished through access of the decreased voltage control port (ϕL11(E), ϕL11(F)); the decreased voltage detection setting data port (ϕL16(D), ϕK11(D)); and the flag register (ϕK26).

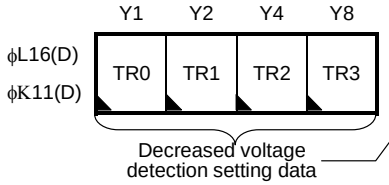
ϕL11(E) (decreased voltage control 1)



Note: If the decreased voltage detection function is not being used, set the WAIT ENA bit to "0" for reduced consumption current.



Note: The STOP F/F changes to the reset state, with a CPU standby interval (100 ms), after system reset; after release of the CKSTP instruction; and after detection of power off using the power-off detection circuit.



TR3	TR2	TR1	TR0	Data (HEX)	Decreased voltage detection voltage (V)
0	0	0	0	0	0.850
0	0	0	1	1	0.875
0	0	1	0	2	0.900
0	0	1	1	3	0.925
0	1	0	0	4	0.950
0	1	0	1	5	0.975
0	1	1	0	6	1.000
0	1	1	1	7	1.025
1	0	0	0	8	1.050
1	0	0	1	9	1.075
1	0	1	0	A	1.100
1	0	1	1	B	1.125
1	1	0	0	C	1.150
1	1	0	1	D	1.175
1	1	1	0	E	1.200
1	1	1	1	F	1.225

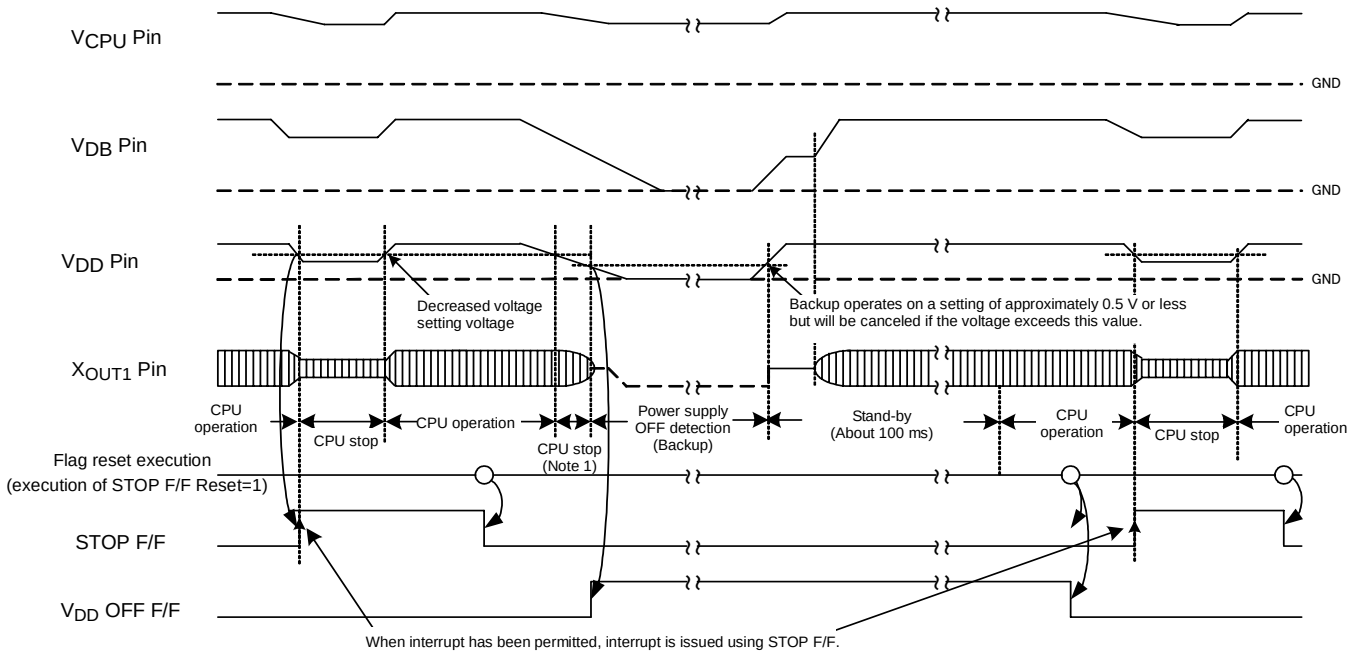
Note: Decreased voltage detection voltage detected V_{DD} pin level.

Note: Any fall below the decreased voltage detection voltage will cause the STOP F/F to be set to "1"; and the CPU will stop as a result of decreased voltage detection.

Note: The decreased voltage detection value is a standard value. The constant voltage of the V_{EE} pin is used as the standard voltage of the decreased voltage detection circuit. Since this V_{EE} voltage varies from product to product, the decreased voltage detection value also varies at the same time.

Note: If a high-speed oscillator clock is being used for the CPU clock, assign the decreased voltage setting data to between 0H ~ 6H (0.85 V ~ 1.00 V). Do not make any other setting.

(4) Decreased voltage detection, power supply off detection timing

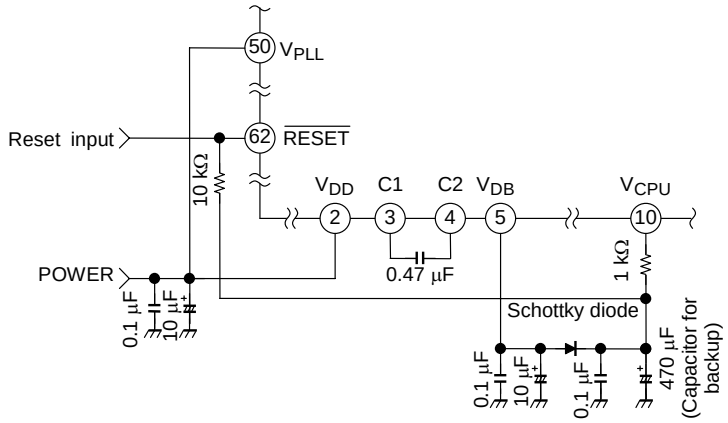


Example of timing operation

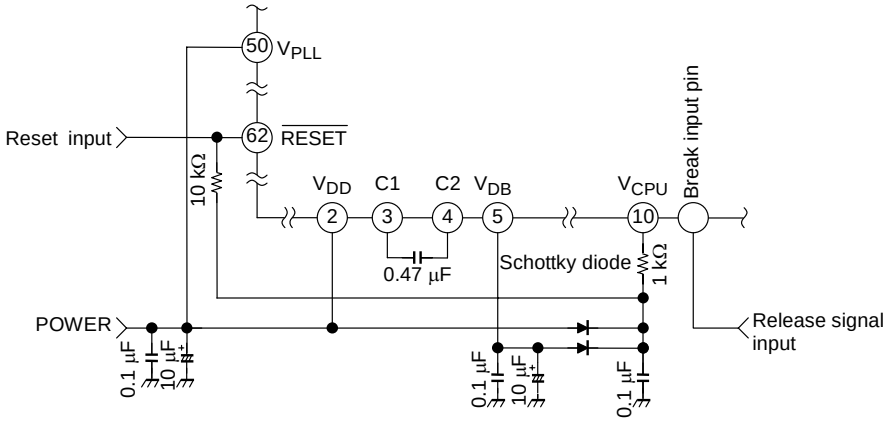
Note 1: Decrease voltage is detected and CPU operation is suspended. It is then necessary to detect the V_{DD} power supply voltage. When performing power off, therefore, ensure that the fall time from the decreased voltage detection voltage to the detection of the power supply voltage (approximately 0.5 V) is equal to or greater than the timing period for operation of decreased voltage detection (i.e., two or 16 instruction cycles). Failure to do so will cause CPU malfunction.

Note 2: STOP F/F is reset during standby time.

(5) Backup circuit



Example Capacitor Backup Circuit (1)



Example Battery Backup Circuit (2)

Note: If backup operation using a CKSTP/WAIT instruction is available, use release signal input to perform the release operation as necessary. Moreover, on execution of the CKSTP command, connect an external capacitance of 4.7 mF or more for the V_{CPU} pin resistance as in Example Capacitor Circuit (2) above.

Note: The diode shown in the circuit diagrams should be a Schottky diode with a low VF and a small reverse-leakage current.
Recommended diodes: 1SS357, 1SS393

Note: Set the backup capacitor capacity value according to the required backup time.

Note: The "H" level of reset input requires the application of a V_{CPU} level voltage. Therefore set high impedance at the time of reset off.

Note: The V_{CPU} pin power supply is a logic power supply with a timing circuit, ALU, data memory and all registers. The V_{CPU} pin power supply should usually be retained at the time of backup.

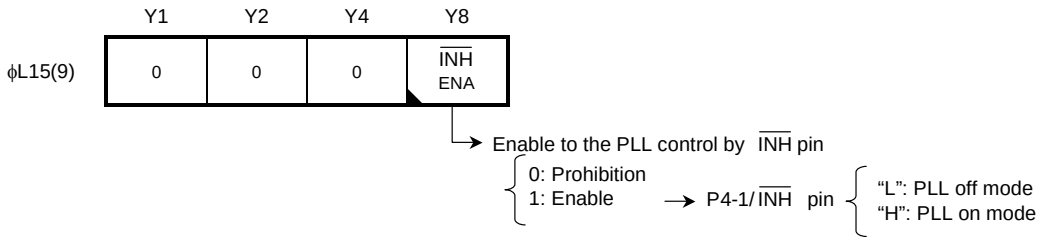
4. PLL OFF mode

The PLL can be turned on or off depending on the contents of the reference selection port. If all the contents of the reference selection port are set to "1", PLL off mode applies. (Refer to the section on the reference frequency divider.)

When the $\overline{INH}$ ENA bit is set to "1", the PLL can be turned on or off with the $\overline{INH}$ pin. The $\overline{INH}$ pin input serves as PLL off mode at "L" level, and serves as PLL on mode on the "H" level. As a result, it is possible quickly to set PLL off mode when changing batteries These data are accessed by an OUT1 instruction specifying 9h for the data select port (ϕK/L1A) and [CN = 5H] for the operand.

Moreover, PLL off mode can be set by decreased voltage detection.
(Refer to the section in 3. Backup mode by hardware.)

The V_{PLL} pin serves as low consumption current at the time of PLL off mode. Moreover, the power supply for a VPLL terminal can be turned off at this time.



Note: PLL off mode applies during clock stop mode, hard wait mode, and when power off occurs as a result of the power supply off detection function.

Note: The V_{PLL} pin power supply is a prescaler and programmable counter power supply. When only the V_{PLL} pin power supply is turned off, the setting method of dividing frequency and the value of dividing frequency are maintained because the V_{CPU} power supply is used. Moreover, when the PLL is on, the level of the applied V_{PLL} pin voltage can supply power to the PLL regardless of the V_{DD} pin or the potential of the V_{CPU} pin.

Note: $\overline{INH}$ input pin is used together with the P4-1 pin. The functionality becomes effective when the $\overline{INH}$ input is enabled, and the external interrupt function (INTR2) and the break function are enabled. Moreover, the input state can be judged by reading the P4-1 input data of an I/O Port 4 input port (ϕK33).

Note: The I/O port control port of P4-1 pin becomes invalid and is forced to enter the input state if $\overline{INH}$ input has been enabled.

Note: Set the Y1/Y2/Y4 bit of the above-mentioned port to "0".

○ Register port

The G-register, data register and DAL address register, which were mentioned in the description of the CPU, are arranged on the I/O map, and treated as one of the internal ports. The carry flag can also be accessed from an I/O map. (Refer to the section on I/O access of the stack register.)

Of these registers, the G-register, the carry flag, and the data register have a four-page interrupt stack register corresponding to the four stack levels. On execution of interrupt processing, these contents are automatically stored in the interrupt stack register together with the contents of data selection and automatically returned on execution of an RNI instruction. (Refer to the section on the interrupt stack register.)

1. G-register (ϕL/K18, ϕL/K19)

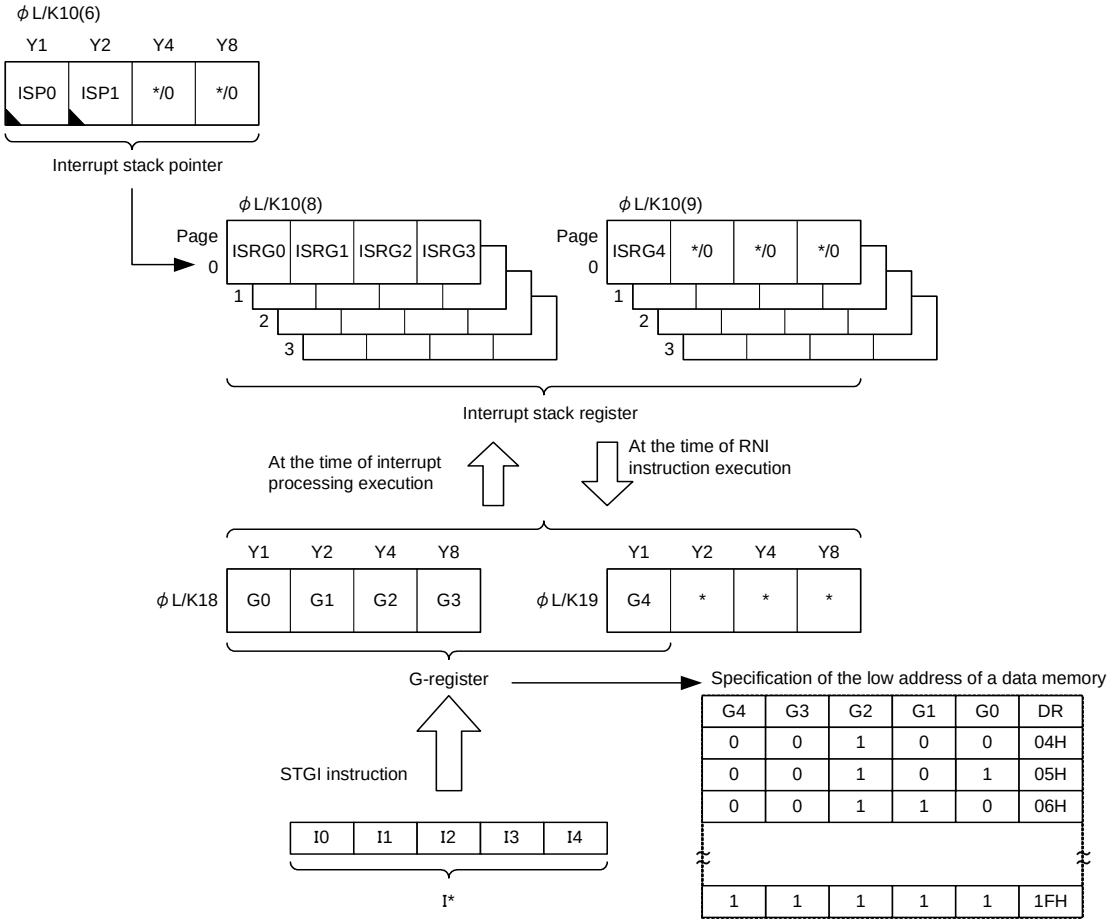
This register addresses the row addresses (DR = 04H ~ 1FH) of the data memory during execution of the MVGD instruction and MVGS instruction. The register is accessed with the OUT1/IN1 instruction for which [CN = 8H ~ 9H] has been specified in the operand. Moreover, if the STGI instruction is used, data can be set to this register with a single instruction.

This register has a four-level interrupt stack register. On the issuing of interrupt, the contents of the G-register are evacuated to the interrupt register specified by the interrupt stack pointer and returned by the RNI instruction.

Note: The contents of this register are only valid when the MVGD instruction and MVGS instruction are executed and are ineffective when any other instruction is executed. Moreover, this register is unaffected by the MVGD instruction and MVGS instruction.

Note: All of the data memory row addresses can be specified indirectly by setting data 00H to 1FH in the G-register (DR = 00H ~ 1FH).

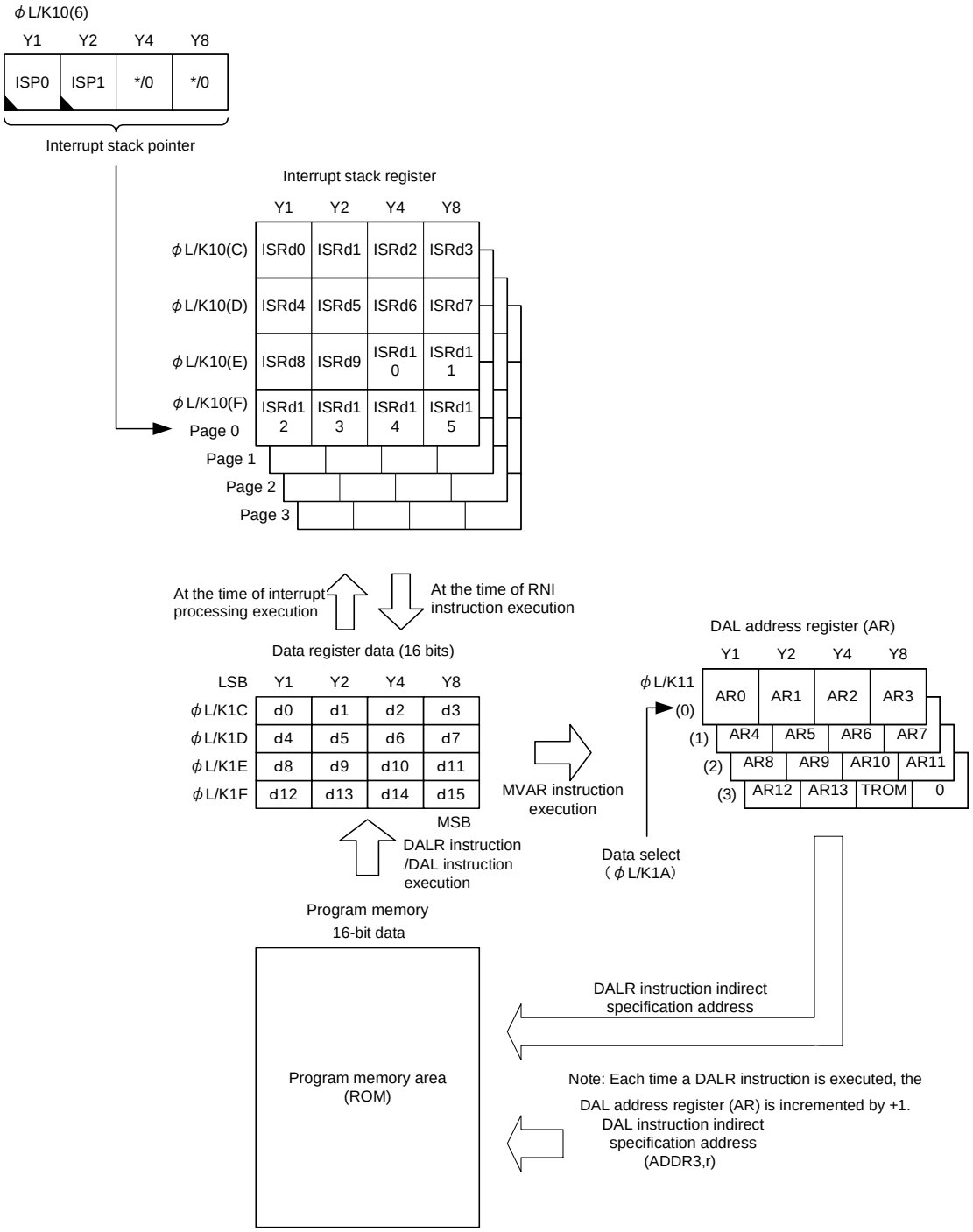
Note: It is possible to rewrite and reference the contents of the interrupt stack registers ISRG0 ~ ISRG4 (ϕL/K10(8), ϕL/K10(9)) through programming.



2. Data register (ϕL/K1C ~ ϕL/K1F), DAL address register (ϕL/K11(0) ~ ϕL/K11(3)) and control bit

The data register is 16-bit register for which the program memory data is loaded when the DAL instruction and DALR instruction are executed. The contents of this register are loaded into the data memory in 4-bit units with the execution of the OUT1/IN1 instructions for which [CN = CH ~ FH] has been specified in the operand. This register can be used for loading LCD segment decoding operations, radio band edge data and data related to binary-to-BCD conversion.

The data register has a four-level interrupt stack register. On the issuing of interrupt, the 16 data register bits are evacuated to the interrupt register specified by the interrupt stack pointer and returned by the RNI instruction.



The DAL address register (AR) is a register that specifies the program-memory-indirect when the DALR instruction is executed with the 16-bit register.

There are two types of commands that load the program memory data: the DAL instruction and the DALR instruction. For the DAL instruction, the contents of the (six-bit) ADDR3 in the operand and of the general register (r) become the reference address of the program memory. For the DALR instruction, the 14 bits of the DAL address register become the reference addresses. When the DAL instruction is executed, the program memory area (0000H ~ 03FFH) becomes the reference area. All the areas in the program memory area can be referred to by executing the DALR instruction. Whenever the DALR instruction is executed, the content of the DAL address register is increased by +1. Therefore data can be continuously loaded.

Moreover, the content of the data register can be transmitted to the DAL address register in 14 bits with one instruction by executing the MVAR instruction.

The contents of the DAL address register can be accessed in four-bit units on execution of an OUT1/IN1 instruction for which [CN = 1H] is specified in the operand. DAL address register port is divided and indirectly specified with the data selection port (ϕL1A) and set. The data of the specified port to be set beforehand is set and the data port corresponding to it is accessed. Each time the data select port (ϕL/K11) is accessed it is increased by +1. Therefore the data can be continuously accessed after setting up a data selection port.

Note: The DAL address register is valid only when the DALR instruction is executed, and is ineffective when any other instruction is executed. Moreover, the DAL address register is unaffected by the DAL instruction.

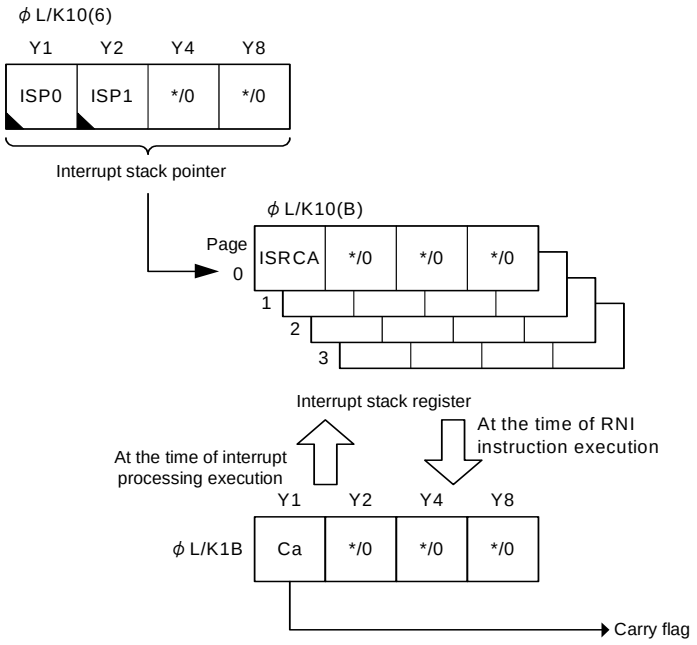
Note: This product has 8 k steps of ROM capacity; if 2000H ~ 3FFFH is specified in the DAL register and the DALR instruction is executed, the contents of the data register will become indeterminate.

Note: It is possible to rewrite and reference the contents of the interrupt stack registers ISRd0~ISRd15 (ϕL/K10(C~F)) through programming.

3. Carry flag (ϕL/K1B)

The carry flag is set when either Carry or Borrow occurs in the result of the calculation instruction execution and is reset if neither of these occurs. This carry flag is accessed with an OUT1/IN1 instruction for which [CN = BH] has been specified.

The carry flag contains a four-level interrupt stack register. When an interrupt is issued, this bit is evacuated to the interrupt register specified by the interrupt stack pointer, and is returned with the RNI instruction.



○ Stack register

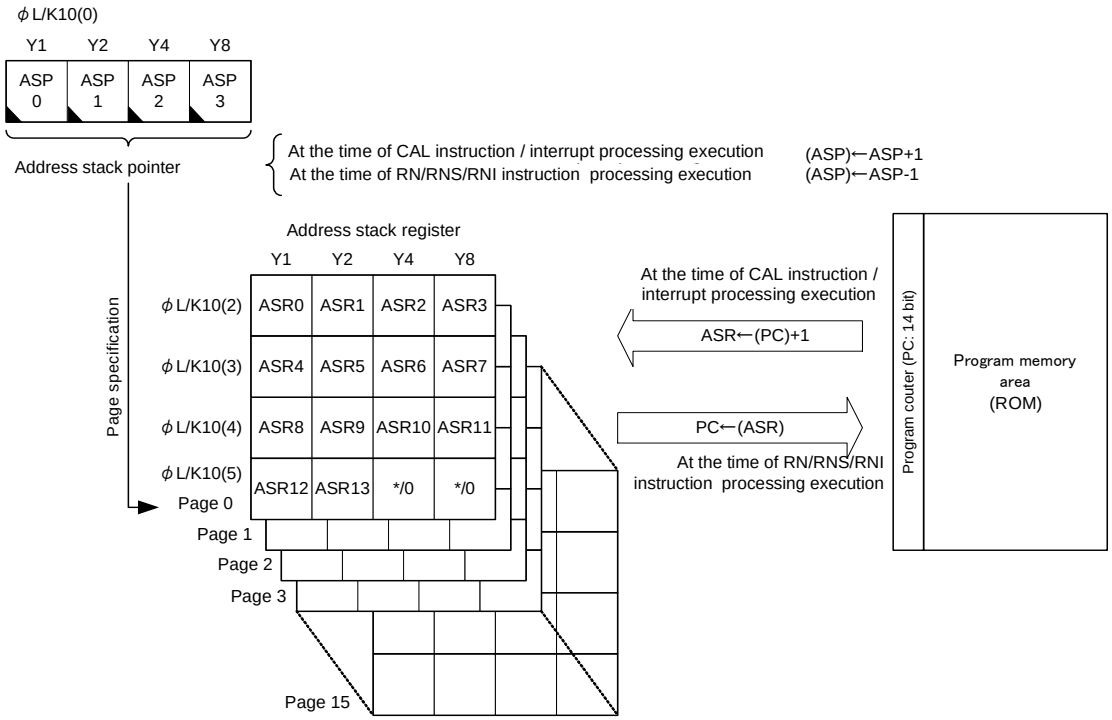
The stack register consists of an address stack register (ASR) and an interruption stack register (ISR). A stack register is used when subroutine call instructions and interrupt processing are executed. Interrupt stack registers comprise 26 G-register, data select, carry flag, and data register bits, as described in the register port item and I/O map. These stack registers are arranged on an I/O map, and are read from and written into with input and output instructions.

1. Address stack register (ASR)

The address stack register (ASR) is a 14 bit × 16 page register. When the subroutine call instruction and the interrupt processing are executed, the value increased by +1 of the content of the program counter, i.e., the return address, is stored in the address stack register. When interrupt processing is executed, a return address that is an interrupt processing execution address is stored in the address stack register. This register consists of 16 pages and is specified by four address stack pointer (ASP) bits. If transmitted to an address stack, an address stack pointer will be adjusted by -1. Then, after processing of the subroutine or interrupt, the address stack pointer is increased by +1 with the RN/RNS instruction or the RNI instruction, the content of the address stack register is transmitted to the program counter, and the program returns from the subroutine or the interrupt processing.

An address stack register comprises 16 pages and features 16 nesting levels.

The address stack register and the address stack pointer are arranged on the I/O map, and their contents can be referred to or rewritten.



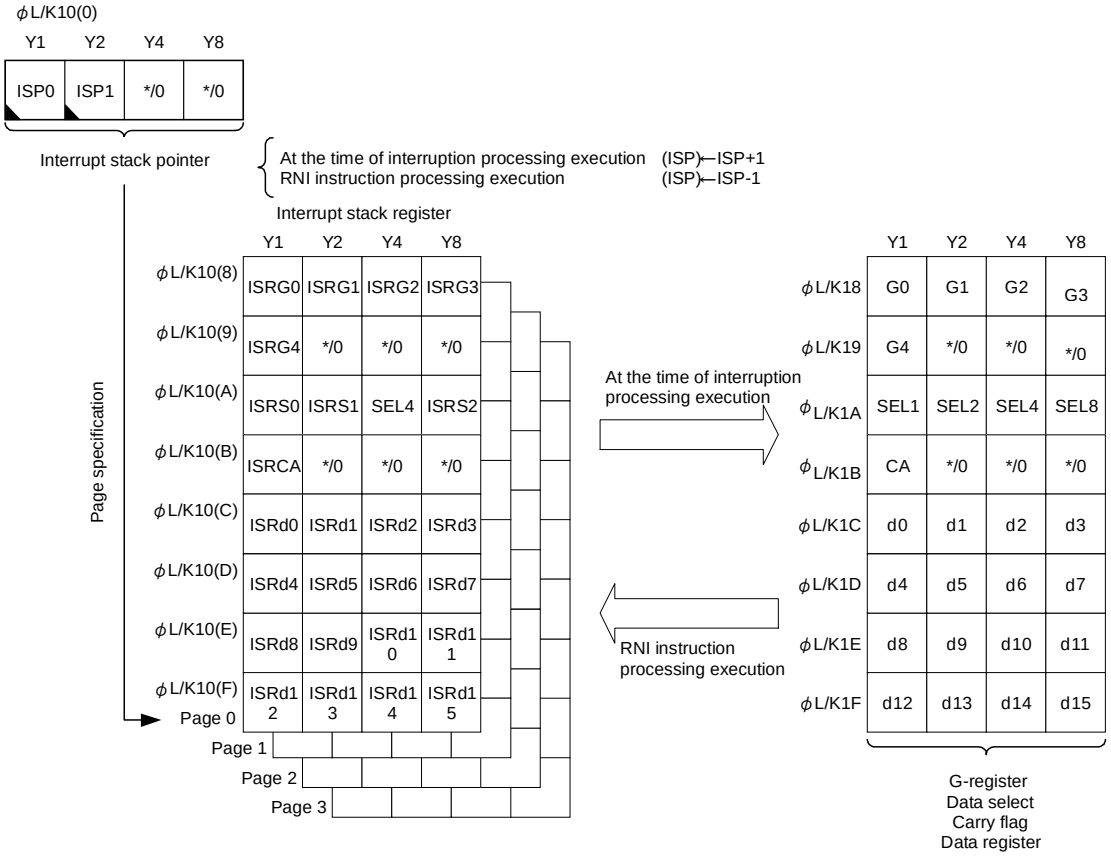
Note: The program memory area consists of 16 kilobytes, and 13 bits are used. Therefore set the most significant bit (ASR13) to “0”.

2. Interrupt stack register (ISR)

The interrupt stack register (ISR) is a 14 bit × 16 page register. When interrupt processing is executed, the contents of the 26-bit G-register, data selection, carry flag, and data register are stored automatically. This register consists of four pages and is specified with a two-bit interrupt stack pointer (ISP). When interrupt is generated, the G-register and other 26-bit register contents are transmitted to the interrupt register. Simultaneously, the interrupt stack pointer is adjusted by -1. When the RNI instruction is executed after the interrupt processing is finished, G-register and other 26-bit register contents are returned and the interrupt stack pointer is increased by +1. In this way, the interrupt stack register (ISR) is used as a save register for when interrupt occurs.

The Interrupt Stack register consists of four pages, and there are four interrupt stack levels.

The interrupt stack register and the interruption stack pointer are arranged on the I/O map, and their contents can be referred to and rewritten.

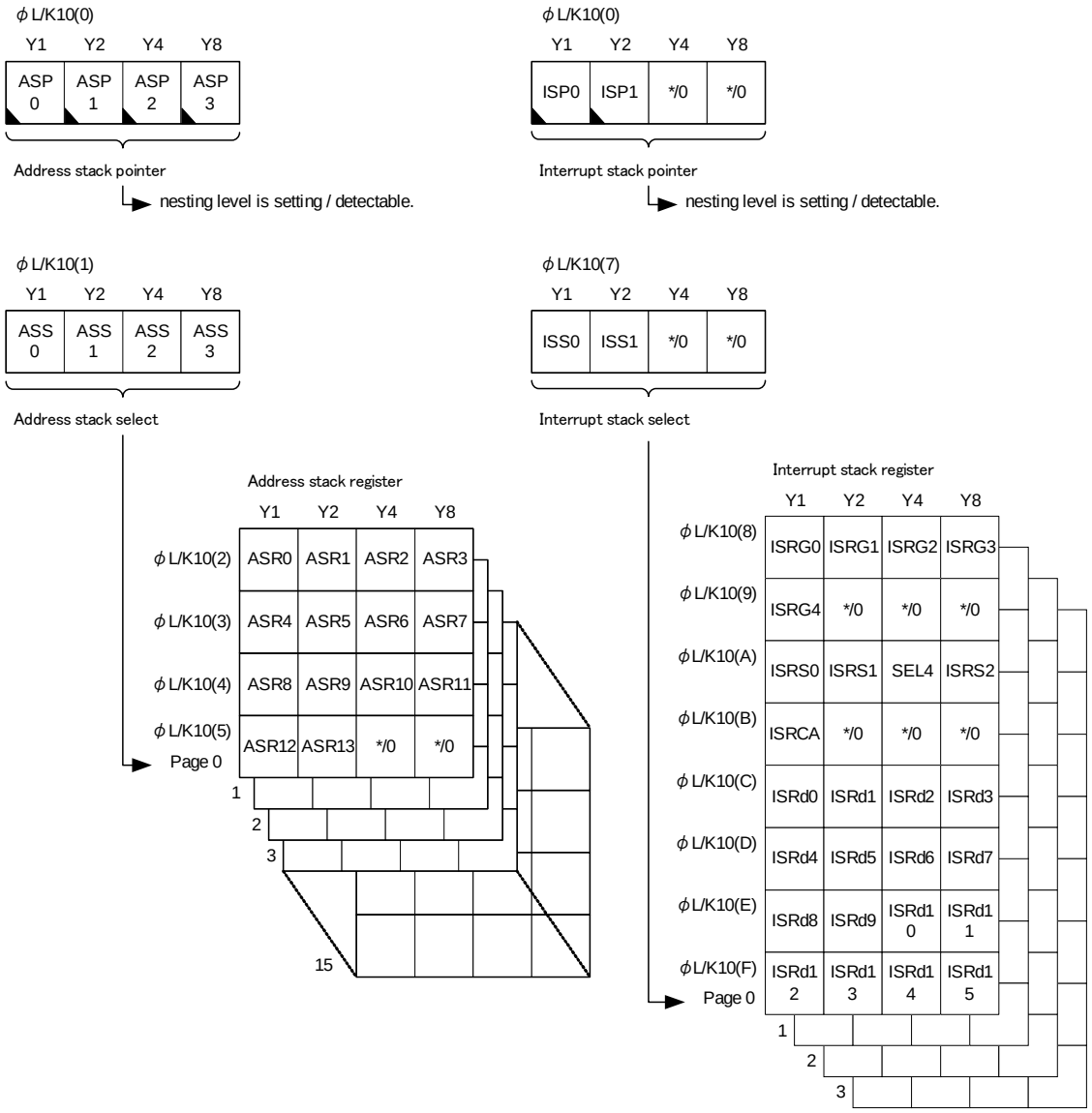


3. I/O access of a stack register

The stack register is arranged in the I/O map. Therefore reading the state of the stack register and rewriting data are possible. The contents of an address stack pointer (ASP) or an interruption stack pointer (ISP) can also be accessed. These data are accessed with an OUT1/IN1 instruction for which [CN = 0H] is specified for the operand, and divided and arranged by the data selection function.

The address stack register and the interrupt stack register have 16 and four pages respectively. When these ports are accessed with the I/O instruction, the page is specified before the stack register is accessed. The address stack selection specifies the page of the address stack register. The interrupt stack selection specifies the page of the interrupt stack register.

Rewriting of address stack registers is set from low-ranking bit, while the 14 address stack register bits are updated by accessing high-ranking bits. Therefore care is required: it is still necessary to access the high-ranking bits even when only low-ranking bits are being changed.



Note: The program memory area is 16 kilobytes and 13 bits are used. Therefore it is necessary to set the most significant bit (ASR13) of the address stack to "0".

○ Interrupt function

There are six types of peripheral hardware for which the interrupt function can be utilized: the INTR1 terminal, the INTR2 terminal, the timer port, the serial interface, the timer counter, and the decreased voltage detection circuit.

This peripheral hardware will issue an interrupt request signal if certain conditions are satisfied. On reception of an interrupt, the data for the G-register, data selection, carry flag, and data register are shunted to an interrupt stack register, and the return address is shunted to the address stack register. The process then branch to the vector address determined by the various interrupt factors and starts the related interrupt processing routine.

The interrupt routine requires preprocessing and post-processing to enable recovery of the same operational state that prevailed when the interrupt occurred. On interrupt, the G-register, data selection, carry flag, and data register are automatically shunted to the interrupt stack register; they are returned from the interrupt stack register on execution of the return instruction for interrupt (RNI). Registers used with other ALU and memory data that cannot be broken must be shunted to and recovered from the data memory for interrupt through the use of programming.

Interrupt priority can be set through programming. During interrupt processing, processing of an interrupt with a priority lower than the interrupt currently being processed is prohibited.

The data of the interrupt stack register and the address stack register return on executing of the return instruction for interrupt (RNI), and the interrupt processing ends.

1. Interrupt control circuit

The interrupt control circuit consists of an interrupt enable flag, interrupt latch, and interrupt priority circuit block. These performs are set and controlled with OUT2/IN2 instructions.

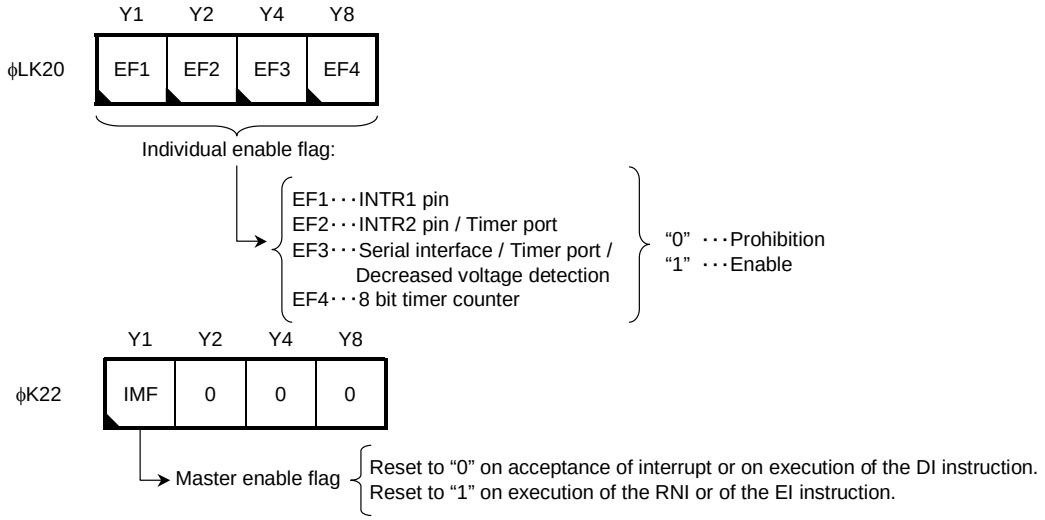
(1) Interrupt enable flags

The interrupt enable flags consist of individual enable flags corresponding to the four interrupt factors, and a master enable flag, which permits and prohibits the whole interrupt processing. The individual enable flags permit and prohibit interrupt corresponding to each interrupt factor. The enable registers of these flags indicate permission if set to “1”, prohibition if reset to “0”.

An individual enable flag is accessed with OUT2/IN2 instructions for which [CN = 0H] has been specified in the operand.

The interrupt master enable flag sets interrupt permission and prohibition. On execution of the EI instruction, the master enable flag is set to “1” and interrupt is permitted. On execution of the DI instruction, the master enable flag is reset to “0” and interrupt is prohibited. When an interrupt request permitted by the individual enable flag is issued in the interrupt-enabled state, the CPU receives the interrupt and, by branching to the different vector addresses, executes the interrupt routine. In interrupt reception processing and interrupt return processing, the master enable flag is in the hold state. When all other interrupts are to be prohibited during interrupt processing, therefore, the DI instruction is executed and interrupt is prohibited.

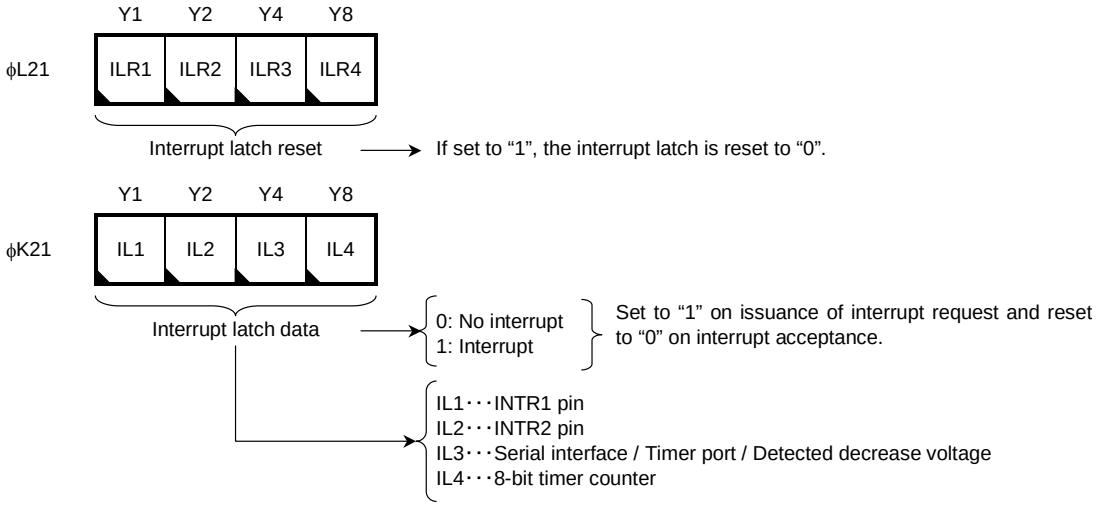
The interrupt master flag can be read into a data memory by an IN2 instruction for which [CN = 2H] is specified in the operand.



Note: Do not change the setting of the individual enable flag during interrupt processing.

(2) Interrupt latch

The interrupt latch is set to “1” through the issuing of an interrupt request from peripheral hardware. If interrupt is enabled, an interrupt reception request will be sent to the CPU, which will execute the interrupt routine and carry out branching. The data latch is automatically reset to “0” if an interrupt is received at this time. Interrupt latch data can read by the program and the existence or nonexistence of an interrupt request can be determined on an individual basis. An interrupt latch that has been set to “1” by interrupt request can also be reset to “0”, and the interrupt request can be canceled or initialized.

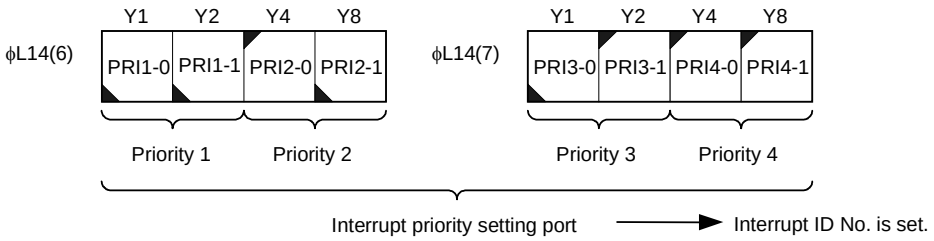


Note: Do not execute interrupt latch reset during interrupt processing.

(3) Interrupt priority circuit block

The interrupt priority circuit is a circuit that determines the order in which interrupts are processed if interrupt requests occur simultaneously or if interrupt is enabled after multiple interrupt requests have occurred. Vector addresses to the interrupt routine are also generated by this block. The interrupt priority level can be set through programming. The priority level is determined by setting the interrupt ID No. corresponding to each interrupts factor to the interrupt priority level setting port. The interrupt priority level setting ports are composed of priority levels 1 to 4, and the circuit sets the interrupt ID No. in order of the priority levels 1 to 4. For instance, when the interrupt priority level is set in the order of serial interface (2), INTR1 pin (0), INTR2 pin (1) and timer counter (3), then 2h, 0h, 1h, and 3h (ϕL14(6) = 2h, ϕL14(7) = dh) are set to priority levels 1 to 4. These ports can be accessed with an OUT1 instruction for which [CN = 4H] is specified in the operand and 6h and 7h are specified for the data selection ports (ϕK/L1A).

Interrupt ID No.	Interrupt Factor	Vector Address
0	INTR1 pin	0001H
1	INTR2 pin / timer port	0002H
2	Serial interface / timer port / decreased voltage detection	0003H
3	Timer counter	0004H



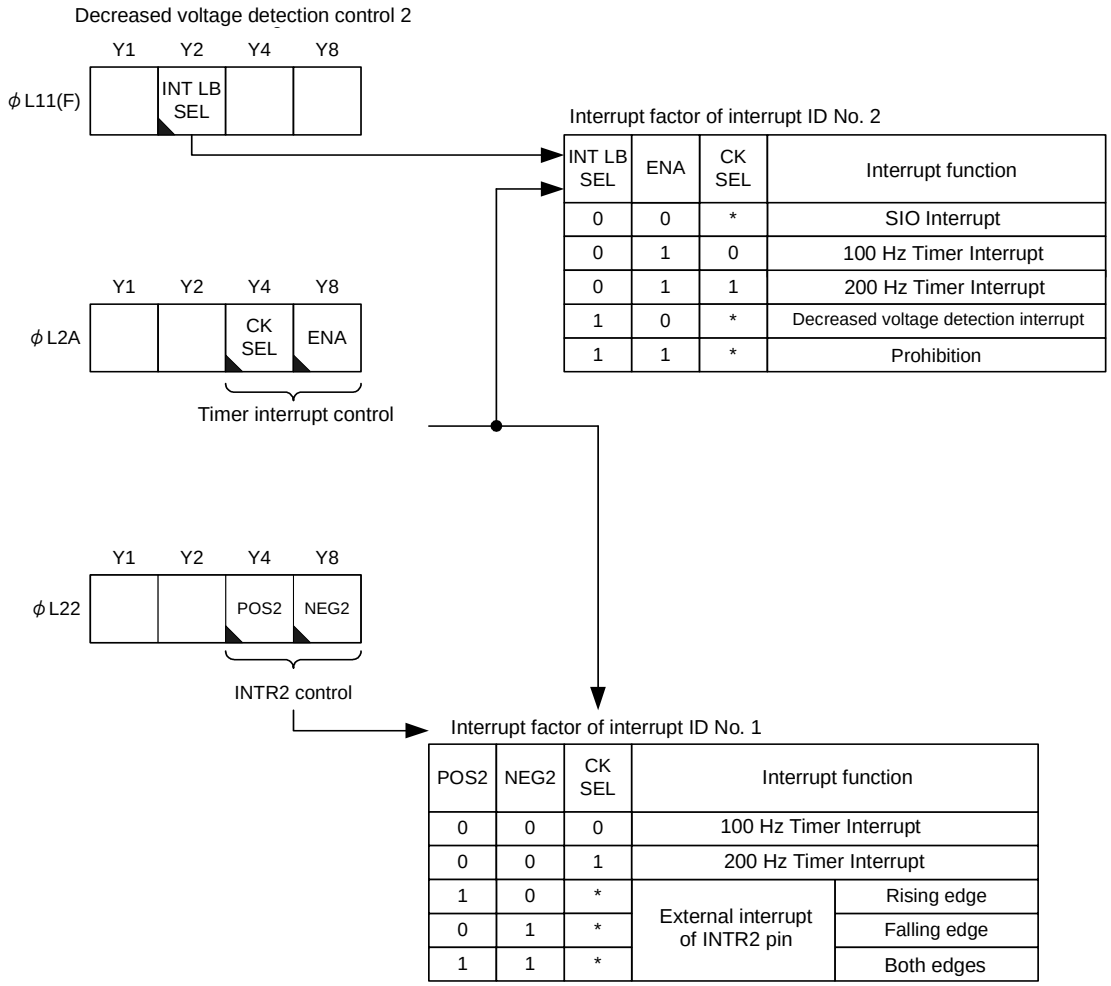
Note: Do not set the same interrupt ID No. to each interrupt priority level.

Note: Do not change the interrupt priority setting during interrupt permission and interrupt processing.

Note: Interrupt priority after system reset reverts to an order corresponding to that of the interrupt ID No.’s (i.e., ID No. 0 → Priority Level 1).

(4) Change of interrupt factor

From among the ID numbers, ID Nos. 1 and 2 can be used to select, respectively, INTR2 pin / timer port and serial interface / timer port / decreased voltage detection. These changes are made through the control port in each block. Since selection is possible through the following settings, select according to the specification. These settings are also made when routine initialization is being carried out. Do not perform the change while interrupt enable or interrupt processing is in progress. Carry out any change in a state other than these states, and always reset the interrupt latch after the change.



INT LB SEL	ENA	CK SEL	Interrupt function
0	0	*	SIO Interrupt
0	1	0	100 Hz Timer Interrupt
0	1	1	200 Hz Timer Interrupt
1	0	*	Decreased voltage detection interrupt
1	1	*	Prohibition

POS2	NEG2	CK SEL	Interrupt function	
0	0	0	100 Hz Timer Interrupt	
0	0	1	200 Hz Timer Interrupt	
1	0	*	External interrupt of INTR2 pin	Rising edge
0	1	*		Falling edge
1	1	*		Both edges

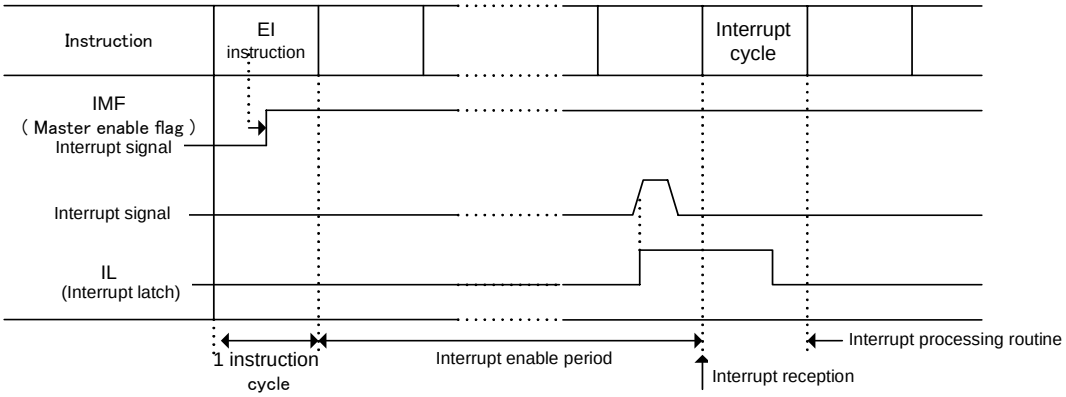
2. Interrupt Reception Processing

The interrupt request is held until interruption is received, it interrupts by system reset operation or the program and it resets a latch to "0" through programming. Interrupt reception operation is as shown below.

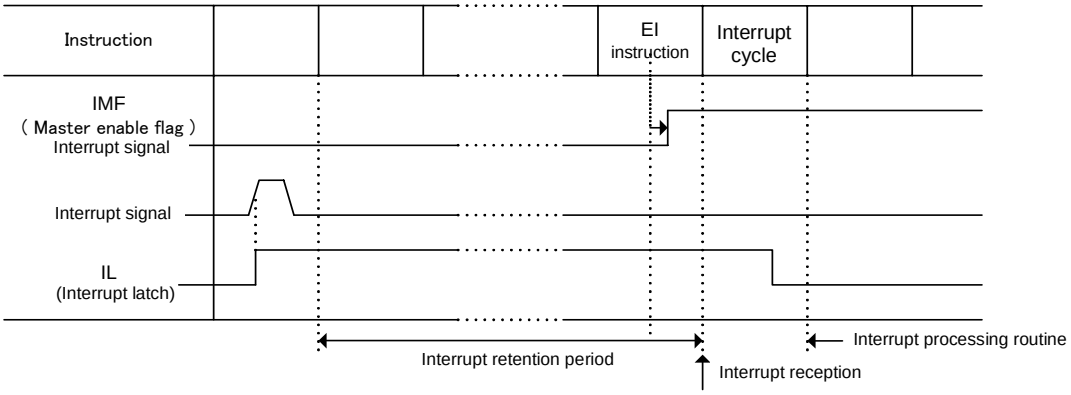
1) Each item of peripheral hardware outputs each interrupt request and sets the interrupt latch to “1” if the interrupt conditions are fulfilled.
2) If an interrupt enable flag corresponding to a particular interrupt factor or a master enable flag is set to “1”, the CPU receives its interrupt, and the corresponding interrupt latch is reset to “0”.
3) Any interrupt with a priority level below the accepted interrupt factor is prohibited.
4) The contents of the address stack pointer (ASP) and the interrupt stack pointer (ISP) are adjusted by -1.
5) The contents of the program counter (PC) are evacuated to the address stack register. The contents of the carry flag (Ca), G-register (G-REG), data selection and data register (DATA) are evacuated to the interrupt stack register. At this time, the contents of the program counter change to the next address for the time the interrupt was received or the next address for which interrupt was enabled.
6) The contents of the vector address corresponding to the received interrupt are transferred to the program counter.
7) The contents of the vector address are executed.

Steps 2) to 6) are executed in one instruction cycle. This instruction cycle is called an “interrupt cycle”.

In the case of an interrupt enable period



In the case of an interrupt retention period



3. Return Processing from the Interrupt Processing Routine

The only RNI instruction is used to return the operational state to the processing being carried out before reception of the interrupt from the interrupt routine.

Execution of the RNI instruction causes the following processing to be carried out automatically in sequence.

1) Interrupt of the priority below the returning interrupt factor is permitted.
2) The contents of the interrupt stack register specified by the interrupt stack pointer are returned to the G-register, data selection, carry flag, and data register; and the contents of the address stack register data specified by the address stack pointer are returned to the program counter.
3) The contents of the address stack pointer (ASP) and the interrupt stack pointer (ISP) are adjusted by +1.

The RNI instruction for the above-mentioned processing is processed in one instruction cycle.

Note: Always execute the return from interrupt using the RNI instruction.

4. Interrupt Processing Routine

If interrupt has been permitted, the CPU accepts the interrupt request regardless of the program executed at that time when the interrupt request is issued. To return to the original program on execution of interrupt processing, therefore, it is necessary to restore the original operational state, as if interrupt processing had not occurred. For this reason, it is necessary to perform shunting and return operations within the interrupt processing routine, at least for those register and data memories that can be operated within the interrupt processing routine.

(1) Evacuation processing

When the CPU accepts the interrupt, it automatically evacuates the content of G-register, data selection, carry flag and data register to the interrupt stack register. The contents of the area of the data memory and the general register used by the interrupt processing routine are evacuated as necessary by the program before use

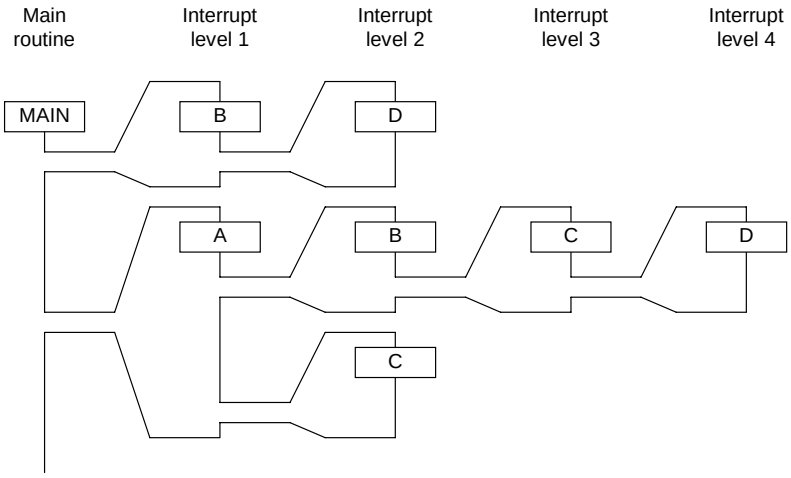
(2) Return processing

The contents of the G-register, data selection, carry flag, and data register return automatically when the RNI instruction is executed. Therefore the return processing works in the opposite way to that of the evacuation processing previously mentioned.

5. Multiplex Interrupt

Multiplex interrupt is a method of processing other interrupts during interrupt processing.

As shown in the figure, the separate interrupt factors C and D are processed during the interrupt processing of interrupt factors A and B. The depth of interrupt at this time is called the interrupt level.



Example of multiplex interrupt

Exercise particular care regarding the following points when using multiplex interrupt:

1) The priority of the interrupt factors
2) Restrictions on the address stack levels used when interrupt requests are issued.
3) Shunting processing for the carry flag, data memory, etc.

(1) Priority of interrupt factor

The order of priority for multiplex interrupt becomes A < B < C < D as shown in the figure.

When an order of priority of this type applies, the processing of interrupt C must have priority during the interrupt processing of A or B, while the processing of interrupt D is in turn given priority during execution of interrupts C.

Multiplex interrupt requires the setting of priority levels. For example, for interrupt factors A and B, let us assume that a request is issued for factor A every 10 ms, with an interrupt processing time of 4 ms; and that a request is issued for factor B every 2 ms, with an interrupt processing time of 1 ms. When there is no order of priority for A and B, then, should an A interrupt request occur during the interrupt processing of B, it may sometimes be the case that the A interrupt processing is executed and the B interrupt processing is not. In such a case, it is necessary to set the order of priority of A < B through programming and prohibit any A interrupt during interrupt processing of B, and also allow a B interrupt to be received even during the interrupt processing of A.

Priority ordering of this kind is set through the priority level ports (ϕL14(6), ϕL14(7)), described in the item on the interrupt priority circuit block. Setting interrupt priority in the order of factors A < B < C < D prohibits during the processing of a prioritized interrupt any interrupt with the same priority level or lower. For example, all interrupts are prohibited during factor D interrupt, while during processing of a factor C interrupt, factor D interrupt is enabled while factor A, B and C interrupts are prohibited. Any change in the interrupt order is prohibited during the processing of an interrupt. To prohibit the acceptance of a higher-priority interrupt factor during the execution of a lower-priority interrupt, use a DI/EI instruction to prohibit interrupt in the program area where prohibition is required.

(2) Restriction of address stack levels

As described in the section on interrupt reception processing, when an interrupt request is issued, the return address is automatically evacuated to the address stack register; and the G-register, data selection, carry flag and data register are automatically evacuated to the interrupt stack register. There are four interrupt stack levels and 16 address stack levels. The content of the interrupt stack register and the address stack register is broken when the interrupt stack levels and the address stack levels are exceeded; it is therefore necessary to use them in such a way to ensure they are not exceeded. Since it can also be used with the execution of a subroutine call command, the address stack register should take into account the address stack levels for both interrupt and subroutine calls.

(3) Evacuation processing

When using multiplex interrupt, it is necessary to secure the evacuation area for evacuation processing separately for each Interrupt factor.

○ External Interrupt and Timer Counter Functions

There are two types of pin for external interrupt: INTR1 and INTR2. An interrupt request is issued on detection of the edge of the signal applied to pins INTR1 and INTR2, whether rising, falling or both. The interrupt input pins also combine the functions of I/O port; break during backup; and, in the case of the INTR2 pin, PLL $\overline{\text{INH}}$ input pin.

The timer counter is an 8-bit binary counter and has timer mode and pulse width measurement mode functions. In pulse width measurement mode, the pulse width input from the external interrupt pin (INTR1) is measured. This can be used for purposes such as detecting the leader pulse of a remote control.

1. External Interrupt Function

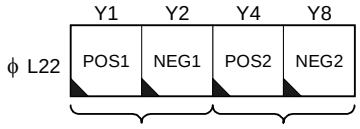
There are two types of pin for external interrupt, INTR1 and INTR2, and an interrupt request is issued on detection of the edge of these inputs. The inputs incorporate a Schmitt circuit and a noise canceller, the frequency of the CPU clock (low-speed oscillation clock: 75 kHz; high-speed oscillation clock: 300 ~ 600 kHz) being used for the noise-filtering clock. Any pulse of less than 1 ~ 3 clocks of the CPU clock is removed as noise; and an interrupt is generated when a pulse at or over 1 ~ 3 clocks of the CPU clock (at the time of a 75 kHz oscillation: 13.3 ~ 40 μs) is input. Either the rising or the falling edge, or both, can be selected for each pin.

The pin used for the external interrupt function also serves as an I/O port. Interrupt will be permitted if edge selection is enabled through use of the external interrupt control port. The external interrupt input state can be read from the I/O port 4 input data port (ϕK33), which is used in combination.

The INTR1 pin is used in combination with the input pin of the pulse width measurement mode function of the timer counter. The INTR1 control port is also used to control the logical setting of the pulse.

(Refer to the section on the timer counter.)

The external interrupt of the INTR2 pin is selected together with the timer port interrupt. When external interrupt of the INTR2 pin is used, it is necessary to set the timer port. (Refer to the sections on the timer port and on changing the interrupt factor.) The program will branch to address 0001H if an INTR1 pin interrupt is received, to address 0002H if an INTR2 pin interrupt is received.



INTR2 external interruption / Control of timer port interruption

POS2	NEG2	Interrupt Function	Edge Select
0	0	100/200Hz timer interrupt	I/O port function
1	0	External interrupt of INTR2 pin	Rising edge
0	1		Falling edge
1	1		Both edges

Control of INTR1 external interruption

POS1	NEG1	Interrupt Function	Edge Select
0	0	External interrupt prohibition	I/O port function
1	0	External interrupt of INTR1 pin	Rising edge
0	1		Falling edge
1	1		Both edges

Note: The function becomes effective when $\overline{\text{INH}}$ input function and break function are permitted on setting of the external interrupt function.

Note: When interrupt is permitted, the I/O port 4 control port becomes invalid and is forced to change to an input port.

2. Timer Counter Function

The timer counter consists of an 8-bit binary counter, a counter coincidence register, a digital comparator, and a control circuit for controlling these items.

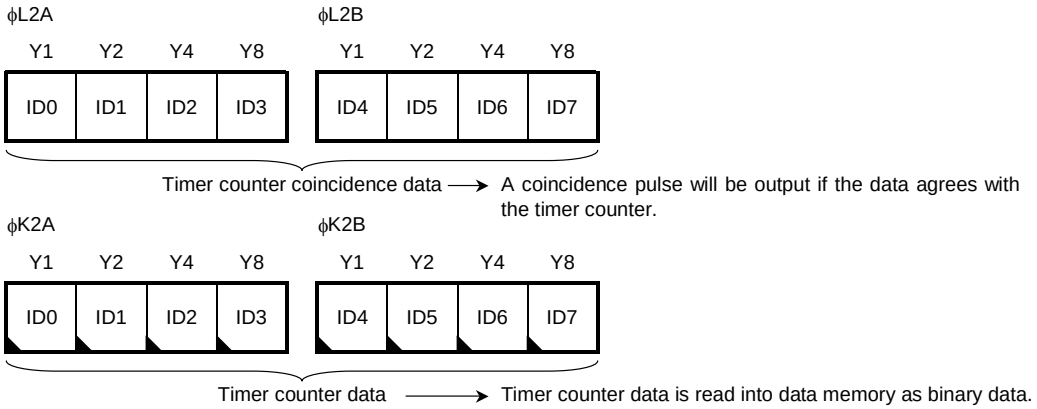
The timer counter function has a timer mode and a pulse width measurement mode.

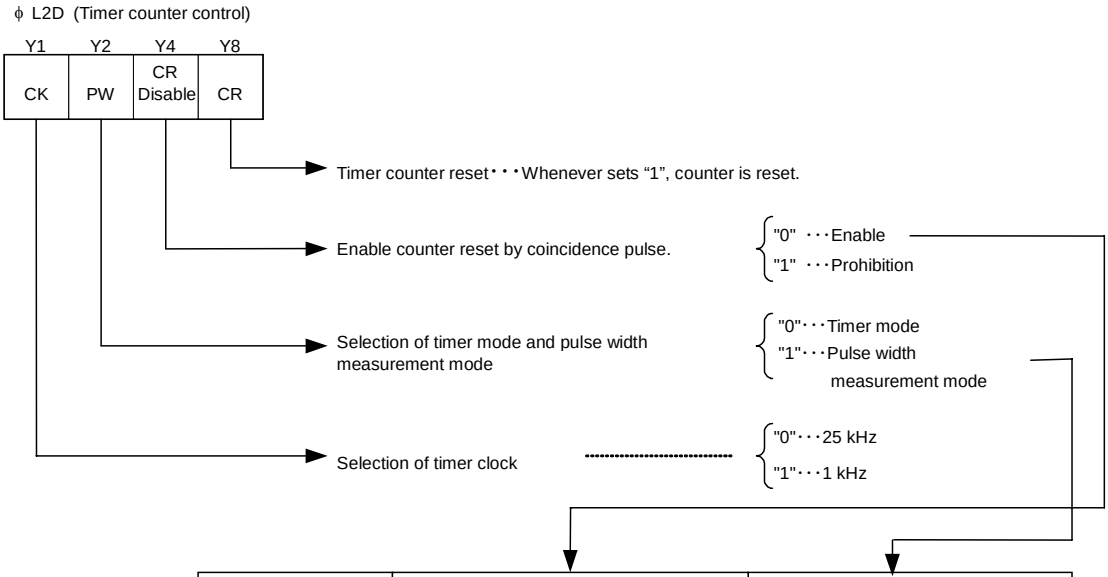
The timer mode is a mode for detecting a regular time. The coincidence signal pulse is output and the interrupt request is issued when the timer clock is input to the 8-bit binary counter and is in agreement with the contents of the counter coincidence register. In pulse width measurement mode, measurement of pulse width and detection of pulse width are performed through calculation of the timer counter between "H" or "L" levels input from the INTR1 pin. Pulse width detection can be used to detect the leader pulse of remote controls.

For both timer mode and pulse width measurement mode, a timer clock of 25 kHz or 1 kHz can be used.

(1) Timer counter register configuration

The timer counter register consists of counter data, a coincidence register and a control register.





INTR1 control (ϕ L22)		Clock enable logic of INTR1 input signal (Effective only when CR Disable = 0 is set.)	Reset condition of INTR1 input signal (Effective only when CR Disable = 0 is set.)
POS1	NEG1		
0	0	Not counted	—
1	0	Counted in “H” level	Falling edge
0	1	Counted in “L” level	Rising edge
1	1	Always in operation	Both edges

Note: This becomes invalid when the settings CR Disable = 1 and PW = 0 apply as above.

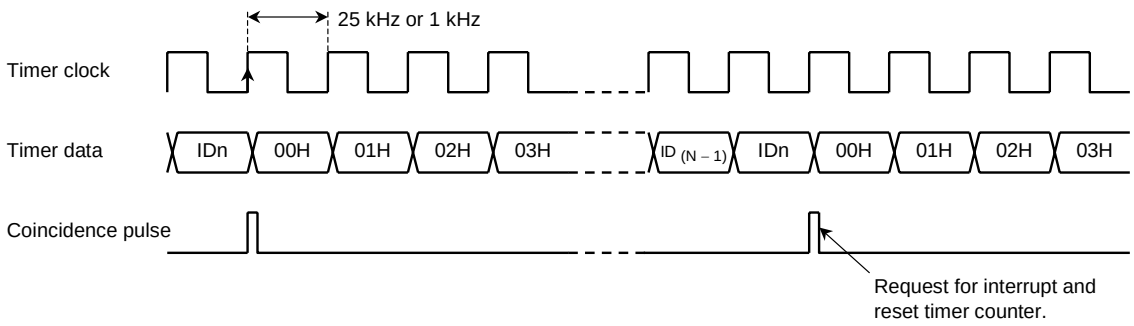
(2) Timer mode

Timer mode is a mode for detecting a regular time. Whenever the regular time is detected, an interrupt request is executed and the counter reset. At this time, the control bit is set to 25 kHz or 1 kHz, the PW bit to “0”, and the CR bit to “0”.

At this time, the timer coincidence data is

Timer time = IDn (coincidence data) × timer clock cycle IDn ≧ 1 (HEX)

This sets the data for required timer interval.



(3) Pulse width measurement mode

Pulse width measurement mode enables the detection and measurement of the “H” or “L” pulse width of the INTR1 input.

The control bit at this time is used to select 1 kHz or 25 kHz for the timer clock and set “1” to the PW bit. If the PW bit is set to “1”, the INTR1 input becomes the input enable signal of the counter clock and the timer clock is input to the timer counter in the enabled state. Then, if the coincidence data values and counter values match, a timer interrupt is issued.

The input logic is used in combination with the external interrupt logic setting (POS1/NEG1 bit).The timer counter is “H” level if the POS1 bit and NEG1 bit are set to “1” and “0” respectively; and “L” level if the POS1 bit and NEG1 bit are set to “0” and “1” respectively.

- Pulse width detection

The pulse width detection function detects a pulse width equal to or greater than a regular pulse width. This function can be used for detection of the leader pulse of remote controls and data detection. At this time the control bit is set to “0” for the GR Disable bit, and the timer counter is automatically reset on completion of pulse width measurement. With automatic reset, no timer interrupt will be issued when the pulse width is below the set value. Only on input of a pulse equal to or greater than the detection pulse width is a timer interrupt issued and detection enabled. This feature enables the detection of data from remote control devices when used in combination with external interrupts.

The detection pulse width at this time is as follows:

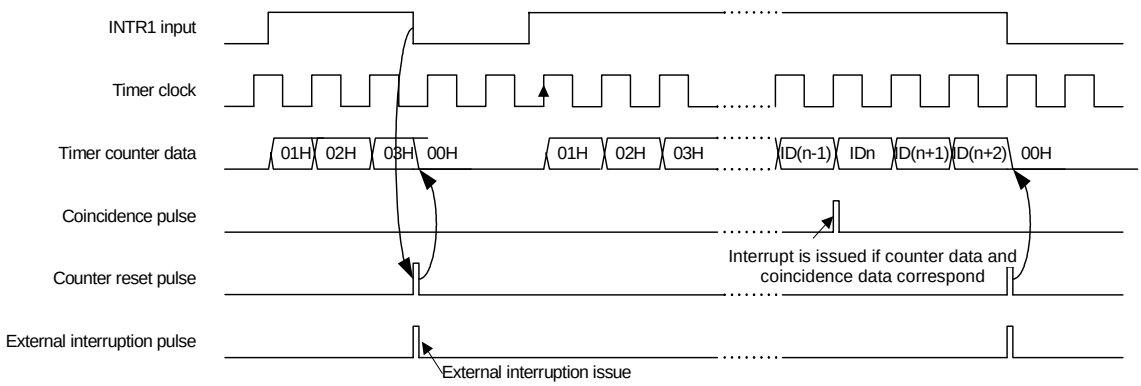
Detection pulse width = Idn (coincidence data) × the cycle of timer clock Idn ∞ 1(HEX)

- Measurement of pulse width

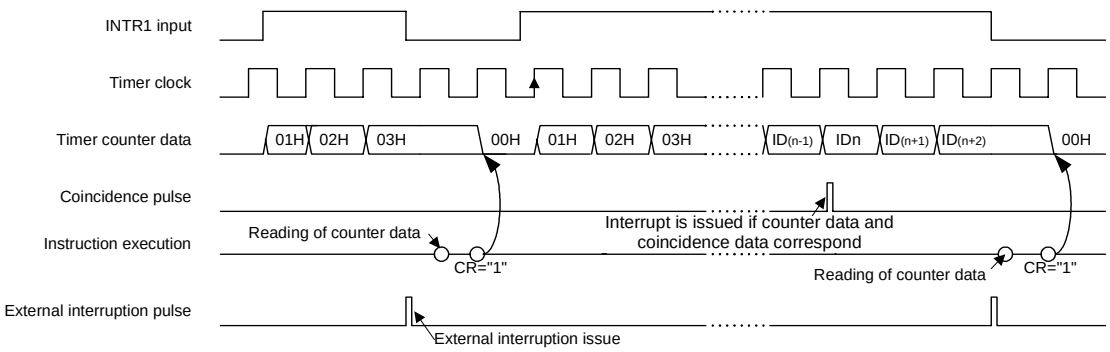
When the pulse width is being measured, the CR Disable bit of control bit is set to “1”, setting to prohibited status the execution of reset to the timer counter when pulse width measurement is finished. On completion of pulse width measurement, the issuing of the external interrupt is detected, and the pulse width can be measured by referencing the timer counter value. The pulse width at this time is as follows:

Pulse width = CTn (timer counter data) × the cycle of timer clock

After reading of the timer counter data (CR = “1”), the timer counter is reset and initialized.



Example of timing of pulse width detection operation in pulse width measurement mode (CR Disable = “0”)



Example of timing of pulse width detection operation in pulse width measurement mode (CR Disable = “1”)

Note: The counter is reset whenever the CR bit is set to “1”. Execute reset if necessary.

Note: The end of measurement can be detected through the concomitant use of external interrupt.

○ Internal Interrupts and the Interrupt Function

There are four types of internal interrupt: timer port, timer counter, serial interface, and decreased voltage detection. Of these, three types of interrupt: timer port; serial interface; and decreased voltage detection; can serve a double purpose and act as interrupts for other factors. Select and use the necessary interrupt factor.
(Refer to the section on changing the interrupt factor.)

1. Timer Port Interrupt

The timer port interrupt is generated on the rising edge of a 100 Hz or 200 Hz timer. For details, refer to the item on the timer port function.

2. Timer Counter Interrupt

The timer counter interrupt is generated if the timer counter value corresponds to the coincidence register value. For details, refer to the item on the timer counter function.

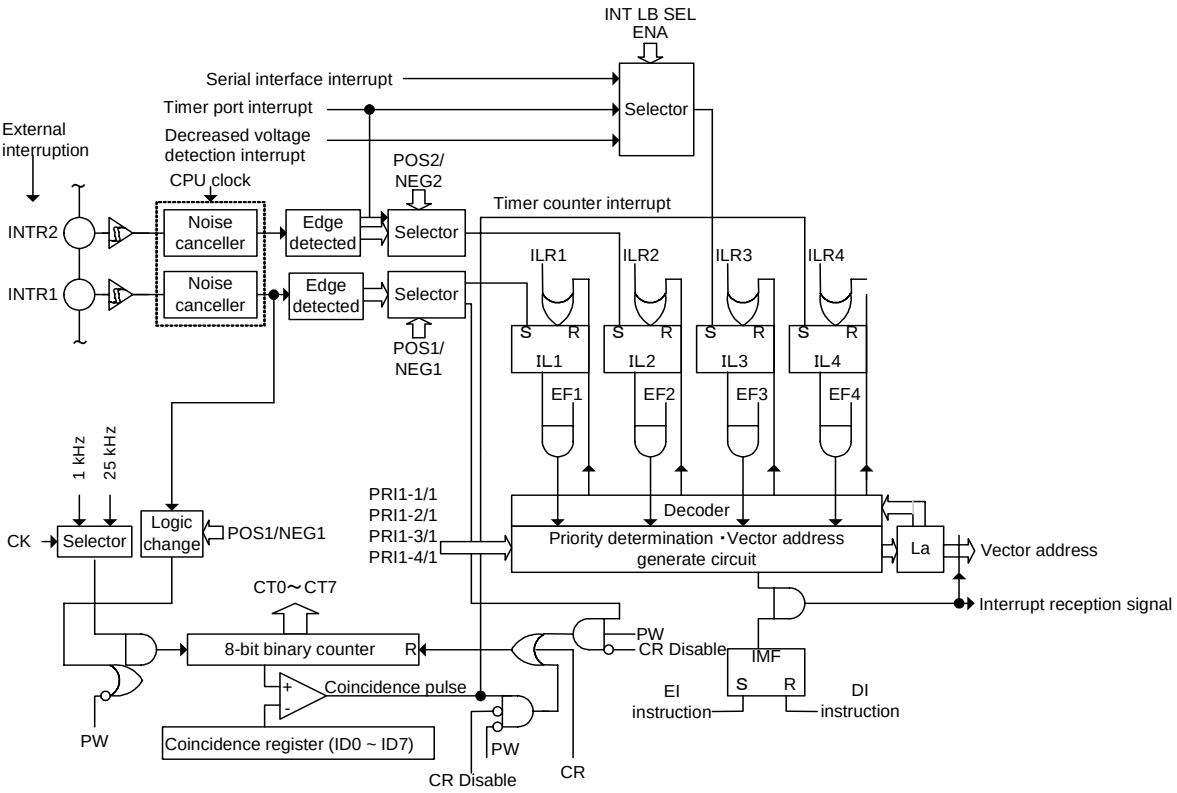
3. Serial Interface Interrupt

The serial interface interrupt is generated on the ending of serial interface operation. For details, refer to the item on the serial interface function.

4. Interrupt for Decreased Voltage Detection

The interrupt for decreased voltage detection is generated on detection of decreased voltage. For details, refer to the item on the decreased voltage detection function.

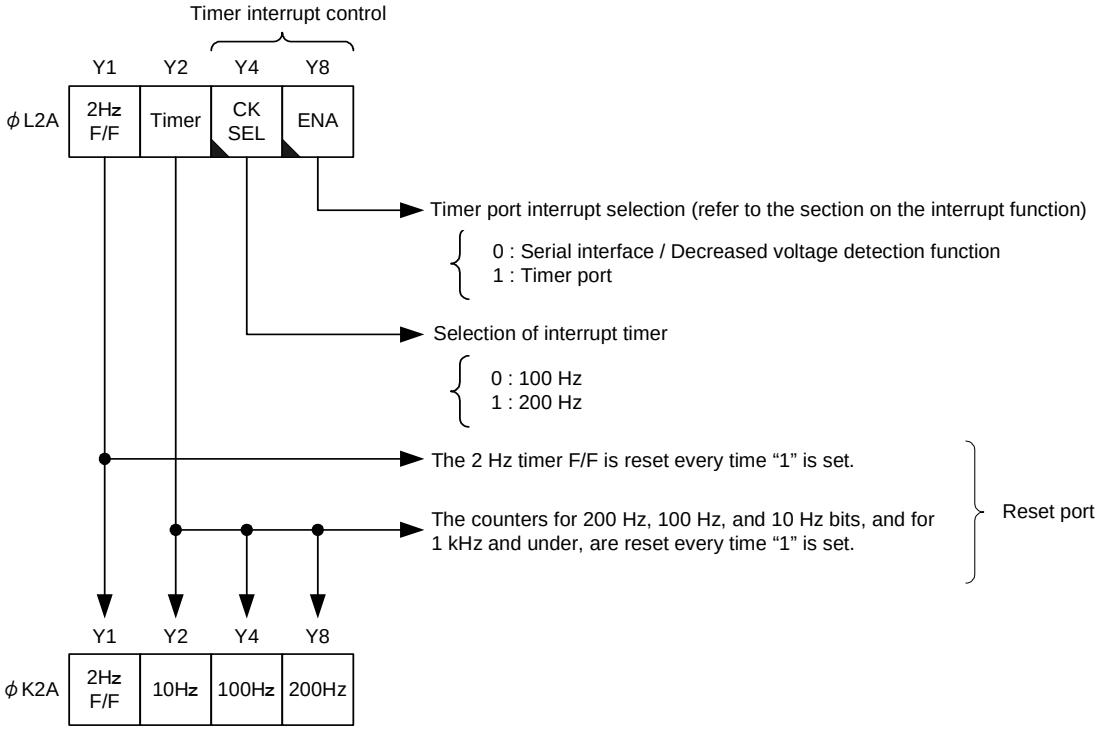
5. Interrupt Block Configuration



○ Timer port

Equipped with 200 Hz, 100 Hz, 10 Hz and 2 Hz F/F bits, the timer is used for counting of clock operations and of tuning scan mode. Through selection in the timer port for interrupt, interrupts can be generated with a 100 Hz or 200 Hz rising edge.

1. Timer port

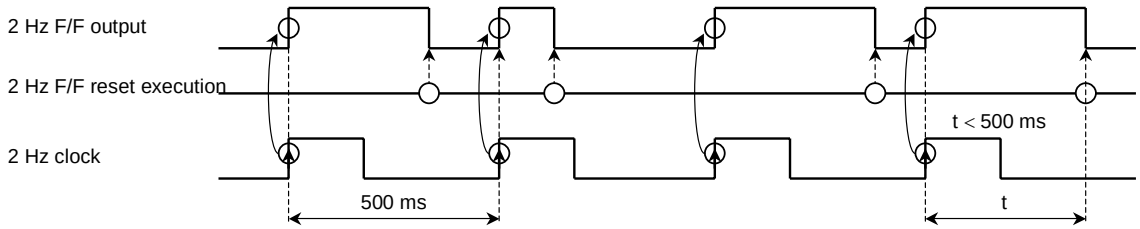


The timer ports are accessed with an OUT2/IN2 instruction for which [CN = AH] has been specified in the operand.

2. Timer port timing

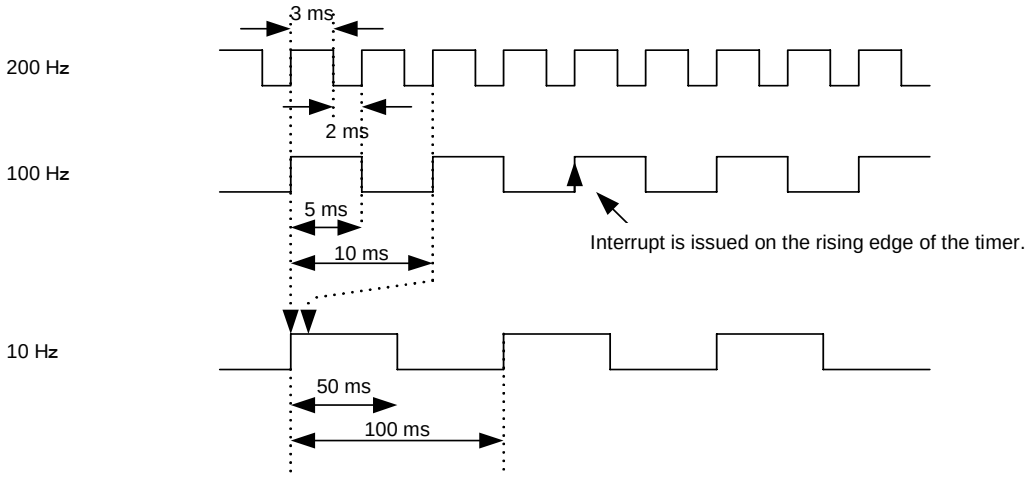
The 2 Hz timer F/F is set with the 2 Hz (500 ms) signal and is reset by setting "1" in the 2 Hz F/F of the reset port. This bit is usually used as a clock counter.

The 2 Hz timer F/F can only be reset with the 2 Hz F/F of the reset port; therefore not resetting within a 500 ms cycle will result in count errors and failure to obtain the correct time.



The 10 Hz, 100 Hz and 200 Hz timer is output to 10 Hz, 100 Hz and 200 Hz bits respectively with frequency pulses of 100 ms, 10 ms and 5 ms respectively. The 10 Hz and 100 Hz timers have a duty cycle of 50%. The 200 Hz timer is output at a duty cycle of 60% with a high level of 3 ms and a low level of 2 ms. Counters at 1 kHz or below will be reset whenever the reset port's timer bit is set to "1".

100 Hz or 200 Hz timer can be selected for the interrupt. When timer interrupt is enabled, interrupt is generated on the rising of this pulse. If interrupt is received, a program will branch to 0003H address.



○ Input and Output Ports

A maximum of 45 I/O ports are available for the input/output of control signals. These 45 I/O ports include 36 CMOS I/O ports and 9 N-ch open-drain I/O ports. Up to one exclusive input ports and two exclusive output ports are also available.

I/O port 3 can be set to the pull-down or pull-up state, while I/O ports 3, 4, 6 and 8 can be set to backup release (break function). Individual input and output ports also serve as the pins for peripheral equipment. Switch them according to the specifications.

1. I/O Ports, Input-only Ports (IN/IN2) and Output-only Ports (OT1/OT2)

Each of the I/O ports, exclusive input ports and exclusive output ports has the following dual-purpose functions and features.

I/O port		Pin Number	Combination and Additional Function		Input impression tolerance	Structure	Break Function
			Pin name	Funciton			
I/O port 6	P6-0 ~ P6-3	11 ~ 14	ADin1 ~ ADin3	6 bit A/D converter analog input	0~VDB (VDD × 2)	Nch	○
I/O port 10	P10-0 ~ P10-3	15 ~ 18	COM1 ~ COM3	LCD driver common output	0~VLCD (3V)	CMOS	—
I/O port 12	P12-0 ~ P12-3	19 ~ 22	S1 ~ S4	LCD driver segment output			
I/O port 13	P13-0 ~ P13-3	23 ~ 26	S5 ~ S8				
I/O port 14	P14-0 ~ P14-3	27 ~ 30	S9 ~ S12				
I/O port 15	P15-0	31	S13				
	P15-1	32	S14				
I/O port 16	P16-0	33	S15				
	P16-1	34	S16				
	P16-2	35	S17/Xin2	LCD driver segment output / High speed oscilattoer			
	P16-3	36	S18/Xout2				
I/O port 3	P3-0	37	SCK1/RX1	Serial interface (CMOS input and output)			○
	P3-1	38	SDIO1 / TX1				
	P3-2	39	SI1				
	P3-3	40	PCTRin	Pulse counter input			
I/O port 4	P4-0	41	INTR1	External interruption input / PLL inhibit input			
	P4-1	42	INTR2/$\overline{\text{INH}}$				
	P4-2	43	BUZR	Buzzer output			
	P4-3	44	VRout1	Electrical volume			
I/O port 5	P5-0	45	VRin1				—
	P5-1	46	VRcom				
	P5-2	47	VRin2				
	P5-3	48	VRout2				
Exclusive input port	IN	49	IFin	IF input	0~VPLL		
Exclusive output port	OT1	53	DO1/P	Phase comparator output	0~VDB (VDD × 2)		
	OT2	54	DO2/N/Tin				
I/O port 9	P9-0	55	Tout		0~5.5V	Nch	
	P9-1	56	MUTE	Mute output	0~VLCD (3V)	CMOS	
	P9-2	57	DDCK2 / TEST	DC - DC converter clock output for VT / Test input			
I/O port 8	P8-0	58	VDET	DC - DC converter voltage detection input for VT	0~5.5V	Nch	○
	P8-1	59	DDCK1	The DC-DC converter clock output for VT			
			SI2	Serial interface (Nch open drain input and output)			
	P8-2	60	SCK2 / RX2				
	P8-3	61	SDIO2 / TX2				

I/O port 3 is a CMOS I/O port. Pins P3-0 to P3-2 are also used as the serial interface and pin P3-3 is also used as a pulse counter input pin. These pins can be set to pull-up or pull-down state and to the break function.
(→ Refer to the sections on Serial interface and Pulse counter.)

I/O ports 4 and 5 are CMOS I/O ports. Pins P4-0 and P4-1 are also used as external interrupt input pins. Pin P4-1 is also used as the PLL inhibit input pin. Pin P4-2 is also used as the buzzer output pin. Pins P4-3 and P5-0 to P5-3 are also used as the electronic volume pins. Pins P4-0 to P4-3 can be set to the break function.
(→ Refer to the sections on External interrupt, Back-up, Buzzer output and Volume.)

I/O port 6 is a N-ch open-drain I/O port. Voltage can be applied up to the V_{DB} pin level. This port is also used for the 6-bit A/D converter analog input, and can be set to the break function.
(→ Refer to the sections on A/D converter.)

I/O port 8 is an N-ch open-drain I/O port. Voltage can be applied up to 5.5 V. Pin P8-0 is also used as the doubler voltage detection input pin for the DC-DC converter of VT. Pin P8-1 is also used as the clock output pin for the DC-DC converter of VT. Pins P8-1 to P8-3 are also used as the serial interface. These pins can be set to the break function.
(→ Refer to the sections on the DC-DC converter of VT and Serial interface.)

I/O port 9 consists of the N-ch open-drain pin (P9-0) and the CMOS pins (P9-1 and P9-2). P9-0 is also used as the Tr output pin for LPF. Pin P9-1 is also used as the MUTE output pin. P9-2 is also used as the clock output pin for the DC-DC converter. In addition, pin P9-2 is pulled down to serve as the test mode input pin when pin $\overline{\mathrm{RESET}}$ is at the “L” level. This pin must be in the open state or at the “L” level during test mode input.
(→ Refer to the sections on MUTE output, DC-DC converter of VT and Phase comparator.)

I/O ports 10 to 16 are CMOS I/O ports, and also serve as the LCD driver output pins. Pins P16-2 and P16-3 are also used as high-speed oscillators. (→ Refer to the sections on the LCD driver and System clock control circuit.)

The exclusive input port is the IN input pin of IFin input combination. The IN input can be switched by the program.

The two phase comparator output pins can be used as the exclusive output ports (OT1/OT2). These pins output any of three values; an “H” level that is the V_{DB} pin level, “L” level and High impedance.

The I/O circuit of 41 pins at I/O ports 3, 4, 5, 8, 9 and 10 to 16 uses the V_{LCD} (3 V) power supply pin. Voltage can be applied up to 3 V, and a stable output current can be obtained because the output is not heavily reliant on the V_{DD} pin power supply. Pin IN2 of I/O port 6 can accept voltage up to the V_{DB} pin level and pin IN can accept voltage up to the V_{PLL} pin level

Note: When setting individual pins as input/output ports, refer to the corresponding sections on the Dual-purpose Function.

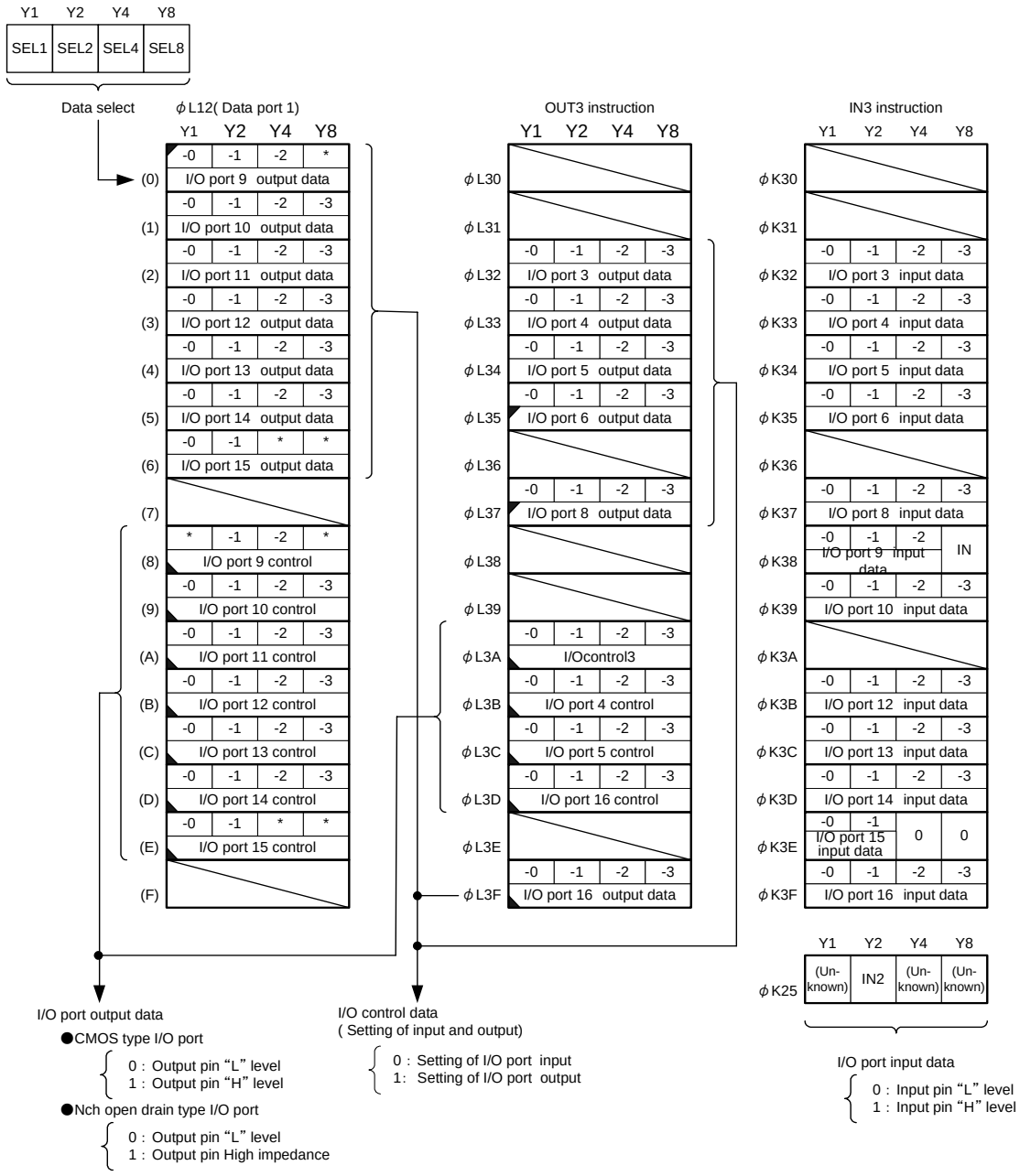
Note: The “H” level of OT1/OT2 output is the V_{DB} level. All the other CMOS I/O ports output the V_{DD} level.

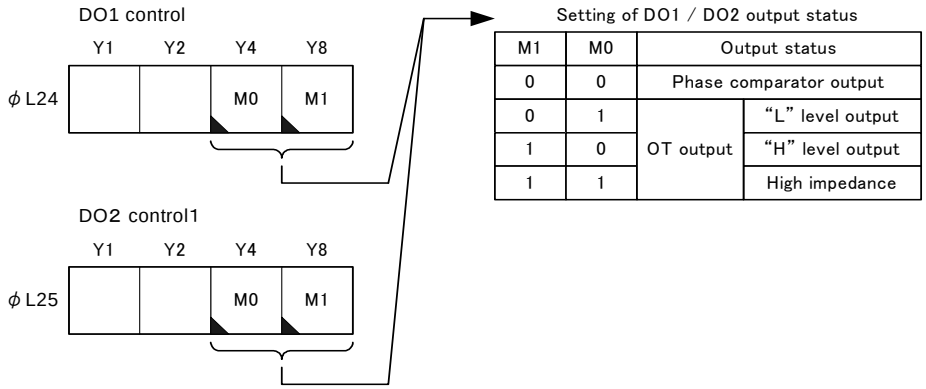
Note: The IN input at the input-only port uses the V_{PLL} power supply. The “H” level is $V_{PLL} \times 0.8$ or higher and the “L” level is $V_{PLL} \times 0.2$ or lower. When the VPLL power supply is turned off with the tuner off, IN input becomes unfixed. The input level for the other pins is $V_{DD} \times 0.8$ or higher at the “H” level and $V_{DD} \times 0.2$ or lower at the “L” level.

Note: After a system reset, pin MUTE/P9-1 is set to the MUTE output and all the other input and output pins are set to the I/O port input or high impedance. The MUTE output becomes the “L” level during system reset, and becomes the “H” level after release.

Note: When the clock stop instruction is executed, the “L” level is outputted at all the pins that have been set to the I/O port ouput. After the clock stop is released, the previous state is outputted.

2. Control Ports of Input and Output Ports





I/O port input/output settings are determined at the I/O control data ports. Set the I/O control data port bit corresponding to each port to “0” to program as an input port or set to “1” to program as an output port.

Determine the output state of an output port by setting the I/O port output data port. Set the output data bit corresponding to each port to “1” to output the “H” level or set to “0” to output the “L” level.

I/O control data and I/O port output data are programmed and controlled at the OUT1 instruction data port-3, the OUT3 instruction.

When the IN3 instruction is executed, the pin state is read into the data memory. Note that execution of the IN3 instruction has no influence on the contents of the output latch.

OT1/OT2 output is programmed by the contents of the DO control port. (→ Refer to the section on Phase comparator.)

Note: There is no I/O control port for N-ch open-drain ports (I/O ports 6, 8 and 9-0). To set these ports as input ports, set high impedance by specifying output data to “1”.

Note: I/O port 1, I/O port 2, ... correspond to pin names P1-0 to P1-3, P2-0 to P2-3, ...

Note: The contents of output ports become unfixed after a system reset. It is recommended that the output data be determined before output setting.

Note: Data select port increments by 1 automatically when ϕL10 to ϕL15, ϕK10 and ϕK11 on the I/O map are accessed.

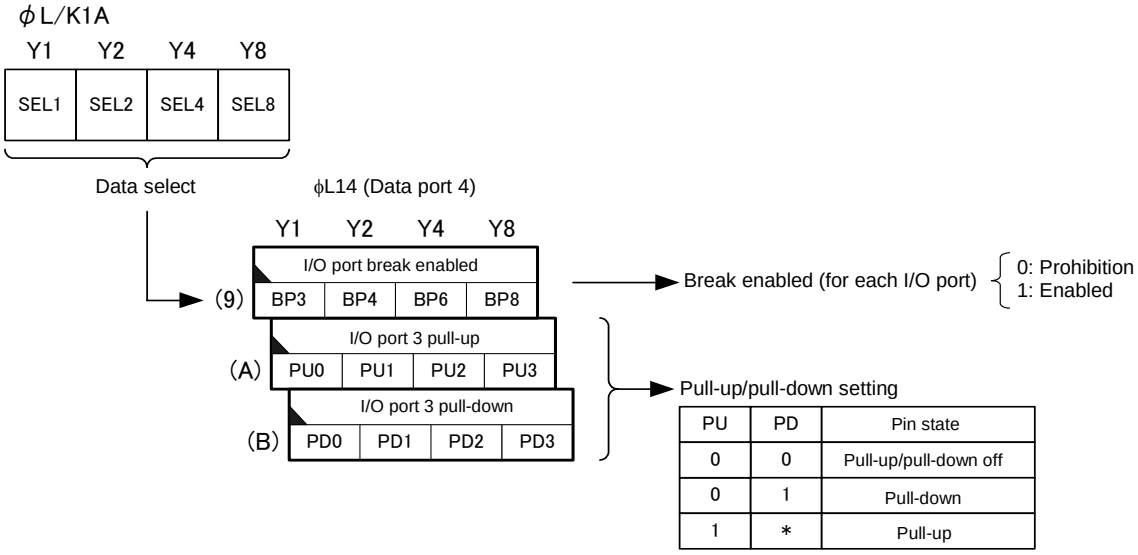
Note: The state of a pin that has been set to output is read when the IN3 instruction is executed.

Note: All the input circuits have the AND structure, which turns the AND gate on only when data reading (IN instruction) is executed. There is little influence on consumption current; even when the input is in the floating condition or has midpoint potential. This enables pull-up at a potential lower than the V_{DD} potential and output at three levels. Pay close attention to setting to the break pin, serial interface or interrupt input, because the consumption current will increase rapidly when the input has midpoint potential.

3. Break Setting and Pull-up/Pull-down Setting

16 pins of I/O ports 3, 4, 6 and 8 can be set as backup release pins (break pins). If there is a change in the input state of an I/O port that has been set to input, the break pin releases execution of the WAIT or CKSTP instruction and restarts the CPU operation. When the break bit of the MUTE port is "1", the MUTE bit is compulsorily set to "1" when there is a change in the input state. (→ Refer to the section on MUTE output.)

Each pin of I/O port 3 can be programmed to a pull-down or pull-up state with 50 kΩ (standard) at the pull-up/pull-down control port. Adjust settings at the pull-up/pull-down control ports that corresponds to the pins of I/O port 3.



PU	PD	Pin state
0	0	Pull-up/pull-down off
0	1	Pull-down
1	*	Pull-up

Note: BP3, BP4, BP6 and BP8 correspond to I/O ports 3, 4, 6 and 8 respectively. PU0/PD0, PU1/PD1, PU2/PD2 and PU3/PD3 correspond to pins P3-0, P3-1, P3-2 and P3-3 respectively.

Note: Break is enabled only when the I/O port is programmed as an input port. The input pin that has been set as a break pin must not be used at the intermediate level.

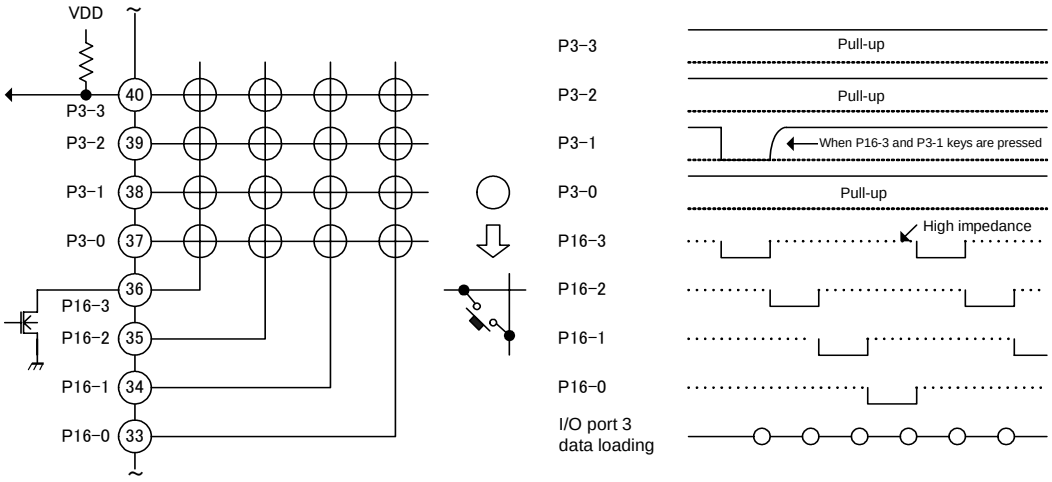
Note: Execution of the wait or clock stop instruction requires reading of the input of the I/O port to be released.

Note: When the serial interface function, the pulse counter function or the interruption input is used and break is enabled, the wait or clock stop instruction is released due to change in the input of the pin. This requires input setting at the I/O control port and reading of input of the I/O port before the instruction is executed.

Note: I/O port 3 can be set to a pull-up or pull-down state when the serial interface function or the pulse counter function is used.

Pull-up and pull-down settings can be used to configure the key matrix. The key matrix is configured with usual I/O port output as the output of the key matrix and the I/O port 3 that has been set to pull-down or pull-up as the key input. Setting the key input to break enables restarting depending on the presence or absence of this key input when the CDSTP or WAIT instruction is executed.

An example configuration of the key input matrix circuit is shown below.



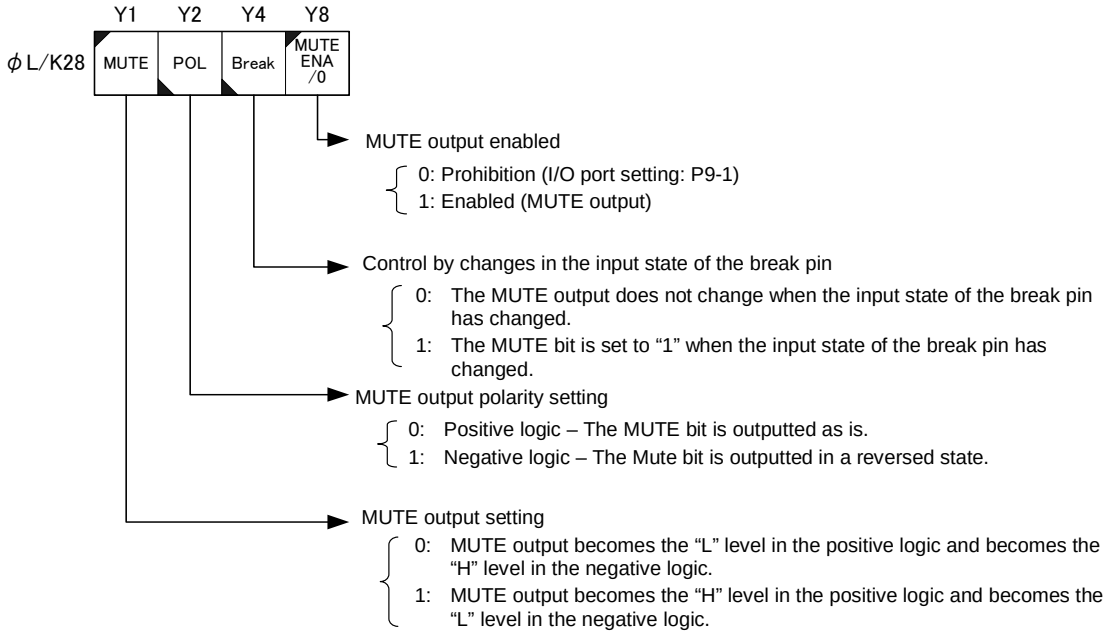
Example of key input matrix circuit

Note: After the CKSTP instruction is released by key input, there is a standby time of 100 ms. Pay close attention to this time lag.

○ MUTE Output

This is the 1-bit CMOS output port for muting control and also used as P9-1 of the I/O port.
The MUTE output can be reversed by the output logic setting or changes in the I/O port.

1. MUTE Port



The MUTE output is usually used for muting control.

The MUTE output is also used as the I/O port function pin (P9-1). The I/O port and MUTE output pin are switched by the MUTE ENA bit. After a reset, this bit is set to "1" and becomes the MUTE output.

Data set to the MUTE bit is outputted to the MUTE output pin using positive or negative logic. By enabling the I/O port break function (refer to the section on the input and output ports) and setting the break bit to "1", the MUTE bit can be set to "1" each time the input of the I/O port is changed. This function promptly activates the muting state and prevents noise from being generated in the linear circuit when the band is switched or the radio is turned off using the I/O port input.

POL bit sets up the logic of MUTE output. Set it up according to specifications.

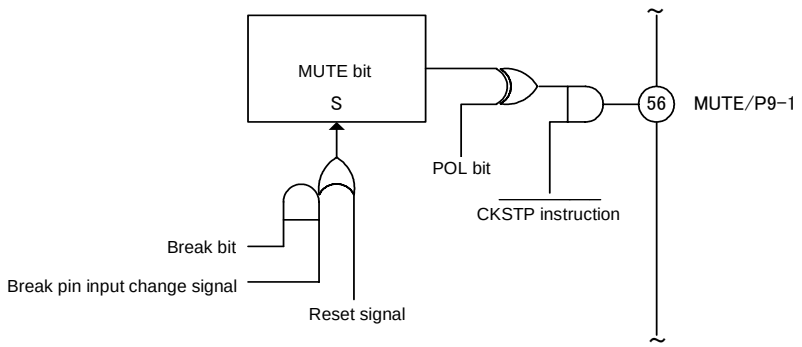
This port is accessed by the OUT2/IN2 instruction with [CN = 8H] specified in the operand.

Note: During a system reset, the "L" level is outputted as the MUTE output. After the reset is released, the "H" level is outputted. During execution of the clock stop instruction, the output becomes the "L" level. After the instruction is released, the previous state is outputted.

Note: When the MUTE is controlled by the break function, the break pin sets the MUTE bit to "1". The state of the MUTE bit can be checked at the MUTE bit (ϕK28). The state of the MUTE pin can be checked at the P9-1, I/O port 9 input data port (ϕK38) .

Note: When the MUTE bit is set to "1", the electronic volume can be set to −∞dB. (→ Refer to the section on Electronic volume.)

2. Circuit Composition of MUTE Output



○ Serial Interface

This is the 2-channel, 1-system serial interface, which has three functions; a three-wire serial interface, two-wire serial interface and full-duplex UART functions.

The serial interface communicates with the extended LSI and microcomputer using CMOS serial interface pins SCK1/TX1 (P3-0), SDIO1 (P3-1) and SI1 (P3-2) or N-ch open-drain pins SCK2/TX2 (P8-2), SDIO2 (P8-3) and SI2 (P8-1) (that can accept voltage up to 5.5V). When the serial interface operation is finished, an interruption is issued.

The serial interface consists of the 4-bit input/output serial counter, the 12-bit serial output latch, the 12-bit serial input latch and the control circuit that controls them.

The basic operations of the serial interface are as follows. For the serial output, the serial data output bit data is outputted as specified by the serial output counter, and the serial counter is moved up or down by the serial clock so that the data is outputted to the serial output pin in the specified order. For the serial input, serial input data is sequentially taken to the serial latch specified by the serial input counter as in the case of the serial input.

1. Control Port and Data Port for Serial Interface

The serial interface executes control and data transmission and receiving using the control port and data port. These ports are assigned in I/O map data port 2 and accessed by the OUT1/IN1 instruction.

Serial interface control 1

	Y1	Y2	Y4	Y8
φL11(7)	M0	M1	PSEL	SIO

Mode setting

Selection of serial interface pin

PSEL	SIO	Serial interface pin
*	0	Each pin for I/O port operation
0	1	I/O port 3 (CMOS)
1		I/O port 8 (N-ch open-drain)

Serial interface mode setting

M1	M0	Serial interface mode
0	0	Operation stop
0	1	2-wired interface
1	0	3-wired interface
1	1	UART

Serial interface control 2

	Y1	Y2	Y4	Y8
φL11(8)	CK0	CK1	OSC0	OSC1

Clock setting

Serial clock (transmission rate) frequency setting

OSC1	OSC0	Oscillator setting	CK1	CK0	2/3-wired interface clock frequency (fSCK)		UART transmission rate (fSCK)		
0	0	Low-speed oscillator (75kHz)	0	0	fosc/2	37.5kHz	–		
			0	1	fosc/4	18.75kHz	fosc/8bps	9375bps	9600bps mode
			1	0	fosc/8	9.375kHz	fosc/32bps	2344bps	2400bps mode
			1	1	fosc/16	4.6875kHz	fosc/64bps	1172bps	1200bps mode
0	1	High-speed oscillator (300kHz)	0	0	fosc/2	150kHz	fosc/16bps	18750bps	19200bps mode
			0	1	fosc/4	75kHz	fosc/32bps	9375bps	9600bps mode
			1	0	fosc/8	37.5kHz	fosc/128bps	2344bps	2400bps mode
			1	1	fosc/16	18.75kHz	fosc/256bps	1172bps	1200bps mode
1	0	High-speed oscillator (450kHz)	0	0	fosc/2	225kHz	fosc/24bps	18750bps	19200bps mode
			0	1	fosc/4	112.5kHz	fosc/48bps	9375bps	9600bps mode
			1	0	fosc/8	56.25kHz	fosc/192bps	2344bps	2400bps mode
			1	1	fosc/16	28.125kHz	fosc/384bps	1172bps	1200bps mode
1	1	High-speed oscillator (600kHz)	0	0	fosc/2	300kHz	fosc/32bps	18750bps	19200bps mode
			0	1	fosc/4	150kHz	fosc/64bps	9375bps	9600bps mode
			1	0	fosc/8	75kHz	fosc/256bps	2344bps	2400bps mode
			1	1	fosc/16	37.5kHz	fosc/512bps	1172bps	1200bps mode

Serial interface control 3

	Y1	Y2	Y4	Y8
φL11(9)	MASTER	POL	NchS	SIS

- SIS → Selection of serial input of SDIO and SI pins
  - 0: Select SDIO input pin
  - 1: Select SI input pin
- NchS → Selection of output form of serial I/O port pin
  - 0: Select CMOS output form
  - 1: Select N-ch open-drain output form
- POL → Selection of serial clock logic for serial data
  - 0: Positive logic output (“L” level outputs SCK clock)
  - 1: Negative logic output (“H” level outputs SCK clock)
- MASTER → Selection of external or internal SCK
  - 0: External clock input (slave)
  - 1: Internal clock output (master)

Serial interface control 4

	Y1	Y2	Y4	Y8
φL11(A)	STPS	SWENA	MSB	SOS

- SOS → Output setting for serial output of pin SDIO
  - 0: Pin SDIO input setting
  - 1: Pin SDIO output setting
- MSB → Selection of order of serial data bits
  - 0: Input/output serial data from the least significant bit
  - 1: Input/output serial data from the most significant bit
- SWENA → Serial wait enable setting
  - 0: Prohibition
  - 1: Enabled

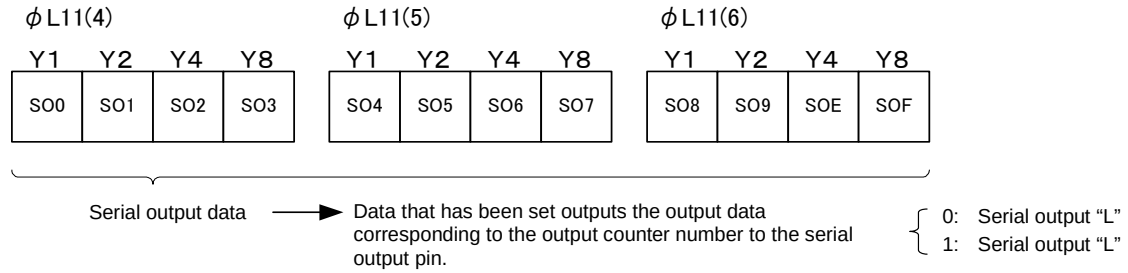
Note: When the serial wait is set to be enabled, the SCK output is compulsorily outputted at the "L" level and becomes the clock wait state when the serial data SOF is outputted. (This is effective only in the 2-wired serial mode.)

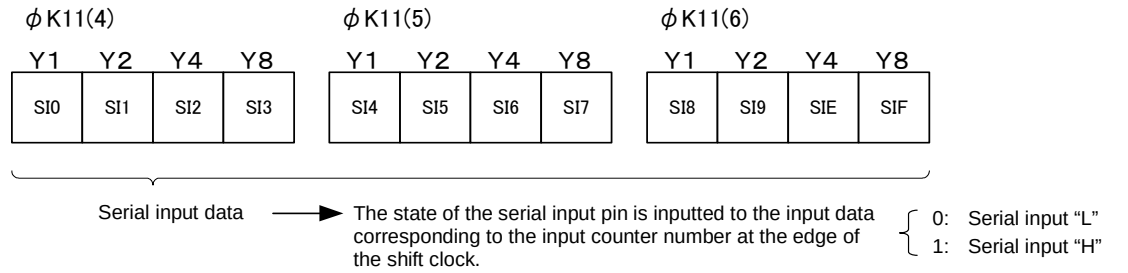
- STPS → Selection of serial clock counter stop condition
  - 0: Select the input clock counter
  - 1: Select the output clock counter

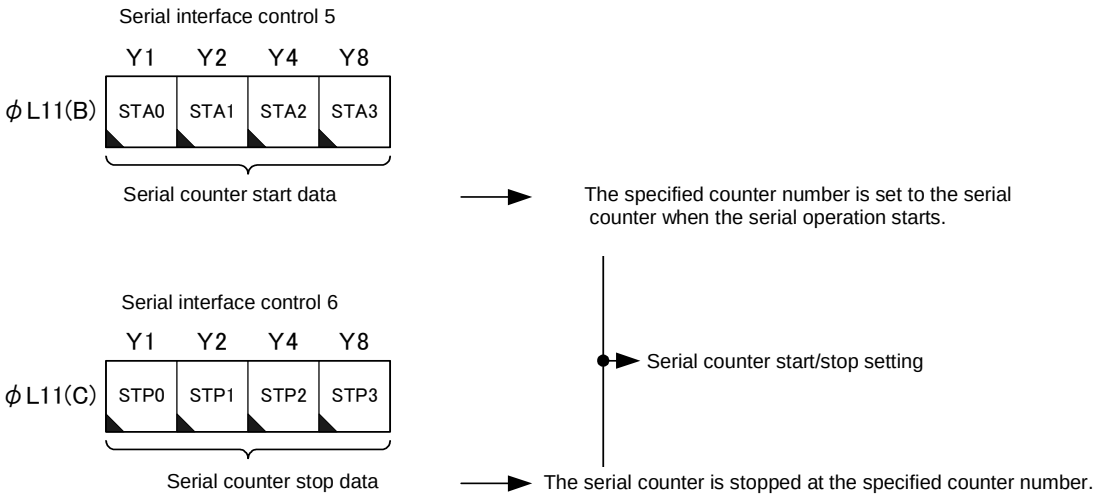
Serial interface control 7

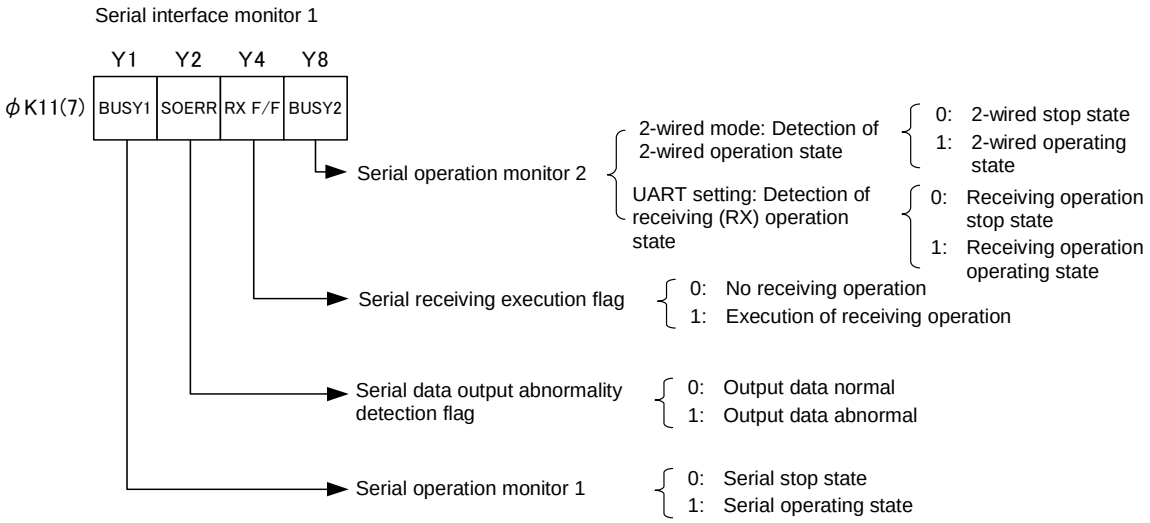
	Y1	Y2	Y4	Y8
φL11(D)	TSTA1	TSTA2	STP	F/F Reset

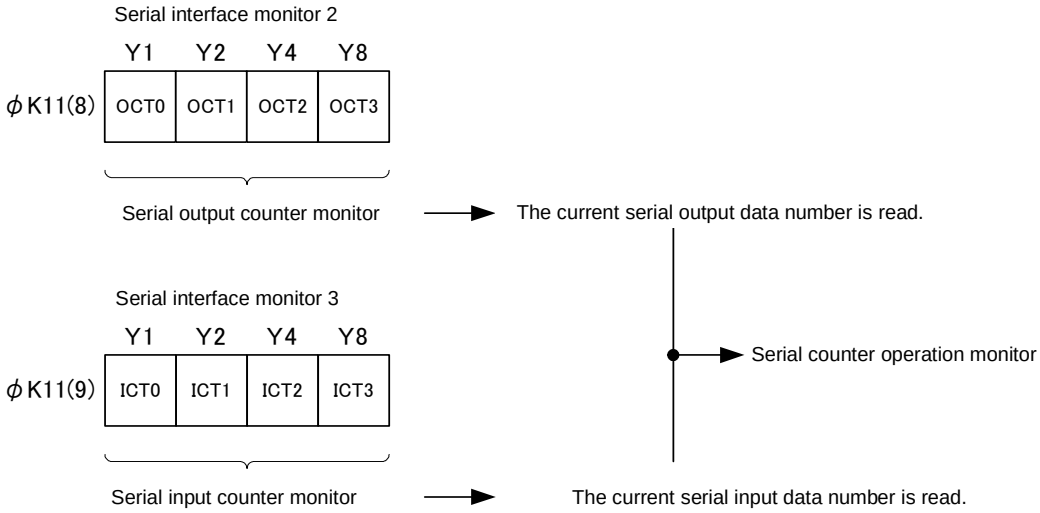
- F/F Reset → Internal flag reset ･･･Resets the internal flag each time "1" is set
- STP → Serial operation stop ･･･Stops serial operation by setting "1"
- TSTA2 → Execute restart in 2-wired mode ･･･Restarts operation by setting "1"
- TSTA1 → Start serial operation in master mode ･･･Starts operation by setting "1"


ϕL11(4)
Y1 Y2 Y4 Y8
SO0 SO1 SO2 SO3
ϕL11(5)
Y1 Y2 Y4 Y8
SO4 SO5 SO6 SO7
ϕL11(6)
Y1 Y2 Y4 Y8
SO8 SO9 SOE SOF
Serial output data
Data that has been set outputs the output data corresponding to the output counter number to the serial output pin.
0: Serial output "L"
1: Serial output "L"


ϕK11(4)
Y1 Y2 Y4 Y8
SI0 SI1 SI2 SI3
ϕK11(5)
Y1 Y2 Y4 Y8
SI4 SI5 SI6 SI7
ϕK11(6)
Y1 Y2 Y4 Y8
SI8 SI9 SIE SIF
Serial input data
The state of the serial input pin is inputted to the input data corresponding to the input counter number at the edge of the shift clock.
0: Serial input "L"
1: Serial input "H"


Serial interface control 5
Y1 Y2 Y4 Y8
ϕL11(B)
STA0 STA1 STA2 STA3
Serial counter start data
The specified counter number is set to the serial counter when the serial operation starts.
Serial interface control 6
Y1 Y2 Y4 Y8
ϕL11(C)
STP0 STP1 STP2 STP3
Serial counter start/stop setting
Serial counter stop data
The serial counter is stopped at the specified counter number.


Serial interface monitor 1
Y1 Y2 Y4 Y8
ϕK11(7)
BUSY1 SOERR RX F/F BUSY2
Serial operation monitor 2
2-wired mode: Detection of 2-wired operation state
0: 2-wired stop state
1: 2-wired operating state
UART setting: Detection of receiving (RX) operation state
0: Receiving operation stop state
1: Receiving operation operating state
Serial receiving execution flag
0: No receiving operation
1: Execution of receiving operation
Serial data output abnormality detection flag
0: Output data normal
1: Output data abnormal
Serial operation monitor 1
0: Serial stop state
1: Serial operating state


Serial interface monitor 2
Y1 Y2 Y4 Y8
ϕK11(8)
OCT0 OCT1 OCT2 OCT3
Serial output counter monitor
The current serial output data number is read.
Serial interface monitor 3
Y1 Y2 Y4 Y8
ϕK11(9)
ICT0 ICT1 ICT2 ICT3
Serial counter operation monitor
Serial input counter monitor
The current serial input data number is read.

1-1. Serial Interface Setting and Control Bits

(1) Serial pin setting (PSEL and SIO bits)

I/O ports 3 or 8 can be used as serial input/output pins. I/O port 3 has a CMOS structure and I/O port 8 has an N-ch open drain structure. Since voltage up to 5.5V can be applied to I/O port 8, it can do an interface with LSI of 5 V system easily.

I/O port 3 is usually used for communication with LSI that drives the V_{DD} power supply in the same power supply system. This port can also be used as a N-ch open-drain port, and accept voltage up to the power supply of the V_{LCD} pin (3 V). Therefore, it can be used as an interface with LSI in power supply systems of 3 V or below.

Set this control bit to “0” when the serial interface is not used.

SIO	PSEL	Serial interface pin	Pin structure	Pin type	Maximum applicable voltage
0	*	Each pin I/O Port operation	-	-	-
1	0	I/O port3	CMOS	CMOS or Nch open drain	~VLCD (3 V)
1	1	I/O port8	Nch open drain	Nch open drain	~5.5 V

Note: These bits are reset to “0” after a system reset.

(2) Type of serial operation (M0 and M1 bits)

The serial operation can be selected from three serial interface modes; 3-wired type, 2-wired type and UART. Set this control bit to “0” when the serial interface is not used. When a mode is selected, the pins are switched to the function pins as listed below.

M1	M0	Serial interface mode	Name of pin being used					
			Select I/O port 3			Select I/O port 8		
0	0	Operation stop	P3−0	P3−1	P3−2	P8−1	P8−2	P8−3
0	1	2-wired interface	SCK1	SDIO1	P3−2	P8−1	SCK2	SDIO2
1	0	3-wired interface	SCK1	SDIO1	SI1(P3−2)	SI2(P8−1)	SCK2	SDIO2
1	1	UART	RX1	TX1	P3−2	P8−1	RX2	TX2

Note: These bits are reset to “0” after system reset.

(3) Selection of serial operation clock (CK0, CK1, OSC0 and OSC1 bits)

The serial operation clock sets the serial interface operating speed. When the 2- or 3-wired master mode is selected, operation speed can be selected from four types, fosc/2, fosc/4, fosc/8 and fosc/16. When UART is selected, operation speed can be selected from three types, 9600/2400/1200 bps. When a high-speed oscillator is used, the operation speed of the 2- or 3-wired type can be accelerable to 300 kHz, which enables the use of the UART transmission rate, 19200 bps. Refer to the following table and select the operation clock.

When the 2- or 3-wired slave mode is selected, these bits revert to “don't care” state, which enables serial clock operation at an operation speed of up to 200 kHz.

Note: The duty of the 2- or 3-wired mode is always 50%.

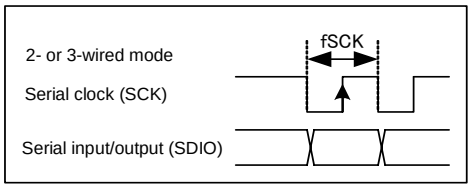
Note: When the high-speed oscillator is prohibited, the OSC0 and OSC1 bits revert to “don't care” state.

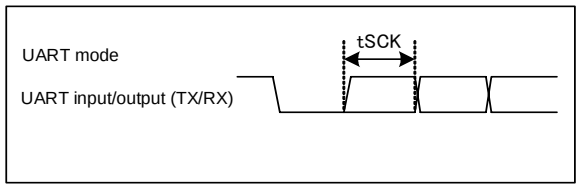
Note: Set all of these bits to “0” when the 2- or 3-wired slave mode is selected.

Note: These bits are reset to “0” after a system reset.

Serial clock (transmission rate) frequency setting

OSC1	OSC0	Oscillator setting	CK1	CK0	2- or 3-wired interface clock frequency (fSCK)		UART transmission rate (fSCK)		
0	0	Low-speed oscillator (75kHz)	0	0	fosc/2	37.5kHz	–		
			0	1	fosc/4	18.75kHz	fosc/8bps	9375bps	9600bps mode
			1	0	fosc/8	9.375kHz	fosc/32bps	2344bps	2400bps mode
			1	1	fosc/16	4.6875kHz	fosc/64bps	1172bps	1200bps mode
0	1	High-speed oscillator (300kHz)	0	0	fosc/2	150kHz	fosc/16bps	18750bps	19200bps mode
			0	1	fosc/4	75kHz	fosc/32bps	9375bps	9600bps mode
			1	0	fosc/8	37.5kHz	fosc/128bps	2344bps	2400bps mode
			1	1	fosc/16	18.75kHz	fosc/256bps	1172bps	1200bps mode
1	0	High-speed oscillator (450kHz)	0	0	fosc/2	225kHz	fosc/24bps	18750bps	19200bps mode
			0	1	fosc/4	112.5kHz	fosc/48bps	9375bps	9600bps mode
			1	0	fosc/8	56.25kHz	fosc/192bps	2344bps	2400bps mode
			1	1	fosc/16	28.125kHz	fosc/384bps	1172bps	1200bps mode
1	1	High-speed oscillator (600kHz)	0	0	fosc/2	300kHz	fosc/32bps	18750bps	19200bps mode
			0	1	fosc/4	150kHz	fosc/64bps	9375bps	9600bps mode
			1	0	fosc/8	75kHz	fosc/256bps	2344bps	2400bps mode
			1	1	fosc/16	37.5kHz	fosc/512bps	1172bps	1200bps mode





(4) Serial operation condition setting

● MASTER bit (Selection of external/internal SCK clock)

Set the master or slave mode. Select the internal clock for the serial clock (SCK) to set the serial operation to master mode, and select the external clock to set the serial operation to slave mode.

If the master setting is selected, the serial operation will start and the serial clock will be outputted when start setting is made by the serial start bits (TSTA1 and TSTA2 bits), and the operation will stop under the serial counter stop condition. The serial clock selected by the clock selection bits (CK0, CK1 bit) will be outputted.

If the slave setting is selected, the serial operation will start automatically when the external clock is inputted. For the 2- or 3-wired type, frequencies no higher than 200 kHz (fSCK) can be inputted as the external clock.

Selection of external or internal SCK clock (MASTER bit)
- 0: External clock input (slave)
- 1: Internal clock output (master)

Note: Select the slave setting when the UART is selected.

Note: This bit is reset to “0” after a system reset.

● POL bit (Selection of serial clock logic for serial data)

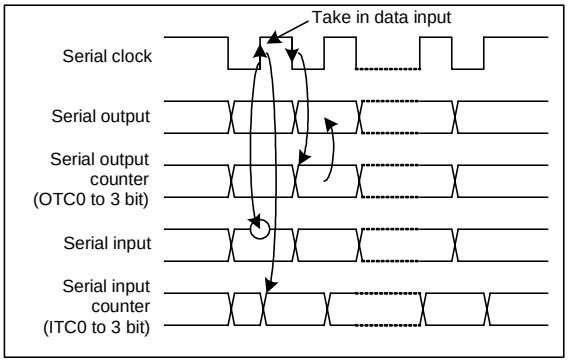
Select the logic for shift clock input/output of the serial clock.

When "1" is set to the bit of POL and a master setup is selected, serial operation stops on the "H" level in the state of a stop, if operation starts, the serial clock outputs and it stops on "H" level. When the POL bit is set to “0”, the logic will be reversed, that is, the operation will start from the “L” level.

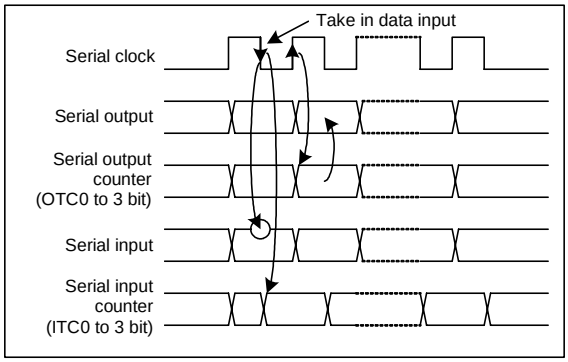
Together with the output logic, this bit controls the serial counter operation edge by the serial clock input/output and the serial input take-in edge. The timing operation by the POL bit is as shown below.

Selection of serial clock logic for serial data (POL bit)
- 0: Positive logic output (SCK clock is outputted from the “L” level)
- 1: Negative logic (SCK clock is outputted from the “H” level)

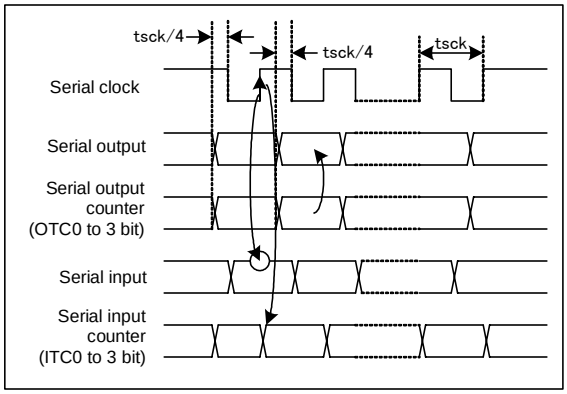
(A) 2-wired master and slave and 3-wired slave modes (POL=”1”)



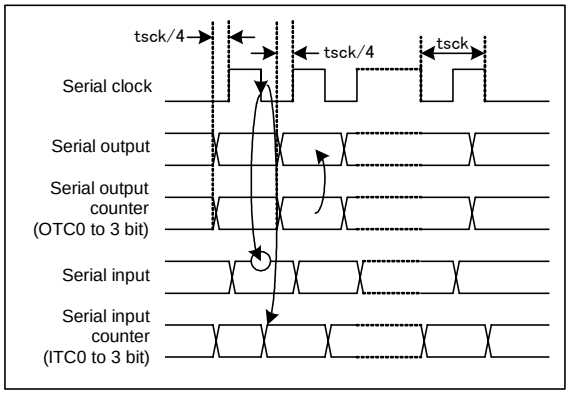
(A) 2-wired master and slave and 3-wired slave modes (POL=”1”)



(C) 3-wired master mode (POL=”1”)



(D) 3-wired master mode (POL=”0”)



Note: When the 3-wired master mode is selected, the serial output (serial output counter) changes in timing shifted by tsck/4.

Note: When the 2-wired master mode is selected, the serial clock is operated by the input of the SCK pin clock. Therefore, the serial operation will not start if the SCK pin clock does not output waveforms for some reason.

Note: Set to POL = “0” when UART is selected.

Note: This bit is reset to “0” after a system reset.

● NchS bit (Selection of output form for the serial I/O port pins)

Set the serial interface input/output circuit type. Setting this bit to “0” to select the CMOS circuit form, and setting this bit to “1” to select the N-ch open-drain circuit.

Selection of output form for serial I/O port pins (NchS bit)
- 0: Select the CMOS output form
- 1: Select the N-ch open-drain output form

NchS	I/O port 3	I/O port 8
0	CMOS type	Setting disabled
1	N-ch open-drain type	

Note: Select the N-ch open-drain setting when the 2-wired mode is selected.

Note: This bit is also effective when the UART is selected.

Note: This bit is reset to “0” after a system reset.

● SIS bit (Selection of SDIO pin or SI pin for serial input)

Select a serial input pin. Set this bit to “0” to select the SDIO pin for serial input. Set this bit to “1” to select the SI pin for serial input.

The I/O port function is enabled for the SI pin. Therefore, when the SI input pin is used for serial input, it is necessary to set the I/O port corresponding to this pin as an input port. When the SDIO pin is used for serial input, the SI pin can be used as an I/O port.

Selection of SDIO or SI pins for serial input (SIS bit)
- 0: Select the SDIO input pin
- 1: Select the SI input pin

Note: When the SI pin is selected, set the I/O port corresponding to this pin as an input port.

Note: When the SDIO input is selected, the SI pin can be used as a normal I/O port.

Note: Select the SDIO input when UART is selected.

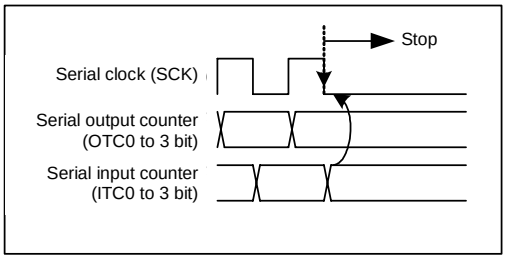
Note: This bit is reset to “0” after a system reset.

● STPS bit (Selection of the serial clock counter stop condition)

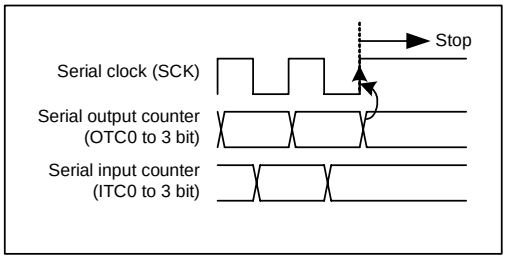
The serial operation stops when it becomes the stop position of a serial counter. There are two types of serial counters, the serial output counter and the serial input counter. The stop condition is switched between the output and input counters.

Selection of serial clock counter stop condition (STPS bit)
- 0: Select the input clock counter
- 1: Select the output clock counter

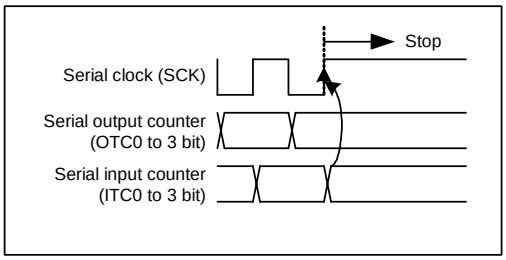
(A) 2- or 3-wired mode (POL="0", STP="0")



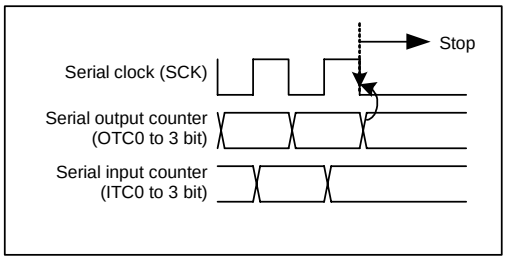
(B) 2- or 3-wired mode (POL="0", STP="1")



(C) 2- or 3-wired mode (POL="1", STP="0")



(D) 2- or 3-wired mode (POL="1", STP="1")



Note: Set to STPS = "1" (Select the clock output counter) as shown in (B) when the 2-wired or UART mode is selected.

Note: This bit is reset to "0" after a system reset.

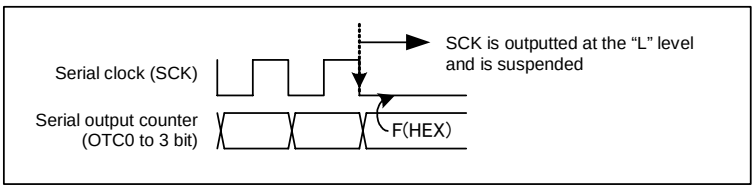
● SWENA bit (Serial wait enable)

This control bit is effective only when the 2-wired mode is selected. usually, set this bit to "1" when the 2-wired mode is selected.

If serial wait is enabled in the 2-wired mode, the SCK is outputted at the "L" level and becomes the clock wait state and the serial clock is suspended when the serial output counter (OCT0~3) becomes "F" (HEX).

Serial wait enabling setting (SWENA bit)
- 0: Prohibition
- 1: Enabled (Set to "1" when the 2-wired setting is selected)

When the 2-wired mode is selected (POL="1", STP="0", SWENA="1")



Note: Set to SWENA = "0" when the 3-wired or UART mode is selected.

Note: This bit is reset to "0" after system reset.

● SOS bit (Output setting for SDIO pin serial output)

This control bit switches the serial data input/output pin (SDIO pin) between data output and input. Set this bit to "0" for serial data input or set to "1" for serial data output.

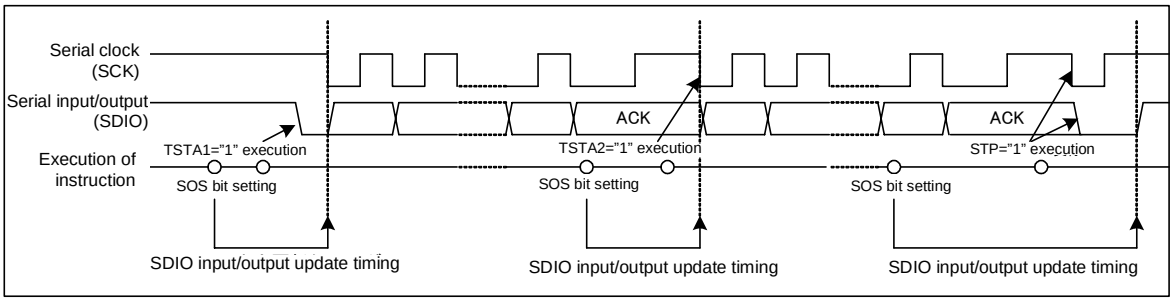
In the 3-wired mode, switching between input and output is executed when the instruction to this bit is executed. In the 2-wired mode, switching between input and output is updated and determined under the following conditions after this bit is specified.

Output setting for SDIO pin serial output (SOS bit)
- 0: SDIO pin input setting
- 1: SDIO pin output setting

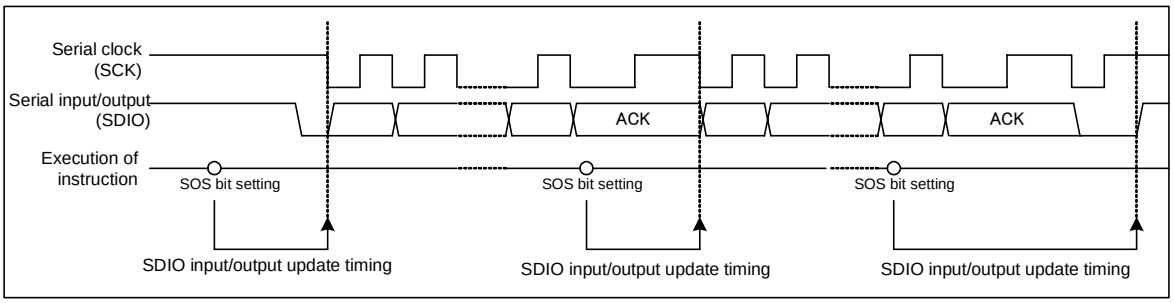
Update timing of SDIO pin input/output switching in the 2-wired mode

- Stop condition
- Falling edge of the shift clock when the communication is started
- Falling edge of the serial clock after ACK input/output

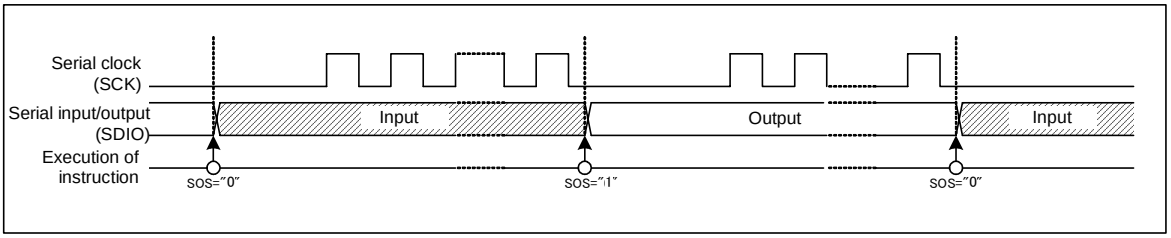
SDIO input/output switching timing in the 2-wired mode (master mode)



SDIO input/output switching timing in the 2-wired mode (slave mode)



SDIO input/output switching timing in the 3-wired mode



Note: If the SOS bit is set in the 3-wired mode, the input/output of the SDIO pin will be updated when the instruction is executed.

Note: Always set the SOS bit to "1" when UART is selected.

Note: This bit is reset to "0" after a system reset.

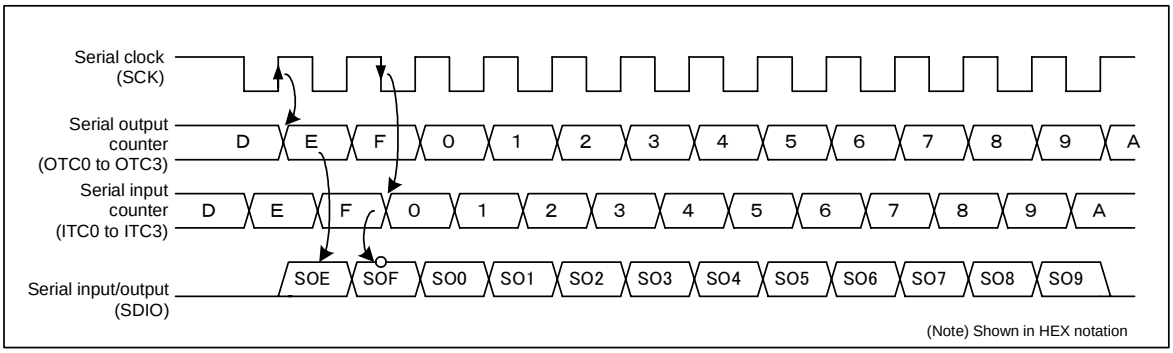
● MSB bit (Selection of the order of serial data bits)

This control bit controls the arrangement of serial data input/output data. Select whether data input/output started from the most or the least significant bit respectively.

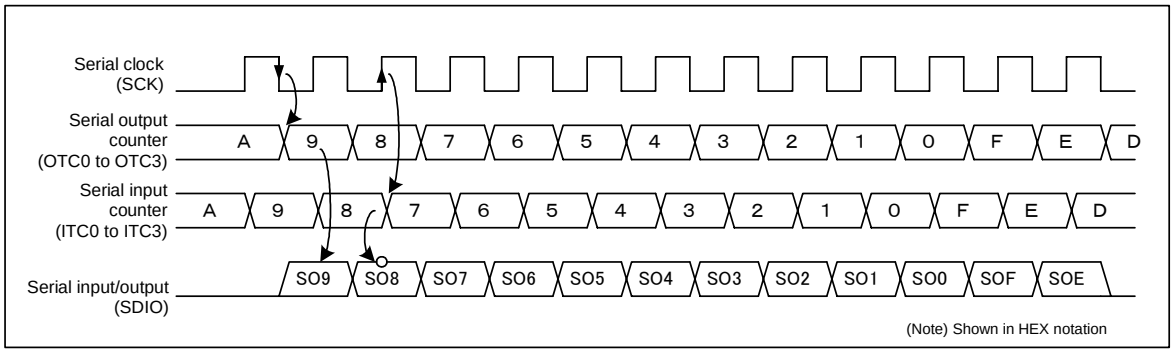
For the serial interface, serial data specified by the serial counter is inputted and outputted. The MSB bit controls the serial counter to count up or down. When the MSB bit is set to “0”, the serial counter counts up. When the MSB bit is set to “1”, the serial counter counts down.

Selection of the order of serial data bits (MSB bit)
- 0: Input/output serial data beginning with the least significant bit
- 1: Input/output serial data beginning with the most significant bit

Serial counter and serial input/output timing (when MSB= “0” and POL= “0”)



Serial counter and serial input/output timing (when MSB= “1” and POL= “1”)



Note: Serial data corresponding to the serial output counter is outputted to the serial output pin. The state of the serial input pin corresponding to the serial input counter is stored in the serial input data at the edge.

Note: Input and output serial counters have up and down edges reverse to each other.

Note: If any serial input/output data not present in the serial counter is designated, the output will be “L” and the input will be “don't care”.

Note: This bit is reset to “0” after a system reset.

● Serial counter, Serial data
(STA0 to 3, STP0 to 3, OCT0 to 3 and ICT0 to 3 bits, SO0 to SO9/SOE/SOF, SI0~SI9/SIE/SIF)

The serial counter consists of the serial input counter (ICT0 to 3) that counts the serial input clock and the serial output counter (OCT0 to 3) that counts the serial output clock. When stop is executed (STP = “1”), these serial counters are preset to the stop data (STP0 to 3). When start is executed (TSTA1 = “1”, TSTA2 = “1”) or the external serial clock is started, these serial counters are preset to serial counter start data (STA0 to 3) and counted by the serial clock. When the serial counter coincides with the serial stop data (STP0 to 3), the serial counter is stopped and an interruption is issued.

The operating state can be checked on the serial counter monitor (ICT0 to 3, OCT0 to 3).

- Serial counter start data (STA0 to 3 bits)

  → When the serial operation is started, the start data is set to the serial counter.

- Serial counter stop data (STP0 to 3 bits)

  → When a stop is executed (STP = “1”), the stop data is set to the serial counter. After the serial counter operation, the serial operation is stopped in the stop data position, and an interruption issued.

- Operation monitor for serial output counter (OCT0 to 3 bits)

  → The operating state of the serial output counter can be detected.

- Operation monitor for serial input counter (ICT0 to 3 bits)

  → The operating state of the serial input counter can be detected.

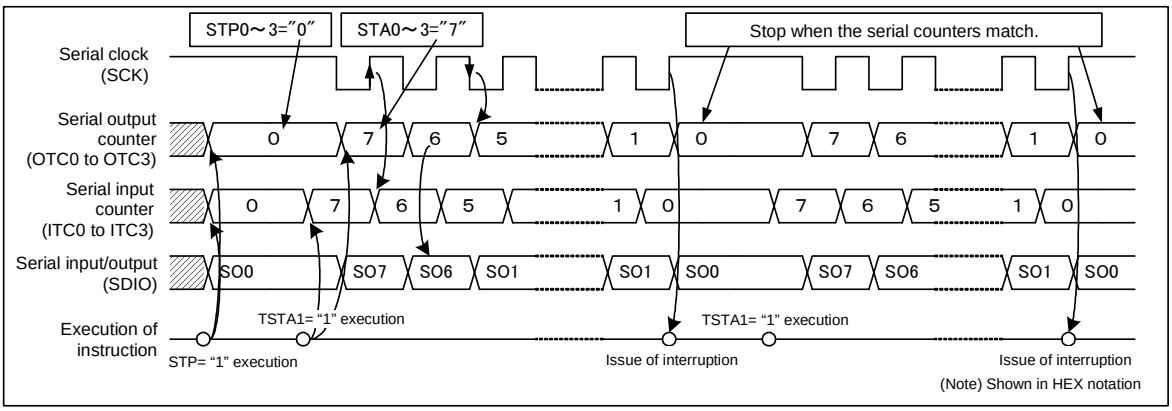
Serial data consists of 12 bits each of serial output data (SO0 to SO9/SOE/SOF) and serial input data (SI0 to SI9/SIE/SIF). For serial output data, the serial data corresponding to the serial output counter number is outputted to the serial output pin. For serial input data, the state of the serial data input pin is read at the edge of the serial clock corresponding to the serial input counter number.

When the 2-wire mode is selected, the SOE/SOF bits in the serial output data are automatically set to “1” when the serial operation is started or when stop is executed (STP = “1”) with the master setting. usually, the bits of SO0/SI1 to SO7/SI7 are used for serial input/output data. The SOE bit is used as the output bit of the serial stop state,while the SOF/SIF bits are used as input/output data of ACK.

When UART is selected, the bits of SO0/SI1 to SO7/SI7 are used for UART input/output data, while the SO8/SI8 bits are used as parity bits. The SO9 bit is used for the output of the stop output data.

When the 3-wire mode is selected, up to 14 bits of serial data can be inputted and outputted. Set the serial data start and stop data according to the number of bits, and specify this number.

Example of serial operation timing when the 3-wire mode is selected (when MSB= “0”, POL= “0” and STPS= “1”)



(5) Start and stoppage of serial operation

● TSTA1 and TATA2 bits (Start of serial operation)

The TSTA1 bit controls the start of serial operation in the master mode. When this bit is set to “1”, the serial clock will be outputted and the serial interface operation will start.

When start is executed in the 3-wire mode, the serial counter start data (STA0 to 3) will be preset in the serial input/output counters, and serial output data corresponding to the start data will be outputted. After that, serial data (SO0 to SO9, SOE, SOF) will be outputted sequentially according to the serial clock (SCK).

When start is executed in the 2-wire mode, the start condition pulse will be outputted to the serial data output. When this start condition is satisfied, the serial operation will be started. When start is executed in the UART mode, the start pulse will be outputted from the TX pin, and then the same operation as in the 3-wire mode will be executed.

In slave mode, operation can be started by the external serial clock without the need to use this control bit.

The TSTA2 bit controls the restart of serial operation in the 2-wire master mode. When start is executed by the TSTA1 bit, the start condition will be outputted, the 8-bit serial clock will be active and the operation will enter the serial wait state. When the TSAT2 bit is set to “1”, the serial operation will be restarted for serial input/output.

- Start of serial operation in the master mode (TSTA1 bit)

  → When this bit is set to “1” in the master mode, serial operation will start.
  When in 2-wire mode, the start condition will be outputted automatically.
  When in UART mode, the start pulse will be outputted.

- Execution of restart in the 2-wire mode (TSTA2 bit)

  → When this bit is set to “1”, the operation will be restarted.

Note: When these bits are set to “0”, the system will be in a “don't care” state.

Note: Allow the wait time that corresonds to at least one cycle of the serial operation clock between execution of stop (STP = “1”) and execution of start (TSTA = “1”).

● STP bit (Stoppage of serial operation)

The STP bit controls the compulsive stoppage of serial operation, the initialization of internal state and the output of the stop condition.

When the STP bit is set to “1” (stop is executed), the serial counter stop data (STP0 to 3) is preset to the serial counter and initializes the internal state. When a stop is executed during serial operation in master mode, the serial clock operation will be stopped.

When a stop is executed in the master 2-wire mode, the stop condition will be automatically outputted from the serial data output and the serial clock in addition to the operation as mentioned above.

- Stoppage and initialization of serial operation in the master mode (STP bit)

  → When this bit is set to “1”, the operation will be stopped and initialized. In the 2-wire mode, the stop condition will be outputted automatically.

Note: When this bit is set to “0”, the system will be in a “don't care” state.

Note: After setting the condition, be sure to execute stoppage (STP = “1”) for internal initialization.

(6) Serial operation monitor

● BUSY1/BUSY2 bits (Operation monitor)

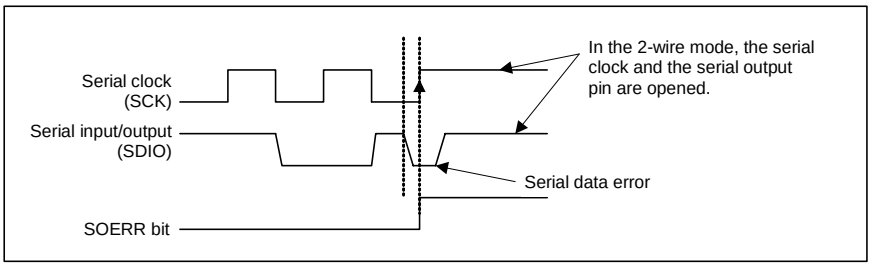
The BUSY1/BUSY2 bits detect the serial operating state. The BUSY1 bit can detect the serial clock operating state, while the BUSY2 bit can detect the operating state in the 2-wire mode or the receiving operation state in the UART mode. When interruption is enabled, it will be issued at the falling edge of the BUSY1 bit and the program will branch to address 0001H.

● SOERR bit (2-wire serial output error flag)

The SOERR bit is used to detect arbitration in the 2-wire multi master mode. When serial data is outputted in the master mode, the output state is compared to the internal output data. If there is any discrepancy between them, the serial operation will be stopped automatically and the SOERR bit set to "1". When this state is detected, the serial clock and data respectively will be opened and the operation will continue. For normal arbitration detection, the serial operation will be stopped by the clock supplied from another master. When the 2-wire operation is completed, FF Reset = "1" will be set and the flag will be reset.

This detection is carried out during serial output setting, regardless of the master or slave mode. Therefore, program processing is required if any discrepancy occurs in the output data due to noise or for any other reason. Usually, provide a timer to detect this bit if there is no issue involving interruption or the BUSY1 signal does revert to "L" after a certain time has elapsed. If the detected bit is "1", set the STP bit to "1" to execute stop and initialization.

In any other modes than the 2-wire mode, this bit is in the "don't care" state.



● RX F/F bit (Receiving flag)

The RX F/F bit detects the receiving of UART or the 3-wire slave. This bit is effective only in slave mode. When the serial clock receives input or UART when in slave mode, this bit is set to "1". After receiving is completed, refer to the received serial data. This bit is reset to "0" by setting the FF Reset bit to "1".

● F/F Reset bit (Internal flag reset)

This bit initializes the internal flag. Each time this bit is set to "1", the internal flag will be reset.

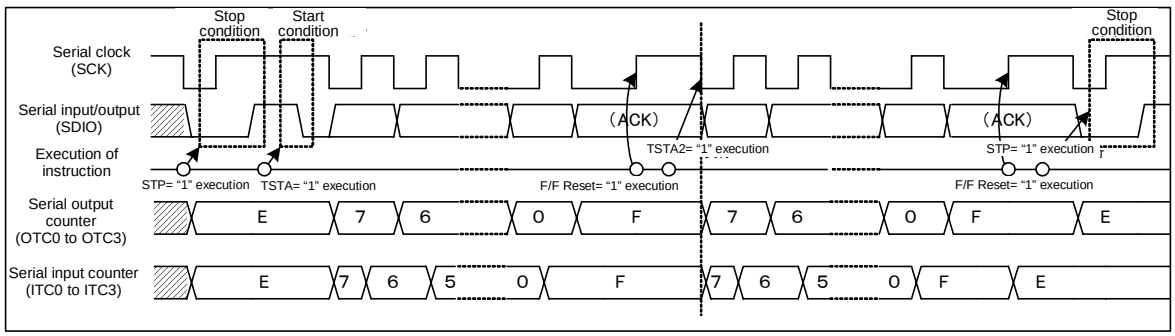
Serial receiving execution flag (RX F/F), the serial data output error detection flag in the 2-wire mode, and the serial wait are reset and released.

In the 2-wire mode, the system will enter the wait state after output of the serial output data SOF bit. Usually, the SOF/SIF bits are used as the acknowledgement of (ACK) bits. After reading the ACK bit input/output, serial operation will be restarted by execution of the F/F Reset bit.

- Internal flag reset (F/F Reset bit)

  → "The internal flag is reset each time this flag is set to "1".
  The wait state is released in the 2-wire mode.

Start and stop operation timing in the 2-wire mode



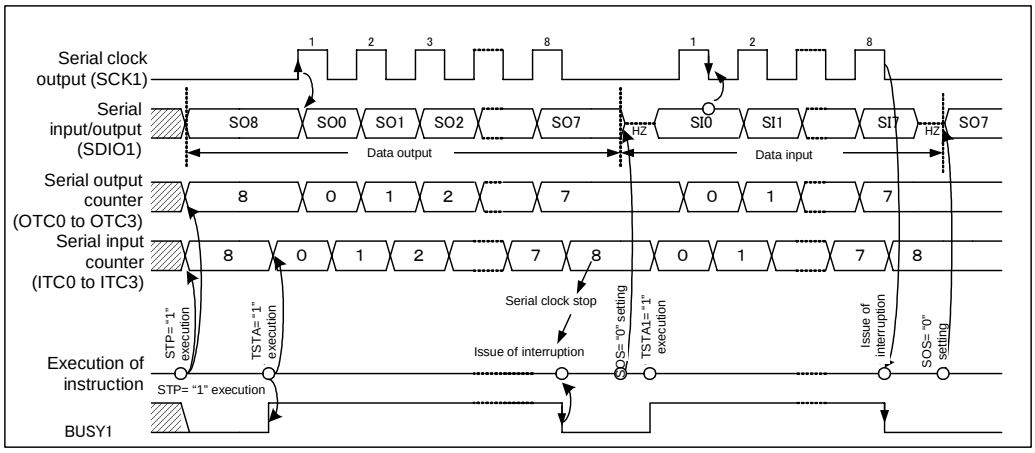
1-2. Examples of Serial Mode Settings

Examples of settings in the 3-wire, 2-wire and UART modes are shown below. Adjust settings according to the required specifications.

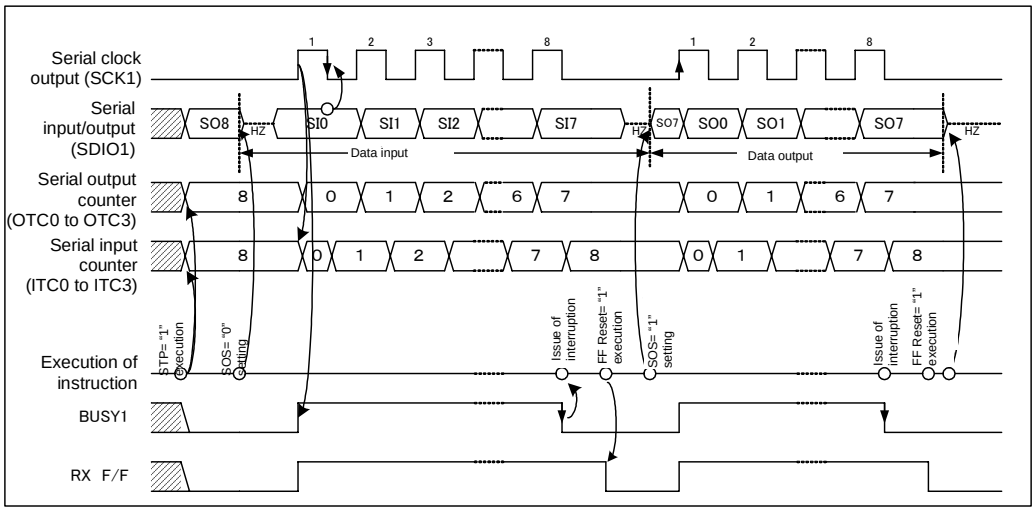
(1) Example of 3-wire serial mode setting

Setting bit	Condition setting data
M0, M1	3-wire setting (M0 = 0, M1 = 1)
CK0, CK1, OSC0, OSC1	Serial clock frequency setting
MASTER	Master setting (MASTER = 1): Refer to an example of master operation timing. Slave setting (MASTER = 0): Refer to an example of slave operation timing.
POL	Serial clock stop state = L、 Data output at the rising edge and data input at the falling edge (POL = 0)
NchS	CMOS setting (NchS = 0)
SIS	Setting of SDIO pin to serial input (SIS = 0)
STPS	Setting of stop condition to input counter (STPS = 0)
SWENA	Stop weight disabled (SWENA = 0)
MSB	Output beginning with the least significant bit (MSB = 0)
SOS	Data output: SOS = 1, Data input: SOS = 0
STA0~3	Serial input/output start data: 0h
STP0~3	Serial input/output stop data: 8h
PSEL, SIO	Select CMOS pin (SDIO1, SCK1) (PSEL = 0, SIO = 1)

- Example of serial interface timing in the 3-wire master mode

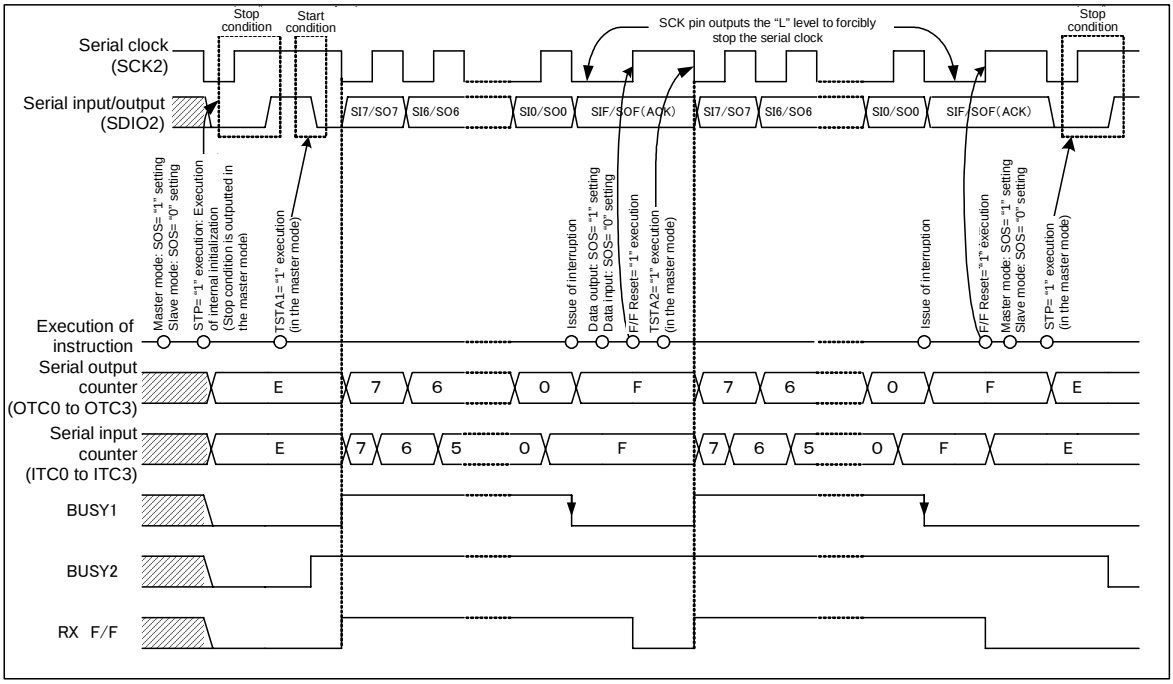


- Example of serial interface timing in the 3-wire slave mode



(2) Example of serial mode setting in the 2-wire mode

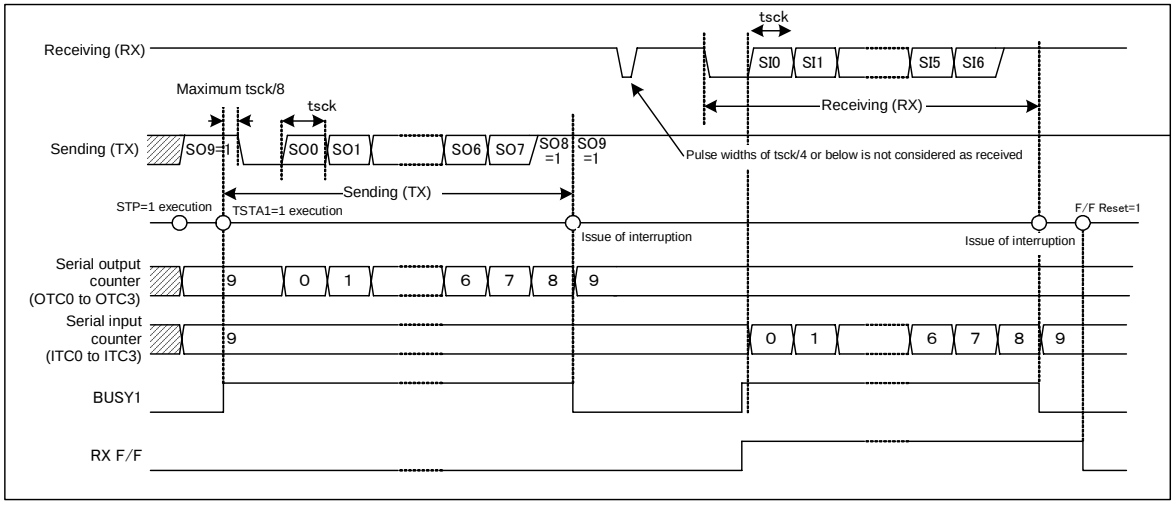
Setting bit	Condition setting data
M0, M1	2-wire setting (M0 = 0, M1 = 1)
CK0, CK1, OSC0, OSC1	Serial clock frequency setting
MASTER	Master setting (MASTER = 1): Refer to an example of master operation timing. Slave setting (MASTER = 0): Refer to an example of slave operation timing.
POL	Serial clock stop state = H、 Data output at the falling edge and data input at the rising edge (POL = 1)
NchS	N-ch open drain setting (NchS = 1)
SIS	Setting of SDIO pin to serial input (SIS = 0)
STPS	Setting of stop condition to input counter (STPS = 1)
SWENA	Stop weight enabled (SWENA = 1)
MSB	Output beginning with the most significant bit (MSB = 1)
SOS	Data output: SOS = 1, Data input: SOS = 0
STA0~3	Serial input/output start data: 7h
STP0~3	Serial input/output stop data: Eh
PSEL, SIO	Select N-ch open-drain pin (SDIO2, SCK2) (PSEL = 1, SIO = 1)



Note: The start condition (STA1 = "1") cannot be outputted at the ACK input/output timing during 2-wire operation (BUSY2 = "1") in the master mode. Output the stop condition, and then the start condition.

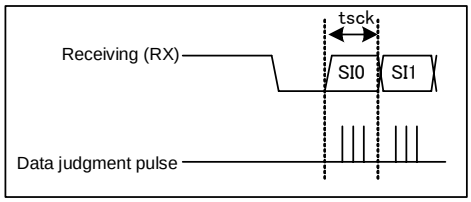
(3) Example of UART mode setting

Setting bit	Condition setting data
M0, M1	UART setting (M0 = 0, M1 = 1)
CK0, CK1, OSC0, OSC1	Transmission rate setting
MASTER	Master setting (MASTER = 0)
POL	Serial clock stop state = H、 Data output at the falling edge and data input at the rising edge (POL = 0)
NchS	N-ch open drain setting (NchS = 1)
SIS	Setting of serial data pin to RX pin (SIS = 0)
STPS	Setting of stop condition to input counter (STPS = 1)
SWENA	Stop weight disabled (SWENA = 0)
MSB	Output beginning with the least significant bit (MSB = 0)
SOS	Data output (SOS = 1)
STA0~3	Serial input/output start data: 0h
STP0~3	Serial input/output stop data: 9h
PSEL, SIO	Select N-ch open-drain pin (TX2, RX2) (PSEL = 1, SIO = 1)



Note: When a pulse width of tsck/4 or below is inputted during receiving (RX), the start of receiving will be cancelled.

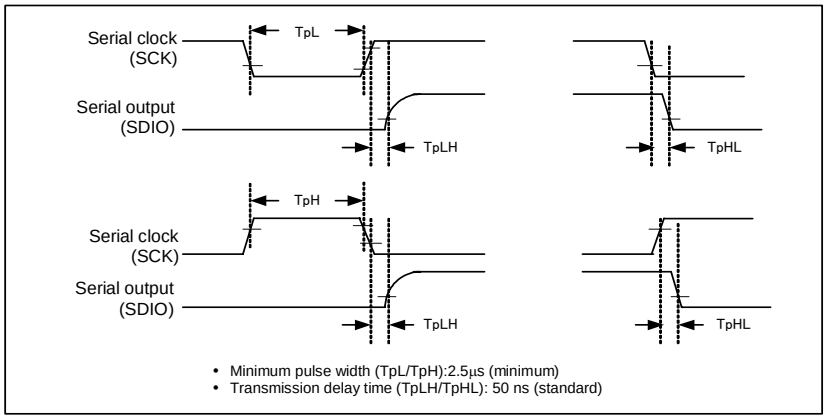
Note: The UART circuit has a data judgment circuit. When receiving starts, the data judgment circuit outputs a 3-pulse data judgment pulse in the data position to judge the RX pin state. When at least two of these pulses record the same data, the received data is read as the serial data input. In other words, if noise occurs in one pulse in the pulse output position, the data can be received normally.



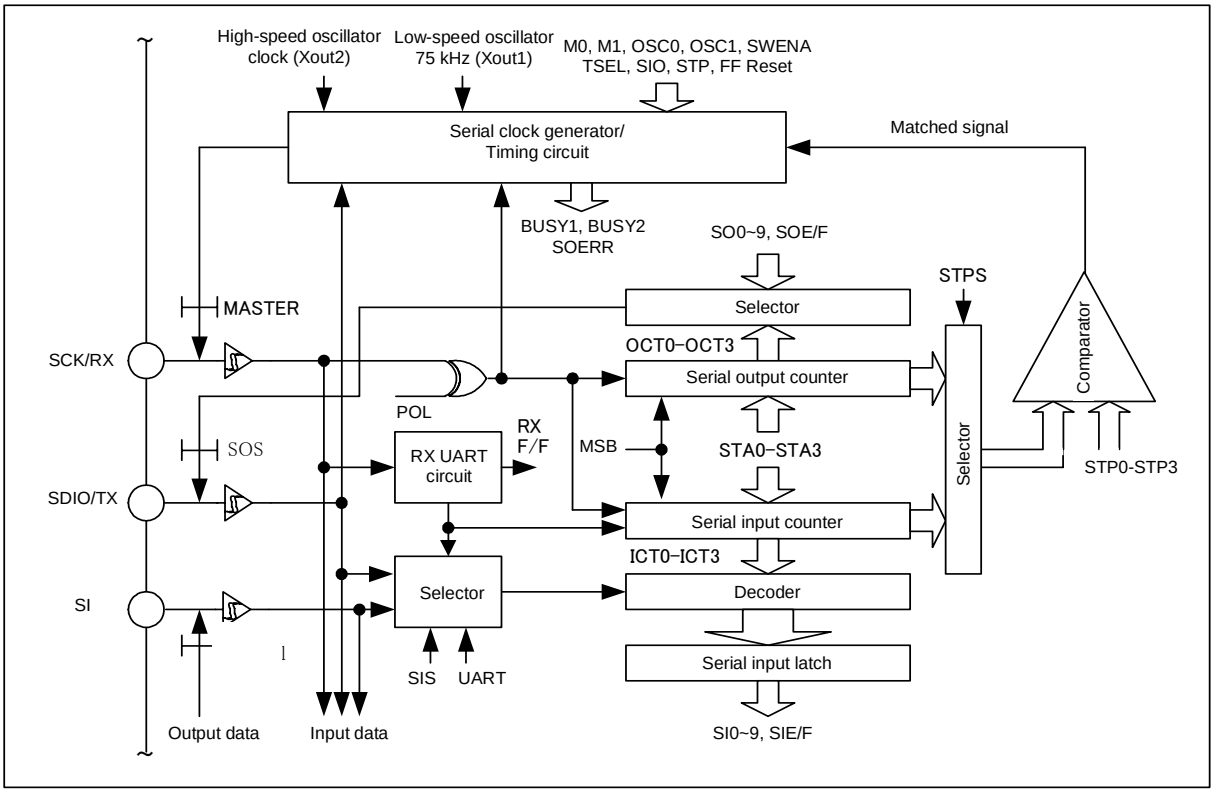
Note: This example shows sending and receiving without parity. The SO8 bit output is outptted as the stop bit. In the specification with parity, the SO8/SI8 bits can be assigned to parity. However, if transmission (TX) starts immediately after the issue of interruption, the stop bit width cannot be secured. In this case, after the interruption is issued, allow the operation to wait for a stop bit width or more before sending is executed.

Note: UART of this product supports the full/duplex specification. If sending and receiving operations are executed at the same time, they can be carried out normally. However, interruption is issued when either operation is completed and the BUSY1 bit becomes “0”. Determine receiving operation using the RX F/F bit.

1-3. Serial Clock Timing



2. Serial Interface Configuration



Note: When the serial interface function is working, the serial input-only pin (SI) can be used as an I/O port. To use it as the SI pin, you need to set the I/O port to input.

Note: All the serial interface pins are Schmitt input.

Note: When the serial interface function is used and the I/O port input is enabled to break, the wait or clock stop instruction will be released due to changes in serial input. Note that this requires input setting from the I/O port control and reading of the I/O port input before execution of the instruction. When the clock stop is released, CPU execution will be started after 100 ms of standby.

Note: When the serial interface function is used, I/O port 3 can be set to a pull-up/pull-down state.

○ Pulse Counter

The pulse counter is the 8-bit up/down counter that can detect the clock number through the CMOS input from PCTRin (P3-3) pin. It can be used for counting and detection of tape running.

1. Pulse counter control ports and data ports

Pulse counter control 1

	Y1	Y2	Y4	Y8
φL2B	POS	NEG	DOWN	*

Up/down setting of 8-bit up and down counter

0: Up count operation
1: Down count operation

Counter input edge setting for input pin (PCTRin pin)

POS	NEG	P3−3/PCTRin	Input edge
0	0	P3−3	−
1	0	PCTRin	Rising edge
0	1		Falling edge
1	1		Both edges

Pulse counter control 2

	Y1	Y2	Y4	Y8
φL2C	CTR RESET	OVER RESET	*	*

Overflow detection F/F reset
OVER F/F is reset each time “1” is set

Pulse counter reset
8-bit up and down counter is reset each time “1” is set

φK2B				φK2C				φK2D			
Y1	Y2	Y4	Y8	Y1	Y2	Y4	Y8	Y1	Y2	Y4	Y8
PC0	PC1	PC2	PC3	PC4	PC5	PC6	PC7	OVER	0	0	0
2^0							2^7				
LSB							MSB				

Pulse counter data

Overflow detection

0: Counter measured value ≤ 2^8-1
1: Counter measured value ≤ 2^8 (Overflow state)

The pulse counter measures the number of pulses of the input of PCTR in the (P3-3) pin.

The POS and NEG bits specify the input pin clock edge from the rising edge, the falling edges and both edges. This bit is fixed in the normal operation.

The DOWN bit sets the up or down of the 8-bit counter. When this bit is set to “0”, the up count operation becomes active. When this bit is set to “1”, the down count operation becomes active. Up and down counts can be switched freely. If the clock edge is inputted during execution of the switch instruction, this count will be cancelled, please remain aware of this.

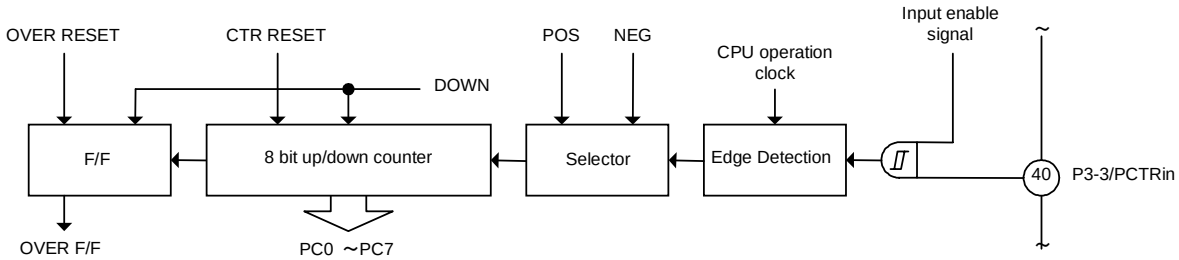
The OVER F/F bit is set to “1” when an edge of 2^8 or higher is inputted. To activate a count operation of 8 bits or more, this OVER F/F bit is detected to add or subtract the number of times of overflow on the data memory. After detection is carried out by this bit, set the OVER RESET bit to “1” to reset OVER F/F.

The CTR RESET bit resets the 8-bit counter only. The counter will be reset each time this bit is set to “1”.

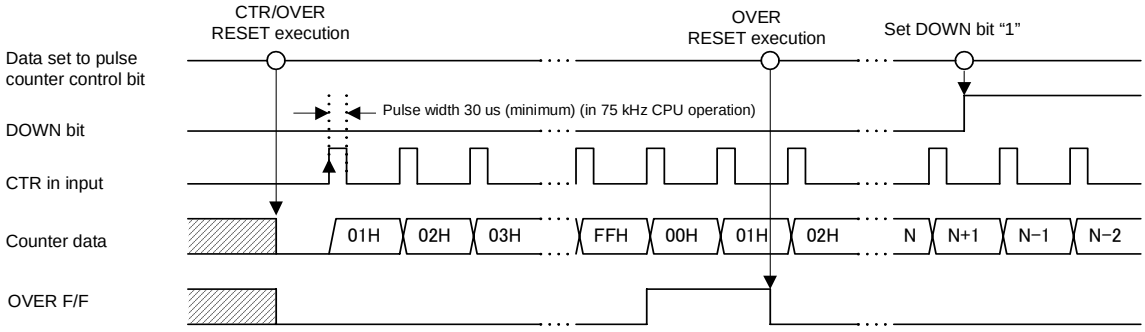
Counter data is loaded into the data memory in binary format.

Pulse counter control and data loading are accessed by the OUT2/IN2 instruction with [CN = BH~DH] specified in the operand.

2. Pulse Counter Circuit Configuration



3. Example of Pulse Counter Timing



Note: The CTRin input pin is the Schumitt input.

Note: The pulse counter uses the CPU operation clock (75 kHz of low-speed clock) to determine the sampling and edges. Input a pulse width of at least twice the CPU operation clock.

Note: When the pulse counter function is used and the I/O port input is enabled to break, the wait or clock stop instruction will be released due to changes in serial input. Note that this requires input setting from the I/O port control and reading of the I/O port input before execution of the instruction. he first pulse is not counted. When the clock stop is released, CPU execution will be started after 100 ms of standby.

Note: When the pulse counter function is used, I/O port 3 can be set to the pull-up/pull-down state.

○ Buzzer Output

Buzzer output can be used for emitting beeps for acknowledgement and alarm purposes during key operations and when in tuning scan mode. The type of buzzer can be selected from combinations of four output modes and eight frequencies.

1. Buzzer Control Ports

Buzzer output control 1

	Y1	Y2	Y4	Y8
φL15(0)	BF0	BF1	*	BEN

Buzzer frequency selection data

Buzzer output enable bit

0: Buzzer output Prohibitiond ("L" level when POL= "0", "H" level when POL= "1")
1: Buzzer output enabled

BF1	BF0	Buzzer frequency	Duty
0	0	1kHz	2/3
0	1	1.56kHz	1/2
1	0	2.08kHz	2/3
1	1	3kHz	2/3

Note: 2/3 duty has the ratio of "H" level to "L" level of 2:1 when POL= "0".
It is reversed when POL= "1".

Buzzer output control 2

	Y1	Y2	Y4	Y8
φL15(1)	BM0	BM1	BUZR ON	POL

Buzzer output mode

Buzzer output logic setting

0: Positive logic output. The buzzer frequency is outputted in the positive logic from the "L" level.
1: Negative logic output. The buzzer frequency is outputted in the negative logic from the "H" level.

Selection of I/O port 4 P4-2 or buzzer output

0: Select I/O port 4 (P4-2)
1: Select buzzer output

BM1	BM0	Buzzer output mode	
0	0	Continuous output	Mode A
0	1	Single output	Mode B
1	0	10-Hz intermittent output	Mode C
1	1	10-Hz intermittent output at 1 Hz intervals	Mode D

	Y1	Y2	Y4	Y8
φK26		BUZR 10Hz		

Buzzer dedicated 10-Hz timing operation monitor

Note: When the BEN bit is set to "1", 10 Hz operates at the base clock of 100 Hz.
Refer to the 10-Hz timer when Mode D is selected.

The buzzer output is also used as the P4-2 I/O port. It can be switched to buzzer output by setting the BUZR ON bit to “1” and setting the P4-2 I/O control port to output.

Once the buzzer frequency, mode and logic are specified, set the buzzer enable bit to “1”, and the buzzer will be emitted. Set the buzzer enable bit to “0” for condition setting.

In the continuous output mode (Mode A), when the buzzer enable bit is set to “1”, the buzzer frequency will be outputted continuously. Set the bit to “0” to stop the buzzer output.

In the single output mode (Mode B), a 50-ms buzzer will be outputted and stopped each time the buzzer enable bit is set to “1”. In this mode, the buzzer output time can be extended by 50 ms to issue a 100-ms buzzer by setting the buzzer enable bit to “1” again during output of the 50-ms buzzer. The buzzer output time can be further extended to 150 ms by setting the bit to “1” again during extended 50 ms. This facilitates adjusting the buzzer output time.

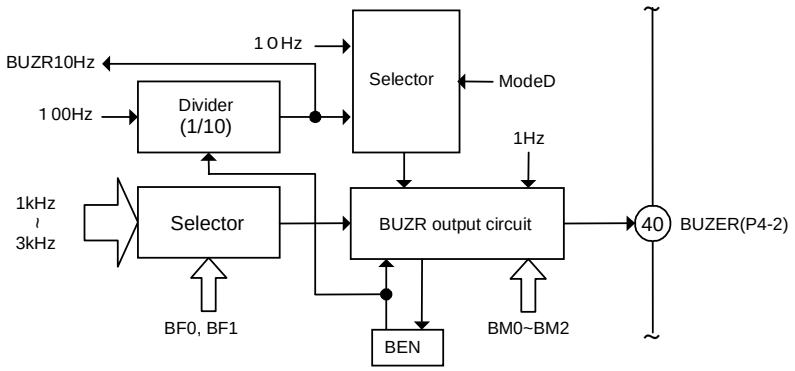
In the 10-Hz intermittent output mode (Mode C), the cycle of 50-ms buzzer ON and OFF respectively will be repeated continuously by setting the buzzer enable bit to “1”. Set the bit to “0” to stop the buzzer output.

In the 10-Hz intermittent output mode at 1Hz intervals (Mode D), when the buzzer enable bit is set to “1”, the cycle of 50-ms buzzer ON and OFF respectively will be outputted for 500 ms, the buzzer will be stopped for 500 ms and again the cycle of 50-ms buzzer ON and OFF will be outputted for 500 ms. These cycles are repeated until the buzzer output is stopped by setting the bit to “0”.

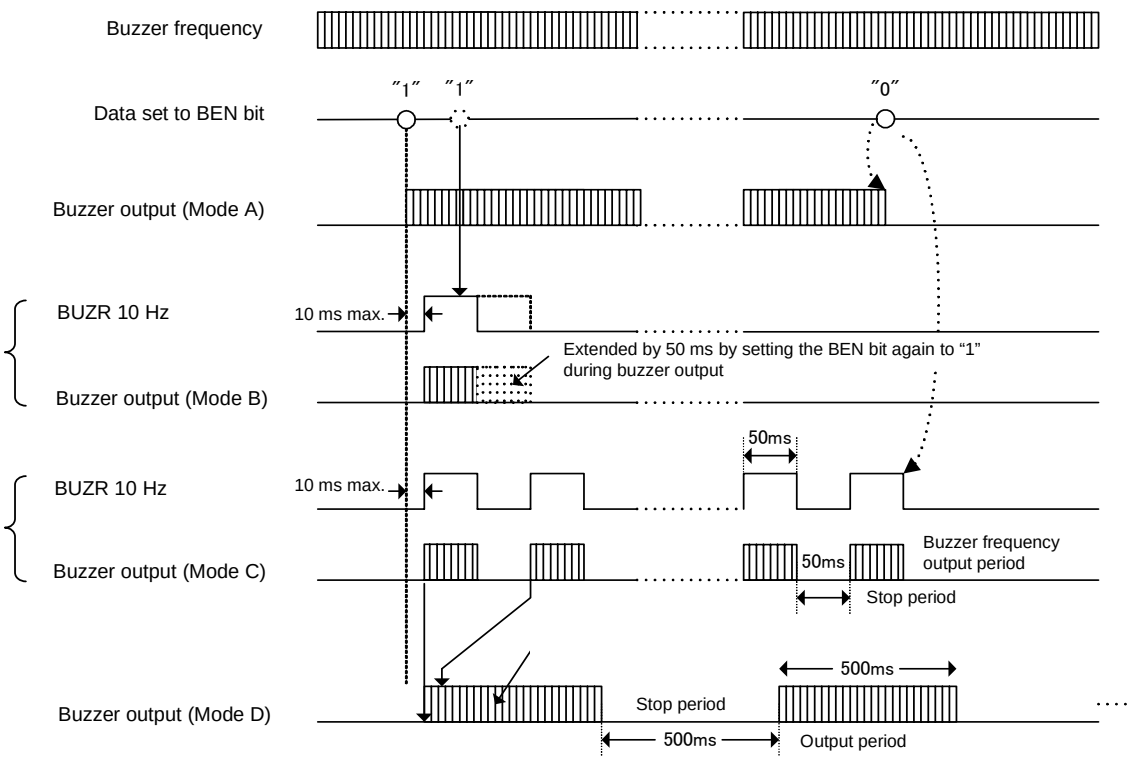
In Modes B, C and D, a 50 ms buzzer will be outputted and stopped even if the enable bit is set to “0” to stop the buzzer in the buzzer output state. The buzzer output state can be checked based on the details of the BUZR 10 Hz bit. When the BUZR 10 Hz bit is set to “0”, it shows the buzzer output state. When the bit is “1”, it shows the buzzer is stopped. Refer to the 10 Hz timer in Mode D.

Buzzer control can be accessed at OUT1 instruction data port 6.

2. Buzzer Circuit Configuration



3. Buzzer Output Timing



Note: To output the buzzer, set P4-2 to the output state (set the I/O control port to "1").

Note: The buzzer is stopped compulsory by setting BEN = 0.

Note: When the frequency setting is changed during buzzer output in Mode B, it will be updated and the 10-Hz timing change points changed.

○ LCD Driver

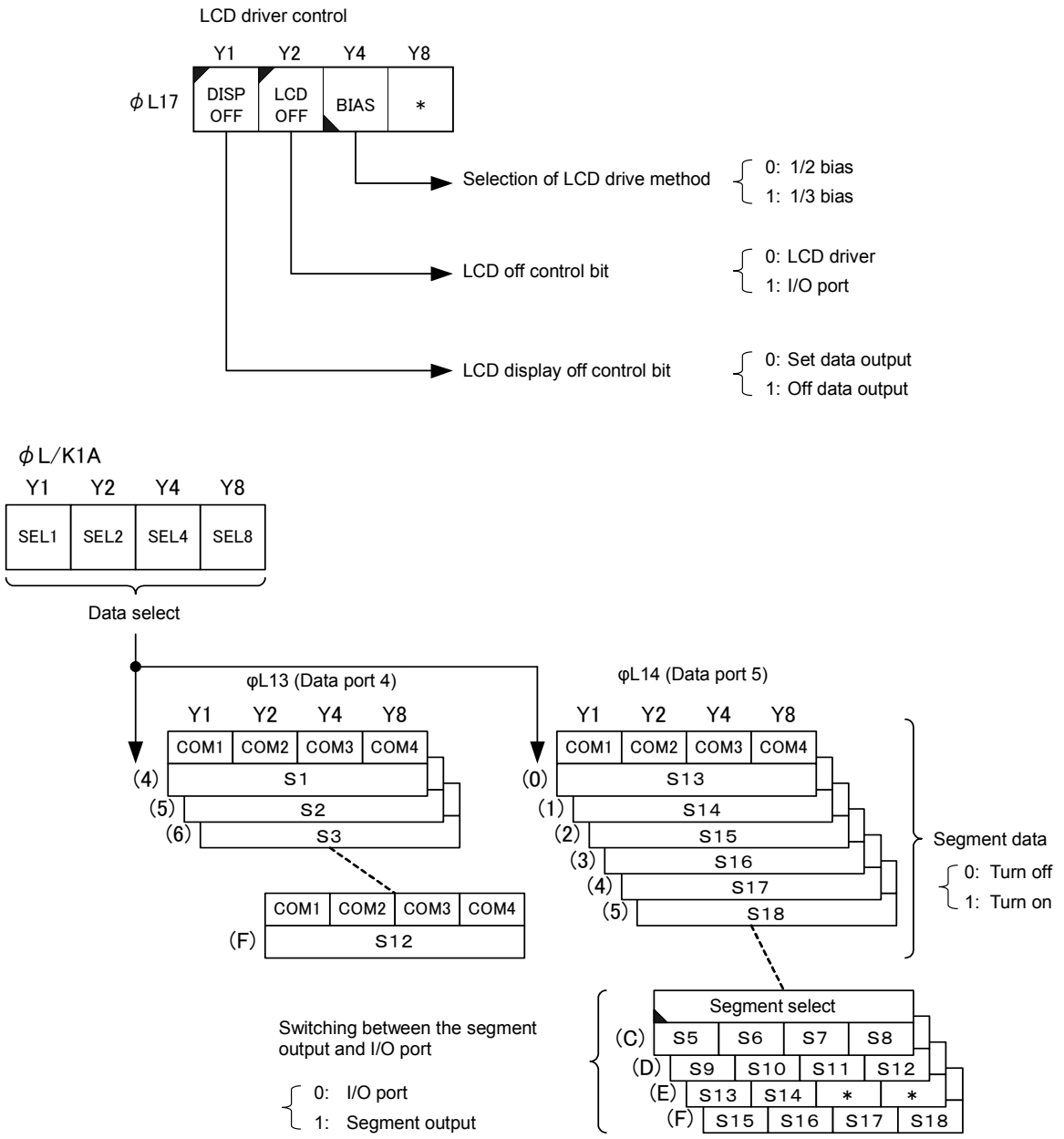
The LCD driver is also used as an I/O port, and it allows a maximum of 72 segments to turn on. When the LCD driver is enabled, I/O port 10 is switched to COM1 to COM4 pins and I/O port 12 is switched to S1 to S4 pins. Each of the 14 pins of I/O ports 13, 14, 15 and 16 can be set to segment pin output.

The driving method of the LCD driver can be selected from 1/4 duty, 1/2 bias (frame frequency 62.5 Hz) and 1/3 bias drive (frame frequency 125 Hz).

The LCD driver is built-in the constant voltage for display (V_{EE} = 1.5 V) and the doubler circuit (V_{LCD} = 3.0 V) that increases the display voltage. The LCD driver ensures a stable LCD display; even if the supply voltage fluctuates. (→ Refer to the section on the CD driver doubler circuit.)

In the 1/2 bias mode, the LCD driver provides common output at three potentials V_{LCD}, V_{LCD} × 1/2 and GND, and provides segment output at two potentials V_{LCD}, GND. In the 1/3 bias mode, the LCD driver provides common and segment outputs at four potentials V_{LCD}, V_{LCD} × 2/3, V_{LCD} × 1/3 and GND.

1. LCD Driver Ports



Note: Segment data controls the segments on/off corresponding to the common and segment outputs.

The LCD driver control ports are assigned to data control ports 4 and 5; as selected at the select port. These ports are accessed by using the OUT1 instruction with [CN = 3H, 4H] specified in the operand.

● LCD driver segment data

The LCD driver segment data is specified at data ports 4 and 5 (ϕL13 and ϕL14). When the segment data port is set to “0”, the LCD display turns off. When the port is set to “1”, the LCD display turns on.

● LCD OFF bit

The LCD OFF bit controls switching between the LCD output pin and the I/O port. After a reset, the pin that serves as both an I/O port and LCD driver is in the I/O port state. Set this bit to “0” when using the LCD driver function. When the LCD driver function is enabled, four of the I/O port pins P10-0 to P10-3 are switched to the COM1 to COM4 output pins, and four pins P12-0 to P12-3 are switched to the S1 to S4 output pins.

Note: This bit is set to “1” after a system reset.

● DISP OFF bit

The DISP OFF bit allows all the LCD display to turn off without setting segment data. Setting this bit to “1” turns all the LCD display off. At this time, the segment data is retained. When the DISP OFF bit is set to “0”, the previous display will appear on the LCD as it is.

Note: Segment data can be rewritten during DISP OFF.

Note: After the CKSTP instruction is executed, the DISP OFF bit is set to “1”. After the CKSTP instruction is released, set the DISP OFF bit to “0” as required.

Note: This bit is reset to “0” after system reset.

● BIAS bit

The BIAS bit selects the liquid crystal driving method. Set this bit to “0” to select the 1/2 bias method (frame frequency 62.5 Hz) or set to “1” to select the 1/3 bias method (frame frequency 125 Hz)

Note: In the 1/3 bias mode, the consumption current becomes about 100 μA larger than that in the 1/2 bias mode.

Note: This bit is reset to “0” after a system reset.

● Segment select port

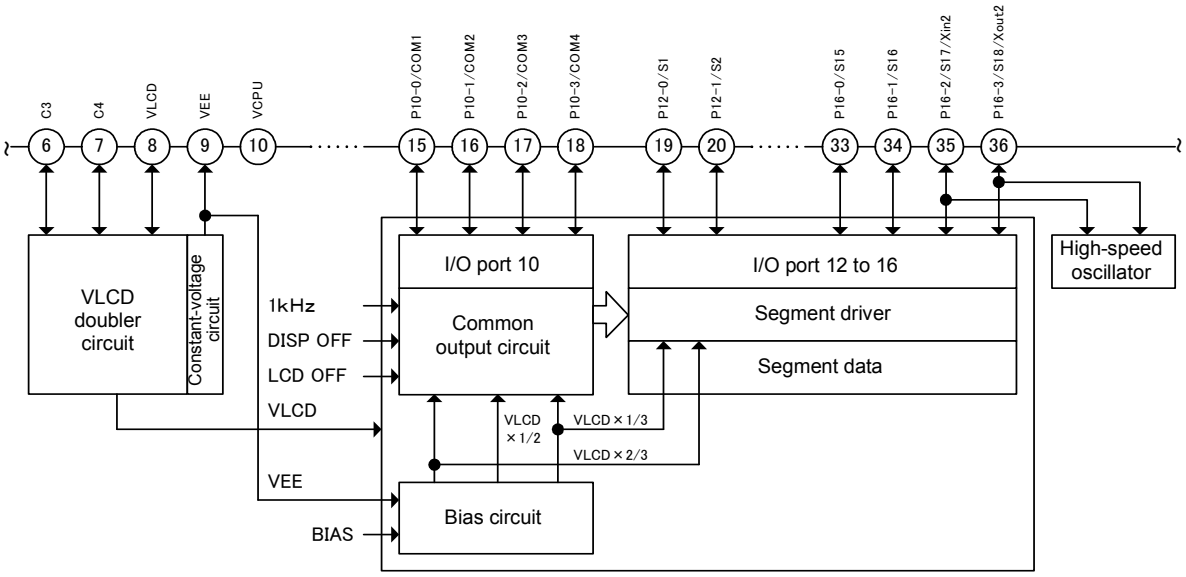
Each of the 14 pins of I/O ports 13 to 16 can be switched to a segment pin. Set the bit corresponding to each segment to “1” to use the pin for segment output, or set to “0” to use the pin as an I/O port. The S5 to S8 bits correspond to pins P13-0 to P13-3 respectively. The S9 to S12 bits correspond to pins P14-0 to P14-3 respectively. The S13 and S14 bits correspond to pins P15-0 and P15-1 respectively. The S15 to S18 bits correspond to pins P16-0 to P16-3 respectively.

Note: Segment output and I/O port setting can be made regardless of the LCD off control bit (LCD OFF). However, the pins that have been set to segment output require setting of the LCD off control bit to the LCD driver to enable segment output.

Note: Pins S21 and S22 are also used as high-speed oscillator pins. When they are set to high-speed oscillator pins, the high-speed oscillator function has priority and this port becomes to “don't care” state.

Note: This bit is reset to “0” after a system reset.

2. LCD Driver Configuration



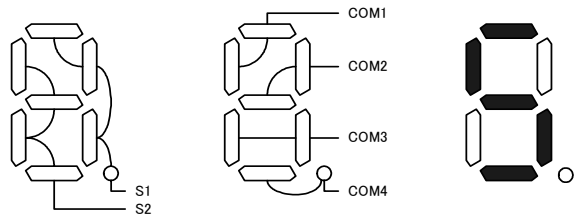
Note: After a system reset, all the pins that also serve as the LCD driver pins will be the I/O port input state.

Note: The LCD driver pins are also used as I/O ports and high-speed oscillator pins.

3. LCD Driver Operation Timing

● LCD output waveform in the 1/2 bias mode (BIAS bit= “0”)

In the 1/2 bias mode, the potential of the LCD driver waveform is outputted as V_{LCD} and GND and the V_{EE} level is outputted at a frame frequency of 62.5 Hz.

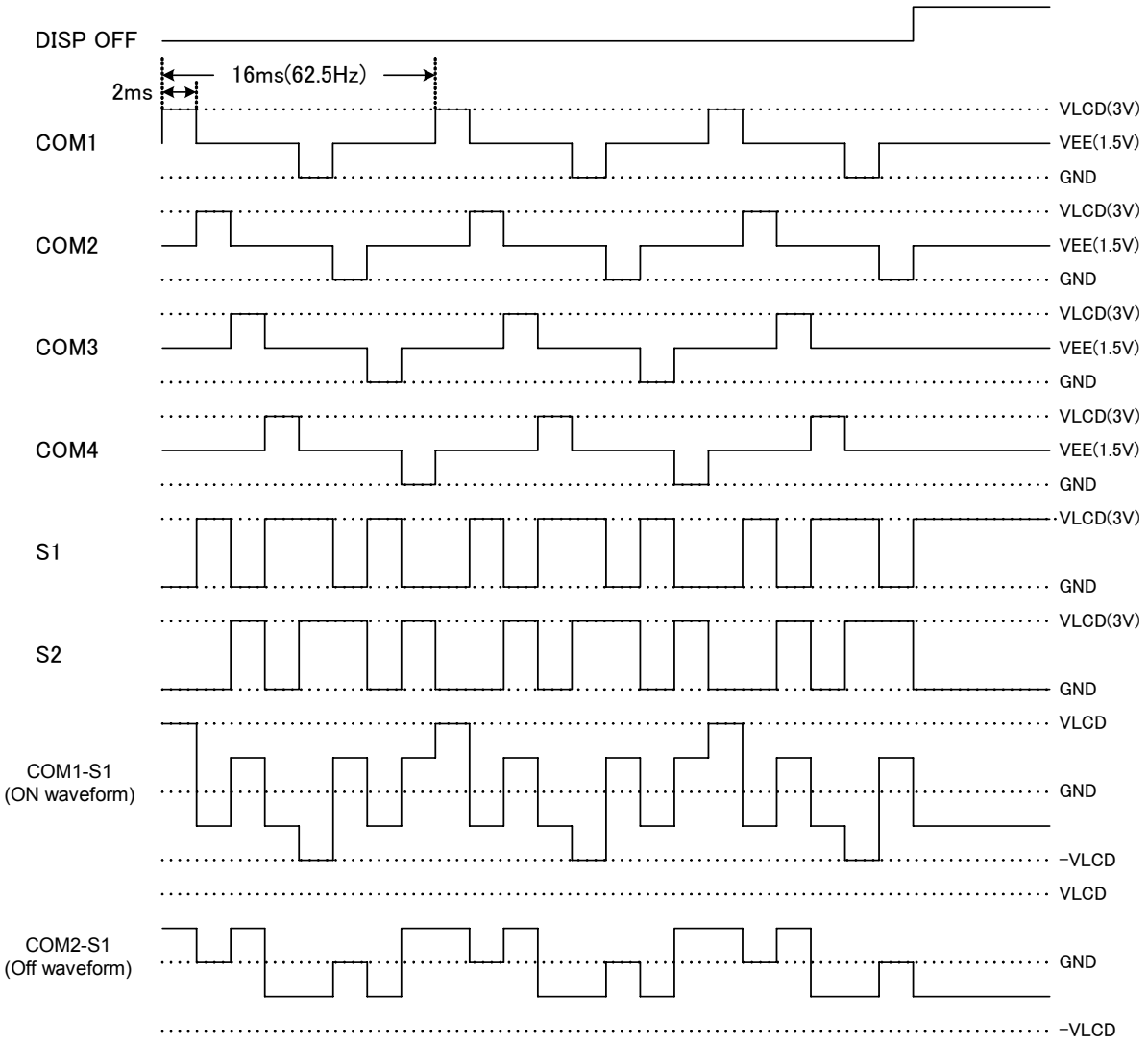


Example of segment data

Segment data 1(ϕL13, ϕL14)

	Y1	Y2	Y4	Y8
0 (S1)	COM1	COM2	COM3	COM4
	1	0	1	0
1 (S2)	COM1	COM2	COM3	COM4
	1	1	0	1

Data select(ϕL/K1A)

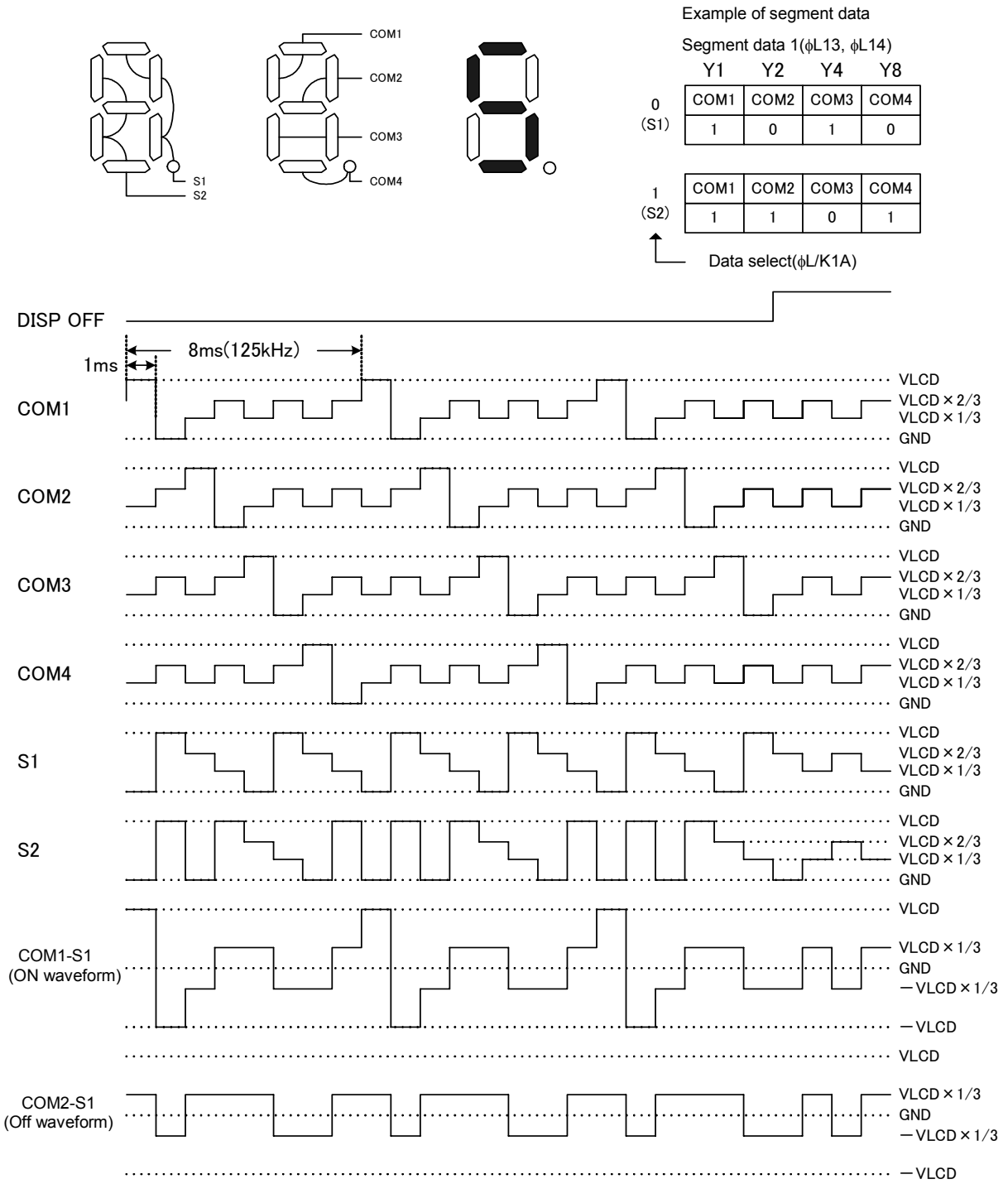


Note: Setting the DISP OFF bit to “L” causes the common output to revert to the VLCD × 1/2 level and turns all the display off.

Note: All the common and segment outputs are fixed to the “L” level in the clock stop mode and for 100 ms after this is released.

● LCD output waveform in the 1/3 bias mode (BIAS bit= “1”)

The potential of the LCD driver waveform is outputted as V_{LCD} and GND, and the intermediate potential levels, 1/3 and 2/3 of potential V_{LCD} are outputted at a frame frequency of 125 Hz.



Note: Setting the DISP OFF bit to “1” outputs unselected waveforms as common and segment outputs.

Note: All the common and segment outputs are fixed to the “L” level in the clock stop mode and for 100 ms after this is released.

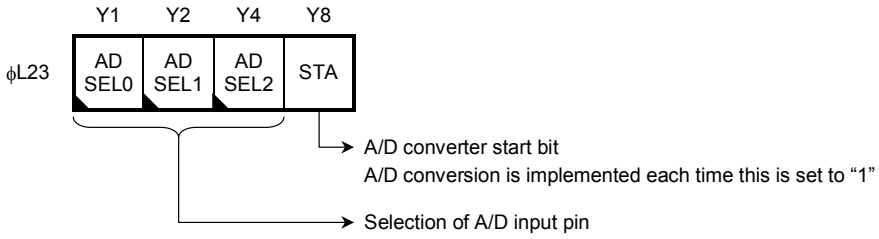
Note: In the 1/3 bias mode, the frame frequency is twice as high as that in the 1/2 bias mode.

Note: In the 1/3 bias mode, the consumption current becomes about 100 μs larger than that in the 1/2 bias mode.

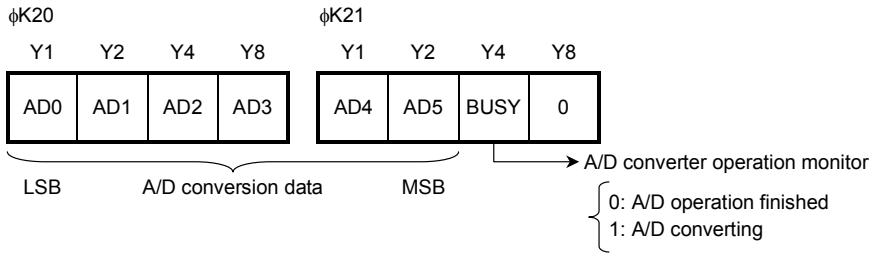
○ A/D Converter

The A/D converter has four channels with 6-bit resolution, and can be used for measuring electrical field strength, measurements of battery and cell voltages and key input using ladder resistance.

1. A/D Converter Control Port and Data Port



SEL2	SEL1	SEL0	AD input
0	0	0	ADin1
0	0	1	ADin2
0	1	0	ADin3
0	1	1	ADin4
1	*	*	$V_{EE}/2$



The A/D converter operates using a serial comparison system with 6-bit resolution. The standard voltage for A/D conversion is the internal power supply (V_{DD}), which is divided into 64 parts. The divided voltage is compared to the A/D input voltage and the data is outputted to the A/D conversion data port. The A/D conversion input uses the multiplex method; consisting of four channels of external input pins (ADin1 to ADin4 pins) and the half potential of the V_{EE} pin voltage. The desired method can be selected by the AD SEL0 to 2 bits.

The A/D converter carries out A/D conversion each time the STA bit is set to "1", and finishes operation after 6 machine cycles (240 μs). Completion of the A/D converter operation can be determined by checking the BUSY bit. Once the A/D conversion is finished, the A/D conversion data is taken into the data memory.

The results of the A/D conversion can be obtained by performing the following calculation:

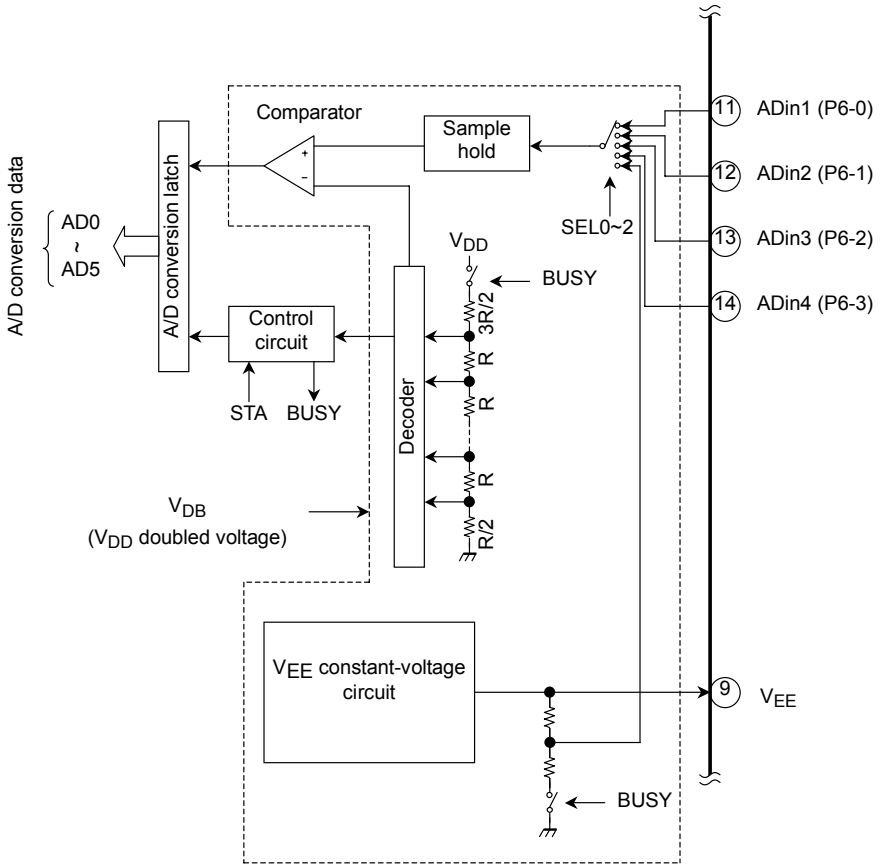
$$V_{DD} \times \frac{n - 0.5}{64} \ (63 \geqq n \geqq 1) \ \leqq \text{A/D input voltage} \ \leqq V_{DD} \times \frac{n + 0.5}{64} \ (62 \geqq n \geqq 0)$$

(n: A/D conversion data value [decimal scale])

$V_{EE}/2$ for A/D input is used for battery detection. The V_{EE} potential is normally 1.5 V. The half potential of the V_{EE} pin voltage, 0.75 V, is selected for A/D input. Through the A/D conversion of this potential, the reference potential, V_{DD}, can be detected. When the V_{DD} potential is 1.5 V, the A/D conversion data is 20H. As the V_{DD} potential becomes lower, the A/D data becomes higher. When the V_{DD} potential is 0.75 V, the A/D conversion data is 3FH.

This control is accessed by using the OUT2/IN2 instructions with [CN = 3H, 4H] specified in the operand.

2. A/D Converter Circuit Configuration



The A/D converter consists of a 6-bit D/A converter, a sample hold, a comparator, an A/D conversion latch and a control circuit. The 6-bit D/A converter and the comparator operate only when the BUSY bit is "1". Therefore, the A/D converter consumes no current when it is not operating. The half potential of V_{EE} constant voltage can be selected as the A/D input.

The A/D converter operates on the doubled voltage V_{DB} ($V_{DD} \times 2$).

Note: Set to "1" the I/O port –6 (N-ch open-drain) output data corresponding to the A/D input pin to be used, to use the pin in the input state.

Note: The V_{EE} contant-voltage potential is used for the LCD driver driving voltage and the reference voltage of reduced-voltage detection circuit for the DC-DC converter for CPU and VT.

Note: Voltage of 0 V to V_{DB} pin level can be applied to the A/D input pin.

○ Programmable Counter

The programmable counter consists of a 2-modulus pre-scalar, a 4-bit and 12-bit programmable counter and a port that controls these elements.

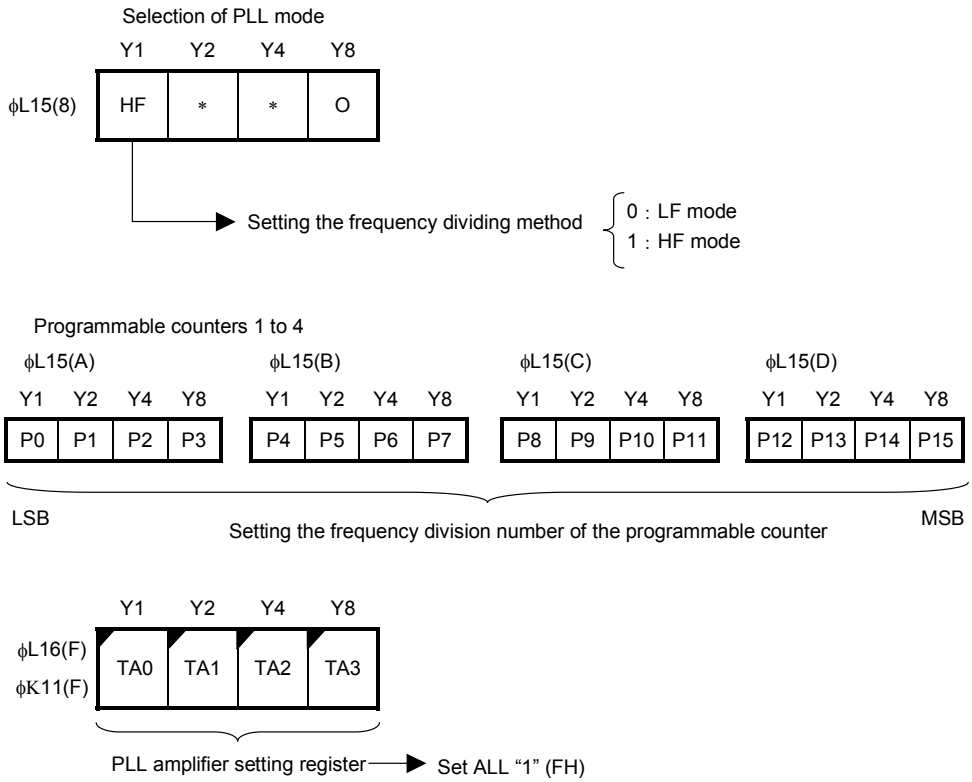
The programmable counter stops operation in the PLL off mode, and operates in the PLL on mode respectively. The radiation and consumption current can be reduced when the programmable counter is used in combination with the 1-chip tuner with a built-in 1/16 pre-scaler.

The frequency divided by the programmable counter is inputted to the phase comparator, and the phase difference from the reference frequency is outputted from the phase comparator. The internal clock of the programmable counter can also be used to detect phase difference of the phase comparator and the doubler clock for DC-DC converter for VT.

(→ Refer to the sections on Reference frequency divider, DC-DC converter for VT and Phase comparator.)

1. Program Counter Control Port

The PLL mode selection port is used for setting the frequency dividing method, while the programmable counter port is used for setting the frequency division number.



The selection of the PLL mode and setting of the frequency division number of programmable counter are assigned to data port 6 that has been selected at the select port. These controls are accessed by using the OUT1 instruction with [CN = 5H] specified in the operand.

There are two types of frequency division methods; the direct frequency division method (LF mode) and the pulse swallow method (HF mode). Select a method depending on the frequency to be used and the frequency division number that has been set.

The programmable counter has 12 bits (P4 to P15) in the LF mode and 16 bits (P0 to P15) in the HF mode. The frequency division number is specified by writing it to the MSB bit (ϕL15(D). Once the MSB bit is set, all the data of P0 to P15 will be updated. Therefore, the MSB bit must be accessed and specified last, even when part of the data is changed.

The PLL input (OSCin) has an input amplifier. Set this amplifier gain at the PLL amplifier setting registers. Set all of these registers to "1" (FH).

Note: Set the Y8 bit of the PLL mode select port (ϕL15(8)) to "0".

Note: All the PLL amplifier setting registars are set to "1" after a system reset.

Note: In the PLL amplifier setting registers, the TA0 and TA1 bits are for the OSCin input amplifier gain setting and the TA2 and TA3 bits are for the IFin input amplifier gain setting respectively.

2. Setting the Frequency Dividing Method and Gain of The Programmable Counter

Using the HF bit, select the pulse swallow or direct frequency division methods; depending on the received frequency.

The programmable counter is used in combination with the 1-chip tuner with a built-in 1/16 or 1/8 pre-scaler. Usually, use the tuner to input the local oscillation frequency, which is then inputted to the OSCin input in the MW/LW/SW wavebands. The tuner local oscillation frequency is divided into 16 or 8 parts and the divided frequency is inputted to the OSCin input in the FM/TV band mode.

The OSCin input has an input amplifier that allows small-amplitude operation. The input amplifier has the registers (ϕL16(F), ϕK11(F)) to adjust the amplifier gain. Set all of these registers to "1" (FH).

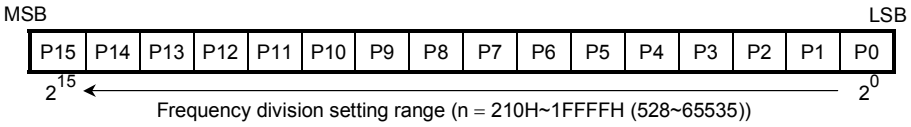
Mode	HF	Frequency dividing method	OSCin operation input frequency range	Example of receive band	Frequency dividing range
LF	0	Direct frequency dividing method	0.5~4 MHz	MW/LW	10H~FFFH (16~4095)
HF	1	Pulse swallow method (1/15・16)	1~30 MHz	SW/FM/TV	210H~FFFFH (528～65535)

Note: The local oscillation input is common to each mode and is inputted to the OSCin pin.

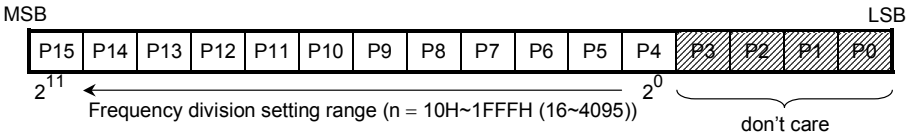
3. Setting the Frequency division number

Set the frequency division number for the programmable counter at P0 to P15 bits in the binary format.

- Pulse swallow method (16 bits)



- Direct frequency division method (12 bits)



Note: Set the frequency division value in consideration of the tuner pre-scaler frequency division.

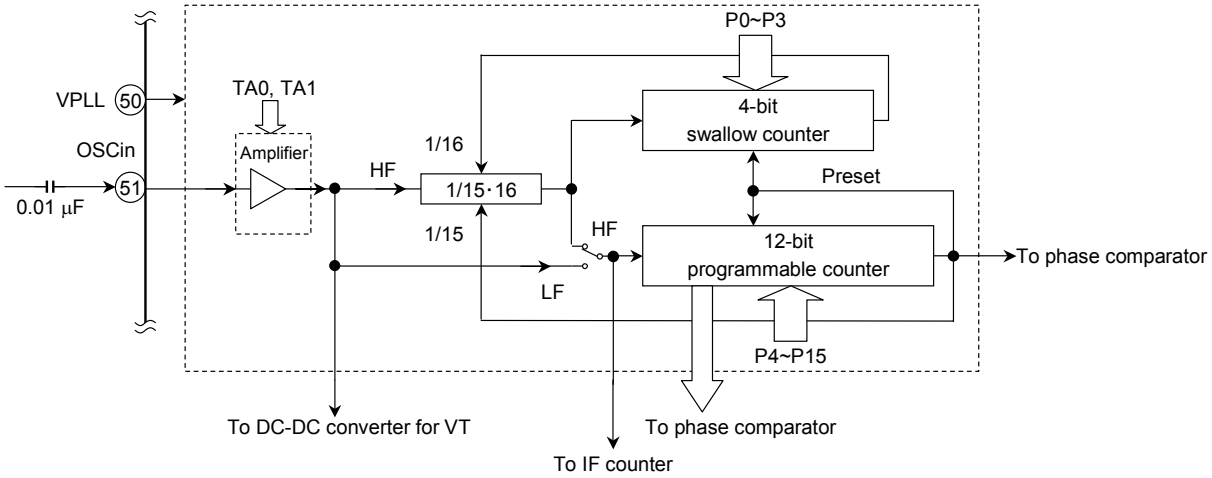
Note: Set the frequency division number by writing it into the MSB bit (ϕL15(D)).

4. Programmable Counter Circuit Configuration

The circuit consists of an amplifier, 1/15・16 2-modulus pre-scaler, a 4-bit swallow counter and a 12-bit binary programmable counter. When the HF mode is selected, the 1/15・16 pre-scaler, the 4-bit swallow counter and the 12-bit binary programmable counter are used. When the LF mode is selected, only the 12-bit binary programmable counter is used.

The OSCin input clock is supplied to the DC-DC converter for VT, and used as the doubler clock. The clock divided by the programmable counter is also supplied to the phase comparator and the IF counter.

(→ Refer to the sections on DC-DC converter for VT and Phase comparator.)



Note: The programmable counter uses the V_{PLL} pin power supply. This power supply can be supplied regardless of the power supply level of the V_{DD}/V_{CPU} pin. In the PLL off mode, the V_{PLL} pin power supply can be turned off. The programmable counter setting registers use the V_{CPU} pin power supply, so that the contents of the registers are retained after the V_{PLL} pin power supply is turned off.

Note: The OSCin pin has an amplifier that allows small-amplitude operation with coupled capacitor. The OSCin input is subject to high impedance in the PLL off mode.

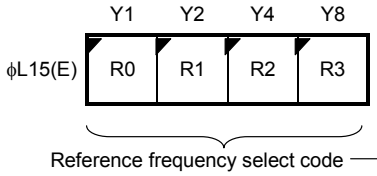
○ Reference Frequency Divider

The external 75 kHz crystal oscillation frequency is divided to generate the following ten types of PLL reference frequency signals; 1 kHz, 1.39 kHz, 1.56 kHz, 2.78 kHz, 3 kHz, 3.125 kHz, 5 kHz, 6.25 kHz, 12.5 kHz and 25 kHz respectively. These signals can be selected by the reference port data.

The selected signal is supplied as a reference frequency for the phase comparator as described below. The PLL on/off is controlled by the contents of the reference port.

1. Reference Port

This is an internal port for selecting ten types of reference frequency signals. This port is located in data port 6 as selected at the select port, and can be accessed by using the OUT1 instruction with [CN = 5H] specified in the operand. When the reference port is set to all "1", all the programmable counters, IF counters, reference counters and the phase comparator will be stopped and enter the PLL off mode. When the reference port setting is set, the frequency division setting data for the programmable counter will be updated. Therefore, the frequency division number of the programmable counter must be determined before setting the reference port.



R3	R2	R1	R0		Oscillation frequency
0	0	0	0	0	1 kHz
0	0	0	1	1	1.3889 kHz
0	0	1	0	2	1.5625 kHz
0	0	1	1	3	2.7778 kHz
0	1	0	0	4	3 kHz
0	1	0	1	5	3.125 kHz
0	1	1	0	6	5 kHz
0	1	1	1	7	6.25 kHz
1	0	0	0	8	12.5 kHz
1	0	0	1	9	25 kHz
1	0	1	0	A	Prohibition
1	0	1	1	B	Prohibition
1	1	0	0	C	Prohibition
1	1	0	1	D	Prohibition
1	1	1	0	E	Prohibition
1	1	1	1	F	PLL off mode

Note: After a system reset, this port is set to all "1" and becomes to PLL off mode.

Note: When the $\overline{INH}$ pin input permission is set by using the $\overline{INH}$ ENA bit, the PLL off mode becomes the $\overline{INH}$ input or the PLL off mode as shown above.

○ Phase Comparator and Lock Detection port

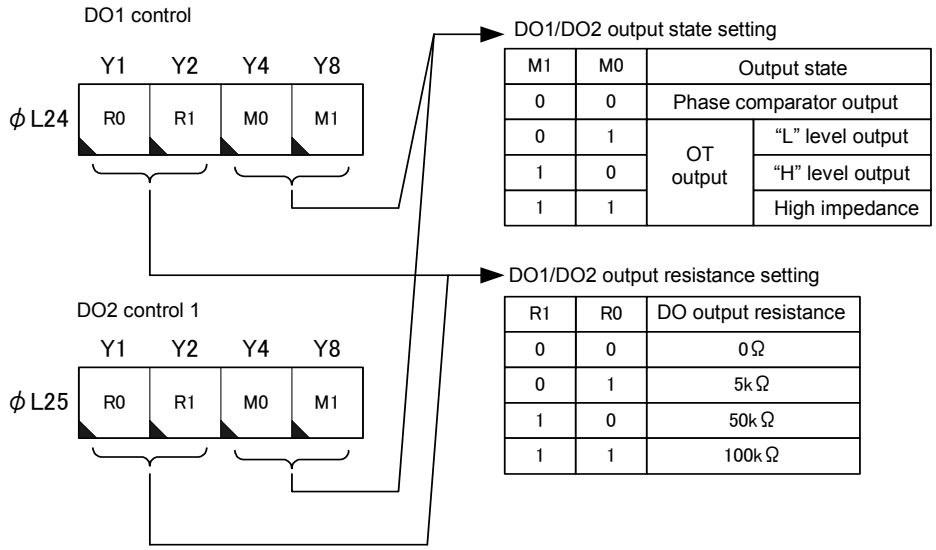
The phase comparator compares the reference frequency supplied from the reference frequency divider and the programmable counter divided frequency output to determine the phase difference and outputs errors. It then controls the voltage control oscillator (VCO) through the low-pass filter to match the frequency and phase difference of these two signals.

There are two pins available for the phase comparator, each including individually adjustable output resistance. This resistance can be set to three types, namely 5, 50 and 100 kΩ. It also includes automatic switching by detection of the phase difference, the N-channel transistor for an LFP amplifier that withstands 5.5 V and the external charge pump output mode.

The phase comparator and the charge pump output use the DC-DC converter power supply (V_{DB}: $V_{DD} \times 2$) for CPU.

Note that the phase comparator output pins (DO1/2) can be used as general-purpose output ports by using the DO control port.

1. Phase Comparator (DO) Control Port and Unlock Detection Port

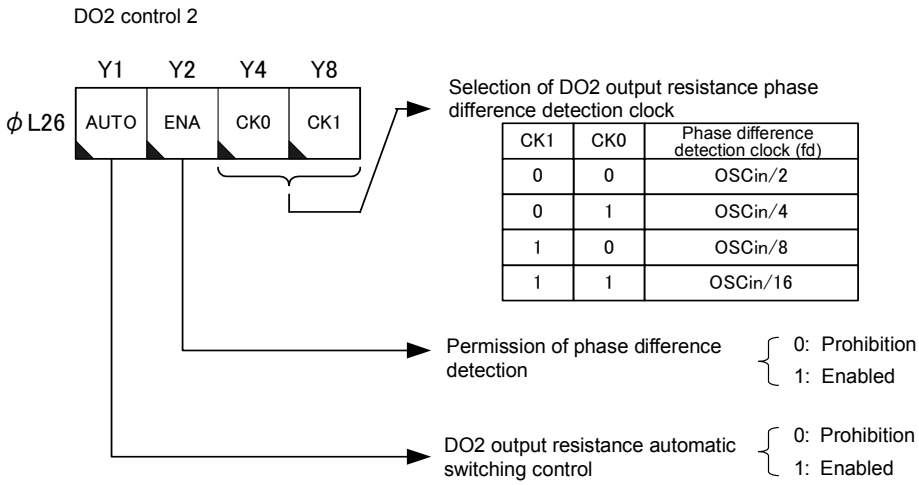


DO1/DO2 output state setting

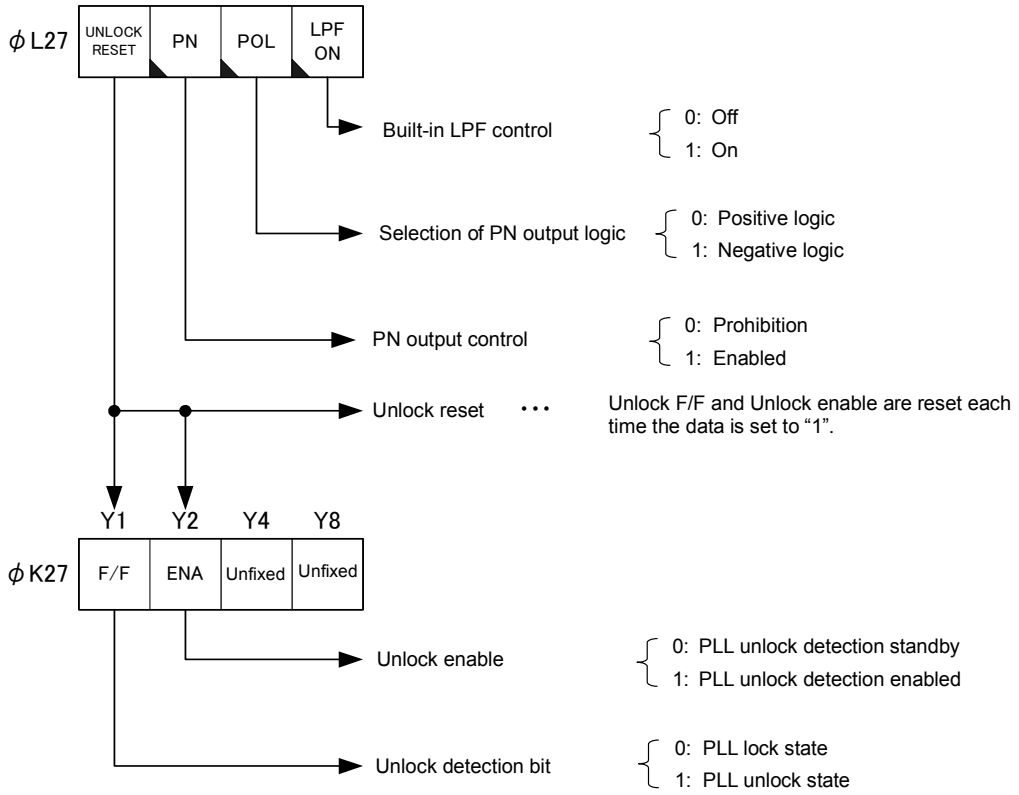
M1	M0	Output state	
0	0	Phase comparator output	
0	1	OT output	"L" level output
1	0		"H" level output
1	1		High impedance

DO1/DO2 output resistance setting

R1	R0	DO output resistance
0	0	0Ω
0	1	5kΩ
1	0	50kΩ
1	1	100kΩ



CK1	CK0	Phase difference detection clock (fd)
0	0	OSCin/2
0	1	OSCin/4
1	0	OSCin/8
1	1	OSCin/16



Note: Y4/Y8 bits of the unlock port (ϕK27) become unfixed.

The phase comparator control port and the unlock detection ports are accessed by using the OUT2 instruction with [CN = 4H, 5H, 6H, 7H] and the IN2 instruction with [CN = 7H] specified in the operand. These control bits are reset to "0" after a system reset.

● Output mode setting (M0 and M1 bits)

The M0 and M1 bits are used for setting the phase comparator output (DO1/2 output pin) state. The phase comparator output, the "H" and "L" levels and high impedance (HZ) state can be set.

Note: If the PLL off mode is selected, the "HZ" will be retained in the phase comparator output state, and the "H"/"L" level will be retained when the "H"/"L" level is selected.

Note: When PN = "1" is selected, the PN output mode has the priority.

● Output resistance setting (R0 and R1 bits)

The R0 and R1 bits are used for setting the output resistance of the phase comparator output individually for DO1 and DO2 pins. They can be set to four states; the normal output buffer state, 5 kΩ, 50 kΩ and 100 kΩ.

Note: The output resistance is set regardless of the output mode (M0, M1) and the PN output mode. Therefore, set these bits to "0" when the "H"/"L" level or the PN output mode is selected.

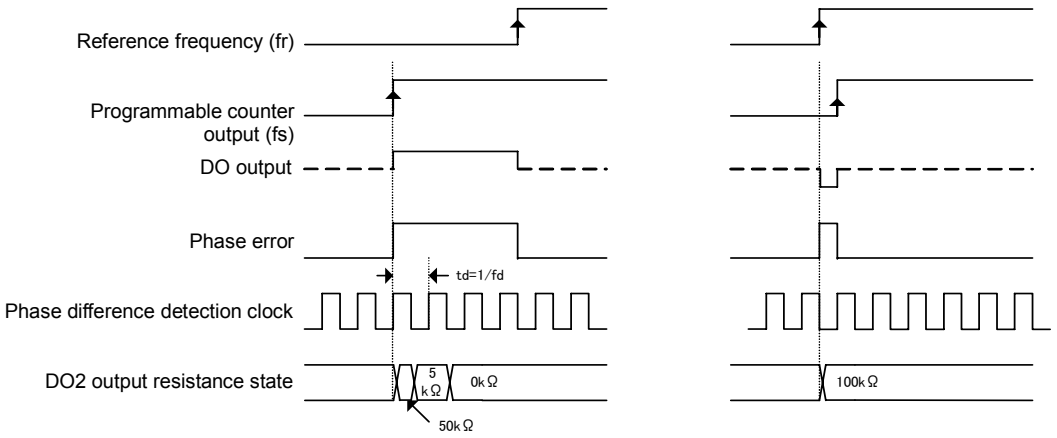
Note: When the DO2 pin is set to the automatic phase difference switching mode, the R0/R1 bits of DO2 control 1 becomes to the "don't care" state.

● Automatic phase difference switching mode (DO2 control 2 port: AUTO, ENA, CK0 and CK1 bits)

The DO2 pin has an automatic phase difference switching mode that switches the output resistance automatically; depending on the phase difference. In this mode, the output resistance becomes higher as the phase difference pulse becomes shorter, and vice versa. In other words, the system operates with a higher resistance in the lock state and conversely, with a lower resistance in an unlocked state. By using this mode, the lock up time can be improved.

When the ENA bit is set to "1", the phase difference detection operation is enabled. When the AUTO bit is set to "1", the DO2 output resistance switching is implemented.

Phase difference detection is implemented using the operation clock from the programmable counter circuit. This clock counts the unlock state in the binary format. Four types of OSCin input, 1/2, 1/4, 1/8 and 1/16 can be selected for this clock. The output resistance setting time can be switched by switching the clock. This control selects the clock frequency using the CK0 and CK1 bits. Select the clock frequency depending on the lock up time. After locking, turn off automatic switching and set the output resistance to fixed settings (R0 and R1 bits) as needed.



<Timing example 1>

Output resistance value	Phase difference resistance period	
	fr<fs (Example-1)	fr>fs (Example-2)
100kΩ	—	0～td/2
50kΩ	0～0.5×td	0～1.5×td
5kΩ	0.5×td～td	td～2.5×td
0kΩ	td～2×td	2×td～2.5×td

<Timing example 2>

CK1	CK0	Phase difference detection clock (fd)
0	0	OSCin/2
0	1	OSCin/4
1	0	OSCin/8
1	1	OSCin/16

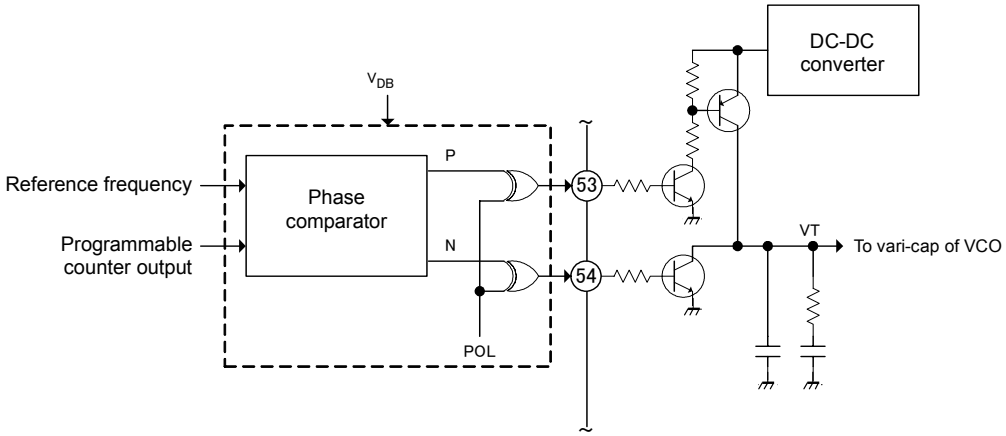
Note: When PN = "1" is selected, the PN output mode has priority.

Note: Effective only when the DO2 output mode setting is in the phase comparator output state.

● PN output mode (PN and POL bits)

The PN output mode is available using an external charge pump. When this mode is selected, the two DO1/2 pins are switched to the P- and N-output pins. The P/N output logic can be reversed by using the POL bit.

An example of the use of an external charge pump is shown below. Configure the circuit depending on your desired characteristics.



Example of use of the external charge pump (when PN= “1”)

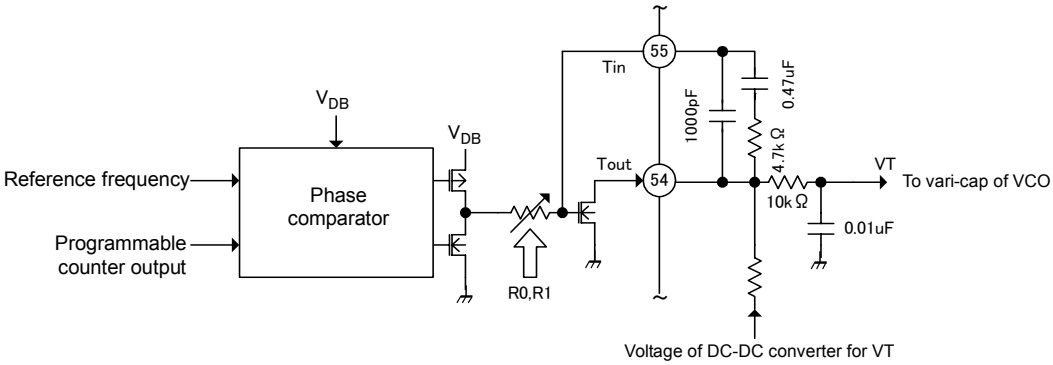
Note: Set the POL bit to “0” unless the PN output mode is selected.

Note: When the PN output mode is selected, the output will be CMOS output and the “H” level will be the V_{DB} pin level outputp.

● Built-in LPF amplifier (LPF ON bit)

This amplifier incorporates the N-channel FET transistor for LPF. This transistor withstands 5.5 V and it can configure the voltage control oscillator (VCO) that can vary the VT within a range of 0 to 5.5 V.

Setting the LPF ON bit to “1” turns the built-in LPF on. Pins DO2 and P9-1 are then switched to the FET gate input (Tin) and the FET drain pin (Tout) respectively. The DO2 phase comparator output is connected to the FET gate pin. The LPF can be configured only by connecting an external filter resistor and capacitor.



Configuration of built-in low-pass filter amplifier (when LPF ON= “1”)

Note: When the built-in LPF is used, the DO2 output mode, resistor setting and the automatic phase difference switching mode are available.

Note: The Tout output withstands up to 5.5 V. Do not use voltages exceeding this limit.

Note: Set the resistance values for R0 and R1 depending on your desired characteristics.

Note: The filter circuit constants shown above are for reference only. Examine and design actual circuits according to the system band configuration and your desired characteristics.

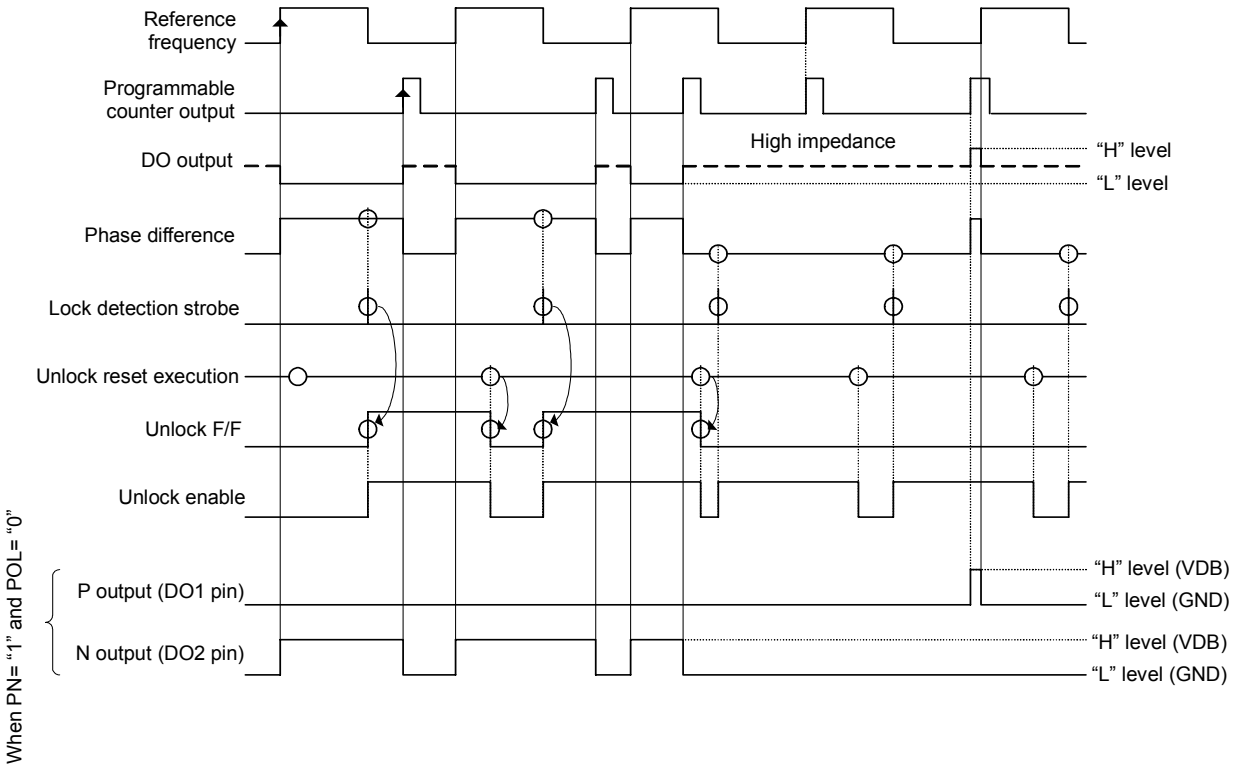
Note: The Tout pin is also used as pin P9-0. When the built-in LPF is used, the P9-0 output data will be invalid.

● Unlock detection port (UNLOCK RESET, UNLOCK F/F and ENA bits)

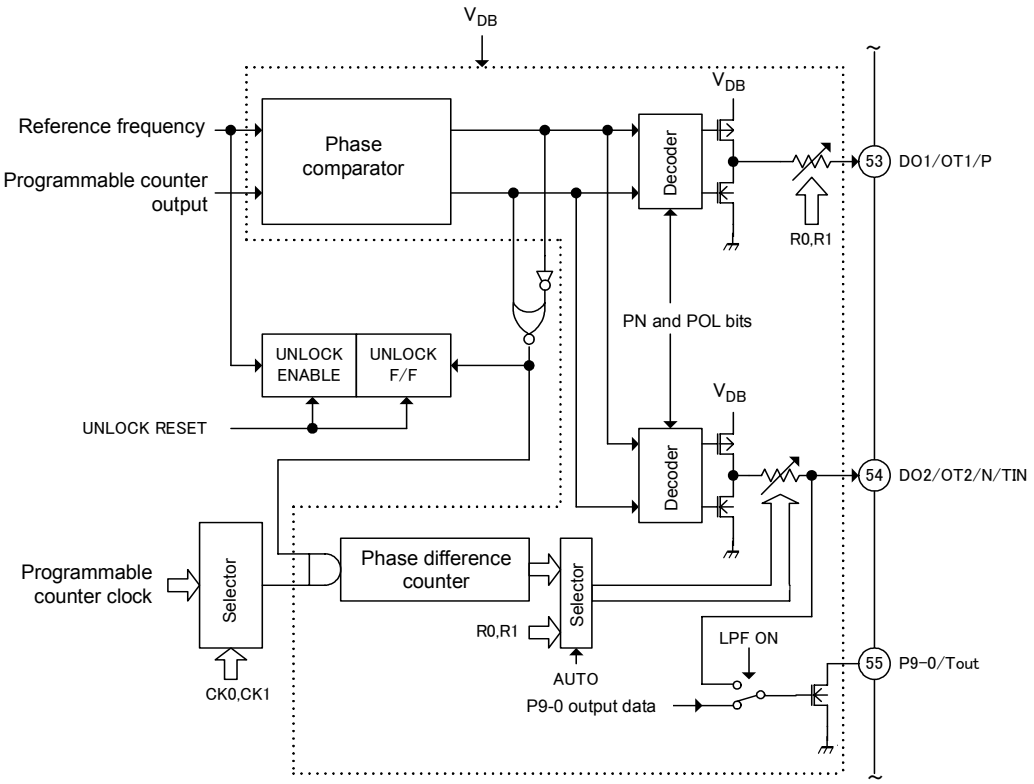
The unlock F/F detects the phase difference between the programmable counter frequency-divided output and the reference frequency at the timing with a phase shift of about 180° . If the phases do not match, or are in an unlocked state, the unlock F/F will be set. Each time the unlock reset bit is set to "1", the unlock F/F will be reset.

To detect the phase difference during the reference frequency cycle, it is necessary to provide an unlock F/F reset time no shorter than the reference frequency cycle before the unlock F/F is accessed. The enable bit is provided for this purpose. Make sure that the unlock enable is set to "1" before the unlock F/F is accessed.

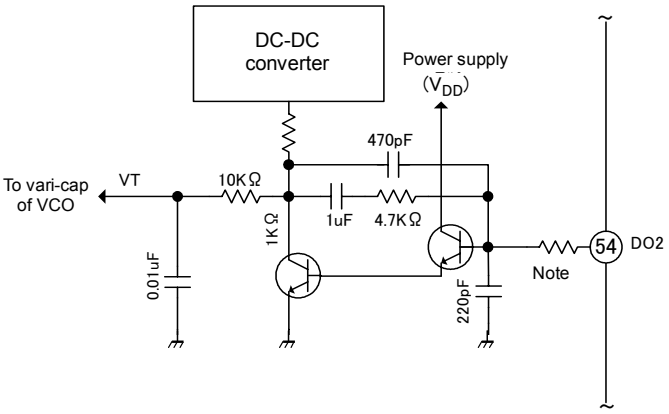
2. Phase Comparator and Unlock Port Timing



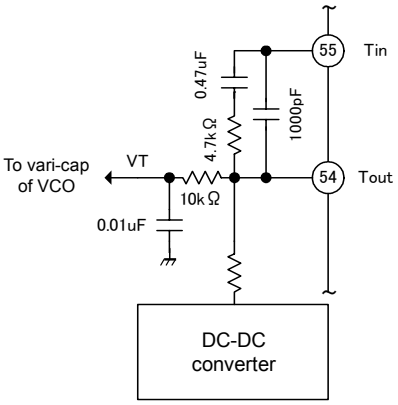
3. Phase Comparator and Unlock Port Circuit Configuration



Note: The phase comparator circuit block uses the V_{DB} power supply. Therefore, the V_{DB} power supply level is outputted as the "H" level of the phase comparator output pin (DO).



Example of external low-pass filter amplifier circuit



Example of built-in low-pass filter amplifier circuit

Note: The phase comparator pin has a built-in resistor. Add an output resistor if needed.

Note: For details of the DC-DC converter, refer to the section on the DC-DC converter for VT. When the DCK1 internal doubler transistor is used for the DC-DC converter voltage, design the tuner circuit to widen the variable range of the tuning voltage (VT).

Note: In the PLL off mode, the phase comparator output (DO1/2) will be "Hz". When the external low-pass filter (LPF) is used, the external LPF base potential will be unfixed, and the consumption current will increase from the power supply (V_{DD}) through the transistor. In the tuner off state (PLL off mode), fix the phase comparator output (DO1/2) to the "L" level output.

Note: The filter circuit constants shown above are for reference only. Examine and design actual circuits according to the system band configuration and your desired characteristics.

○ DC-DC Converter for VT

This product incorporates the DC-DC converter for the PLL low-pass filter.

The DC-DC converter increases voltage by using coil induced electric power. There are two methods for increasing voltage; using the built-in N-channel transistor and using the external transistor. Select either method depending on the voltage to be increased. This product also a VT clamps function to prevent exposure to voltage exceeding a certain limit. The clamp function is helpful for reducing the consumption current and protecting this product.

1. Control Port of DC-DC Converter for VT

Control 1 for DC-DC converter for VT

	Y1	Y2	Y4	Y8
φL15(5)	VDET SEL	0	VDET ENA	*

Permission of detection voltage input for DC-DC converter
- 0: Prohibition
- 1: Enabled

Selection of detection voltage for DC-DC converter
- 0: Detection voltage 0.75 V
- 1: Detection voltage 1.00 V

Control 2 for DC-DC converter for VT

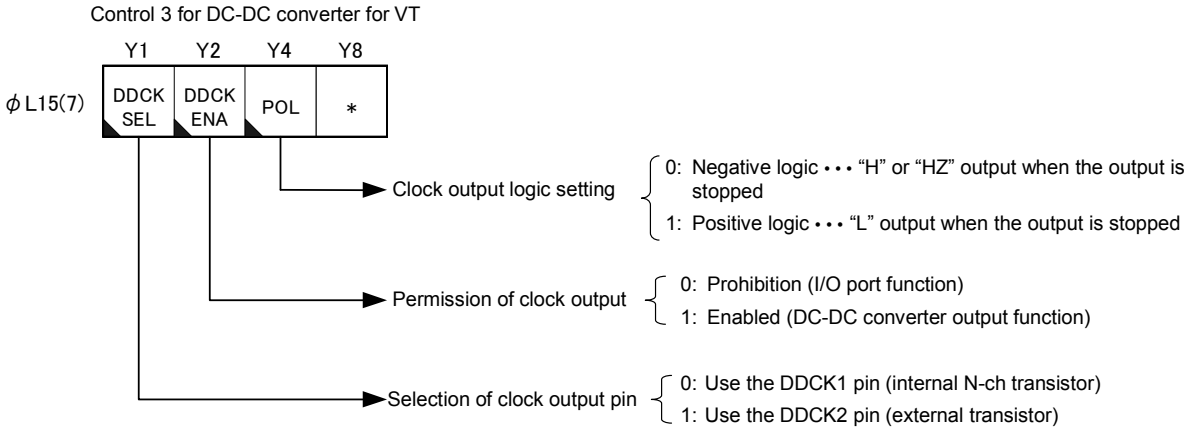
	Y1	Y2	Y4	Y8
φL15(6)	DD0	DD1	DD2	DD3

Selection of clock output frequency for DC-DC converter

DD3	DD2	DD1	DD0		Output frequency	Remarks
0	0	0	0	0	Clock stop	POL=0 → DDCK output "L", POL=1 → DDCK output "H" or "HZ"
0	0	0	1	1	PCTRin	External clock can be used from the P3-3/PCTRin pin input. (Note)
0	0	1	0	2	75kHz	75 kHz low-speed oscillator clock
0	0	1	1	3	fosc/2	Programmable counter clock Note: fosc is the OSCin input clock frequency.
0	1	0	0	4	fosc/4	
0	1	0	1	5	fosc/8	
0	1	1	0	6	fosc/16	
0	1	1	1	7	fosc/32	
1	0	0	0	8	fXT2	High-speed oscillator clock Note: Enable the high-speed oscillator when it is used.
1	0	0	1	9	fXT2/2	
1	0	1	0	A	fXT2/4	
1	0	1	1	B	fosc/3 Note	Programmable counter clock Note: The duty of fosc/3, or the ratio of the "H" or "HZ" level to the "L" level is 2:1 when POL= "0". The ratio is reversed when POL= "1". Note: fosc is the OSCin input clock frequency.
1	1	0	0	C	fosc/6	
1	1	0	1	D	fosc/12	
1	1	1	0	E	fosc/24	
1	1	1	1	F	fosc/48	

Note: Any clocks other than the fosc/3 clock have a duty of 50%.

Note: Enable the pulse counter function when using the PCTRin input clock



The DC-DC converter for VT outputs the double clock using the DDCK1 (also used as pin P8-1) or the DDCK2 (also used as pin P9-2). Setting the DDCK ENA bit to "1" enables the doubler operation. The DDCK SEL bit is used to select the pin to be used.

The clamp function is provided to keep the doubled voltage at or below a certain voltage. The clamp is controlled by the doubler detection voltage pin VDET (also used as pin P8-1). The doubled voltage is divided by resistance and the resultant potential is inputted into the VDET pin. When the VDET pin potential becomes lower than 0.75 V or 1.00 V, the doubler clock will operate. When the potential becomes higher than these values, the doubler clock will be stopped. The detection voltage can be selected from 0.75 V and 1.00 V and the detection operation is enabled by setting the VDET ENA bit to "1".

The doubler clock can be selected from 15 types. Select a frequency that is a little influence by the tuner beat or other factors.

The control port for the DC-DC converter for VT is assigned to data port 5, and is accessed by using the OUT1 instruction with [CN = 4H] specified in the operand. These control bits are reset to "0" after system reset.

Note: Set the Y2 bit of the Control 1 for the DC-DC converter for VT (ϕL15 (5)) to "0".

Note: When the doubler clock pin (DDCK1/2) and the doubler detection voltage input (VDET) are selected, the I/O port output data and control data of the same pins will be in "don't care" state.

Note: The DC-DC converter detection voltage input (VDET ENA bit) must be disabled ("0") in the PLL off mode or when it is not being used; otherwise it will increase the consumption current.

2. Setting of DC-DC Converter for VT

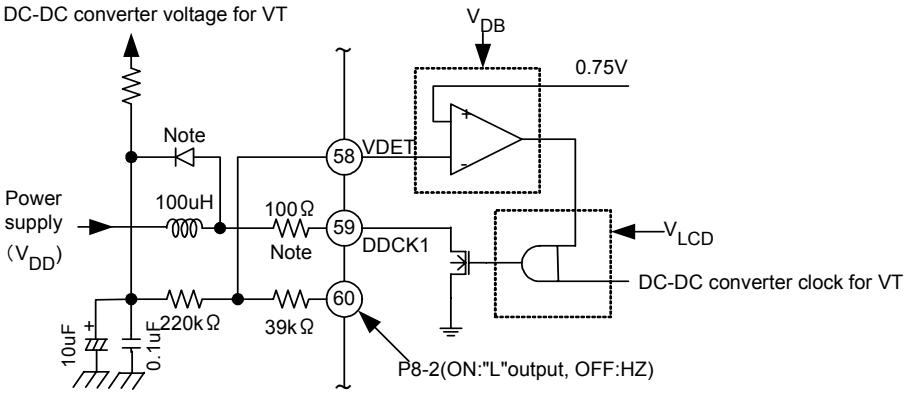
(1) Example of using the DDCK1 internal doubler transistor

The DDCK1 pin includes an N-ch transistor for the DC-DC converter, and it can drive the coil directly. This transistor can withstand 6 V and no voltage over this level is permitted. Usually, the doubler clamp function is used to keep the limit the voltage. Set the POL bit to “0” when the DDCK1 pin is used.

Shown below is an example of a DC-DC converter circuit using the DDCK1 pin.

The clock output of the DDCK1 pin supplies coil-induced pulses through the diode to increase the voltage. The increased voltage is then supplied to the low-pass filter as the doubled voltage for VT.

In the following example, pin P8-2, composed of pins 60, controls the turning the divided resistance on/off. When the doubler is on, the program outputs the I/O port “L” level to turn the resistance division on. When the doubler is off, the output is set to “HZ” (input setting) to disconnect the resistance division. Alternately, you can use the GND rather than the 60-pin connection. However, when the GND connection is used, the current from the V_{DD} power supply is always consumed through the coil and the divided resistance in the doubler off state. This way, this control function prevents the current from being consumed in the doubler system circuit when the doubler is off. Note that this control is unnecessary and the GND connection may be used instead, when the power supply used turns off in the tuner off state or when it doesn’t matter if the consumption current is increased in the system.



Example of internal DC-DC transistor doubler circuit

Note: Use the low-VF shot key diode for the diode shown above.
Recommended diode: 1SS357

Note: Determine the doubler coil constant depending on the DC-DC converter clock frequency and the doubler current capacity.

Note: Connect as required, when the output resistance 100 Ω of the DDCK1 pin shown above or the clock output affects the tuner characteristics.

Note: It doesn’t matter if a zener diode of 5.5 V or below is used as a substitute for the clamp circuit (VDET). Using the zener diode eliminates the need to use the VDET and doubler on/off control pins.

Note: When the clamp circuit is used, operation is stopped if the doubled voltatge exceeds the specified level. If the doubled voltage is supplied exceeding the specified voltage while the voltage of DC-DC converter for VT is supplied, the doubler function operates intermittently and may affect the tuner characteristics. To prevent this, it is recommended that doubler and low-pass filter load capacities that will not exceed the detection voltage be determined during tuner operation.

Note: The N-ch transistor buffer gate signal for the DDCK1 pin uses the V_{LCD} (3 V) power supply. This allows stable doubler operation, even if the V_{DD} power supply is reduced.

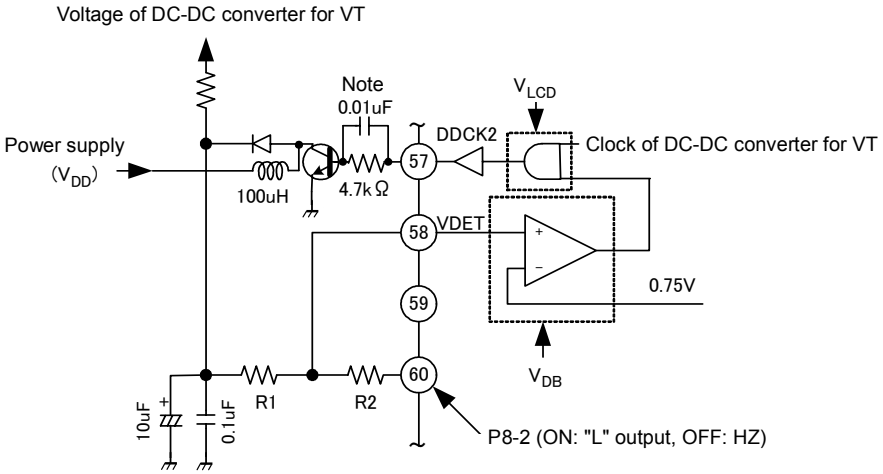
Note: When this product is used as shown above, design the tuner circuit to widen the variable range of the tuning voltage (VT).

Note: The filter circuit constants shown above are for reference only. Examine and design the actual circuits according to your desired characteristics.

(2) Example of using the DDCK2 external doubler transistor

The DDCK2 pin outputs the DC-DC converter clock in the CMOS type. The external transistor is used to increase the voltage like the DDCK1 pin. The doubled voltage can be set freely by using the external transistor. When the DDCK2 pin is used, set the POL bit to “1”.

Shown below is an example of a DC-DC converter circuit using the DDCK2 pin. Determine the R1/R2 resistance according to your desired doubled voltage. The P8-0 pin control is the same as for the DDCK1 pin.



Example of external DC-DC transistor doubler circuit

Note: Determine the doubler coil constant depending on the DC-DC converter clock frequency and the doubler current capacity.

Note: It doesn’t matter if a zener diode is used as a substitute for the clamp circuit (VDET). Using the zener diode eliminates the need to use the VDET and doubler on/off control pins (P8-2).

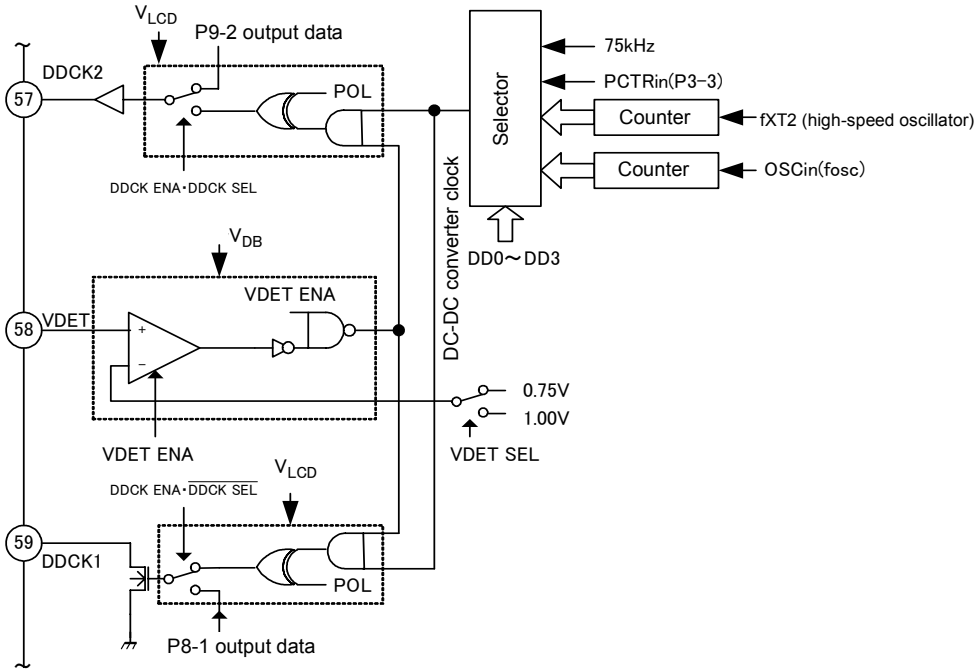
Note: Add the charge up capacitor for the base input of the external transistor when the doubler capacity is insufficient.

Note: When the doubler function is turned off by using pin P8-2, turn it off when the voltage of the DC-DC converter for VT has decreased sufficiently. A high voltage is applied to pin P8-2, and this may cause damage.

Note: The prebuffer power supply for the DDCK2 pin output uses a V_{LCD} (3 V) pin power supply, allowing stable doubler operation, even if the V_{DD} power supply is reduced. Note that the V_{DD} power supply level is outputted as the “H” level of the DDCK2 pin output.

Note: The filter circuit constants shown above are for reference only. Examine and design actual circuits according to your desired characteristics.

3. Configuration of DC-DC Converter for VT



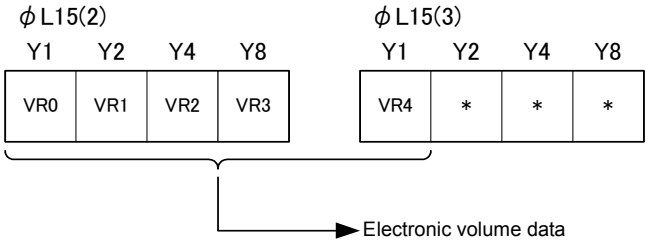
Note: Comparison voltage for the doubler detection voltage (VDET) is the divided voltage of the V_{EE} constant voltage (1.5 V) pin voltage.

○ Electronic Volume

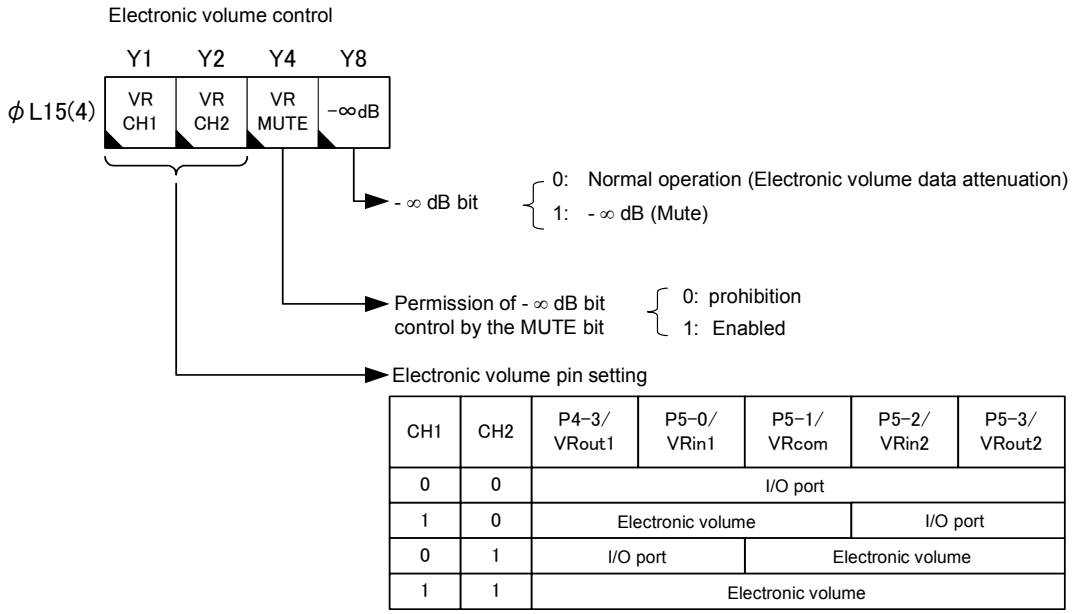
This product incorporates 2-channel 32-step (0 to −78 dB, −∞ dB) electronic volume. This allows digitization of volume control of headphone amplifier and reduction of parts.

The electronic volume pins are also used as I/O port 5 and I/O port pin P4-3. Channels can be switched between channels 1 and 2, which support monaural and stereo sound. The attenuation of the electronic volume is in –2 db steps within the range of –0 to –40 db and in –4 db steps in a range of –40 db to –78 db.

1. Electronic Volume Data Port and Control Port



STEP	−∞dB	VR4	VR3	VR2	VR1	VR0	Attenuation
1	1	*	*	*	*	*	−∞dB
	0	0	0	0	0	0	
2	0	0	0	0	0	1	−78dB
3	0	0	0	0	1	0	−74dB
4	0	0	0	0	1	1	−70dB
5	0	0	0	1	0	0	−66dB
6	0	0	0	1	0	1	−62dB
7	0	0	0	1	1	0	−58dB
8	0	0	0	1	1	1	−54dB
9	0	0	1	0	0	0	−50dB
10	0	0	1	0	0	1	−46dB
11	0	0	1	0	1	0	−42dB
12	0	0	1	0	1	1	−40dB
13	0	0	1	1	0	0	−38dB
14	0	0	1	1	0	1	−36dB
15	0	0	1	1	1	0	−34dB
16	0	0	1	1	1	1	−32dB
17	0	1	0	0	0	0	−30dB
18	0	1	0	0	0	1	−28dB
19	0	1	0	0	1	0	−26dB
20	0	1	0	0	1	1	−24dB
21	0	1	0	1	0	0	−22dB
22	0	1	0	1	0	1	−20dB
23	0	1	0	1	1	0	−18dB
24	0	1	0	1	1	1	−16dB
25	0	1	1	0	0	0	−14dB
26	0	1	1	0	0	1	−12dB
27	0	1	1	0	1	0	−10dB
28	0	1	1	0	1	1	−8dB
29	0	1	1	1	0	0	−6dB
30	0	1	1	1	0	1	−4dB
31	0	1	1	1	1	0	−2dB
32	0	1	1	1	1	1	−0dB



CH1	CH2	P4−3/ VRout1	P5−0/ VRin1	P5−1/ VRcom	P5−2/ VRin2	P5−3/ VRout2
0	0	I/O port				
1	0	Electronic volume			I/O port	
0	1	I/O port		Electronic volume		
1	1	Electronic volume				

The electronic volume pins are also used as port 5 and port P4-3 pins.

These pins are switched to electronic volume pins by using the VR CH1 and VR CH2 bits. Set this bit to “1” to use the pin as an electronic volume pin. The electronic volume has two channels. Channel 1 (VR CH1 bit) and Channel 2 (VR CH2 bit); corresponding to VRout1/VRin1 and VRout2/VRin2 pins respectively, and the channels are individually adjustable.

The electronic volume attenuation is set by the electronic volume data, which has 5 bits. Setting the most significant bit updates the lower 4 bits of the electronic volume data, meaning the most significant bit must be accessed; even if only the lower bits are changed.

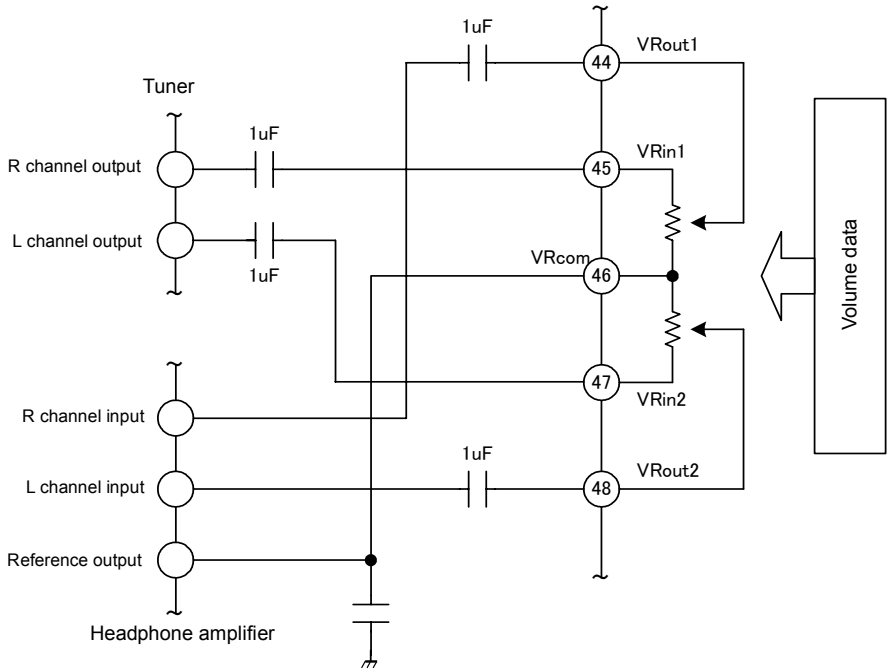
The volume can be muted only by setting the –∞dB bit. When this bit is set to –∞dB, the electronic volume data will be retained, and the previous attenuation recovered when –∞dB is released again. Note that the –∞dB state obtained by setting all the electronic volume data to “0” is the same operation as the state obtained by the –∞dB bit setting.

The electronic volume can also be set to –∞dB, depending on changes in the I/O port input. When there are changes in the inputs of the I/O port that has been enabled to break and the MUTE bit is set to “1”, the volume will be in muted (–∞dB) state. This is used for quick muting, for example, when band switching. This setting is enabled be setting the VR MUTE bit to “1”. This is set by the internal MUTE bit, it is also effective to set the MUTE/P9-1 pin as the I/O port. (→ Refer to the sections on MUTE output.)

The electronic volume control port is assigned to data port 5, and is accessed by using the OUT1 instruction with [CN = 4H] specified in the operand. The electronic volume control port is reset to “0” after a system reset.

2. Electronic Volume Configuration and Circuit Example

The electronic volume is configured by connecting the tuner and headphone amplifier as shown below.



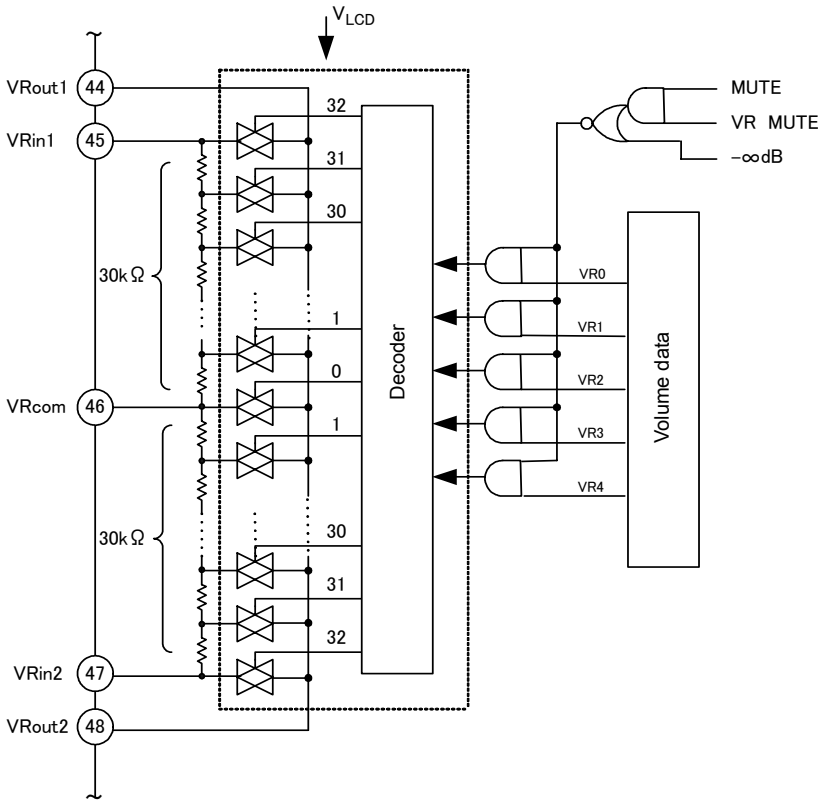
Example of electronic volume connection circuit

The electronic volume reference voltage (VRcom) is usually connected to the reference output pin of the headphone amplifier. When the reference output pin is not available, connect this potential to the GND level or the V_{EE} pin (1.5 V constant voltage). If the reference voltage (VRcom) is connected to GND, the distortion factor becomes 0.1% or below when the input level (VRin) is 0.2 Vp-p or below. Caution must be taken as the distortion will be worse when this input level is exceeded.

Note: The circuit shown above is for reference only. Examine and design actual circuits according to your desired characteristics.

3. Electronic Volume Configuration

The electronic volume is composed of a decoder, analog switches and resistors and the control circuit. The decoder, analog switches and resistors are powered by the V_{LCD} pin (3 V) power supply, which allows stable operation, even if the V_{DD} pin power supply fluctuates.



Note: The analog circuit in the electronic volume circuit is powered by the V_{LCD} pin (3 V) power supply. Therefore, up to 3 V can be inputted to VRin1/2. The logic section is powered by the V_{CPU} pin power supply.

Note: Volume switching by the zero cross detection is unavailable, hence noise may occur when the attenuation is switched.

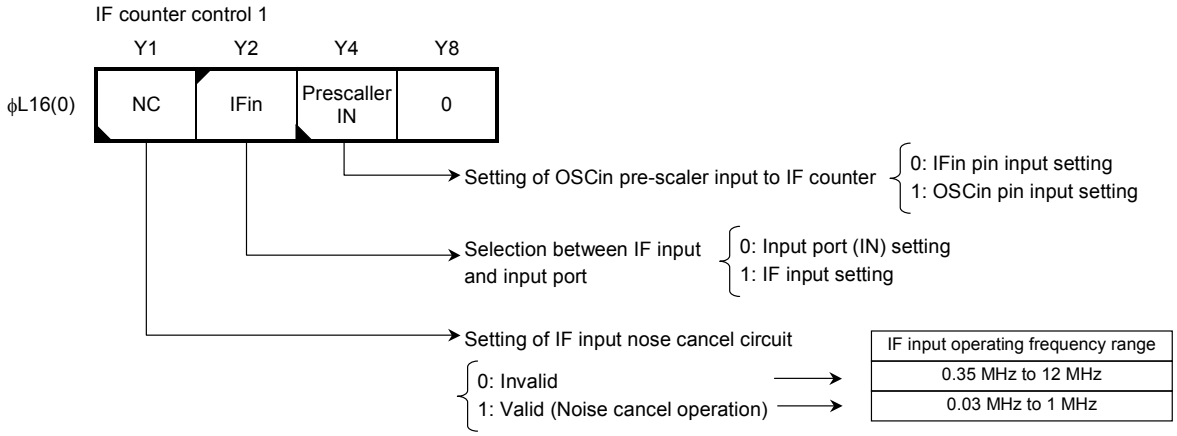
Note: The VRin1/2 input total resistance is 30 kΩ (typ.).

Note: The electronic volume distortion factor is 0.05% at the typical and 0.1% at the maximum (with VRin = 0.4 Vp-p input).

○ IF Counter

This is a 20-bit general-purpose counter that counts the intermediate frequency (IF) of FM or AM during auto tuning and can be used to detect auto stop signals. It can also measure the VCO of the analog tuner and detect the received frequency.

4. IF Counter Control Ports and Data Ports



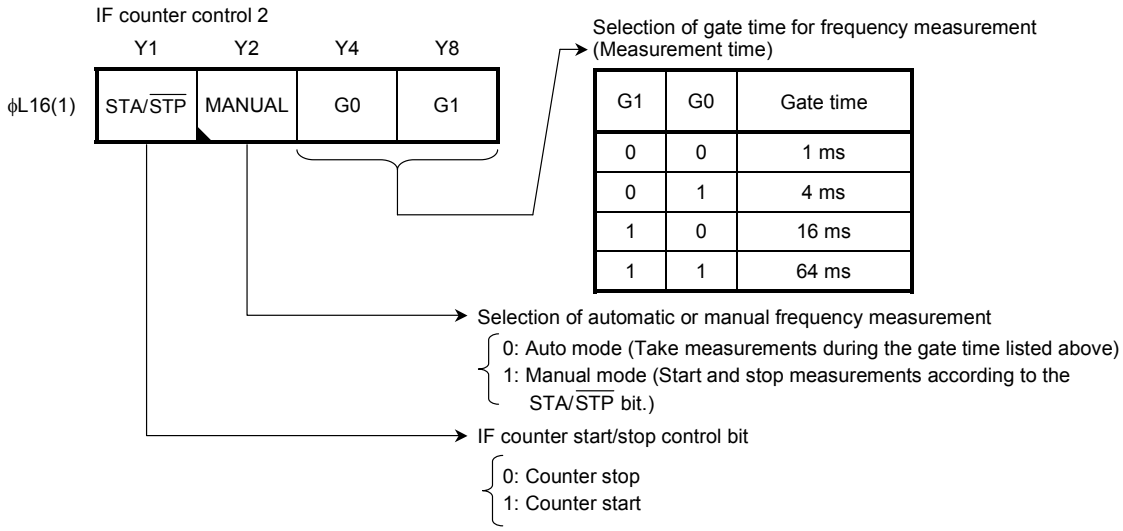
Note: When the input port setting is selected, frequency detection can be carried out by CMOS input to the IF counter.

Note: When the IF input setting is selected, the IF input amplifier turns off when in the PLL off mode. To use the IF counter in the PLL off mode, select the input port setting (CMOS input).

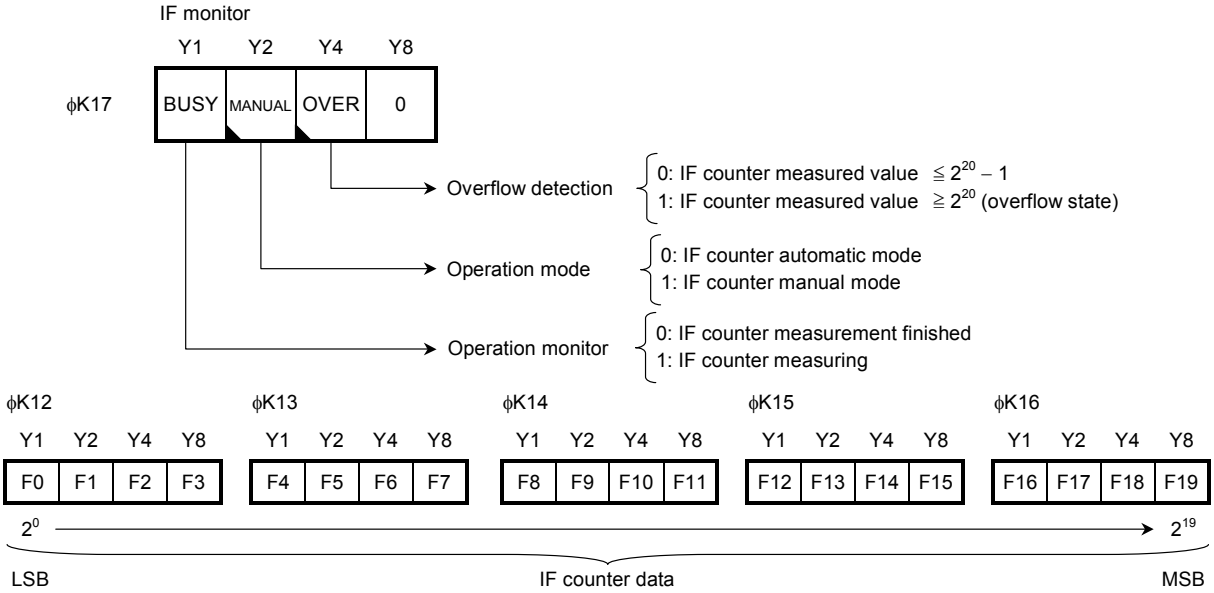
Note: When the counter input is set to the prescaler input, the 1/15･16 prescaler is fixed to 16 frequency divisions in the pulse swallow method and this frequency is inputted to the IF counter.

Note: For the input frequency range when the prescaler input setting is selected, refer to the section on Programmable counter.

Note: Set the Y8 bit of the IF control 1 port (ϕL16 (0)) to “0”.



Note: In the PLL amplifier setting register, the TA0 and TA1 bits are used for setting the OSCin input amplifier, and the TA2 and TA3 bits are used for setting the IFin input amplifier.



The IF counter calculates the IF signals usually from the tuner and detects the auto stop signal. When the IFin bit is set to "1", the IFin input amplifier will operate and the IF counter will be enabled. The gain of the input amplifier can be changed by the amplifier setting register port (ϕL16 (F), ϕK11 (F)). Set this register to all "1". In the PLL off mode, this amplifier is disabled and the IFin input becomes high impedance.

The IF input frequency range varies depending on the NC bit. When the NC bit is set to "1", the internal noise cancel circuit operates. When the NC bit is "0", the frequency range is 0.35 to 12 MHz. When the NC bit is "1", the noise cancel circuit operates and the frequency range is 0.03 to 1 MHz. Set this bit depending on the IF frequency to be detected.

The IF counter has two counting methods; namely the automatic and manual IF counter modes respectively. Counting is carried out using the following methods:

(1) Automatic IF counter mode

To select the automatic mode for the IF counter, set the MANUAL bit to "0", and specify the gate time depending on the frequency band to be measured. When the STA/$\overline{\text{STP}}$ bit is set to "1", the IF counter will start operation, the clock will be inputted during the specified gate time, the number of these input pulses will be counted, and the counter will stop the operation. Whether or not the IF counter has finished counting can be checked by referring to the BUSY bit. The OVER bit becomes "1" when there is a pulse input a measured value of 2^{20} or over.

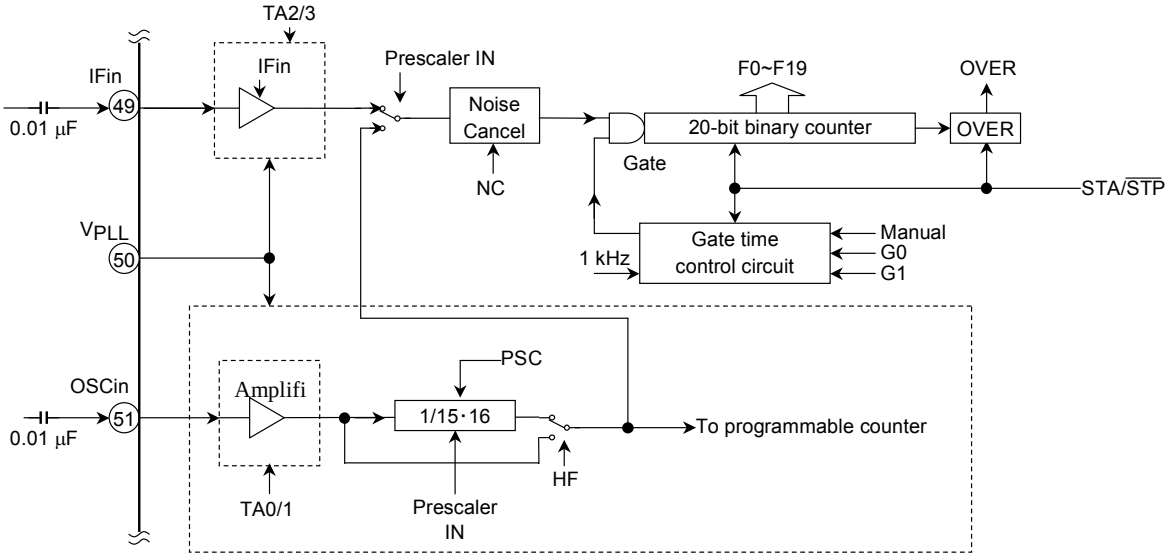
The frequency being inputted can be measured by checking that the BUSY and OVER bits are set to"0" and loading the IF data of F0 to F19.

(2) Manual IF counter mode

Use this mode when the frequency is measured by controlling the gate time using the internal time base (for example, 10 Hz). Set the MANUAL bit to "1" to activate the manual mode. At this time, the gate time setting reverts to "don't care" state. Counting starts by setting the STA/$\overline{\text{STP}}$ bit to "1". By setting the STA/$\overline{\text{STP}}$ bit to "0", counting is finished and the data is loaded in binary format.

5. IF Counter Configuration

The IF counter is composed of an input amplifier, a gate time control circuit and a 20-bit binary counter. The OSCin prescaler clock can be inputted as the IF counter input.

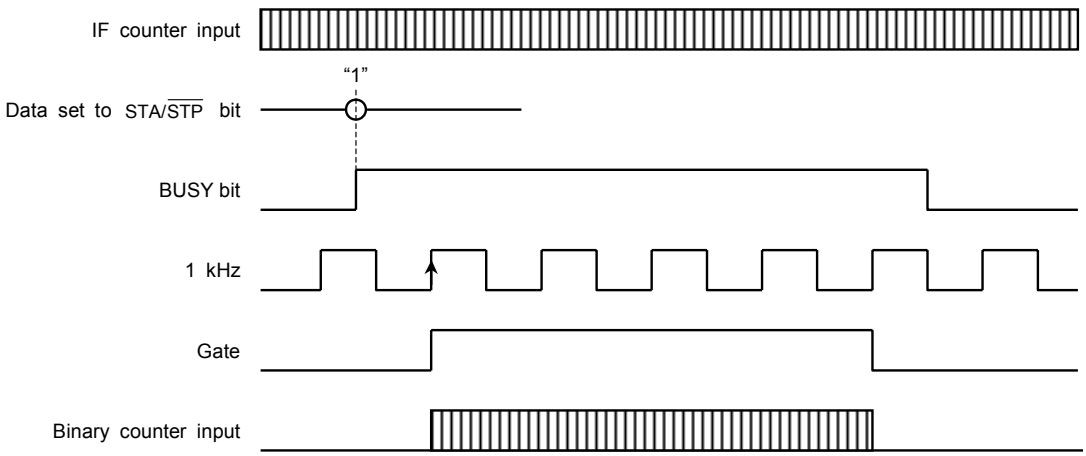


Note: All the binary counters of the IF counter operate at the rising edge.

Note: When the OSCin prescaler clock is counted by the IF counter, 1/15・16 is fixed to the 1/16 frequency division by setting the PLL mode to HF mode. The clock is directly inputted when in LF mode.

Note: The IF counter input amplifier, the OSCin input amplifier and the programmable counter are powered by the V_{PLL} pin power supply. This power supply level can be supplied regardless of the V_{DD}/V_{CPU} pin power supply level. In PLL off mode, the V_{PLL} pin power supply can be turned off. The IF counter control register and the IF counter power supply use the V_{CPU} pin power supply. Therefore, the contents of the register will be retained after the V_{PLL} pin power supply is turned off.

Note: The IFin pin has a built-in amplifier that allows small-amplitude operation by linking to the capacitor. In PLL off mode, the IFin input becomes high impedance.

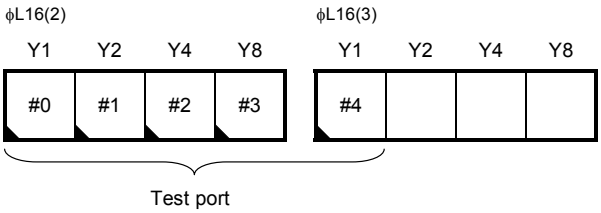


Example of operation timing in automatic IF counter mode

Note: The IF counter ues the 1 kHz clock. There is a delay of up to 1 ms from the time when the start instruction is executed to the time when the gate opens.

○ Test Port

This is the internal port used to test the device functions. These ports are assigned to data port 7 and can be accessed by using the OUT1 instruction with [CN = 6H] specified in the operand. Set all to “0” in the normal program.



Setting the following data to test ports #3 to #0 enables various signals to be output from the MUTE pin.

#3	#2	#1	#0	Data	MUTE pin output
0	0	0	0	0	MUTE output
0	0	0	1	1	Programmable counter frequency
0	0	1	0	2	Reference frequency
0	0	1	1	3	2 Hz
0	1	0	0	4	Prohibition
~	~	~	~	~	
1	1	1	1	F	

Note: The MUTE pin is also used for pin P9-1. This pin must be set as the MUTE pin when you need signals to be output from the MUTE pin.

○ Application to Emulator Chip

When the $\overline{\text{RESET}}$ pin is at the “L” level and pulses are inputted to the TEST pin, various kinds of test modes will be activated and the device will operate as an emulator chip. Three types of test modes are available, and the software development tool can be configured by using three devices.

You can confirm the radio operation while developing software by connecting this software development tool to the tuner IC.

Absolute Maximum Rating (Ta = 25°C)

Characteristics	Symbol	Rating	Unit
Supply voltage (Note 1)	V_{DD}	−0.3 ~ 4.0	V
Output withstand voltage 1 (Note 2)	V_{O1} (*)	−0.3 ~ V_{DB} + 0.3	V
Output withstand voltage 2 (Note 2)	V_{O2} (*)	−0.3 ~ 6.0	V
Input voltage 1 (Note3)	V_{IN1} (*)	−0.3 ~ V_{LCD} + 0.3	V
Input voltage 2 (Note3)	V_{IN2} (*)	−0.3 ~ V_{CPU} + 0.3	V
Input voltage 3 (Note3)	V_{IN3} (*)	−0.3 ~ 6.0	V
Input voltage 4 (Note3)	V_{IN4} (*)	−0.3 ~ V_{PLL} + 0.3	V
Input voltage 5 (Note3)	V_{IN5} (*)	−0.3 ~ V_{DD} + 0.3	V
Input voltage 6 (Note3)	V_{IN6} (*)	−0.3 ~ V_{DB} + 0.3	V
Power dissipation	P_D	100	mW
Operating temperature	T_{opr}	−10 ~ 60	°C
Storage temperature	T_{stg}	−65 ~ 150	°C

Note 1: The supply voltage (V_{DD}) indicates the maximum rating of five pins, V_{DD}, V_{CPU}, V_{DB}, V_{PLL} and V_{LCD}.
The relationship of the potentials is as follows: $V_{DD} \leq V_{LCD}$, $V_{DD} \leq V_{DB}$, $V_{DD} \leq V_{CPU}$, $V_{CPU} \leq V_{LCD}$

Note 2: Each output voltage corresponds to the following pin:
V_{O1}: I/O port 6 pin, V_{O2}: D_{DCK1}, Tout, I/O port 8 pin

Note 3: Each input voltage corresponds to the following pin:
V_{IN1}: All I/O port pins except for those listed below
V_{IN2}: $\overline{RESET}$ pin
V_{IN3}: I/O port 8 pin, P9-0 pin
V_{IN4}: OSC_{in} and IF_{in} pins
V_{IN5}: $X_{in}1$ pin
V_{IN6}: I/O port 6 and T_{in} pins

Electrical Characteristics (Unless otherwise specified, Ta = 25°C, V_{DD} = V_{PLL} = 1.5 V, VDB = V_{CPU} =3.0 V)

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Operating supply voltage range (Note 1)	V_{DD}	—	(V_{DD}) (*)	0.9	~	1.8	V
	V_{CPU}	—	(V_{CPU}) (*)	1.2	~	3.6	
	V_{PLL}	—	(V_{PLL}) PLL operation (*)	0.9	~	1.8	
Memory retention voltage range	V_{HD}	—	(V_{CPU}) Backup mode (*)	0.75	~	3.6	
Operating supply current (Note 2)	I_{DD1}	—	PLL operation, OSCin = 30 MHz	—	1.0	1.5	mA
	I_{DD2}	—	During operation of CPU only (PLL off and LCD driver operating)	—	150	300	μA
	I_{DD3}	—	In the hard wait mode (Crystal oscillation only)	—	120	—	
	I_{DD4}	—	In the soft wait mode (CPU intermittent operation only)	—	140	—	
Memory retention current	I_{HD1}	—	(V_{DD}, V_{PLL}) When the CKSTP instruction is executed	—	0.1	10	
	I_{HD2}	—	(V_{CPU}) V_{CPU} = 1.2 ~ 3.6 V, When the CKSTP instruction is executed (Power supply detectin is set to OFF), V_{DD} off (Power supply detectin is set to ON)	—	0.01	0.5	

Note 1: Use supply voltage in the range of $V_{DD} \leq V_{LCD}$, $V_{DD} \leq V_{DB}$, $V_{DD} \leq V_{CPU}$ and $V_{CPU} \leq V_{LCD}$.

Note 2: The operating supply current is the total current of the V_{DD}, V_{CPU} and V_{PLL} pin power supplies.

Crystal Oscillator (X_{in1}, X_{out1})

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Crystal oscillation frequency	f_{XT1}	—	(X_{in1}, X_{out1}) (*)	—	75	—	kHz
Crystal oscillation start time	t_{st1}	—	(X_{in1}, X_{out1}) f_{XT1} = 75 kHz	—	—	1.0	s
Xin1 amplifier feedback resistance	R_{fXT1}	—	(X_{in1} - X_{out1})	—	20	—	MΩ
Xout1 output resistance	R_{OUT1}	—	(X_{out1})	50	100	200	kΩ

High-speed Oscillator (X_{in2}, X_{out2})

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
High-speed oscillation frequency range	f_{XT2}	—	(X_{in2}, X_{out2}) (*)	300	—	600	kHz
High-speed oscillation start time	t_{st2}	—	(X_{in2}, $Xout_2$) f_{XT2} = 300 ~ 600 kHz	—	—	100	ms
Xin2 amplifier feedback resistance	R_{fXT2}	—	(X_{in2} - X_{out2})	—	1	—	MΩ
Xout2 output resistance	R_{OUT2}	—	(X_{out2})	1	2	4	kΩ
Oscillation operating current (Note 3)	I_{XT2}	—	(X_{in2} - X_{out2})	—	50	—	μA

Note 3: This value increases when high-speed oscillator is used.

*: Guaranteed when V_{DD} = V_{PLL} = 0.9 - 1.8 V, V_{CPU} = 1.2 - 3.6 V, and Ta = –10 to 60°C.

Constant Voltage Output (V_{EE}), Voltage Doubled Output (V_{LCD})

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Doubled output	V_{DB1}	—	(V_{DB}) GND reference Clamp off, Charge pump voltage	—	$V_{DD} \times 2$	—	V
	V_{DB2}	—	(V_{DB}) GND reference Clamp voltage = 2.0 V setting	—	2.0	—	
	V_{DB3}		(V_{DB}) GND reference Clamp voltage = 2.5 V setting	—	2.5	—	
	V_{DB4}		(V_{DB}) GND reference Clamp voltage = 3.0 V setting	—	3.0	—	
	V_{LCD}		(V_{LCD}) GND reference	—	$V_{EE} \times 2$	—	
Clamp doubled voltage setting error	ΔV_{DB}		(V_{DB}) When the charge pump pressure is increased V_{EE} = 1.5 V	—	—	0.05	V
			(V_{DB}) When the switching regulator pressure is increased V_{EE} = 1.5 V	—	—	±0.05	
Constant voltage	V_{EE}	—	(V_{EE}) GND reference (*)	1.46	1.50	1.54	V

Programmable Counter, IF Counter Operating Frequency Range

Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Operating frequency range	HF mode	f HF	—	(OSCin) V_{IN} = 0.1 ~ 0.6 V_{p-p} (*)	1.0	~	30	MHz
	LF mode	f LF	—	(OSCin) V_{IN} = 0.1 ~ 0.6 V_{p-p} (*)	0.5	~	4	
	IFin1	f IF1	—	(IFin) V_{IN} = 0.1 ~ 0.6 V_{p-p} (*) NC = 0 setting	0.35	~	12	
	IFin2	f IF2	—	(IFin) V_{IN} = 0.1 ~ 0.6 V_{p-p} (*) NC = 1 setting	0.03	~	1	
Input amplitude range	HF mode	V_{HF}	—	(OSCin) f_{IN} = 1.0 ~ 30 MHz (*)	0.1	~	0.6	V_{p-p}
	LF mode	V_{LF}	—	(OSCin) f_{IN} = 0.5 ~ 4 MHz (*)	0.1	~	0.6	
	IFin1	V_{IF1}	—	(IFin) f_{IN} = 0.35 ~ 12 MHz (*) NC = 0 setting	0.1	~	0.6	
	IFin2	V_{IF2}	—	(IFin) f_{IN} = 0.03 ~ 1 MHz (*) NC = 1 setting	0.1	~	0.6	
Input amplifier feedback resistance		Rf_{IN1}	—	(OSCin)	250	500	1000	kΩ
		Rf_{IN2}	—	(IFin)	250	500	1000	kΩ

*: Guaranteed when V_{DD} = V_{PLL} = 0.9 - 1.8 V, V_{CPU} = 1.2 - 3.6 V, and Ta = –10 to 60°C.

I/O Ports 1 to 6 (P1-0 to P16-3) , Serial Interface (SCK1/2, RX1/2, SDIO1/2, TX1/2) (Note 4)

Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Output current	"H" level	I_{OH1}	—	V_{DD} = 0.9 V, V_{LCD} = 3.0 V, V_{OH} = V_{DD} − 0.2 V (except for I/O ports 6,8 and P9-0)	−0.4	−0.8	—	mA
		I_{OH1L}	—	V_{DD} = 0.9 V, V_{LCD} = 3.0 V, V_{OH} = V_{DD} − 0.2 V (except for I/O ports 6,8 and P9-0)	—	−0.5	—	
	"L" level	I_{OL1}	—	V_{DD} = 0.9 ~ 1.8 V, V_{LCD} = 3.0 V, V_{OL} = 0.2 V (except for I/O port 8 and P9-0)	0.4	0.8	—	
		I_{OL2}	—	V_{DD} = 0.9 ~ 1.8 V, V_{LCD} = 3.0 V, V_{OL} = 0.2 V (P8-0 to P8-3)	2	4	—	
		I_{OL3}	—	V_{DD} = 0.9 ~ 1.8 V, V_{LCD} = 3.0 V, V_{OL} = 0.2 V (P9-0)	—	20	—	
Input leak current		I_{LI}	—	V_{IH} = V_{DD}, V_{IL} = 0 V (except for I/O ports 6,8 and P9-0)	—	—	±1.0	μA
			—	V_{IH} = V_{DB}, V_{IL} = 0 V (P6-0 to P6-3)				
			—	V_{IH} = 5.5 V, V_{IL} = 0 V (P8-0 to P8-3, P9-0)				
Input voltage	"H" level	V_{IH}	—	(except for I/O ports 6,8 and P9-0)	V_{DD} × 0.8	~	V_{LCD}	V
			—	(P6-0 to P6-3)	V_{DD} × 0.8	~	V_{DB}	
			—	(P8-0 to P8-3, P9-0)	V_{DD} × 0.8	~	5.5	
	"L" level	V_{IL}	—	—	0	~	V_{DD} × 0.2	
Input pull-up/pull-down resistance		R_{IN1}	—	When P3-0 to P3-3 are set to pull-down or pull-up	25	50	100	kΩ
Input pull-down resistance		R_{IN2}	—	(TEST) when $\overline{RESET}$ = "L"	—	10	—	kΩ
SCK input frequency		f_{SIO}	—	When SCK1/SCK2 are set to serial clock input	—	—	200	kHz

Note 4: The electrical characteristics in serial interface conditions are the same as for the I/O ports.

LCD Driver Output (COM1 to COM4 , S1 to S18)

Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Output current	"H" level	I_{OH4}	—	V_{LCD} = 3.0 V, V_{OH} = V_{LCD} − 0.2 V	—	−0.2	—	mA
	"L" level	I_{OL4}	—	V_{LCD} = 3.0 V, V_{OL} = 0.2 V	—	0.5	—	
Bias voltage	1/3 V_{LCD} level	V_{BS2}	—	V_{LCD} = 3 V, no load, when the 1/3 bias type selected	0.85	1.00	1.15	V
	1/2 V_{LCD} level	V_{BS3}	—	V_{LCD} = 3 V, V_{EE} = 1.5 V, no load, when the 1/2 bias selected	1.35	1.5	1.65	
	2/3 V_{LCD} level	V_{BS4}	—	V_{LCD} = 3 V, no load, when the 1/3 bias selected	1.85	2.00	2.15	
LCD driver operating current (Note 5)		I_{LCD2}	—	No load, when the 1/2 bias selected	—	5	—	μA
		I_{LCD3}	—	No load, when the 1/3 bias selected	—	100	—	

Note 5: This value increases when the LCD driver circuit is used.

Electronic Volume (VRout1, VRin1, VRcom, VRin2, VRout2)

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Volume resistance	R_{VR}	—	IN ~ GND resistor	15	30	60	kΩ
Analog switch ON resistance	R_{ON}	—	Analog switch on resistor	—	500	800	Ω
Attenuation error	ΔATT	—	—	—	0	±2.0	dB

A/D Converter (ADin1 to ADin4)

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Analog input voltage range	V_{AD}	—	(ADin1 ~ ADin4)	0	~	V_{DB}	V
Resolution	V_{RES}	—	—	—	6	—	bit
Total conversion error	—	—	—	—	±0.5	±1.0	LSB
Analog input leak	I_{LI}	—	$V_{IH} = V_{DB}$, $V_{IL} = 0$ V (ADin1 to ADin4)	—	—	±1.0	μA

Phase Comparator (DO1/OT1/P, DO2/OT2/N)

Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Output current	"H" level	I_{OH5}	—	$V_{DB} = 3.0$ V, $V_{OH} = V_{DB} - 0.2$ V when the output resistance is off	−0.4	−0.8	—	mA
	"L" level	I_{OL5}	—	$V_{DB} = 3.0$ V, $V_{OL} = 0.2$ V when the output resistance is off	0.4	0.8	—	
Output resistance		R_{OUT1}	—	(DO1, DO2)	—	5	—	kΩ
		R_{OUT2}	—	(DO1, DO2)	—	50	—	
		R_{OUT3}	—	(DO1, DO2)	—	100	—	
Tristate leak current		I_{TL}	—	(DO1, DO2) $V_{DB} = 3.0$ V, $V_{TLH} = 3.0$ V, $V_{TLL} = 0$ V	—	—	±100	nA

DC-DC Converter Voltage Doubler for VT (VDET, DDCK1, DDCK2)

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Doubled voltage range	V_{OUT}	—	—	0	~	5.5	V
Doubled voltage detection setting error	ΔV_{DET}	—	(V_{DET}) V_{EE} = 1.5 V	—	—	±0.05	V
Detection operating current (Note 6)	I_{DET}	—	(V_{DET})	—	10	—	μA
"H" level output current	I_{OH1}	—	(DDCK2) V_{OL} = 0.2 V when DDCK2 is selected	–0.4	–0.8	—	mA
"L" level output current	I_{OL1}	—	(DDCK2) V_{OL} = 0.2 V, when DDCK1 is selected	0.4	0.8	—	
	I_{OL2}	—	(DDCK1) V_{OL} = 0.2 V, when DDCK1 is selected	2	4	—	
Output off leak current	I_{OFF}	—	(DDCK1) V_{IH} = 5.5 V, when DDCK1 is selected	—	—	±1.0	μA

Note 6: This value increases when the tdoubled voltage detection circuit is used.

Transistor for Low-pass Filter (Tout, Tin)

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
"L" level output current	I_{OL3}	—	(Tout) V_{OL} = 0.2 V, Tin = 1.5 V		20	—	mA
Output off leak current	I_{OFF}	—	(Tout) V_{OH} = 5.5 V, Tin = 0 V	—	—	±1.0	μA
Input leak current	I_{LI}	—	(Tin) V_{OB} = V_{IH} = 3.6 V V_{IL} = 0 V	—	—	±1.0	μA

Reset Signal Input ($\overline{RESET}$)

Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Input leak current		I_{LI}	—	V_{IH} = V_{CPU}, V_{IL} = 0 V	—	—	±1.0	μA
Input voltage	"H" level	V_{IH}	—	—	V_{CPU} × 0.8	~	V_{CPU}	V
	"L" level	V_{IL}	—	—	0	~	V_{CPU} × 0.2	

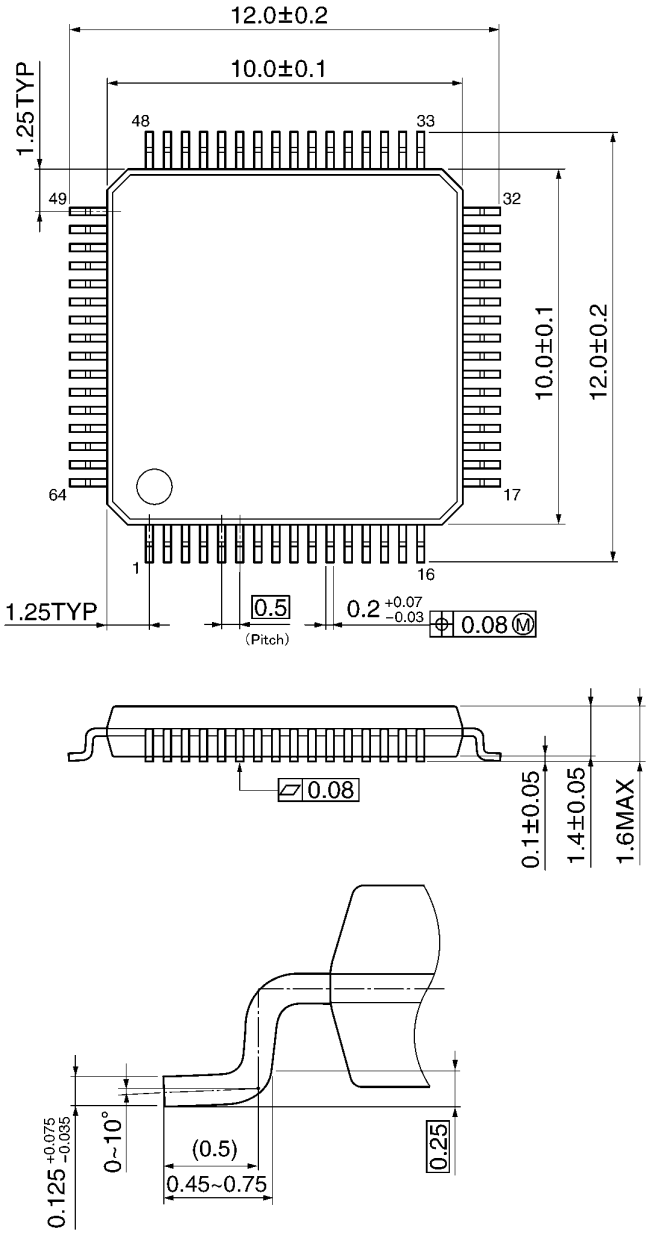
Reduced Voltage Detection Circuit

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Reduced voltage detection setting error	ΔV_{BL}	—	(V_{DD}) V_{EE} = 1.5 V	—	—	±0.03	V
Reduced voltage detection operating current (Note 7)	I_{LI}	—	—	—	20	—	μA

Note 7: This value increases when the detection circuit is used.

Package Dimensions

P-LQFP64-1010-0.50E Unit: mm



Note: Pd-plated leads.

Weight: 0.32 g (standard)

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