TDA2510

CHROMINANCE COMBINATION

FAIRCHILD LINEAR INTEGRATED CIRCUITS

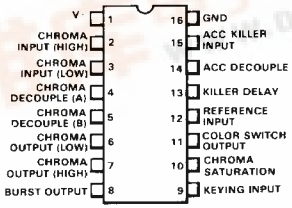
GENERAL DESCRIPTION – The TDA2510 is a monolithic integrated circuit designed for the chrominance function of a color television receiver. It is designed to interface directly with the TDA2521, using a minimum number of external components. The TDA2510 is constructed on a single silicon chip using the Fairchild Planar* epitaxial process.

- **CHROMA AMPLIFIER WITH ACC**
- **CONTROL VOLTAGE AMPLIFIER**
- **BURST SEPARATOR**
- **COLOR KILLER AND COLOR KILLER VOLTAGE DETECTOR**
- **LINEAR ELECTRONIC POTENTIOMETER FOR SATURATION CONTROL**
- **SCHMITT TRIGGER FOR COLOR KILLER**
- **CHROMA DELAY LINE DRIVER STAGE**
- **COLOR BURST OUTPUT STAGE**

ABSOLUTE MAXIMUM RATINGS

Supply voltage	15 V
Collector voltage of chroma output transistor (pin 7) (P_D = 100 mW max)	20 V
Collector current of chroma output transistor (pin 7)	20 mA
Collector current of color killer output transistor (pin 11)	10 mA
Power dissipation	500 mW
Operating temperature range	−25°C to +60°C
Storage temperature range	−55°C to +125°C
Pin Temperature (Soldering 10 s)	260°C

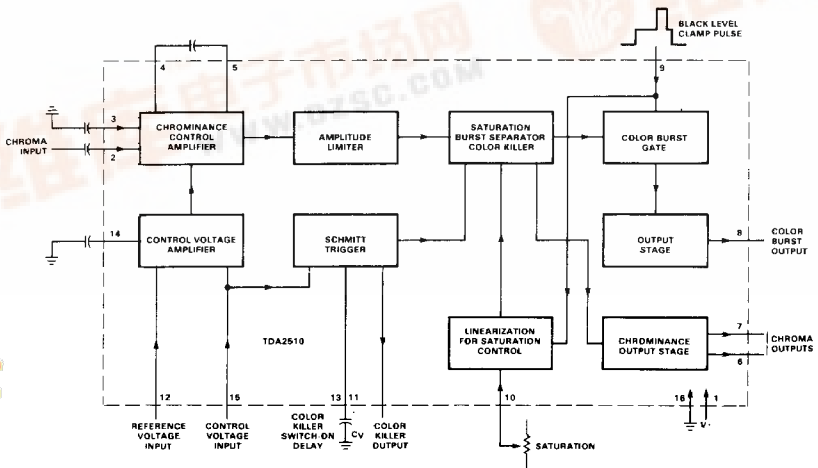
CONNECTION DIAGRAM
16-PIN DIP
(TOP VIEW)
PACKAGE OUTLINE 9B

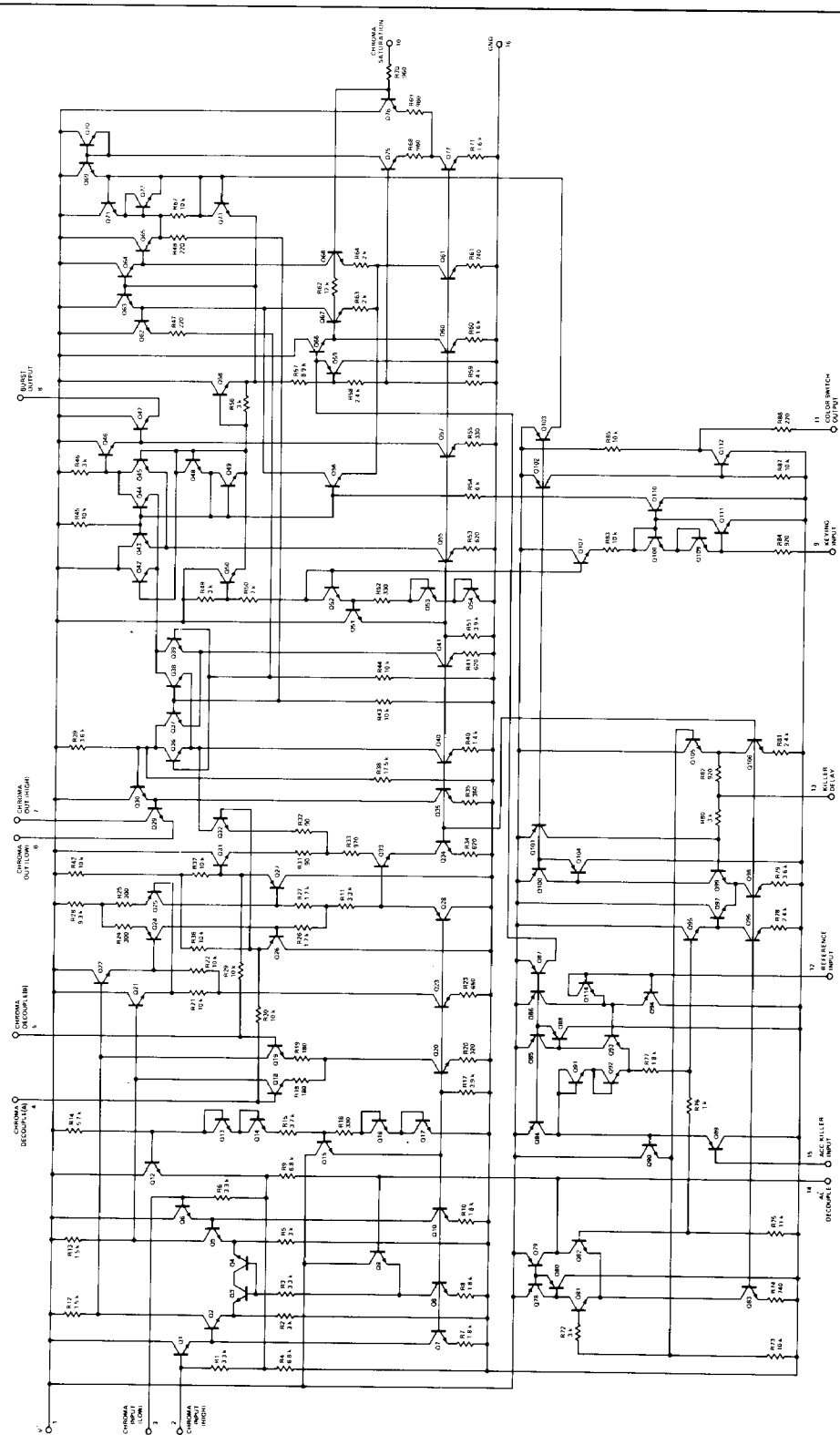


ORDER INFORMATION

TYPE	PART NO.
2510	TDA2510

BLOCK DIAGRAM



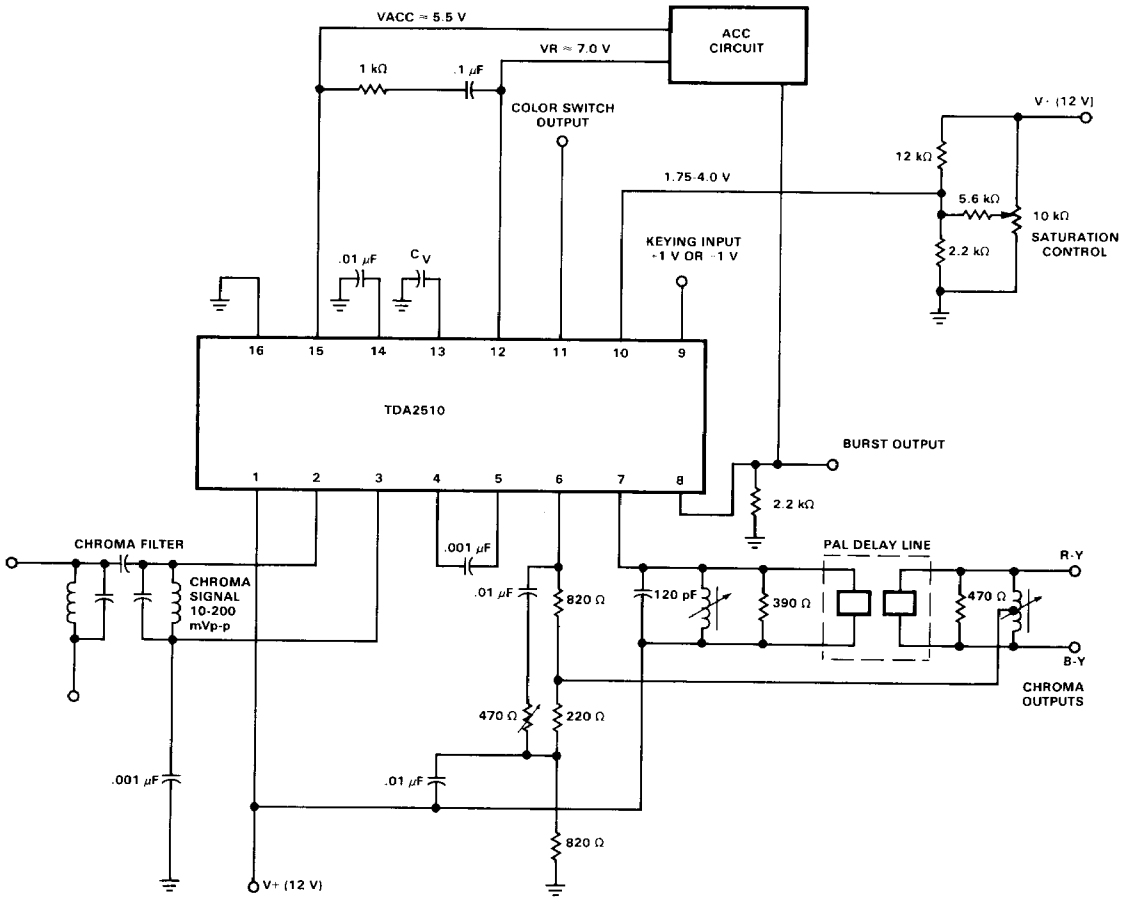


ELECTRICAL CHARACTERISTICS: T_A = 25°C, V+ = 12 V, see test circuit unless otherwise specified.

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Chroma Input (pin 2)					
V_{IN} (Symmetrical or Asymmetrical) Color bars (V_2 p-p)			100		mVp-p
Input Voltage Range (V_2 p-p)	Note 1	−20		+6.0	dB
Input Impedance (Z_2)		2.0			kΩ
Burst Output (Emitter Follower) (pin 8)					
DC Voltage at Burst Output (V_8)			9.0		V
Burst Output (V_8 p-p)	Note 1		0.5		Vp-p
Burst Output Limiting Level			1.5		Vp-p
Chroma Output (without Burst) (pin 6)					
DC Voltage at Chroma Output (V_6)			7.0		V
Chroma Output (Color Bars) at nominal Saturation and Maximum contrast (V_6 p-p)	Note 2		0.5		Vp-p
Signal Plus Noise to Noise Ratio	Note 3	50			dB
Saturation Control Range		−50		+6.0	dB
Phase Angle compared to Burst Output at Nominal Saturation		−5.0		5.0	degrees
Phase angle Shift during Saturation Control Range +6 to −10 dB		−5.0		5.0	degrees
Inputs for Control Voltage and Color Killer (pin 12, 15)	V_{REF} =				
Control Voltage (V_{15})	V_{12} = 7 V		5.5		V
Input Voltage (Color On) V_{15}	V_{12} = 7 V			5.7	V
Input Voltage (Color Off) V_{15}	V_{12} = 7 V	6.0			V
Signal Suppression (Color Off)	V_{12} = 7 V	50			dB
Control Input Impedance (Z_{15})		500			kΩ
Saturation Control Input (pin 10)					
Voltage Range for Linear Control (V_{10})		1.75		4.0	V
Threshold Voltage for > 50 dB suppression	Note 4	1.6	1.75		V
Input Impedance (Z_{10})			10		kΩ
Color Kill Switch Output (pin 11)					
Output Voltage (Color On) V_{11}			V+		V
Output Voltage (Color Off) V_{11}				0.5	V
Internal Resistance			10		kΩ
Burst Gating and Blanking Pulse (pin 9)					
Burst Gating and Blanking Pulse (positive or negative) (± V_9)		±1.0		±4.0	V
Input Impedance (Z_9)			1.0		kΩ
Color Killer Delay (pin 13)					
Delay Time as a Function of C_V			24		ms/μF

NOTES:
1. Burst output kept constant by ACC circuit at approximately 0.5 Vpp.
2. Nominal saturation is defined as maximum saturation − 6 dB, chroma/burst input ratio is approximately 2.
3. Signal plus noise to noise is calculated as V_{IN} (p-p)/6 (V_{noise} (rms)) for a standard color bar signal.
4. Saturation increases with increasing V_{10}.

APPLICATIONS AND TEST CIRCUIT



4