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INTEGRATED CIRCUITS

DATA SHEET

TDA4864J; TDA4864AJ
Vertical deflection booster

Product specification 2003 Oct 31

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FEATURES

- Power amplifier with differential inputs
- Output current up to 2.5 A (p-p)
- High vertical deflection frequency up to 200 Hz
- High linear sawtooth signal amplification
- Flyback generator:
  - TDA4864J: separate adjustable flyback supply voltage up to 60 V
  - TDA4864AJ: internally doubled supply voltage (two supply voltages only for DC-coupled outputs).

GENERAL DESCRIPTION

The TDA4864J and TDA4864AJ are deflection boosters for use in vertical deflection systems for frame frequencies up to 200 Hz.

The TDA4864J needs a separate flyback supply voltage, so the supply voltages are independently adjustable to optimize power consumption and flyback time.

For the TDA4864AJ the flyback supply voltage will be generated internally by doubling the supply voltage and therefore a separate flyback supply voltage is not needed.

Both circuits provide differential input stages.

QUICK REFERENCE DATA

Measurements referenced to pin GND.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{P1}	supply voltage 1		9	–	30	V
V_{P2}	supply voltage 2 for vertical output		V_{P1} – 1	–	60	V
V_{FB}	flyback supply voltage of TDA4864J		V_{P1} – 1	–	60	V
V_{P3}	flyback generator output voltage of TDA4864AJ	$I_{V\text{-}OUT}$ = –1.25 A	0	–	V_{P1} + 2.2	V
V_i	input voltage on					
	pin INN		1.6	–	V_{P1} – 0.5	V
	pin INP		1.6	–	V_{P1} – 0.5	V
I_{P1}	supply current 1	during scan	–	6	10	mA
I_{P2}	quiescent supply current 2	$I_{V\text{-}OUT}$ = 0	–	25	60	mA
$I_{V\text{-}OUT(p\text{-}p)}$	vertical deflection output current (peak-to-peak value)		–	–	2.5	A
T_{amb}	ambient temperature		–20	–	+75	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA4864J	DBS7P	plastic DIL-bent-SIL power package; 7 leads (lead length 12/11 mm); exposed die pad	SOT524-1
TDA4864AJ			

BLOCK DIAGRAM

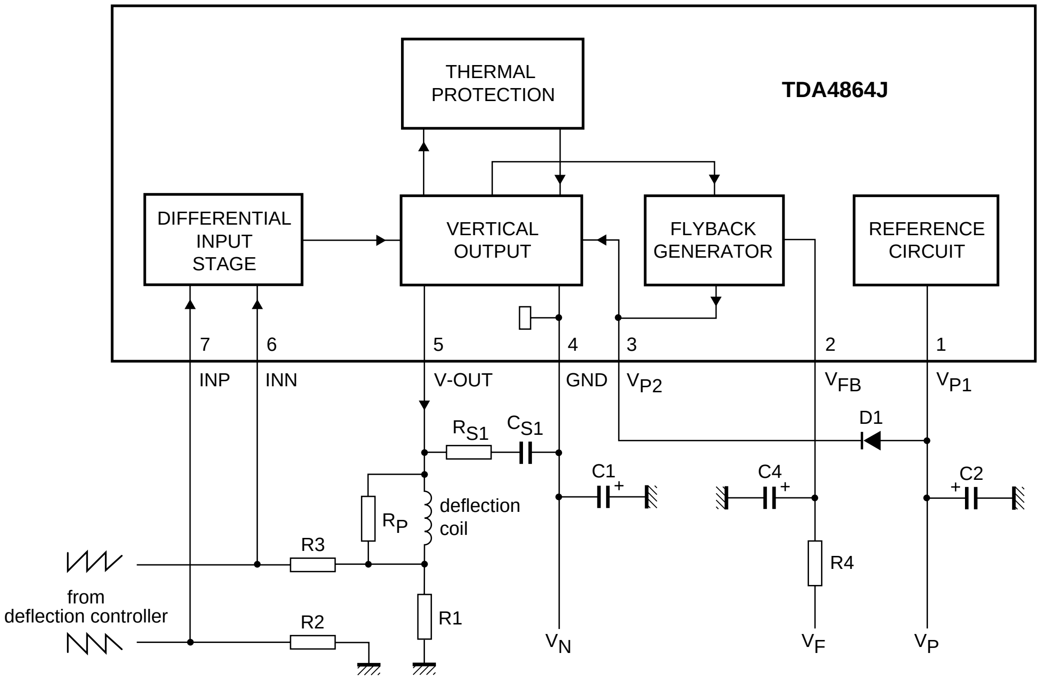


Fig.1 Block diagram of TDA4864J.

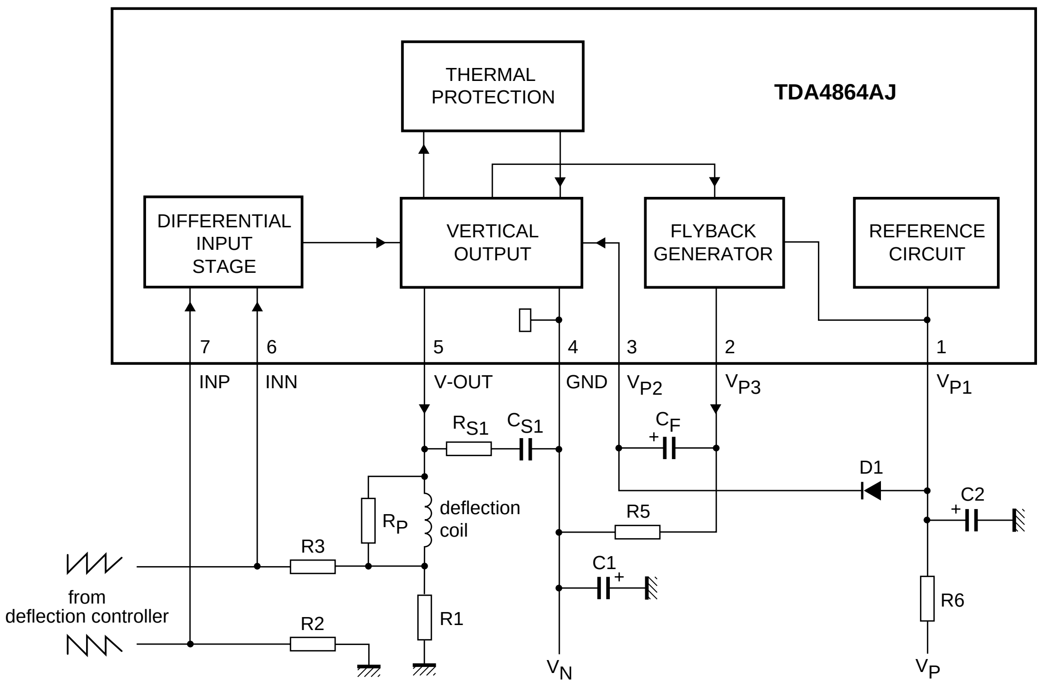


Fig.2 Block diagram of TDA4864AJ.

PINNING

SYMBOL	PIN		DESCRIPTION
	TDA4864J	TDA4864AJ	
V_{P1}	1	1	positive supply voltage 1
V_{FB}	2	–	flyback supply voltage
V_{P3}	–	2	flyback generator output
V_{P2}	3	3	supply voltage 2 for vertical output
GND	4	4	ground or negative supply voltage
V-OUT	5	5	vertical output
INN	6	6	inverted input of differential input stage
INP	7	7	non-inverted input of differential input stage

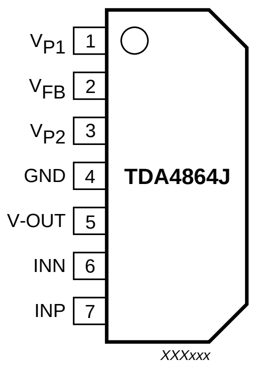


Fig.3 Pin configuration of TDA4864J.

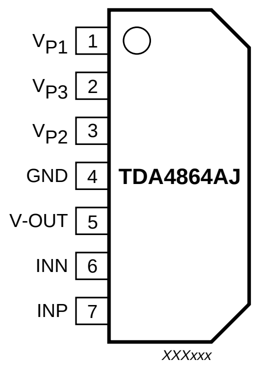


Fig.4 Pin configuration of TDA4864AJ.

FUNCTIONAL DESCRIPTION

Both the TDA4864J and TDA4864AJ consist of a differential input stage, a vertical output stage, a flyback generator, a reference circuit and a thermal protection circuit.

The TDA4864J operates with a separate flyback supply voltage (see Fig.1) while the TDA4864AJ generates the flyback voltage internally by doubling the supply voltage (see Fig.2).

Differential input stage

The differential sawtooth input current signal (coming from the deflection controller) is connected to the inputs (inverted signal to pin INN and non-inverted signal to pin INP). The vertical feedback signal is superimposed on the inverted signal on pin INN.

Vertical output and thermal protection

The vertical output stage is a quasi-complementary class-B amplifier with a high linearity.

The output stage is protected against thermal overshoots. For a junction temperature T_j > 150 °C this protection will be activated and will reduce then the deflection current ($I_{V\text{-}OUT}$).

Flyback generator

The flyback generator supplies the vertical output stage during flyback.

The TDA4864J is used with separate flyback supply voltage to achieve a short flyback time with minimized power dissipation.

The TDA4864AJ needs a capacitor C_F between pins V_{P3} and V_{P2} (see Fig.2). Capacitor C_F is charged during scan, using the external diode D1 and resistor R5. During flyback the cathode of capacitor C_F is connected to the positive supply voltage and the flyback voltage is then twice the supply voltage. For the TDA4864AJ the resistor R6 in the positive supply line can be used to reduce the power consumption.

In parallel with the deflection coil a damping resistor R_P and an RC combination (R_{S1} = 5.6 Ω and C_{S1} = 100 nF) are needed. Furthermore, another additional RC combination (R_{S2} = 5.6 Ω and C_{S2} = 47 to 150 nF) can be used to minimize the noise effect and the flyback time (see Figs 9 and 10).

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages referenced to pin GND; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{P1}	supply voltage 1		–	40	V
V_{P2}	supply voltage 2		–	60	V
V_{FB}	flyback supply voltage of TDA4864J		–	60	V
V_{P3}	flyback generator output voltage of TDA4864AJ		0	V_{P1} + 3	V
V_i	input voltage on				
	pin INN		–	V_{P1}	V
	pin INP		–	V_{P1}	V
$V_{o(V\text{-}OUT)}$	output voltage on pin V-OUT		–	62	V
I_{P2}	supply current 2		–	±1.5	A
$I_{o(V\text{-}OUT)}$	output current on pin V-OUT	note 1	–	±1.5	A
I_{VFB}	current during flyback of TDA4864J		–	±1.5	A
I_{VP3}	current during flyback of TDA4864AJ		–	±1.5	A
T_{stg}	storage temperature		–25	+150	°C
T_{amb}	ambient temperature		–20	+75	°C
T_j	junction temperature	note 1	–	150	°C
V_{es}	electrostatic discharge voltage on all pins	note 2	–300	+300	V

Notes

1. Internally limited by thermal protection; will be activated for $T_j \geq 150$ °C.
2. Equivalent to discharging a 200 pF capacitor through a 0 Ω series resistor.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j\text{-}mb)}$	thermal resistance from junction to mounting base	note 1	6	K/W

Note

1. To minimize the thermal resistance from mounting base to heatsink [$R_{th(mb\text{-}h)}$] follow the recommended mounting instruction: screw mounting preferred; torque = 40 Ncm; use heatsink compound; isolation plate increases $R_{th(mb\text{-}h)}$.

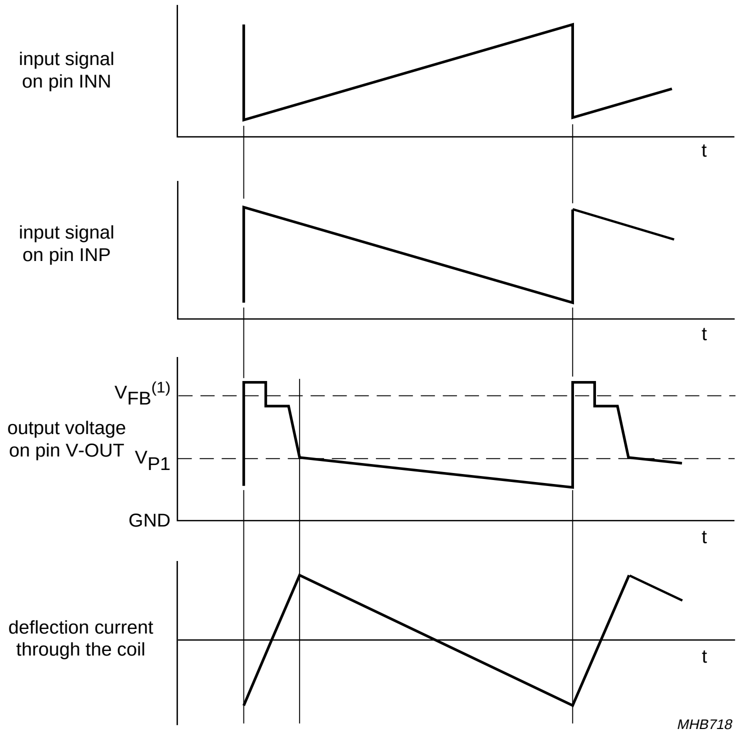
CHARACTERISTICS

V_{P1} = 25 V; T_{amb} = 25 °C; voltages referenced to pin GND; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{P1}	supply voltage 1		9	–	30	V
V_{P2}	supply voltage 2		V_{P1} – 1	–	60	V
V_{FB}	flyback supply voltage of TDA4864J		V_{P1} – 1	–	60	V
V_{P3}	flyback generator output voltage of TDA4864AJ	I_{V-OUT} = –1.25 A	0	–	V_{P1} + 2.2	V
I_{P1}	supply current 1	during scan	–	6	10	mA
I_{P2}	quiescent supply current 2	I_{V-OUT} = 0	–	25	60	mA
Differential input stage						
V_i	input voltage on					
	pin INN		1.6	–	V_{P1} – 0.5	V
	pin INP		1.6	–	V_{P1} – 0.5	V
I_q	input quiescent current on					
	pin INN		–	–100	–500	nA
	pin INP		–	–100	–500	nA
Flyback generator						
I_{VFB}	current during flyback of TDA4864J		–	–	±1.5	A
I_{VP3}	current during flyback of TDA4864AJ		–	–	±1.5	A
$V_{VP2-VFB}$	voltage drop during flyback of TDA4864J					
	reverse	I_{V-OUT} = –1 A	–	–1.5	–	V
		I_{V-OUT} = –1.25 A	–	–2	–	V
	forward	I_{V-OUT} = 1 A	–	2.2	–	V
		I_{V-OUT} = 1.25 A	–	2.5	–	V
$V_{VP3-VP1}$	voltage drop during flyback of TDA4864AJ					
	reverse	I_{V-OUT} = –1 A	–	–1.5	–	V
		I_{V-OUT} = –1.25 A	–	–2	–	V
	forward	I_{V-OUT} = 1 A	–	2.2	–	V
		I_{V-OUT} = 1.25 A	–	2.5	–	V
Vertical output stage; see Fig.5						
I_{V-OUT}	vertical deflection output current		–	–	±1.25	A
$I_{V-OUT(p-p)}$	vertical deflection output current (peak-to-peak value)		–	–	2.5	A
$V_{o(sat)n}$	output saturation voltage to ground	I_{V-OUT} = 1 A	–	1.4	1.7	V
		I_{V-OUT} = 1.25 A	–	1.8	2.3	V
$V_{o(sat)p}$	output saturation voltage to V_{P2}	I_{V-OUT} = 1 A	–2.3	–2	–	V
		I_{V-OUT} = 1.25 A	–2.8	–2.3	–	V
LIN	non-linearity of output signal	note 1	–	–	1	%

Note

1. Deviation of the output slope at a constant input slope.



(1) V_{FB} for TDA4864J; $2V_{P1}$ for TDA4864AJ.

Fig.5 Timing diagram.

INTERNAL PIN CONFIGURATION

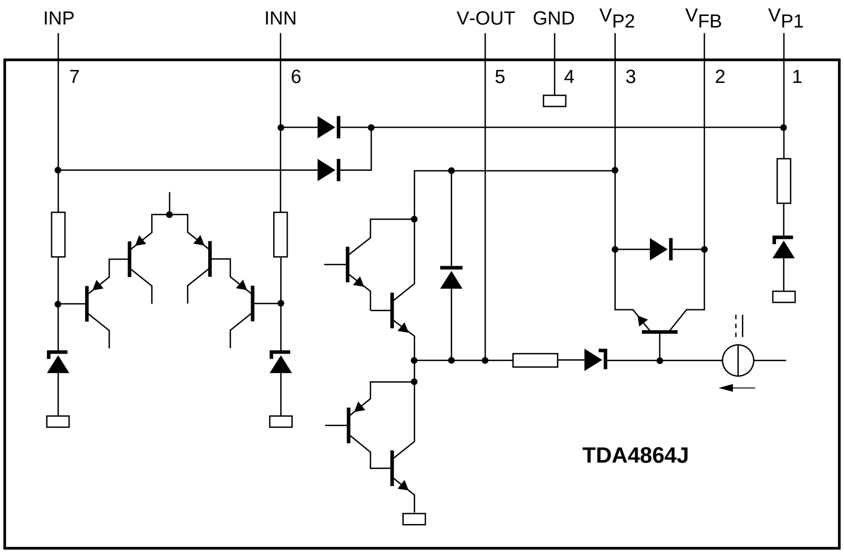


Fig.6 Internal circuits of TDA4864J.

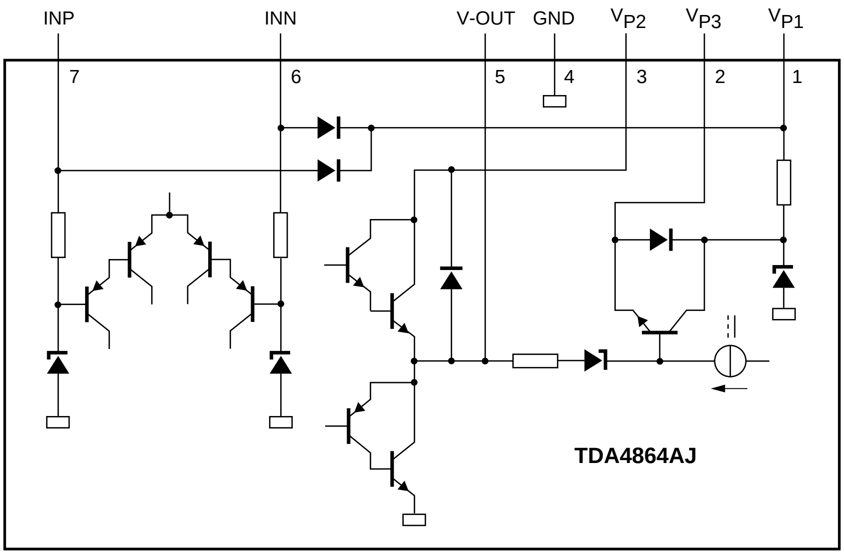


Fig.7 Internal circuits of TDA4864AJ.

APPLICATION INFORMATION

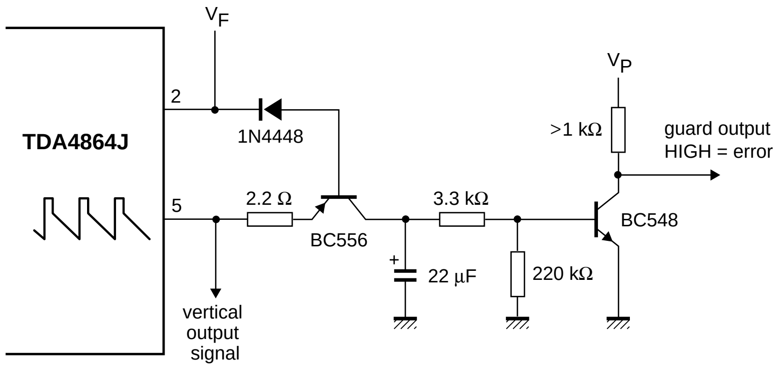
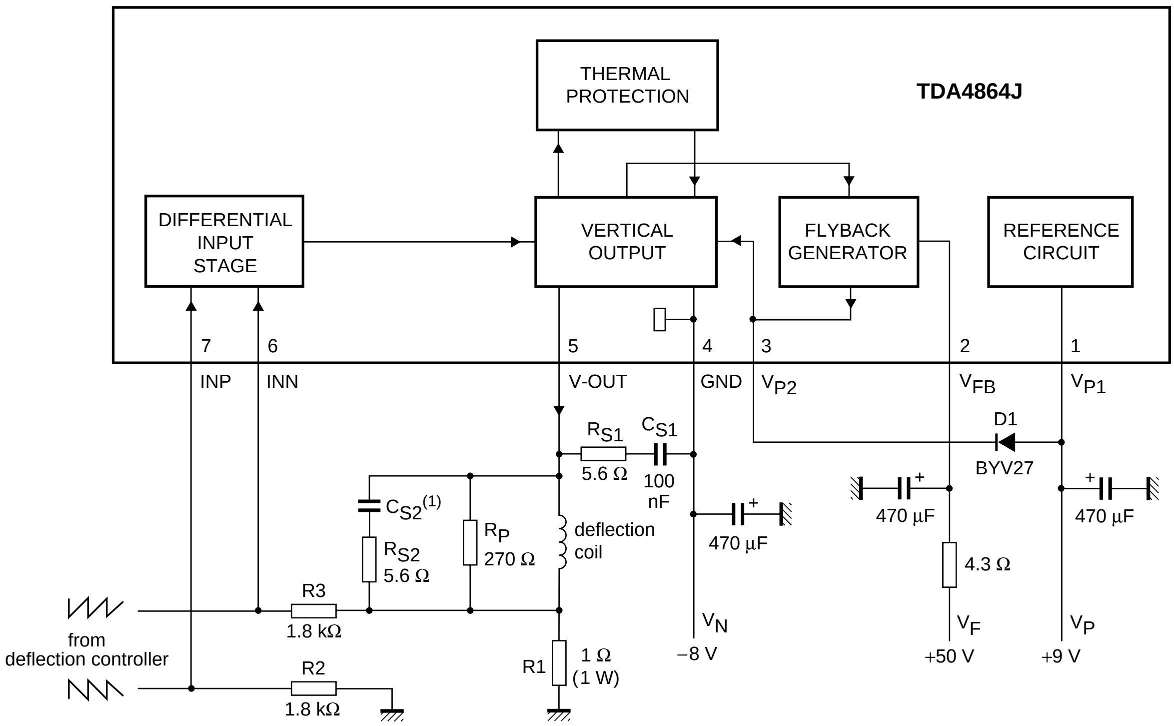


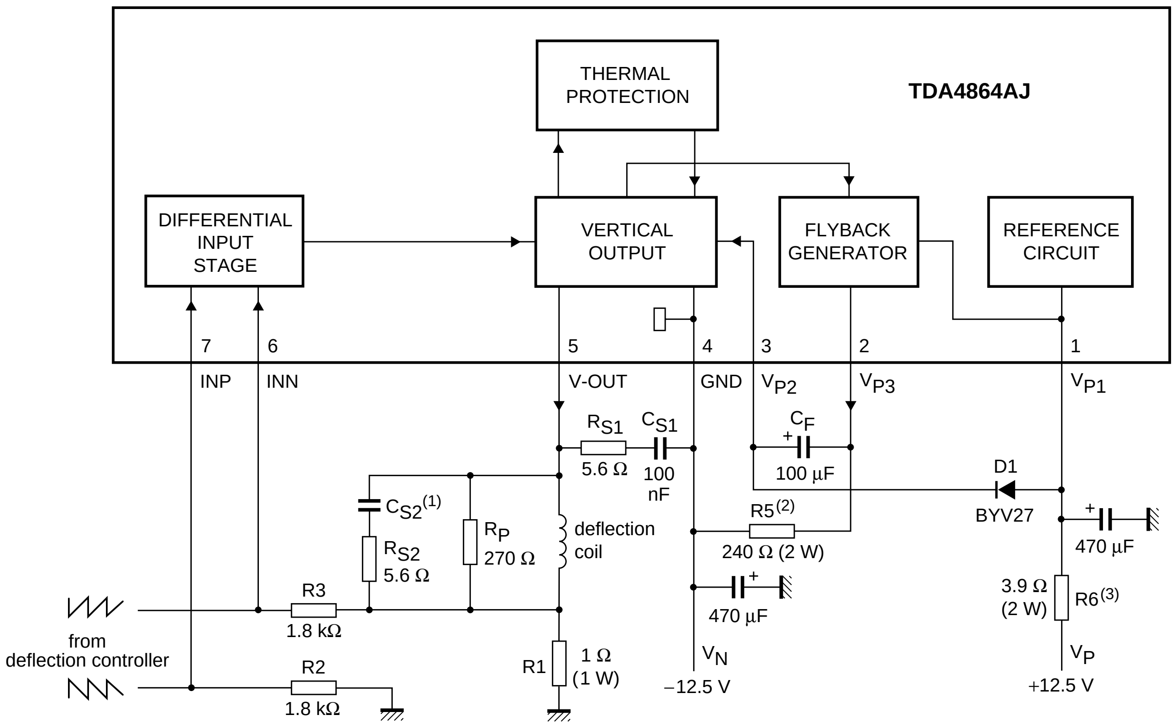
Fig.8 Application circuit with TDA4864J for external guard signal generation.



Attention: the heatsink of the IC must be isolated against ground of the application (it is connected to pin GND).

(1) With C_{S2} (typical value between 47 and 150 nF) the flyback time and the noise behaviour can be optimized.

Fig.9 Application circuit with TDA4864J.



Attention: the heatsink of the IC must be isolated against ground of the application (it is connected to pin GND).

(1) With C_{S2} (typical value between 47 and 150 nF) the flyback time and the noise behaviour can be optimized.

(2) With R5 capacitor C_F will be charged during scan and the value (typical value between 150 and 270 Ω) depends on I_{defl}, t_{flb} and C_F.

(3) R6 reduces the power dissipation of the IC. The maximum possible value depends on the application.

Fig.10 Application circuit with TDA4864AJ.

Example for both TDA4864J and TDA4864AJ

Table 1 Values given from application

SYMBOL	VALUE	UNIT
$I_{defl(max)}$	0.71	A
$L_{deflcoil}$	6	mH
$R_{deflcoil}$	6	Ω
R_P	270	Ω
R1	1	Ω
R2	1.8	kΩ
R3	1.8	kΩ
V_{FB}(1)	50	V
T_{amb}	60	°C
$T_{deflcoil}$	75	°C
$R_{th(j-mb)}$	6	K/W
$R_{th(mb-amb)}$	8	K/W

Note

1. For TDA4864J only.

Table 2 Calculated values

SYMBOL	VALUE		UNIT
	TDA4864J	TDA4864AJ	
V_{P1}	9	12.5	V
V_N	–8	–12.5	V
P_{tot}	3.2	4.4	W
P_{defl}	1.2	1.2	W
P_{IC}	2	3.2	W
$R_{th(tot)}$	14	14	K/W
$T_{j(max)}$	88	105	°C

V_{P1}, V_N and V_{FB} are referenced to ground of application; voltages are calculated with +10% tolerances.

Calculation formulae for supply voltages:

$V_{P1} = -V_{o(sat)p} + (R1 + R_{deflcoil}) \times I_{defl(max)} - U'_L + U_{D1}$

$V_N = V_{o(sat)n} + (R1 + R_{deflcoil}) \times I_{defl(max)} + U'_L$

where

$U'_L = L_{deflcoil} \times 2I_{defl(max)} \times f_v$

f_v = vertical deflection frequency

U_{D1} = forward voltage drop across D1.

Calculation formulae for power consumption:

$$P_{IC} = P_{tot} - P_{defl}$$

$$P_{tot} = (V_{P1} - U_{D1}) \times \frac{I_{defl(max)}}{4} + V_N \times \frac{I_{defl(max)}}{4}$$

$$+ (V_{P1} - V_N) \times 0.01\ \text{A} + 0.2\ \text{W}$$

$$P_{defl} = \frac{R_{deflcoil} + R1}{3} \times I^2_{defl(max)}$$

where

P_{IC} = power dissipation of the IC

P_{tot} = total power dissipation

P_{defl} = power dissipation of the deflection coil.

Calculation formulae for maximum required thermal resistance for the heatsink at $T_{j(max)}$ = 110 °C:

$$R_{th(mb-amb)} = \left(\frac{T_{j(max)} - T_{amb}}{P_{IC}}\right) - R_{th(j-mb)} = 19\ \text{K/W (max.)}$$

Table 3 t_{flb} as a function of V_{FB} for TDA4864J

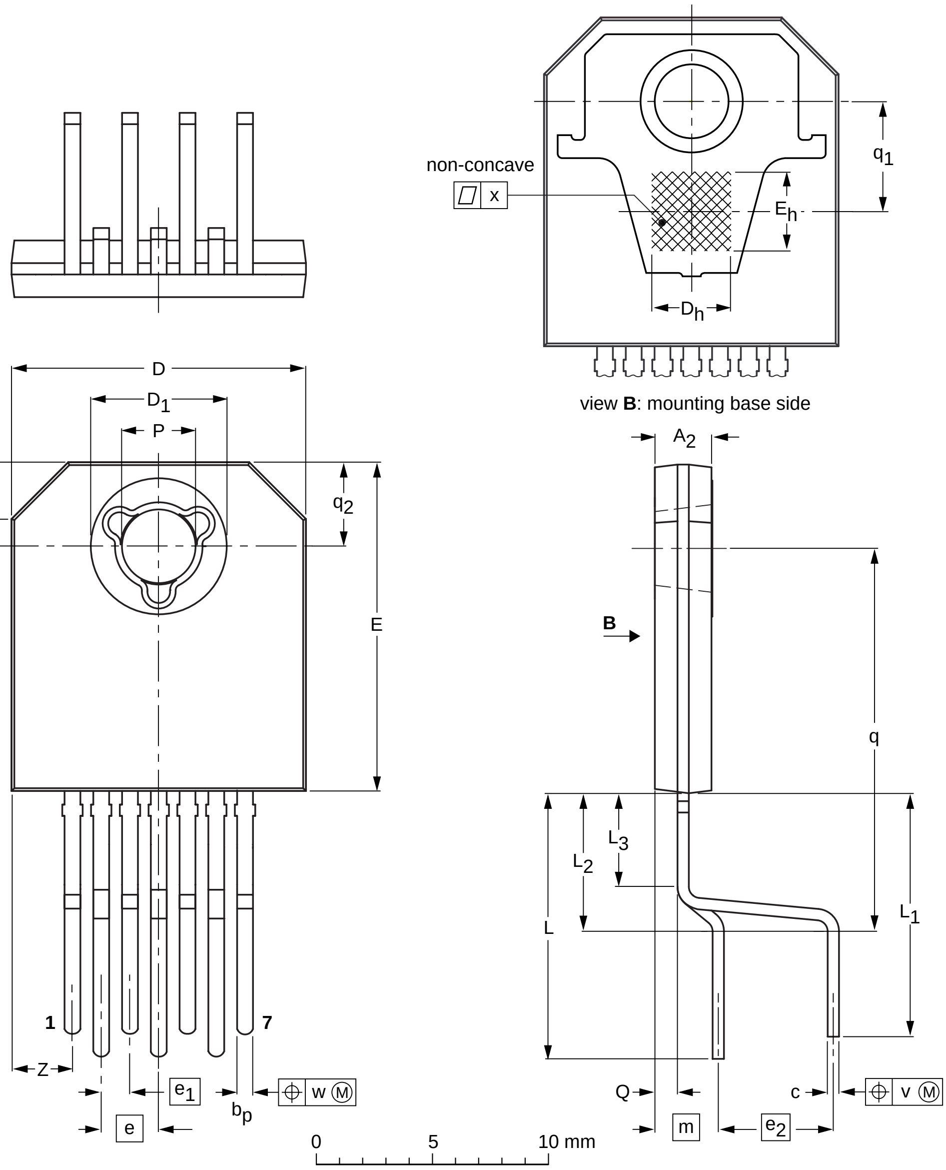
t_{flb} (μs)	V_{FB} (V)
350	30
250	40
210	50

Table 4 t_{flb} as a function of V_{P1} and V_N for TDA4864AJ

t_{flb} (μs)	V_{P1} (V)	V_N (V)	P_{IC} (W)	R6 (Ω)
360	10	–10	2.5	1
290	12.5	–12.5	3.2	3.9
240	15	–15	3.9	6.8

PACKAGE OUTLINE

DBS7P: plastic DIL-bent-SIL power package; 7 leads (lead length 12/11 mm); exposed die pad **SOT524-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A_2(2)	b_p	c	D(1)	D_1(2)	D_h	E(1)	E_h	e	e_1	e_2	k	L	L_1	L_2	L_3	m	P	Q	q	q_1	q_2	v	w	x	Z(1)
mm	2.7 2.3	0.80 0.65	0.58 0.48	13.2 12.8	6.2 5.8	3.5	14.7 14.3	3.5	2.54	1.27	5.08	3 2	12.4 11.0	11.4 10.0	6.7 5.5	4.5 3.7	2.8	3.4 3.1	1.15 0.85	17.5 16.3	4.85	3.8 3.6	0.8	0.3	0.02	2.92 2.37

Notes

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.
2. Plastic surface within circle area D_1 may protrude 0.04 mm maximum.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT524-1						~~00-07-03~~ 03-03-12

SOLDERING

Introduction to soldering through-hole mount packages

This text gives a brief insight to wave, dip and manual soldering. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

Wave soldering is the preferred method for mounting of through-hole mount IC packages on a printed-circuit board.

Soldering by dipping or by solder wave

Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing. Typical dwell time of the leads in the wave ranges from 3 to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg(max)}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Manual soldering

Apply the soldering iron (24 V or less) to the lead(s) of the package, either below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

Suitability of through-hole mount IC packages for dipping and wave soldering methods

PACKAGE	SOLDERING METHOD	
	DIPPING	WAVE
DBS, DIP, HDIP, RDBS, SDIP, SIL	suitable	suitable[1]
PMFP[2]	–	not suitable

Notes

1. For SDIP packages, the longitudinal axis must be parallel to the transport direction of the printed-circuit board.
2. For PMFP packages hot bar soldering or manual soldering is suitable.

DATA SHEET STATUS

LEVEL	DATA SHEET STATUS[1]	PRODUCT STATUS[2][3]	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

Notes

1. Please consult the most recently issued data sheet before initiating or completing a design.
2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.
3. For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

DEFINITIONS

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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