FM IF Amplifier with Pilot Tone Decoding for TV Stereo Application

TDA 4940

Bipolar IC

Type	Ordering code	Package
TDA 4940	Q67000-A1872	DIP 22

The TDA 4940 has been designed as an intercarrier FM IF limiter amplifier. It includes a coincidence demodulator, an AF output and a decoding device. The decoding device is based on the two carrier system ("dual-channel audio") and decodes the pilot carriers during multi-channel audio as used in TV sets.

Features

- Good limiting characteristics
- PLL circuit, eliminates alignment of pilot tone decoder
- Few external components

Maximum ratings

Supply voltage	V_S	16.5	V
Input voltage line flyback	V_{13}	V_S	V
Input voltage mono compulsory	V_7	V_S	V
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−40 to 125	°C
Thermal resistance (system-air)	$R_{th\ SA}$	70	K/W

Operating range

Supply voltage	V_S	10 to 15.8	V
Ambient temperature	T_A	0 to 70	°C

Characteristics

$V_S = 12$ V; $T_A = 25$ °C

		min	typ	max	
Total current consumption	$I_{S\,8}$	16	26	34	mA
Reference voltage	$V_{REF\,5}$	5.2	6	6.8	V
FM section $f_{IF} = 5.74$ MHz; $Q_B \approx 25$; $V_{iIF} = 1$ mV; $\Delta f = \pm 30$ kHz; $f_{mod} = 1$ kHz					
Limiter threshold	$V_{lim\,rms}$		20	40	µV
Input resistance	$R_{i\,2\text{-}3}$	600	800	1000	Ω
AM suppression ($m = 30\%$)	a_{AM}		42		dB
Signal-to-noise ratio ($V_{iIF} = 10$ mV)	$a_{S/N}$		85		dB
Total harmonic distortion	THD		1	3	%
Demodulator input resistance	$R_{i\,19\text{-}20}$	4	5.4	7	kΩ
AF output voltage ($\Delta f = 12.5$ kHz)	$V_{q\,18\,rms}$	200	300	400	mV
AF output resistance	$R_{q\,18}$		100		Ω
Pilot carrier decoding					
Output voltage stereo	V_6	10.5		V_S	V
mono	V_6		6		V
dual audio	V_6	0		1.5	V
Input mono compulsory low	V_7	0		0.7	V
high	V_7	1.3		V_S	V
pulse width	τ_H	500			µs
Input voltage line flyback	$V_{13\,pp}$	4.5		V_S	V
Input resistance	$R_{i\,13}$		33		kΩ

Circuit description

FM section

The TDA 4940 includes an 8-stage limiter amplifier, an FM coincidence demodulator as well as an AF output. Deemphasis is provided by an external *RC* circuit.

Pilot carrier decoding

A PLL synthesizer generates the pilot carrier frequency $f_p = 3.5 \times f_H$. The line flyback pulse is used as reference frequency. Via a high-pass filter, the modulated pilot carrier is routed from the AF output to the synchronous demodulator. However, the internal pilot carrier is synchronized with a phase regulating circuit. Via the external band-pass filter, the synchronously demodulated identifying signals are forwarded to the decoding circuit. Decoding is performed with a frequency-selective, phase-resistant RMS rectifier of very narrow bandwidth as well as a comparator. The "stereo" status ($f_{ST} = f_H/133$), as well as the "dual audio" ($f_{DT} = f_H/57$) and the "mono" status ($f_M = 0$) are evaluated during multiplex operations. The current operating status is provided via a tristate output. It is possible to set "mono" with a positive pulse edge at input 7.

$f_{DT} = f_{ZT}$ = dual tone pilot carrier
f_{ST} = stereo tone pilot carrier
f_M = mono pilot carrier
f_H = horizontal deflection frequency

Application notes

The TDA 4940 has been designed for demodulating the second sound carrier of a TV channel as well as for decoding the pilot signal of "stereo tone" and "dual audio" status.

The component comprises 4 functional sections:

- FM section (amplifier, demodulator)
- Reference frequency generator (for decoding the pilot tone)
- Pilot frequency demodulator
- Signal decoder

FM section

The FM section corresponds to that of type TBA 120 T or TBA 120 U without VTR and volume functions.

Demodulator circuit

The demodulator can be used with a ceramic phase shifter as well as with an LC network in case of external coupling capacitors. Under extreme conditions, the LC network is advantageous with respect to the intercarrier signal-to-noise ratio, since it shows alignment capability.

Pin 18 AF output

The AF output is formed by an emitter follower with typically 2 mA quiescent current. Due to the rectifying effect, high capacitive load may result in harmonic distortion, which, however, can be reduced to a minimum by increasing the quiescent current (resistance of pin 18 to ground). At the AF output the mean value of the DC voltage with THD_{min} is approx. 6 V.

Internal reference frequency generation

Pin 13 Horizontal pulse

For decoding the stereo and dual audio signal, the reference frequencies 3.5x15.625 kHz, 15.625 kHz/133 and 15.625 kHz/57 are required. They are derived from the horizontal frequency with the aid of a PLL. Pin 13 is the input for the horizontal pulse ("frequency standard" of the TDA 4940), which can be offered to the component in both polarities. The internal switching threshold is typically ± 2 V ($\pm 0.7\ V_{min}$; $\pm 4.5\ V_{max}$). The level of the applied signal must ensure that **one** switching threshold is definitely exceeded, but not both.

Pin 12 PLL filter

The PLL filter is connected to pin 12. The voltage of this pin internally controls the VCO of the PLL. The DC voltage value of the PLL ranges from 1.4 V to 5.5 V and amounts to typically 3.5 V in locked current conditions.

Pilot frequency demodulation

Pin 17; 54 kHz input pin 16; output of identification signal; phase control circuit

Pin 17 is the demodulator input for the pilot frequency, pin 16 the corresponding demodulator output. The peak-to-peak voltage at pin 17 is to amount to 150 mV, the rms output voltage of the identification signal is then typically 120 mV. Internally, the demodulator is controlled by the 54.68 kHz rectangular signal, which is derived from the line signal.

The demodulator requires a very small phase differential of pilot carrier frequency and internal 54 kHz frequency, otherwise the demodulating effect is impaired (else the signal amplitude [117/224 Hz] at pin 16 would be extremely decreased). The internal 54 kHz signal is coupled in phase-locked mode with the external pilot frequency (via the PLL described) but the locked phase differential of the two frequencies is yet to be leveled by a control loop.

Figure 1

The control element of this loop is a monoflop generating a triangular voltage (15.625 kHz) at pin 14 **(figure 1).** Depending on the control voltage ($V_{15}-V_5$), this monoflop shifts the break-point on the edge of the triangular signal and thus the phase between pilot and internal frequency. The phase shift range of this circuit lies beyond 180° (on the 54 kHz level).

If no input signal is applied to pin 17 (e.g. in case of channel change) the phase shift circuit is in a quiescent state. The residual voltage differential $V_{15}-V_5$ is the offset voltage of the phase control loop. Its value is typically −40 mV. In case the offset voltage is too high, the phase shift range becomes unsymmetrical, i.e. smaller than 180° in one direction. The result is that not every phase position is adequately regulated.

Proposed remedial measures

− 1.5 MΩ resistor between pin 15 and pin 8 (V_S)
or
− adjustment of the offset voltage (zero phase position) via a high-ohmic potentiometer between V_S, pin 15 and ground,
or

Figure 2

− in case of a channel change (or turn-on of the TV set), short-circuiting of the offset voltage by means of a transistor switch **(figure 2),** so that the control circuit can always start from the zero phase position.

Advantage of the last proposal

If, in case of a fast channel change, the blocking capacitor between pin 15 and 5 was not able to fully discharge via the internal resistance of pin 15 (39 kΩ), the control circuit starts despite this fact from the zero phase position. (A residual voltage at the capacitor has the effect of an offset not being adjusted, which provides the same results as described above).

For decoupling the pilot frequency from the AF signal, a 54 kHz band-pass (from pin 18 to pin 17) is recommendable.

There are two reasons for this:

- Lowering of the AF signal ensures that the pilot frequency demodulator is not overmodulated.
- Noise (during "mono" without second sound carrier) within the range of the odd-order harmonic of 54 kHz is shifted to the identification signal level by the pilot frequency demodulator since this demodulator is internally driven with the aid of a square-wave signal. The 54 kHz bandpass lowers this noise level **(figure 3).** Due to the fact that this kind of bandpass results in an extreme low-impedance load at the AF output (pin 18), harmonic distortions are to be expected (117/274 Hz will be audible in AF).

Figure 3

Remedial measures

- the filter quality should be below 15
- the emitter follower of this output can be set to a low-impedance state by means of a 5.6 kΩ resistance of pin 18 to ground.

or

- a decoupling transistor of pin 18 to bandpass **(figure 4).**

Figure 4
Decoupling transistor

Decoding of the identification signals (117/274 Hz)

Pin 11; Identification signal input

The identification signals coming from the pilot frequency demodulator output (pin 16) are filtered and subsequently input at pin 11 for being decoded via a phase-independent demodulator with a compensating voltage exceeding a threshold value.

Pin 9/10

Pin 9 and 10 are the low-pass filter points of the demodulator. With a bandwidth of 1 Hz 6internally 18 kΩ, externallỹ 10 μF) they have the same noise-suppressing effect as a 2 Hz bandpass around the identification signals (and their odd-order harmonics) at pin 11.

The external electrolytic capacitors of 10 μF each at pin 9 and 10 to ground can be extended to values ranging from 30 μF to 50 μF. These capacitors have to be connected to pin 5. Furthermore, it should be noted that the electrolytic capacitors must be capable of being inversely loaded up to 2 V.

Pin 7
Compulsory mono

The identification signal decoding circuit can be compulsorily set to "mono" via pin 7. In open-circuit state this input is inactive.

Pin 6
Output of identification signal decoding

Output of the identification signal decoding is pin 6, which indicates via three output levels the "stereo", "mono", and "dual audio" status.

Voltage at pin 14

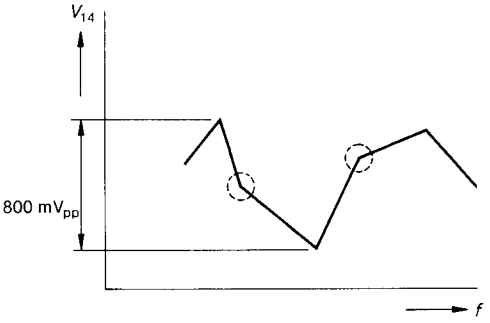


Figure 1

Transistor switch

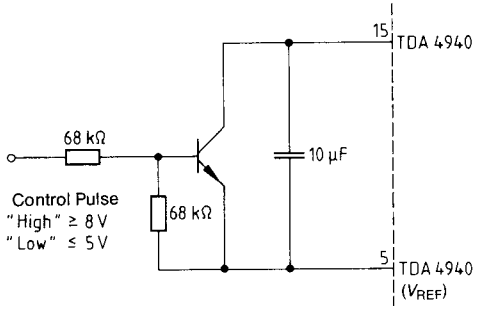


Figure 2

Bandpass for decoupling the pilot frequency from the AF signal

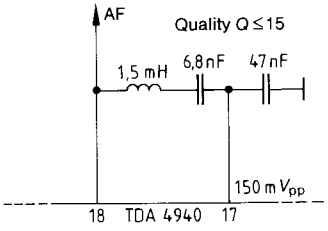


Figure 3

Bandpass for pilot frequency decoupling with decoupling transistor

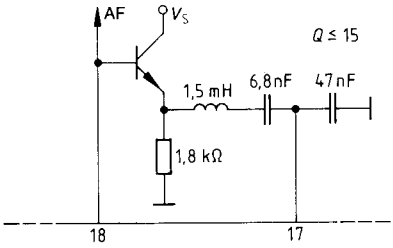
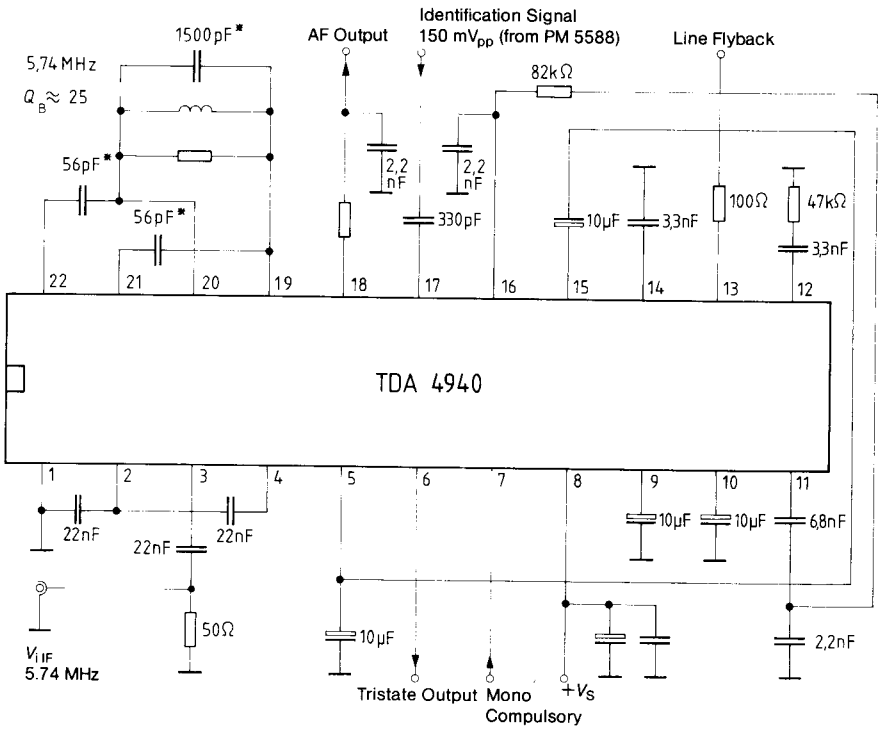


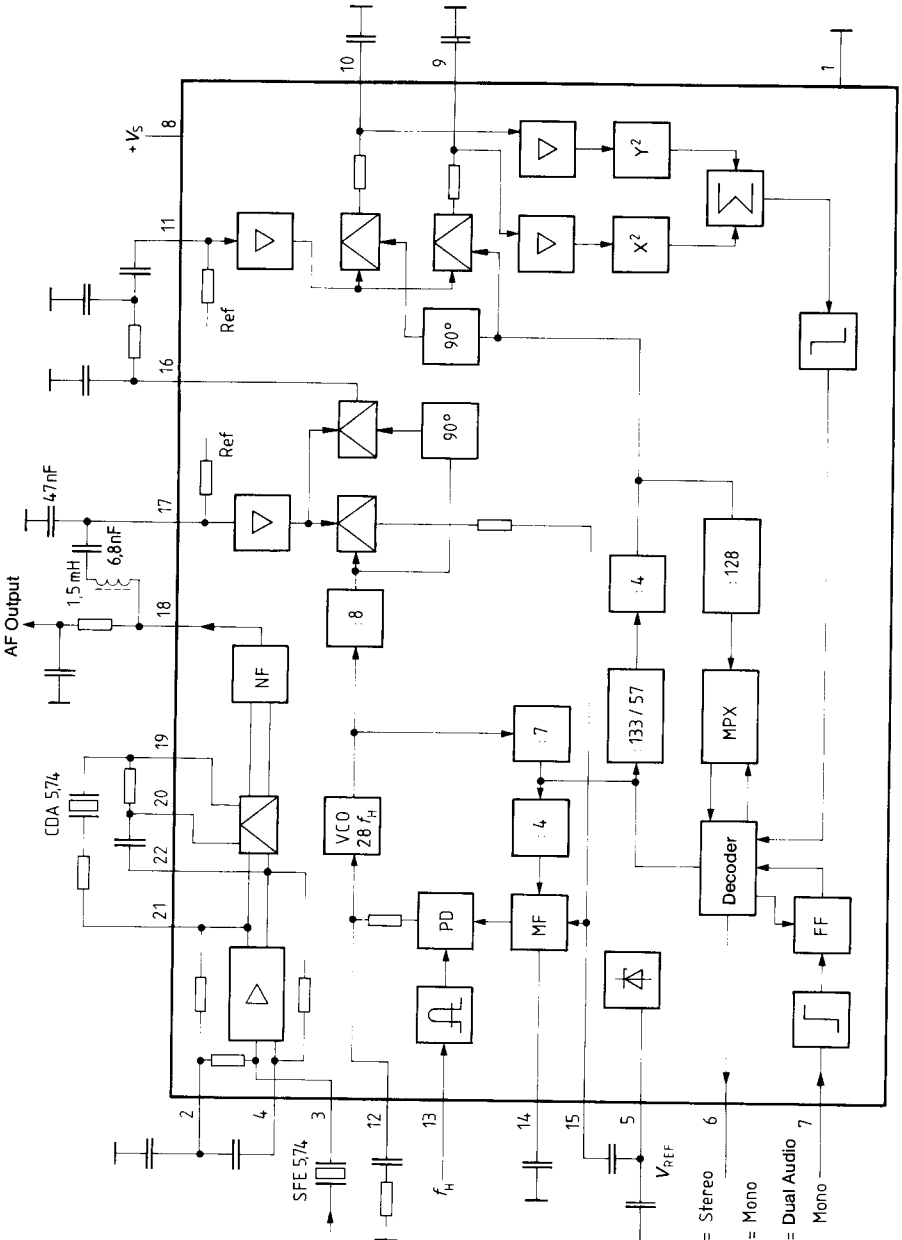
Figure 4

Test circuit

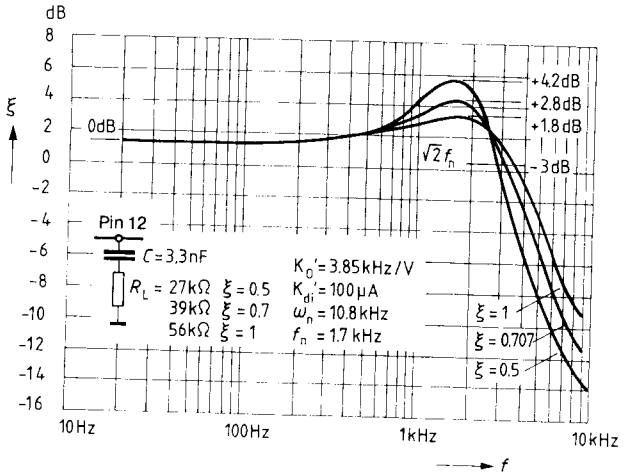


* STYROFLEX Capacitor

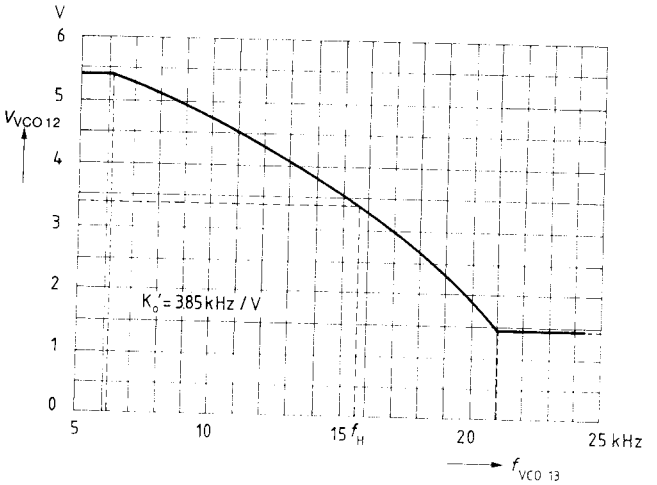
Block diagram



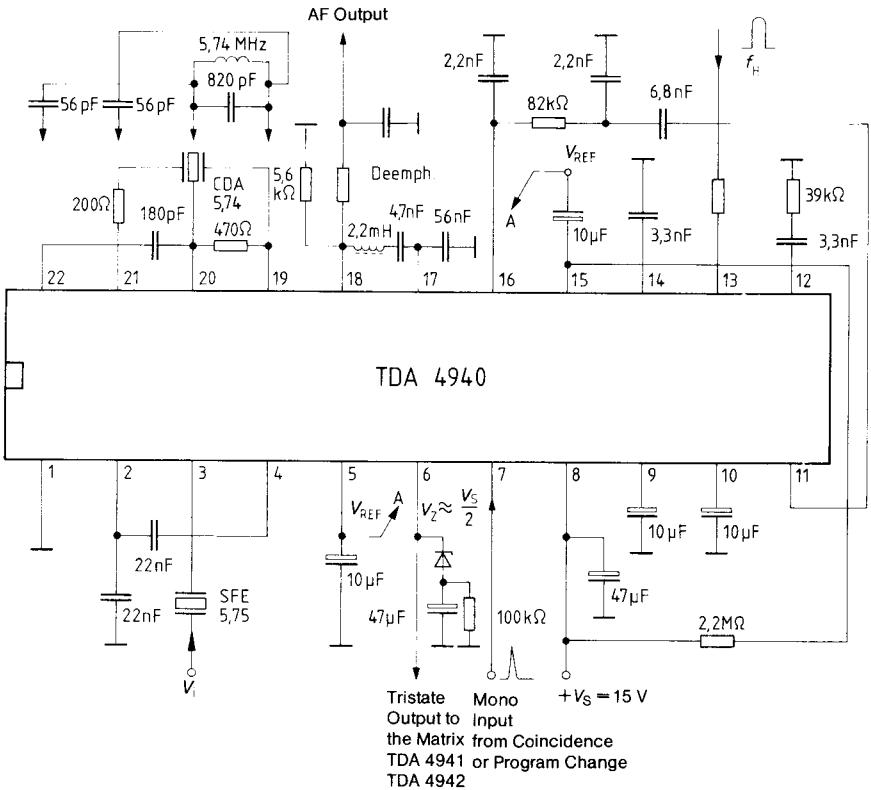
PLL transfer function



VCO tracking



Application circuit



Internal pin Diagram