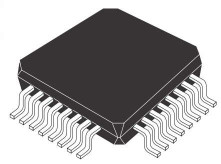
TDA7342

Digitally controlled audio processor

Features

- Input multiplexer
  - Two stereo and one mono inputs
  - One quasi differential input
  - Selectable input gain for optimal adaptation to different sources
- Fully programmable loudness function
- Volume control in 0.3dB steps including gain up to 20dB
- Zero crossing mute, soft mute and direct mute
- Bass and treble control
- Four speaker attenuators
  - Four independent speakers control in 1.25dB steps for balance and fader facilities
  - Independent mute function
- All functions programmable via serial I^{2}C bus



LQFP32

Description

The audioprocessor TDA7342 is an upgrade of the TDA731X audioprocessor family.

Due to a highly linear signal processing, using CMOS-switching techniques instead of standard bipolar multipliers, very low distortion and very low noise are obtained. Several new features like softmute, and zero-crossing mute are implemented. The soft Mute function can be activated in two ways:

1. Via serial bus (Mute byte, bit D0)
2. Directly on pin 21 through an I/O line of the microcontroller

Very low DC stepping is obtained by use of a BICMOS technology.

Order codes

Part number	Package	Packing
TDA7342N	LQFP32	Tube
TDA7342NTR	LQFP32	Tape and reel

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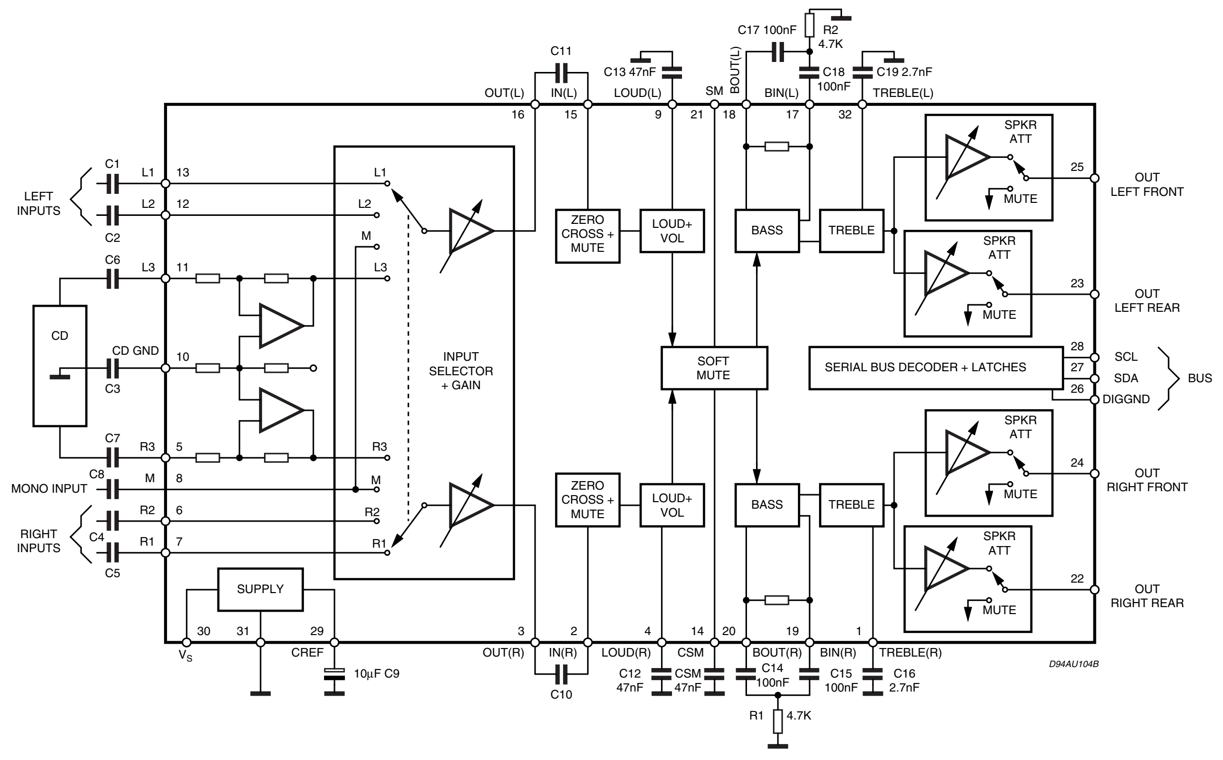
1 Block diagram and pin descriptions

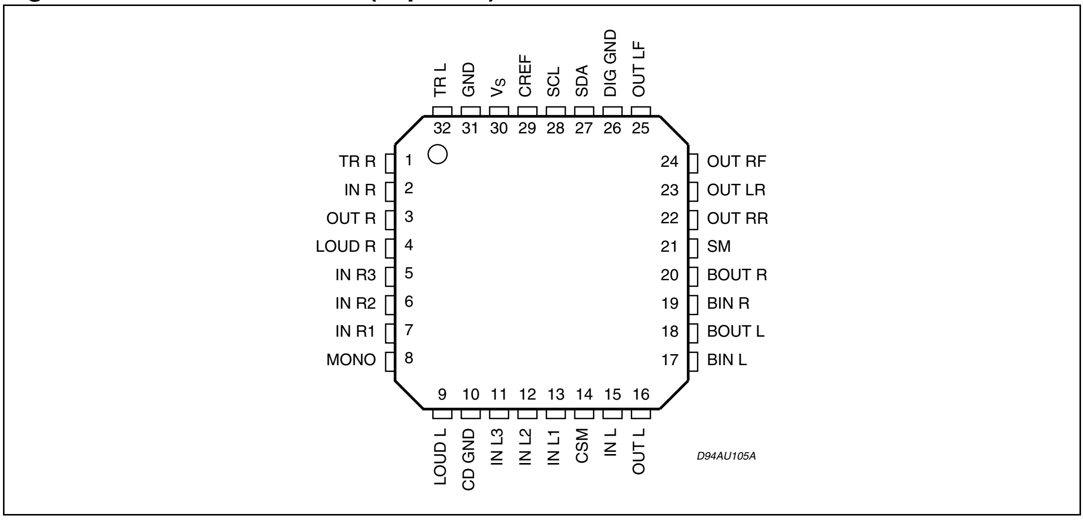
1.1 Block diagram

Figure 1. Block diagram



1.2 Pin description

Figure 2. Pin connections (Top view)



2 Electrical specifications

2.1 Absolute maximum ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_S	Operating supply voltage	10.5	V
T_{amb}	Operating ambient temperature	-40 to 85	°C
T_{stg}	Storage temperature range	-55 to 150	°C

Table 2. Thermal data

Symbol	Parameter	Value	Unit
$R_{th\ j\text{-}amb}$	Thermal resistance junction-pins	150	°C/W

Table 3. Quick reference data

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_S	Supply voltage	6	9	10.2	V
V_{CL}	Max. input signal handling	2.1	2.6		Vrms
THD	Total harmonic distortion V = 1Vrms f = 1KHz		0.01	0.08	%
S/N	Signal to noise ratio		106		dB
S_C	Channel separation		100		dB
	Volume control 0.3dB step	-59.7		20	dB
	Treble control 2dB step	-14		+14	dB
	Bass control 2dB step	-10		+18	dB
	Fader and balance control 1.25dB step	-38.75		0	dB
	Input gain 3.75dB step	0		11.25	dB
	Mute attenuation		100		dB

Table 4. Electrical characteristics
(V_S = 9V; R_L = 10KΩ; R_g = 50Ω; T_{amb} = 25°C; all gains = 0dB; f = 1KHz. Refer to the test circuit, unless otherwise specified.)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Input selector						
R_I	Input resistance		70	100	130	KΩ
V_{CL}	Clipping level	$d \leq 0.3\%$	2.1	2.6		V_{RMS}
S_I	Input separation		80	100		dB
R_L	Output load resistance		2			KΩ
$G_{I\ MIN}$	Minimum input gain		-0.75	0	0.75	dB
$G_{I\ MAX}$	Maximum input gain		10.25	11.25	12.25	dB

Table 4. Electrical characteristics (continued)
(V_S = 9V; R_L = 10KΩ; R_g = 50Ω; T_{amb} = 25°C; all gains = 0dB; f = 1KHz. Refer to the test circuit, unless otherwise specified.)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
G_{step}	Step resolution		2.75	3.75	4.75	dB
e_N	Input noise	20Hz to 20 KHz unweighted		2.3		µV
V_{DC}	DC Steps	Adjacent gain steps		1.5	10	mV
		$G_{IIN}$to G_{IMAX}		3		mV
Differential input (IN 3)						
R_I	Input resistance	Input selector BIT D6 = 0 (0dB)	10	15	20	KΩ
		Input selector BIT D6 = 1(-6dB)	14	20	30	KΩ
CMRR	Common mode rejection ratio	V_{CM} = 1V_{RMS}; f =1KHz	48	75		dB
		f = 10KHz	45	70		dB
d	Distortion	V_I= 1V_{RMS}		0.01	0.08	%
e_{IN}	Input noise	20Hz to 20KHz; Flat; D6 = 0		5		µV
G_{DIFF}	Differential gain	D6 = 0	-1	0	1	dB
		D6 = 1	-7	-6	-5	dB
Volume control						
R_I	Input resistance		35	50		KΩ
G_{MAX}	Maximum gain		18.75	20	21.25	dB
A_{MAX}	Maximum attenuation		57.7	59.7	62.7	dB
A_{STEPC}	Step resolution coarse attenuation		0.5	1.25	2.0	dB
A_{STEPF}	Step resolution fine attenuation		0.11	0.31	0.51	dB
E_A	Attenuation set error	G = 20 to -20dB	-1.25	0	1.25	dB
		G = -20 to -58dB	-3		2	dB
E_t	Tracking error				2	dB
V_{DC}	DC Steps	Adjacent attenuation Steps	-3	0	3	mV
		From 0dB to A_{MAX}		0.5	5	mV
Loudness control						
R_I	Internal resistor	Loud = On	35	50	65	KΩ
A_{MAX}	Maximum attenuation		17.5	18.75	20.0	dB
A_{step}	Step resolution		0.5	1.25	2.0	dB
Zero crossing mute						

Table 4. Electrical characteristics (continued)
(V_S = 9V; R_L = 10KΩ; R_g = 50Ω; T_{amb} = 25°C; all gains = 0dB; f = 1KHz. Refer to the test circuit, unless otherwise specified.)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{TH}	Zero crossing threshold (1)	WIN = 11		20		mV
		WIN = 10		40		mV
		WIN = 01		80		mV
		WIN = 00		160		mV
A_{MUTE}	Mute attenuation		80	100		dB
V_{DC}	DC Step	0dB to Mute		0	3	mV
Soft mute						
A_{MUTE}	Mute attenuation		45	60		dB
T_{DON}	ON Delay time	C_{CSM} = 22nF; 0 to -20dB; I = I_{MAX}	0.7	1	1.7	ms
		C_{CSM} = 22nF; 0 to -20dB; I = I_{MIN}	20	35	55	ms
T_{DOFF}	OFF current	V_{CSM}= 0V; I = I_{MAX}	25	50	75	µA
		V_{CSM}= 0V; I = I_{MIN}		1		µA
V_{THSM}	Soft mute threshold		1.5	2.5	3.5	V
R_{INT}	Pull-up resistor (pin 21)	(2)	35	50	65	KΩ
V_{SMH}	(pin 21) Level high		3.5			V
V_{SML}	(pin 21) Level low	Soft mute active			1	V
Bass control						
B_{BOOST}	Max bass boost		15	18	20	dB
B_{CUT}	Max bass cut		-8.5	-10	-11.5	dB
A_{step}	Step Resolution		1	2	3	dB
R_g	Internal Feedback Resistance		45	65	85	KΩ
Treble control						
C_{RANGE}	Control Range		±13	±14	±15	dB
A_{step}	Step Resolution		1	2	3	dB
Speaker attenuators						
C_{RANGE}	Control range		35	37.5	40	dB
A_{step}	Step resolution		0.5	1.25	2.00	dB
A_{MUTE}	Output mute attenuation	Data word = XXX11111	80	100		dB
E_A	Attenuation set error				1.25	dB
V_{DC}	DC Steps	Adjacent attenuation steps		0	3	mV

Table 4. Electrical characteristics (continued)
(V_S = 9V; R_L = 10KΩ; R_g = 50Ω; T_{amb} = 25°C; all gains = 0dB; f = 1KHz. Refer to the test circuit, unless otherwise specified.)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Audio output						
V_{clip}	Clipping Level	d = 0.3%	2.1	2.6		Vrms
R_L	Output Load Resistance		2			KΩ
R_O	Output Impedance			30	100	Ω
V_{DC}	DC Voltage Level		3.5	3.8	4.1	V
General						
V_{CC}	Supply Voltage		6	9	10.2	V
I_{CC}	Supply Current		5	10	15	mA
PSRR	Power Supply Rejection Ratio	f = 1KHz	60	80		dB
		B = 20 to 20kHz "A" weighted		65		dB
e_{NO}	Output Noise	Output muted (B = 20 to 20kHz flat)		2.5		µV
		All gains 0dB (B = 20 to 20kHz flat)		5	15	µV
E_t	Total Tracking Error	A_V= 0 to -20dB		0	1	dB
		A_V= -20 to -60dB		0	2	dB
S/N	Signal to Noise Ratio	All Gains = 0dB; V_O= 1Vrms		106		dB
S_C	Channel Separation		80	100		dB
d	Distortion	V_{IN} =1V		0.01	0.08	%
Bus inputs						
V_{IL}	Input Low Voltage				1	V
V_{IN}	Input High Voltage		3			V
I_{IN}	Input Current	V_{IN} = 0.4V	-5		5	µA
V_O	Output Voltage SDA Acknowledge	I_O= 1.6mA		0.4	0.8	V

1. WIN represents the MUTE programming bit pair D6, D5 for the zero crossing window threshold
2. Internal pull-up resistor to Vs/2; LOW = softmute active

3 I²C Bus interface

Data transmission from the microprocessor to the TDA7342 and vice versa takes place through the 2 wires of the I²C BUS interface, consisting of the two lines SDA and SCL (pull-up resistors to the positive supply voltage must be externally connected).

3.1 Data validity

As shown in fig. 4, the data on the SDA line must be stable during the high period of the clock. The HIGH and LOW state of the data line can only change when the clock signal on the SCL line is LOW.

3.2 Start and stop conditions

As shown in fig. 5 a start condition is a HIGH to LOW transition of the SDA line while SCL is HIGH. The stop condition is a LOW to HIGH transition of the SDA line while SCL is HIGH.

A STOP condition must be sent before each START condition.

3.3 Byte format

Every byte transferred to the SDA line must contain 8 bits. Each byte must be followed by an acknowledge bit. The MSB is transferred first.

3.4 Acknowledge

The master (microprocessor) puts a resistive HIGH level on the SDA line during the acknowledge clock pulse (see

fig. 6). The peripheral (audioprocessor) that acknowledges has to pull-down (LOW) the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during this clock pulse.

The audioprocessor which has been addressed has to generate an acknowledgment after the reception of each byte, otherwise the SDA line remains at the HIGH level during the ninth clock pulse time. In this case the master transmitter can generate the STOP information in order to abort the transfer.

3.5 Transmission without acknowledge

Avoiding to detect the acknowledge of the audioprocessor, the microprocessor can use a simpler transmission: simply it waits one clock without checking the slave acknowledging, and sends the new data. This approach of course is less protected from misworking and decreases the noise immunity.

Figure 3. Data validity on the I^2C BUS

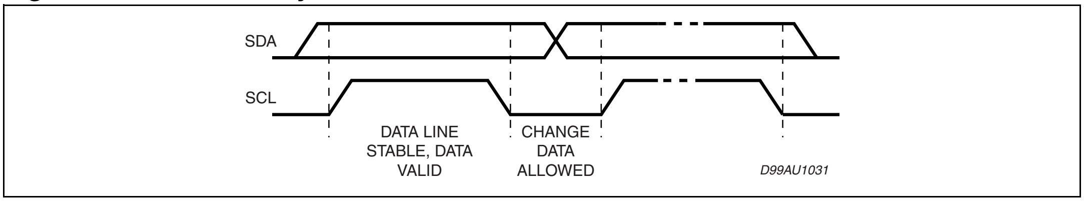


Figure 4. Timing diagram of I^2C BUS

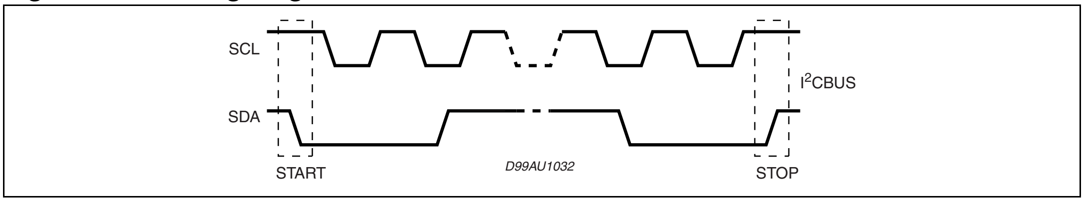
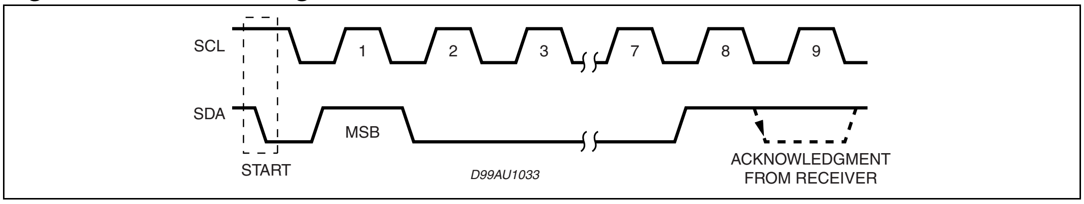


Figure 5. Acknowledge on the I^2C BUS



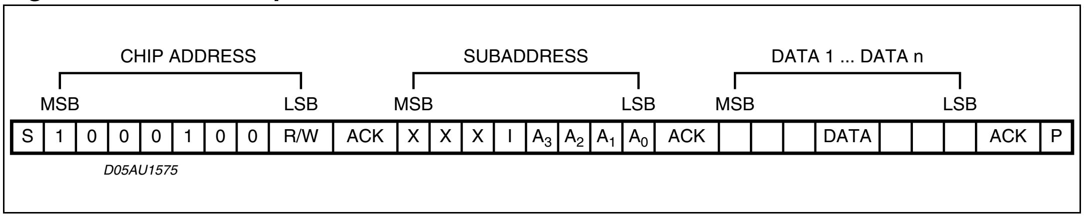
4 Software specification

4.1 Interface protocol

The interface protocol comprises:

- A start condition (s)
- A chip address byte, (the LSB bit determines read/write transmission)
- A subaddress byte.
- A sequence of data (N-bytes + acknowledge)
- A stop condition (P)

Figure 6. Interface protocol



ACK = Acknowledge

S = Start

P = Stop

I = Auto Increment

X = Not used

Max clock speed 500kbits/s

4.2 Auto increment

If bit I in the subaddress byte is set to "1", the auto increment of the subaddress is enabled

Table 5. Subaddress (receive mode)

MSB							LSB	Function
X	X	X	I	A3	A2	A1	A0	
				0	0	0	0	Input selector
				0	0	0	1	Loudness
				0	0	1	0	Volume
				0	0	1	1	Bass, treble
				0	1	0	0	Speaker attenuator LF
				0	1	0	1	Speaker attenuator LR
				0	1	1	0	Speaker attenuator RF
				0	1	1	1	Speaker attenuator RR
				1	0	0	0	Mute

4.3 Transmitted data

Table 6. Send mode

MSB							LSB
X	X	X	X	X	SM	ZM	X

ZM = Zero crossing muted (HIGH active)

SM = Soft mute activated (HIGH active)

X = Not used

The transmitted data is automatically updated after each ACK.

Transmission can be repeated without new chip address.

4.4 Data byte specification

X = not relevant; set to "1" during testing

Table 7. Input selector

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
0		1			0	0	0	not used
0		1			0	0	1	IN 2
0		1			0	1	0	IN 1
0		1			0	1	1	AM mono
0		1			1	0	0	not used
0		1			1	0	1	not used
0		1			1	1	0	not allowed
0		1			1	1	1	not allowed
0		1	0	0				11.25dB gain
0		1	0	1				7.5dB gain
0		1	1	0				3.75dB gain
0		1	1	1				0dB gain
	0							0dB differential input gain (IN3)
	1							-6dB differential input gain (IN3)

For example to select the IN 2 input with a gain of 7.5dB the Data Byte is: X X 1 0 1 0 0 1

Table 8. **Loudness**

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
X	X	X	0	0	0	0	0	0dB
X	X	X	0	0	0	0	1	-1.25dB
X	X	X	0	0	0	1	0	-2.5dB
X	X	X	0	0	0	1	1	-3.75dB
X	X	X	0	0	1	0	0	-5dB
X	X	X	0	0	1	0	1	-6.25dB
X	X	X	0	0	1	1	0	-7.5dB
X	X	X	0	0	1	1	1	-8.75dB
X	X	X	0	1	0	0	0	-10dB
X	X	X	0	1	0	0	1	-11.25dB
X	X	X	0	1	0	1	0	-12.5dB
X	X	X	0	1	0	1	1	-13.75dB
X	X	X	0	1	1	0	0	-15dB
X	X	X	0	1	1	0	1	-16.25dB
X	X	X	0	1	1	1	0	-17.5dB
X	X	X	0	1	1	1	1	-18.75dB
X	X	X	1	D3	D2	D1	D0	Loudness OFF (1)

For example to select -17.5dB attenuation, loudness OFF, the Data Byte is: X X X1 1 1 1 0

NOTE 1: If the loudness is switched OFF, the loudness stage is acting like a volume attenuator with flat frequency response. D0 to D3 determine the attenuation level.

Table 9. **Mute**

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
							1	Soft mute on
						0	1	Soft mute with fast slope ($I = I_{MAX}$)
						1	1	Soft mute with slow slope ($I = I_{MIN}$)
				1				Direct mute
			0		1			Zero crossing mute on
			0		0			Zero crossing mute off (delayed until the next zerocrossing)
			1					Zero crossing mute and pause detector reset
	0	0						160mV ZC Window threshold (WIN = 00)
	0	1						80mV ZC Window threshold (WIN = 01)

Table 9. Mute

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
	1	0						40mV ZC Window threshold (WIN = 10)
	1	1						20mV ZC Window threshold (WIN = 11)
0								Non symmetrical bass cut (note 4)
1								Symmetrical bass cut

An additional direct mute function is included in the speaker attenuators.

Note 4: Bass cut for very low frequencies; should not be used at +16 and +18dB bass boost (DC gain)

Table 10. Speaker attenuators (LF, LR, RF, RR)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
								1.25dB step
X	X	X			0	0	0	0dB
X	X	X			0	0	1	-1.25dB
X	X	X			0	1	0	-2.5dB
X	X	X			0	1	1	-3.75dB
X	X	X			1	0	0	-5dB
X	X	X			1	0	1	-6.25dB
X	X	X			1	1	0	-7.5dB
X	X	X			1	1	1	-8.75dB
								10dB step
X	X	X	0	0				0dB
X	X	X	0	1				-10dB
X	X	X	1	0				-20dB
X	X	X	1	1				-30dB
X	X	X	1	1	1	1	1	Speaker mute

For example an attenuation of 25dB on a selected output is given by: X X X1 0 1 0 0

Table 11. Bass/Treble

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
								Treble step
				0	0	0	0	-14dB
				0	0	0	1	-12dB

Table 11. Bass/Treble (continued)

MSB							LSB	Function
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	
				0	0	1	0	-10dB
				0	0	1	1	-8dB
				0	1	0	0	-6dB
				0	1	0	1	-4dB
				0	1	1	0	-2dB
				0	1	1	1	0dB
				1	1	1	1	0dB
				1	1	1	0	2dB
				1	1	0	1	4dB
				1	1	0	0	6dB
				1	0	1	1	8dB
				1	0	1	0	10dB
				1	0	0	1	12dB
				1	0	0	0	14dB
								Bass steps
0	0	1	0					-10dB
0	0	1	1					-8dB
0	1	0	0					-6dB
0	1	0	1					-4dB
0	1	1	0					-2dB
0	1	1	1					-0dB
1	1	1	1					-0dB
1	1	1	0					2dB
1	1	0	1					4dB
1	1	0	0					6dB
1	0	1	1					8dB
1	0	1	0					10dB
1	0	0	1					12dB
1	0	0	0					14dB
0	0	0	1					146B
0	0	0	0					18dB

For example 12dB Treble and -8dB Bass give the following data byte: 0 0 1 1 1 0 0 1

Table 12. Volume

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
								0.31db fine attenuation steps
						0	0	0db
						0	1	-0.31db
						1	0	-0.62db
						1	1	-0.94db
								1.25db coarse attenuation steps
			0	0	0			0db
			0	0	1			-1.25db
			0	1	0			-2.5db
			0	1	1			-3.75db
			1	0	0			-5db
			1	0	1			-6.25db
			1	1	0			-7.5db
			1	1	1			-8.75db
								10db gain / attenuation steps
0	0	0						20db
0	0	1						10db
0	1	0						0db
0	1	1						-10db
1	0	0						-20db
1	0	1						-30db
1	1	0						-40db
1	1	1						-50db

For example to select -47.81dB Volume the Data Byte is: 1 1 0 1 1 0 0 1

Power on RESET: All Bytes Set to 1 1 1 1 1 1 1 0

NB. Purchase of I^2C Components of STMicrolectronics, conveys a license under the Philips I^2C Patent Rights to use these components in an I^2C system, provided that the system conforms to the I^2C Standard Specifications as defined by Philips.

5 Package information

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label.

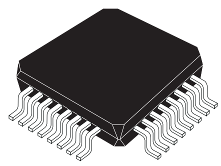
ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Figure 7. LQFP32 Mechanical data & package dimensions

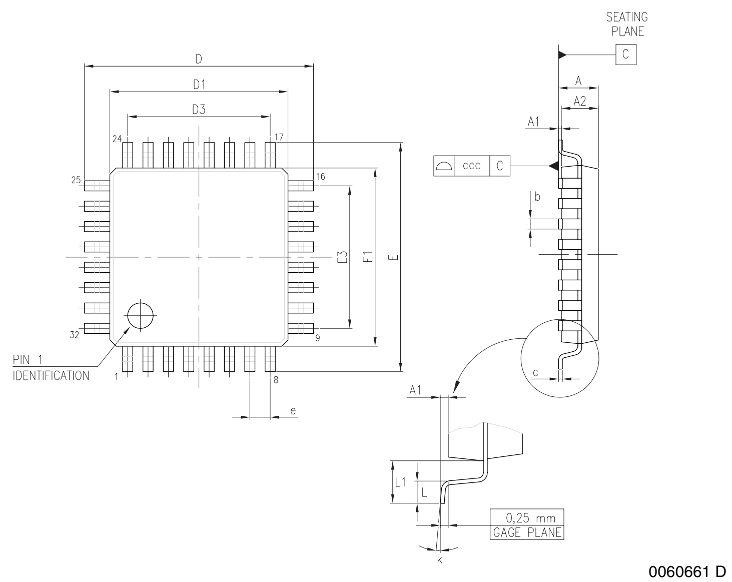
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.600			0.0630
A1	0.050		0.150	0.0020		0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.300	0.370	0.450	0.0118	0.0146	0.0177
c	0.090		0.200	0.0035		0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3		5.600			0.2205	
E	8.800	9.000	9.200	0.3465	0.3543	0.3622
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3		5.600			0.2205	
e		0.800			0.0315	
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1		1.000			0.0394	
K		3.500	7.000		0.1378	0.2756
ccc			0.100			0.0039

OUTLINE AND MECHANICAL DATA

Weight: 0.20gr



LQFP32 (7 x 7 x 1.40mm)



6 Revision history

Table 13. Document revision history

Date	Revision	Changes
24-Jan-2006	1	Initial release.
20-Nov-2006	2	Update package information, layout changes, text modifications.