

INTEGRATED CIRCUITS

DATA SHEET



TDA8043

Satellite Demodulator and Decoder (SDD)

Product specification
Supersedes data of 1997 Nov 07
File under Integrated Circuits, IC02

1998 Feb 13

Satellite Demodulator and Decoder (SDD)

TDA8043

FEATURES

- One-chip Digital Video Broadcasting (DVB) compliant demodulator and concatenated Viterbi/Reed-Solomon decoder with de-interleaver and de-randomizer
- 3.3 V supply voltage (up to 5 V allowed)
- Internal clock divider
- On-chip crystal oscillator
- QPSK/BPSK demodulator:
 - Interpolator to handle variable symbol rates without an external anti-aliasing filter
 - On-chip Automatic Gain Control (AGC) of the analog input I and Q baseband signals or tuner AGC control
 - Two on-chip matched Analog-to-Digital Converters (ADCs; 7 bits)
 - Square-Root Raised-Cosine Nyquist filter with programmable roll-off factor
 - High maximum symbol frequency: 32 Msymbols/s
 - Can be used at low channel Es/No (Symbol energy-to-noise ratio)
 - Internal carrier recovery, clock recovery and AGC loops with programmable loop filters
 - Two carrier recovery loops enabling phase tracking of the incoming symbols
 - Different modulation schemes: Quadrature Phase Shift Keying (QPSK) and Binary-Phase Shift Keying (BPSK)
 - Signal-to-noise ratio (S/N) estimation
 - External indication of demodulator lock.
- Viterbi decoder:
 - Rate $\frac{1}{2}$ convolutional code based
 - Constraint length $K = 7$ with $G_1 = 171_{\text{oct}}$ and $G_2 = 133_{\text{oct}}$
 - Supported puncturing code rates: $\frac{1}{2}$, $\frac{2}{3}$, $\frac{3}{4}$, $\frac{4}{5}$, $\frac{5}{6}$, $\frac{6}{7}$, $\frac{7}{8}$ and $\frac{8}{9}$
 - 4 bits 'soft decision' inputs for both I and Q
 - Truncation length: 144
 - Automatic synchronization to correct puncturing rate and spectral inversion
 - Channel Bit Error Rate (BER) estimation from 10^{-2} to 10^{-8}
 - External indication of Viterbi synchronization lock
 - Differential decoding supported.
- Reed-Solomon (RS) decoder:
 - (204, 188 and $T = 8$) Reed Solomon code
 - Automatic (I²C-bus configurable) synchronization of bytes, transport packets and frames
 - Internal convolutional de-interleaving ($l = 12$; using internal memory)
 - De-randomizer based on Pseudo Random Binary Sequence (PRBS)
 - External indication of RS decoder sync lock
 - External indication of uncorrectable errors (transport error indicator is set)
 - Indication of the number of lost blocks
 - Indication of the number of corrected blocks/bytes.
- I²C-bus interface:
 - I²C-bus interface initializes and monitors the demodulator and Forward Error Correction (FEC) decoder with standby mode; when no I²C-bus is used, default mode is defined
 - 4-bit I/O expander for flexible access to and from the I²C-bus
 - I²C-bus configurable interrupt pin
 - Standby mode for reduced power consumption.
- Package: QFP100
- Boundary scan test.



APPLICATIONS

- Demodulation and FEC for digital satellite TV.

Satellite Demodulator and Decoder (SDD)

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GENERAL DESCRIPTION

This document specifies a DVB compliant demodulator and forward error correction decoder IC for reception of QPSK and BPSK modulated signals for satellite applications.

The TDA8043 can handle variable symbol rates without adapting the analog filters within the tuner. Typical applications for this device are:

- **Single Carrier Per Channel (SCPC):** two or more QPSK or BPSK modulated signals in a single satellite channel (transponder)
- **Multi-Carrier Per Channel (MCPC):** one QPSK or BPSK modulated signal in a single satellite channel (transponder)
- **Simul-cast:** QPSK or BPSK modulated signal together with a Frequency Modulated (FM) signal in a single satellite channel.

The SDD requires the analog in-phase (I) and quadrature (Q) components as an input and provides 8-bit wide MPEG2 transport packet data at the output. The outputs of the SDD can be directly connected to a descrambler (SAA7206) or a demultiplexer (SAA7205).

For evaluation purposes, the output can also be used to monitor internal data, for example I/Q after demodulation.

The SDD requires a single clock frequency which is independent of the received symbol rate, providing the clock frequency is slightly higher than twice the highest symbol frequency.

All loops to recover the data from the received symbols are internal. No external loop components are required. Loop parameters for the clock, carrier recovery and AGC can be controlled via the I²C-bus.

The Forward Error Correction (FEC) unit has a built-in state machine to achieve lock without knowing the system parameters (depuncturing rate, spectral inversion, etc.). Once lock is achieved, all necessary parameters can be read via the I²C-bus. By programming these parameters in advance lock can be achieved more quickly.

The SDD can be controlled and monitored via the I²C-bus. An I²C-bus default mode is specified which makes it possible to use the device by software control. A 4-bit bidirectional I/O expander and an interrupt line are available. By sending an interrupt signal, the SDD can inform the microcontroller of its internal status (lock).

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8043H	QFP100	plastic quad flat package; 100 leads (lead length 1.95 mm); body 14 × 20 × 2.8 mm	SOT317-2

Satellite Demodulator and Decoder (SDD)

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QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V _{DDA}	analog supply voltage		3.0	3.3	3.6	V
V _{DDD}	digital supply voltage		3.0	3.3	3.6	V
I _{DD(tot)}	total supply current	V _{DDD} = 3.3 V; note 1	–	390	–	mA
f _{clk}	clock frequency		–	–	65	MHz
r _s	symbol rate	note 2	0.5	–	32	Msymbols/s
α	nyquist roll-off (selectable)		–	35 or 50	–	%
IL	implementation loss	note 3	–	0.3	–	dB
S/N	signal-to-noise ratio for locking the SDD	QPSK mode; note 1	2	–	–	dB
P _{tot}	total power dissipation	T _{amb} = 70°C; note 1	–	1285	1650	mW
T _{stg}	IC storage temperature		–55	–	+150	°C
T _{amb}	operating ambient temperature		0	–	70	°C
T _j	operating junction temperature	T _{amb} = 70 °C	–	–	125	°C

Notes

- These values are specified for a symbol rate of 27.5 Msymbols/s, a puncturing rate of $\frac{3}{4}$ and a clock frequency of 65 MHz.
- A range from 3 to 32 Msymbols/s can be achieved with one SAW filter. By using an internal clock divider and reducing the external SAW filter bandwidth, symbol rates down to 0.5 Msymbols/s can be achieved by using a 65 MHz crystal clock.
- This data was measured in a laboratory environment at a symbol rate of 27.5 Msymbols/s, a clock frequency of 65 MHz, a signal-to-noise ratio of 4.5 dB and including a tuner.

PINNING

SYMBOL	PIN	I/O	DESCRIPTION
I2	1	I	digital I-input bit 2 (ADC bypass); note 1
I3	2	I	digital I-input bit 3 (ADC bypass); note 1
V _{SSD1}	3	–	digital ground 1
n.c.	4	–	not connected
n.c.	5	–	not connected
I4	6	I	digital I-input bit 4 (ADC bypass); note 1
I5	7	I	digital I-input bit 5 (ADC bypass); note 1
I6	8	I	digital I-input bit 6 (ADC bypass: MSB); note 1
Q0	9	I	digital Q-input bit 0 (ADC bypass: LSB); note 1
V _{DDD1}	10	–	digital supply voltage 1
Q1	11	I	digital Q-input bit 1 (ADC bypass); note 1
Q2	12	I	digital Q-input bit 2 (ADC bypass); note 1
Q3	13	I	digital Q-input bit 3 (ADC bypass); note 1
Q4	14	I	digital Q-input bit 4 (ADC bypass); note 1
V _{SSD2}	15	–	digital ground 2
Q5	16	I	digital Q-input bit 5 (ADC bypass); note 1
Q6	17	I	digital Q-input bit 6 (ADC bypass: MSB); note 1

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SYMBOL	PIN	I/O	DESCRIPTION
V _{SSD3}	18	–	digital ground 3
V _{DD2}	19	–	digital supply voltage 2
PRESET	20	I	set device into default mode
P3	21	I/O	quasi-bidirectional I/O port (bit 3)
P2	22	I/O	quasi-bidirectional I/O port (bit 2)
P1	23	I/O	quasi-bidirectional I/O port (bit 1)
P0	24	I/O	quasi-bidirectional I/O port (bit 0)
V _{DD3}	25	–	digital supply voltage 3
n.c.	26	–	not connected
n.c.	27	–	not connected
PDOCLK	28	O	output clock for transport stream bytes
PDO0	29	O	parallel data output (bit 0)
PDO1	30	O	parallel data output (bit 1)
PDO2	31	O	parallel data output (bit 2)
V _{SS4}	32	–	digital ground 4
PDO3	33	O	parallel data output (bit 3)
PDO4	34	O	parallel data output (bit 4)
PDO5	35	O	parallel data output (bit 5)
n.c.	36	–	not connected
n.c.	37	–	not connected
PDO6	38	O	parallel data output (bit 6)
n.c.	39	–	not connected
V _{DD4}	40	–	digital supply voltage 4
V _{DD5}	41	–	digital supply voltage 5
V _{SS5}	42	–	digital ground 5
V _{DD6}	43	–	digital supply voltage 6
V _{DD7}	44	–	digital supply voltage 7
PDO7	45	O	parallel data output (bit 7)
n.c.	46	–	not connected
n.c.	47	–	not connected
PDOERR	48	O	transport error indicator
PDOVAL	49	O	data valid indicator
PDOSYNC	50	O	transport packet synchronization signal
V _{SS6}	51	–	digital ground 6
SCL	52	I	serial clock of I ² C-bus; note 1
SDA	53	I/O	serial data of I ² C-bus; note 1
INT	54	O	interrupt output (active LOW); note 1
A0	55	I	I ² C hardware address; note 1
RSLOCK	56	O	Reed-Solomon lock indicator
VLOCK	57	O	Viterbi lock indicator
DLOCK	58	O	demodulator lock indicator
V _{DD8}	59	–	digital supply voltage 8
V _{DD9}	60	–	digital supply voltage 9
TEST	61	I	test pin (normally connected to ground); note 1

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SYMBOL	PIN	I/O	DESCRIPTION
TRST	62	I	BST optional asynchronous reset (normally connected to ground); note 1
TCK	63	I	BST dedicated test clock (normally connected to ground); note 1
n.c.	64	–	not connected
n.c.	65	–	not connected
V _{DDD10}	66	–	digital supply voltage 10
V _{SSD7}	67	–	digital ground 7
V _{SSD8}	68	–	digital ground 8
TMS	69	I	BST input control signal (normally connected to ground); note 1
TDO	70	O	BST serial test data out
TDI	71	I	BST serial test data in (normally connected to ground); note 1
V _{DDD11}	72	–	digital supply voltage 11
V _{SSD9}	73	–	digital ground 9
V _{SSD(AD)}	74	–	digital ground for ADC
V _{DDD(AD)}	75	–	digital supply for ADC
V _{ref(B)}	76	O	bottom reference voltage for ADC
V _{SSA1}	77	–	analog ground 1
QA	78	I	analog input Q
V _{ref(Q)}	79	O	AGC decoupling for Q path
IA	80	I	analog input I
V _{SSA2}	81	–	analog ground 2
V _{ref(I)}	82	O	AGC decoupling for I path
V _{DDA}	83	–	analog supply voltage
V _{DDXTAL}	84	–	supply voltage for crystal oscillator
XTALI	85	I	crystal oscillator input
XTALO	86	O	crystal oscillator output
V _{SSXTAL}	87	–	ground for crystal oscillator
V _{DDD12}	88	–	digital supply voltage 12
V _{DDD13}	89	–	digital supply voltage 13
V _{SSD10}	90	–	digital ground 10
n.c.	91	–	not connected
n.c.	92	–	not connected
n.c.	93	–	not connected
V _{AGC}	94	O	AGC output voltage; note 1
n.c.	95	–	not connected
V _{DDD14}	96	–	digital supply voltage 14
V _{DDD15}	97	–	digital supply voltage 15
OUTSD	98	O	general purpose sigma-delta output
I0	99	I	digital I-input bit 0 (ADC bypass: LSB); note 1
I1	100	I	digital I-input bit 1 (ADC bypass); note 1

Note

1. This pin is 5 V tolerant.

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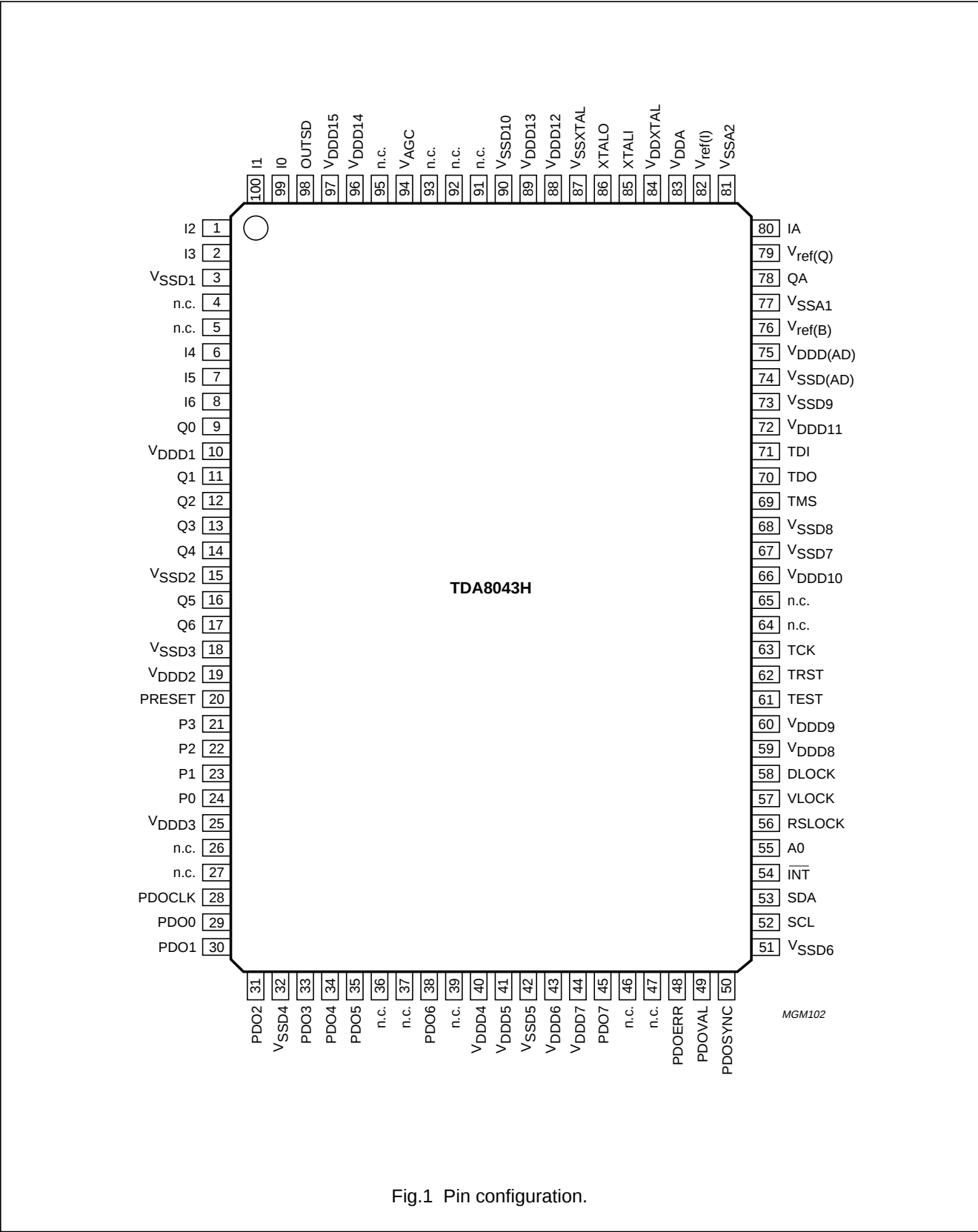


Fig.1 Pin configuration.

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APPLICATION INFORMATION

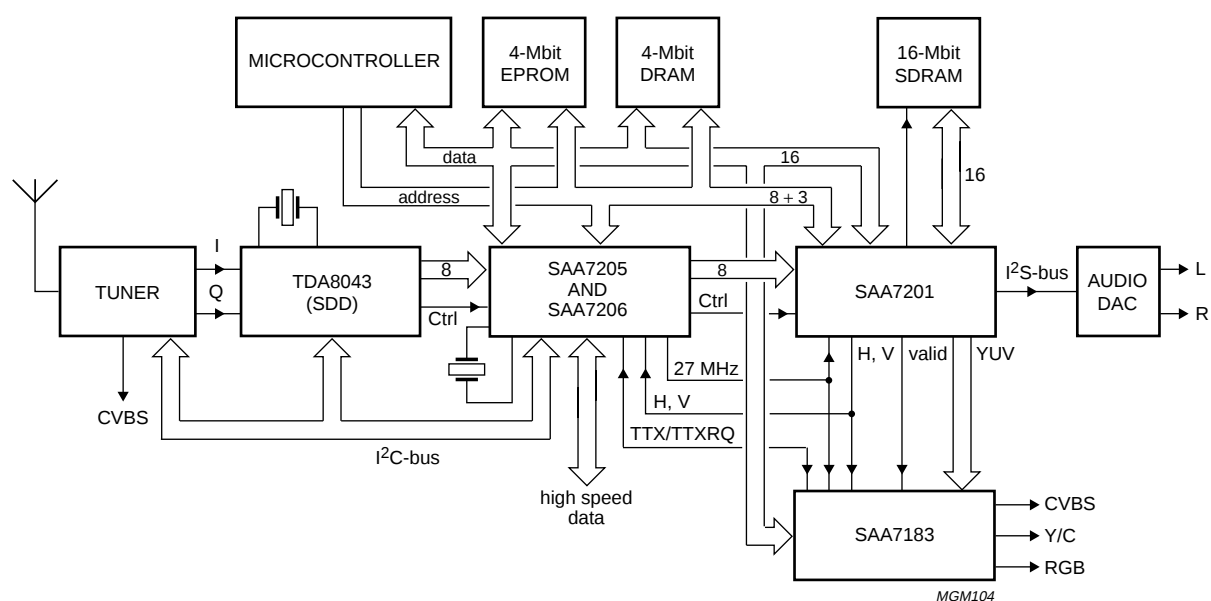
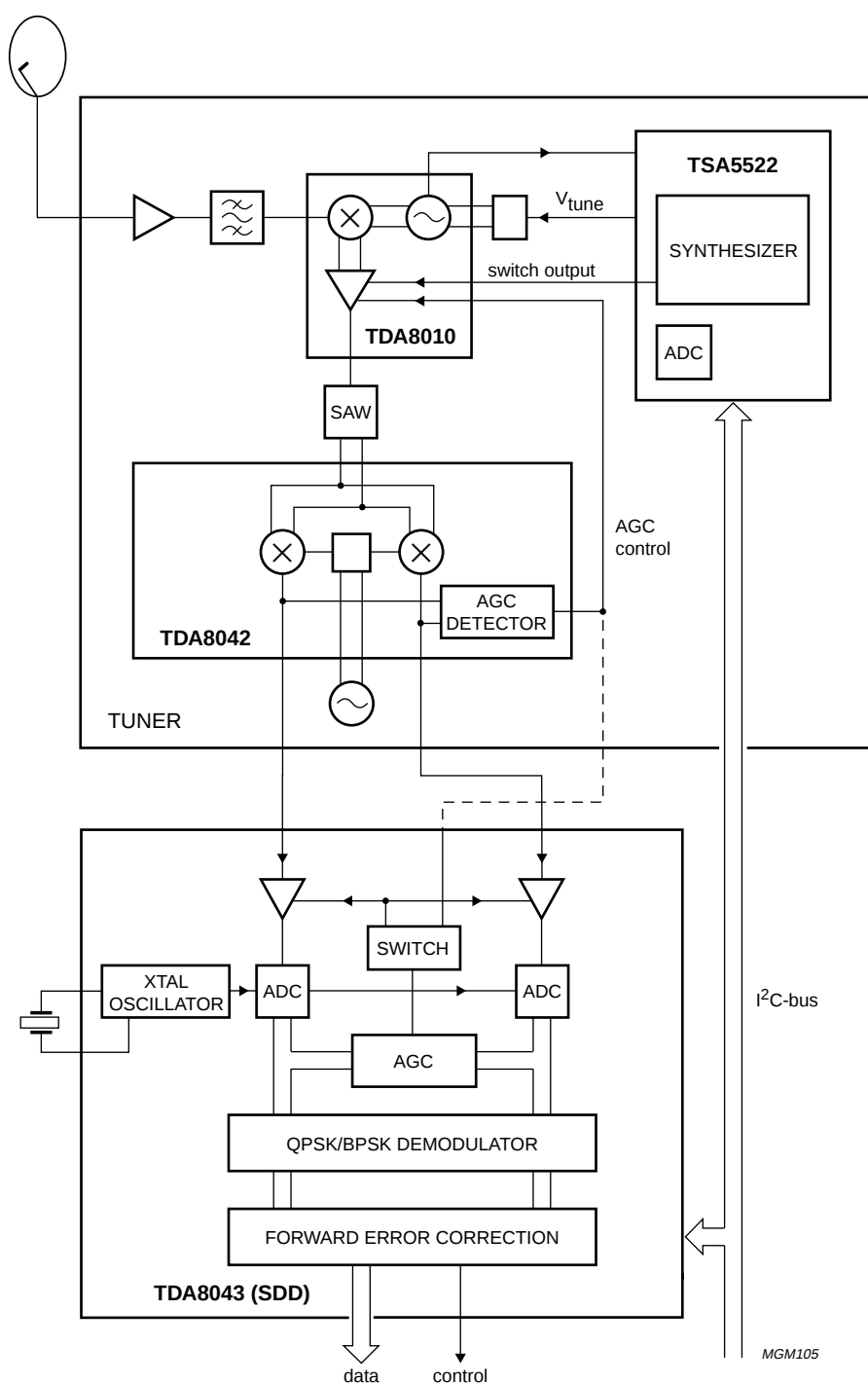


Fig.2 Satellite set-top box concept.

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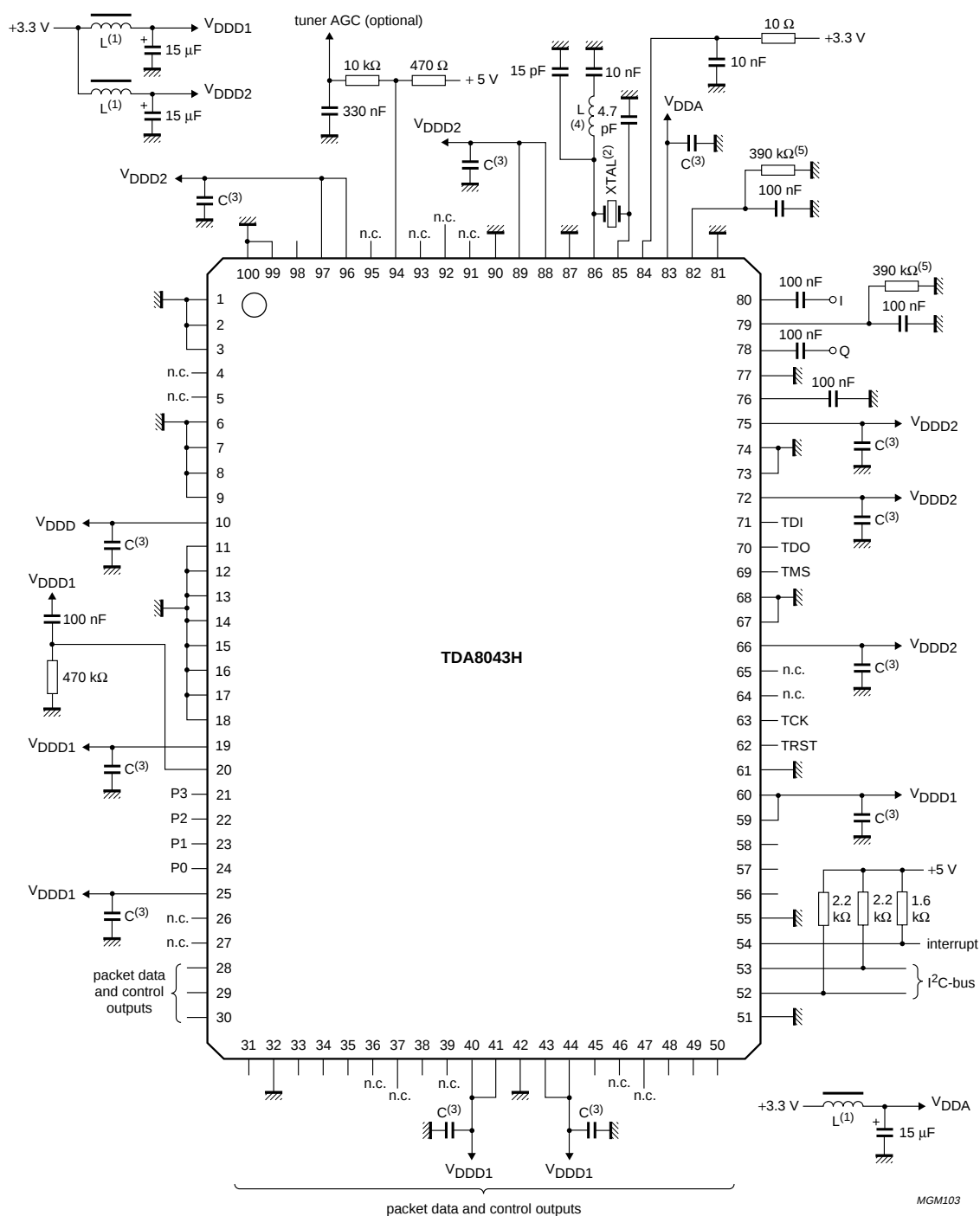


Note: Control for external AGC is also available using the internal AGC sigma-delta converter (indicated with the dashed line).

Fig.3 Application of satellite demodulator and decoder including tuner.

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(1) B = SMD bead type CBD8.9/3/3 Grade 4S2.

(2) XTAL = 65 MHz, 3rd overtone.

(3) C = 6.8 nF, SMD.

(4) L = 560 nH, Taiyo Yuden LAL02.

(5) Value specified for a 65 MHz clock. For other clock frequencies, refer to "Application note AN96108".

If possible, connect 'n.c.' pins to ground to ease power dissipation.

TRST, TCK, TMS, and TDI pins can be connected to ground if they are not used.

Fig.4 Application diagram.

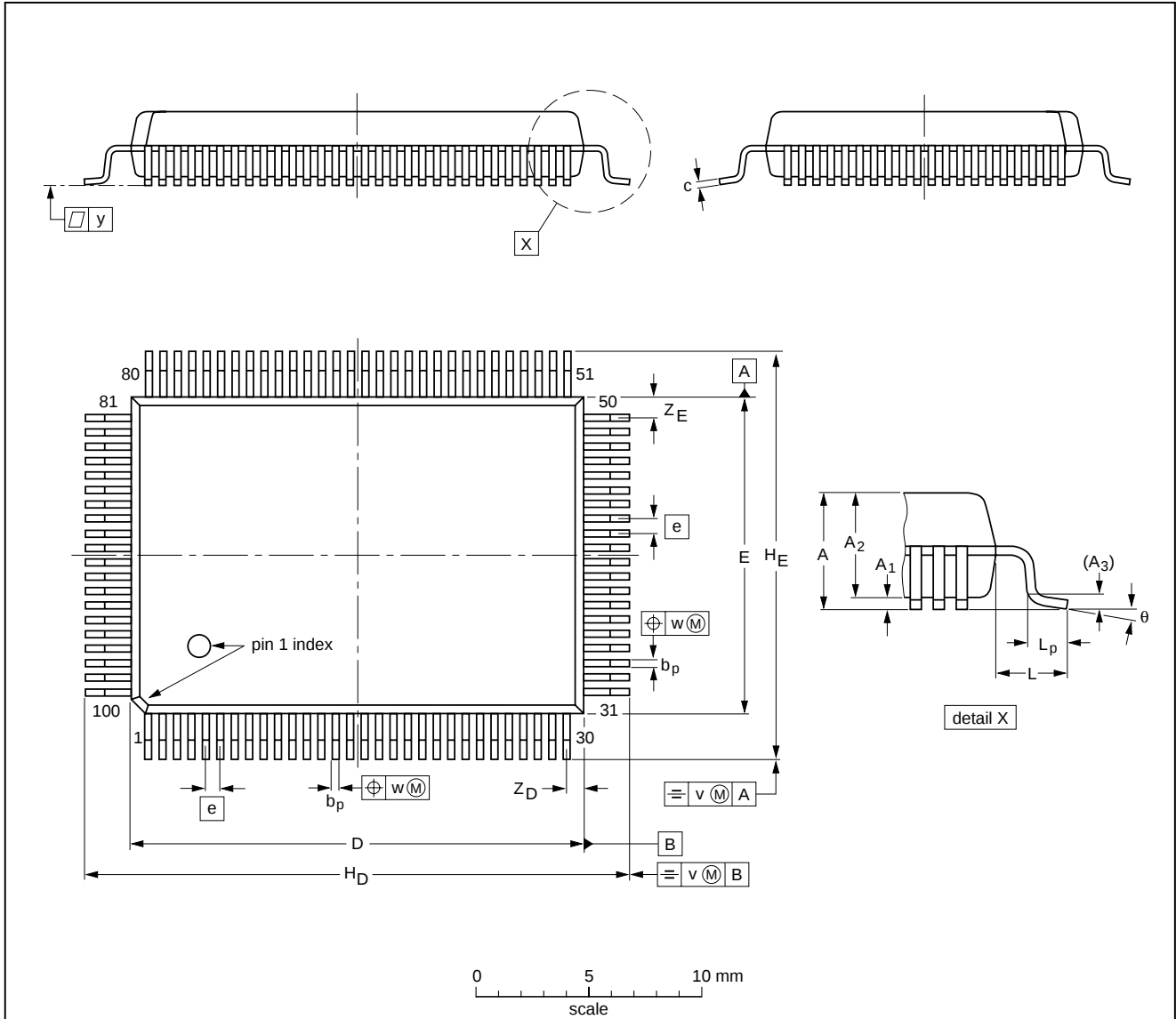
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PACKAGE OUTLINE

QFP100: plastic quad flat package; 100 leads (lead length 1.95 mm); body 14 x 20 x 2.8 mm

SOT317-2



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _D	H _E	L	L _p	v	w	y	Z _D ⁽¹⁾	Z _E ⁽¹⁾	θ
mm	3.20	0.25 0.05	2.90 2.65	0.25	0.40 0.25	0.25 0.14	20.1 19.9	14.1 13.9	0.65	24.2 23.6	18.2 17.6	1.95	1.0 0.6	0.2	0.15	0.1	0.8 0.4	1.0 0.6	7° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT317-2						95-02-04- 97-08-01

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SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our “IC Package Databook” (order code 9398 652 90011).

Reflow soldering

Reflow soldering techniques are suitable for all QFP packages.

The choice of heating method may be influenced by larger plastic QFP packages (44 leads, or more). If infrared or vapour phase heating is used and the large packages are not absolutely dry (less than 0.1% moisture content by weight), vaporization of the small amount of moisture in them can cause cracking of the plastic body. For more information, refer to the Drypack chapter in our “Quality Reference Handbook” (order code 9397 750 00192).

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 50 and 300 seconds depending on heating method. Typical reflow peak temperatures range from 215 to 250 °C.

Wave soldering

Wave soldering is **not** recommended for QFP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering cannot be avoided, for QFP packages with a pitch (e) larger than 0.5 mm, the following conditions must be observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The footprint must be at an angle of 45° to the board direction and must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

CAUTION
Wave soldering is NOT applicable for all QFP packages with a pitch (e) equal or less than 0.5 mm.

Satellite Demodulator and Decoder (SDD)

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DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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NOTES

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NOTES

Philips Semiconductors – a worldwide company

Argentina: see South America

Australia: 34 Waterloo Road, NORTH RYDE, NSW 2113,
Tel. +61 2 9805 4455, Fax. +61 2 9805 4466

Austria: Computerstr. 6, A-1101 WIEN, P.O. Box 213, Tel. +43 160 1010,
Fax. +43 160 101 1210

Belarus: Hotel Minsk Business Center, Bld. 3, r. 1211, Volodarski Str. 6,
220050 MINSK, Tel. +375 172 200 733, Fax. +375 172 200 773

Belgium: see The Netherlands

Brazil: see South America

Bulgaria: Philips Bulgaria Ltd., Energoproject, 15th floor,
51 James Bourchier Blvd., 1407 SOFIA,
Tel. +359 2 689 211, Fax. +359 2 689 102

Canada: PHILIPS SEMICONDUCTORS/COMPONENTS,
Tel. +1 800 234 7381

China/Hong Kong: 501 Hong Kong Industrial Technology Centre,
72 Tat Chee Avenue, Kowloon Tong, HONG KONG,
Tel. +852 2319 7888, Fax. +852 2319 7700

Colombia: see South America

Czech Republic: see Austria

Denmark: Prags Boulevard 80, PB 1919, DK-2300 COPENHAGEN S,
Tel. +45 32 88 2636, Fax. +45 31 57 0044

Finland: Sinikalliontie 3, FIN-02630 ESPOO,
Tel. +358 9 615800, Fax. +358 9 61580920

France: 51 Rue Carnot, BP317, 92156 SURESNES Cedex,
Tel. +33 1 40 99 6161, Fax. +33 1 40 99 6427

Germany: Hammerbrookstraße 69, D-20097 HAMBURG,
Tel. +49 40 23 53 60, Fax. +49 40 23 536 300

Greece: No. 15, 25th March Street, GR 17778 TAVROS/ATHENS,
Tel. +30 1 4894 339/239, Fax. +30 1 4814 240

Hungary: see Austria

India: Philips INDIA Ltd, Band Box Building, 2nd floor,
254-D, Dr. Annie Besant Road, Worli, MUMBAI 400 025,
Tel. +91 22 493 8541, Fax. +91 22 493 0966

Indonesia: see Singapore

Ireland: Newstead, Clonskeagh, DUBLIN 14,
Tel. +353 1 7640 000, Fax. +353 1 7640 200

Israel: RAPAC Electronics, 7 Kehilat Saloniki St, PO Box 18053,
TEL AVIV 61180, Tel. +972 3 645 0444, Fax. +972 3 649 1007

Italy: PHILIPS SEMICONDUCTORS, Piazza IV Novembre 3,
20124 MILANO, Tel. +39 2 6752 2531, Fax. +39 2 6752 2557

Japan: Philips Bldg 13-37, Kohnan 2-chome, Minato-ku, TOKYO 108,
Tel. +81 3 3740 5130, Fax. +81 3 3740 5077

Korea: Philips House, 260-199 Itaewon-dong, Yongsan-ku, SEOUL,
Tel. +82 2 709 1412, Fax. +82 2 709 1415

Malaysia: No. 76 Jalan Universiti, 46200 PETALING JAYA, SELANGOR,
Tel. +60 3 750 5214, Fax. +60 3 757 4880

Mexico: 5900 Gateway East, Suite 200, EL PASO, TEXAS 79905,
Tel. +9-5 800 234 7381

Middle East: see Italy

Netherlands: Postbus 90050, 5600 PB EINDHOVEN, Bldg. VB,
Tel. +31 40 27 82785, Fax. +31 40 27 88399

New Zealand: 2 Wagener Place, C.P.O. Box 1041, AUCKLAND,
Tel. +64 9 849 4160, Fax. +64 9 849 7811

Norway: Box 1, Manglerud 0612, OSLO,
Tel. +47 22 74 8000, Fax. +47 22 74 8341

Philippines: Philips Semiconductors Philippines Inc.,
106 Valero St. Salcedo Village, P.O. Box 2108 MCC, MAKATI,
Metro MANILA, Tel. +63 2 816 6380, Fax. +63 2 817 3474

Poland: Ul. Lukiska 10, PL 04-123 WARSZAWA,
Tel. +48 22 612 2831, Fax. +48 22 612 2327

Portugal: see Spain

Romania: see Italy

Russia: Philips Russia, Ul. Usatcheva 35A, 119048 MOSCOW,
Tel. +7 095 755 6918, Fax. +7 095 755 6919

Singapore: Lorong 1, Toa Payoh, SINGAPORE 1231,
Tel. +65 350 2538, Fax. +65 251 6500

Slovakia: see Austria

Slovenia: see Italy

South Africa: S.A. PHILIPS Pty Ltd., 195-215 Main Road Martindale,
2092 JOHANNESBURG, P.O. Box 7430 Johannesburg 2000,
Tel. +27 11 470 5911, Fax. +27 11 470 5494

South America: Al. Vicente Pinzon, 173, 6th floor,
04547-130 SÃO PAULO, SP, Brazil,
Tel. +55 11 821 2333, Fax. +55 11 821 2382

Spain: Balmes 22, 08007 BARCELONA,
Tel. +34 3 301 6312, Fax. +34 3 301 4107

Sweden: Kottbygatan 7, Akalla, S-16485 STOCKHOLM,
Tel. +46 8 632 2000, Fax. +46 8 632 2745

Switzerland: Allmendstrasse 140, CH-8027 ZÜRICH,
Tel. +41 1 488 2686, Fax. +41 1 488 3263

Taiwan: Philips Semiconductors, 6F, No. 96, Chien Kuo N. Rd., Sec. 1,
TAIPEI, Taiwan Tel. +886 2 2134 2865, Fax. +886 2 2134 2874

Thailand: PHILIPS ELECTRONICS (THAILAND) Ltd.,
209/2 Sanpavuth-Bangna Road Prakanong, BANGKOK 10260,
Tel. +66 2 745 4090, Fax. +66 2 398 0793

Turkey: Talatpasa Cad. No. 5, 80640 GÜLTEPE/ISTANBUL,
Tel. +90 212 279 2770, Fax. +90 212 282 6707

Ukraine: PHILIPS UKRAINE, 4 Patrice Lumumba str., Building B, Floor 7,
252042 KIEV, Tel. +380 44 264 2776, Fax. +380 44 268 0461

United Kingdom: Philips Semiconductors Ltd., 276 Bath Road, Hayes,
MIDDLESEX UB3 5BX, Tel. +44 181 730 5000, Fax. +44 181 754 8421

United States: 811 East Arques Avenue, SUNNYVALE, CA 94088-3409,
Tel. +1 800 234 7381

Uruguay: see South America

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