



# TDE1708DFT

## Intelligent power switch

### Features

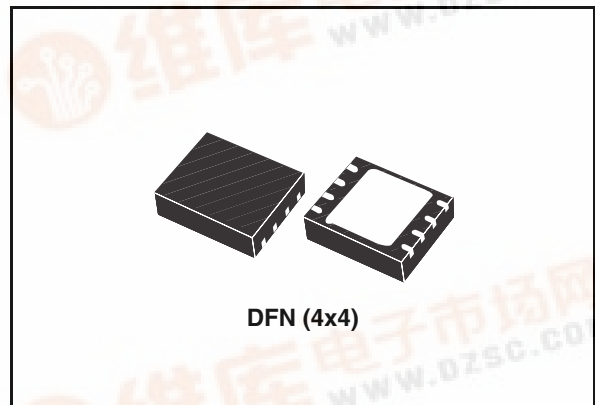
- Low side or high side switch configuration
- 6V to 48V supply voltage range
- Overload and short circuit protections
- Internal voltage clamping
- Supply and output reversal protection
- Thermal shutdown
- GND and vs open wire protection
- Adjustable delay at switch on
- Indicator status led driver
- +5V regulated aux. voltage
- High burst immunity

### Description

The TDE1708DFT is an Integrated Power Switch with up to 48V Power supply capability. Two output configurations are possible:

- Load to Gnd. (High Side Mode)
- Load to VS (Low side Mode)

Especially dedicated to proximity detectors, its internal +5V supply can be used to supply external circuits (See also AN495).



A signal is internally generated to block the In signal, and prevent activation of the output switch, as long as an abnormal condition is detected. The power-on transition, as well as the chip over temperature and the output overcurrent, concur to the generation of such signal. A minimum delay of 25ms (Typ.value) is added to the trailing edge of such signal to ensure that a stable normal situation is present when the signal disappears. The delay (of the disappearance of the block signal; no delay at its on set) can be further increased connecting a capacitor between pin3 and ground. It can drive resistive or inductive loads.

### Order codes

Part number	Temp range, °C	Package	Packing
TDE1708DFT	-25°C to +85°C	DFN(4x4)	Tape and reel

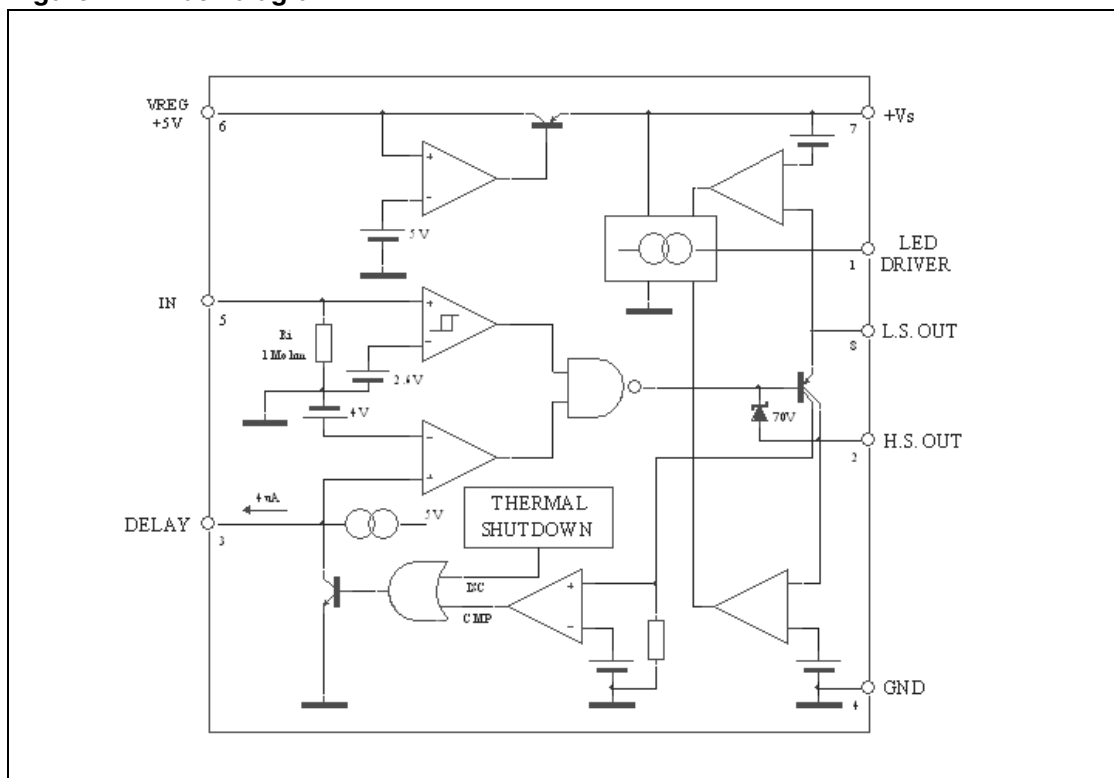
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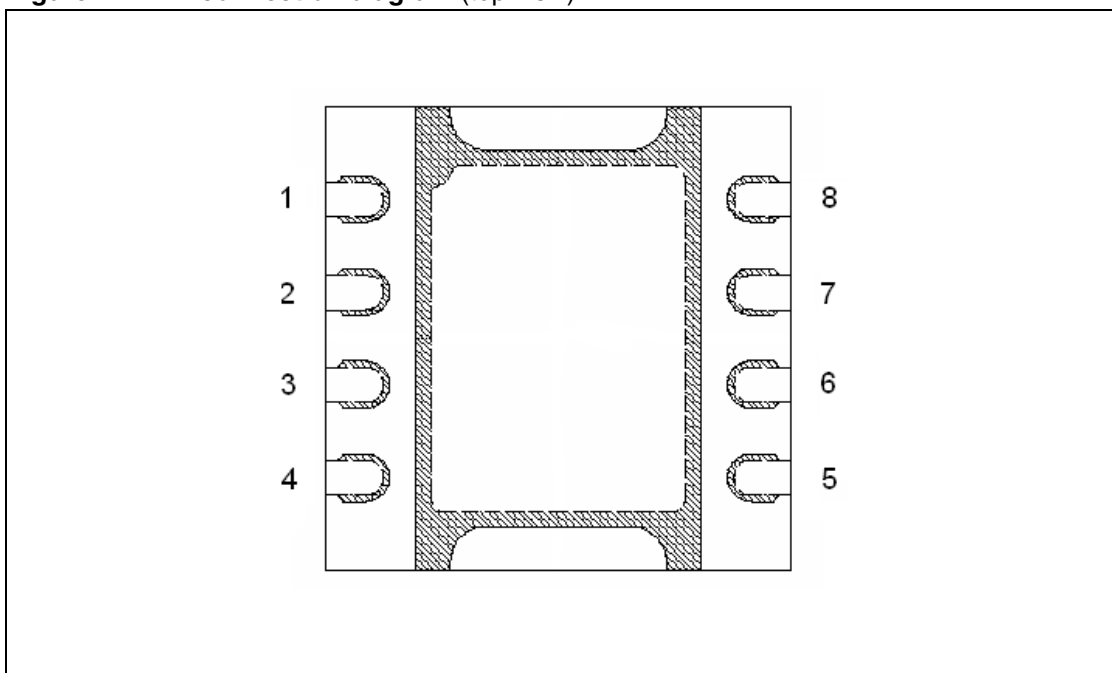
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# 1 Block and pin connection diagrams

Figure 1. Block diagram



**Figure 2. Pin connection diagram (top view)****Table 1. Pin functions**

Pin N°	Function
1	Led driver
2	High side output
3	Delay capacitance source
4	Ground
5	Input
6	Reg. voltage source
7	Supply voltage
8	Low side output

*Note:* Lead frame can be connected to ground.

## 2 Electrical specifications

### 2.1 Thermal data

**Table 2. Thermal data**

Symbol	Description	Value	Unit
$R_{thJA}$	Thermal resistance junction-ambient	Max. 32 <sup>(1)</sup>	°C/W
$R_{thJC}$	Thermal resistance junction-case	Max. 1.2	°C/W

1. Soldered to a 4 layer board with 4 vias in the pad.

### 2.2 Absolute maximum ratings

**Table 3. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_S$	Supply voltage	50	V
$V_S$	Supply reverse voltage	50	V
$I_o$	Output current	internally limited	A
$V_{reg}$	Regulated voltage pin	0 to 7	V
$V_{delay}$	Delay cap. source pin	0 to 5	V
$V_o$	Output diff. voltage	55	V
$V_i$	Input voltage	-10 to 50	V
$T_J$	Junction operating temperature	Internally limited	°C
$T_{stg}$	Storage temperature range	-55 to 150	°C
$P_{tot}$	Power dissipation	internally limited	mW
$E_i$	Energy inductive load	100	mJ

## 2.3 Electrical characteristics

**Table 4. Electrical characteristics**

( $V_S = 24V$  ;  $T_J = -25$  to  $+85^\circ C$  unless otherwise specified).

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$V_S$	Supply voltage		6		48	V
$I_{SR}$	Supply reverse current	$V_{SR} = -48V$			1.5	mA
$I_q$	Quiescent current	$I_{reg} = I_{led} = 0$ ; $V_i < 2V$ ; $V_S = 6$ to $48V$			1.5	mA
$I_o$	Output current	$V_S = 6V$ to $48V$			250	mA
$V_{sat}$	Output voltage drop	$I_o = 200mA$		1	1.5	V
$I_{SCLS}$	Short circuit current in Low side configuration		0.3	0.4	0.6	A
$I_{SCHS}$	Short circuit current in High side configuration		0.25	0.3	0.40	A
$V_{cl}$	Internal voltage clamp	$I_{CL} = 10mA$	55		70	V
$I_{olk}$	Output leakage	(Pin 2) $V_i < 2V$ ; $V_o = 0$ to $V_S$ (Pin 8)		100	300 100	$\mu A$ $\mu A$
$V_{ith}$	Input voltage threshold		2		3	V
$V_{ihis}$	Input threshold hysteresis			300		mV
$I_{lk}$	Input current	$V_i = 5V$		2	5	$\mu A$
$V_{reg}$	Regulated output voltage	$I_{reg} < 5mA$	4.5	5	5.5	V
$I_{scr}$	Short circuit regulated		6	30	50	mA
$I_{reg}$	Output regulator current	$V_S = 35V$ $V_S = 48V$			6 4	mA mA
$I_{old}$	Current source sink led driver	Output ON ( $\pm$ )	2	3	4	mA
$V_{old}$	Voltage drop led driver	$I_{os} = 2mA$ ( $\pm$ )		1.2	1.6	V
$I_{oldk}$	LED driver (off) Leak.	$V_i < 2V$ ; $R_L < 1K\Omega$			10	$\mu A$
$I_{dch}$	Del. cap. charge current	$T_J = 25^\circ C$	2	4	6	$\mu A$
$V_{dth}$	Delay voltage trigger			4		V
$T_{TSD}$	Thermal shutdown temperature			180		$^\circ C$

## 2.4 Dynamic information

**Table 5. Dynamic information**  
( $V_S = 24V$  ;  $T_J = 25^\circ C$  ;  $R_L = 48\Omega$ ).

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$t_{on}$	Propagation turn on time	$V_i = 0$ to 5V		15		$\mu s$
$t_{off}$	Propagation turn off time			15		$\mu s$
$t_{don}$	Delayed turn on time / nF delay capacitor		0.65	1	2	ms
$t_{d\ min}$	Minimum delayed $t_{on}$ Delay capacitor = 0			25		$\mu s$

### 3 Application information

The LED driver tells the output status. It can source or sink current ( $I_{old\ typ} = 3mA$ ), according to the output configuration chosen. The thresholds, represented by the output comparator in the Block Diagram, are set at about 1.5V - 2V.

For instance, in the High Side Load case of the Application Circuit, when the voltage on pin 8 (the output) differs from  $V_{CC}$  less than 1.5V, the output is sensed in "OFF" state and the LED driver is disabled.

If instead pin 8 differs from  $V_{CC}$  more than 3V (the output comparator threshold value plus the drop voltage on the LED), then the output is sensed "ON" and the driver will force the current on the LED.

Figure 3. Low side driver topology

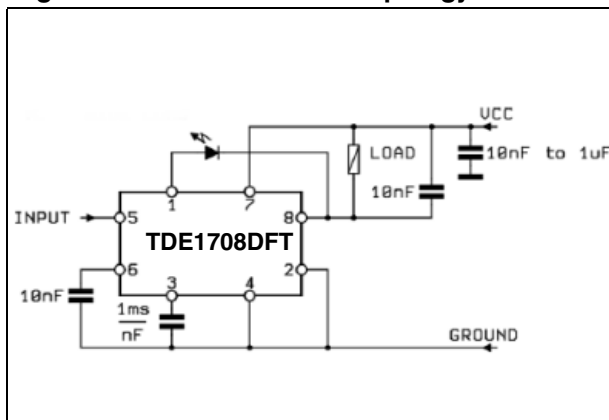
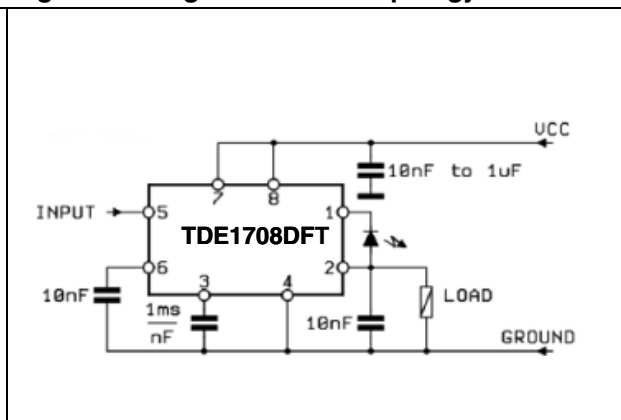


Figure 4. High side driver topology





### 3.1 Adjustable input hysteresis circuit

The TDE1708DFT is a device realized in bipolar technology and therefore it has the usual problems of temperature compensation that such technology involves; despite all it maintains an input dynamics within 1V over industrial temperatures range.

In all input voltage range it will guarantee a high impedance of  $1\text{M}\Omega$  determining an input current about  $2\mu\text{A}$ .

Exploiting this input high impedance is possible connects a sensor directly on it and bypass the obstacle of active signal conditioning circuit using a voltage firm point as ground of sensor, the delay capacitor, connected on the pin 3, as low pass filter and capacitor on Vreg pin to minimize the noise on it and protect for errors the low-voltage internal circuits, according AN495.

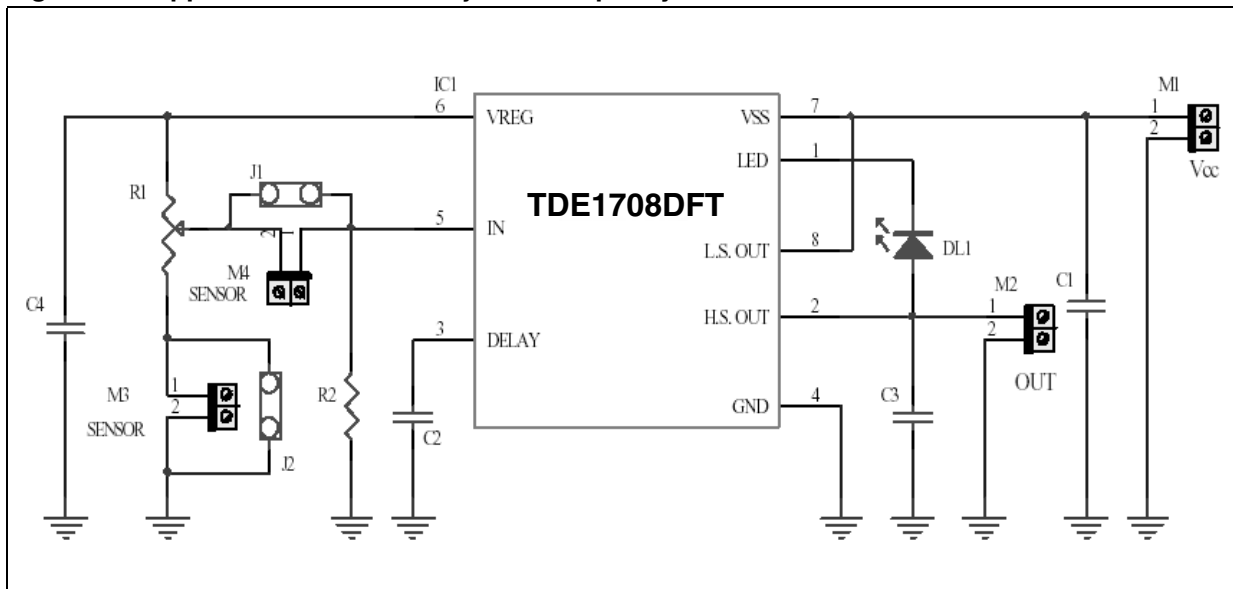
In *Figure 5*, the input external network is optimized for accepting both a sensor with ground connected to the body and a sensor with independent ground.

In order to ground the body of the sensor, J1 has to be shorted, while J2 opened and connect the sensor on M3; in case of independent ground J1 must be opened, J2 shorted and the sensor connected on M4.

DL1 indicate commutation status of the device output and C3 realize a simple output filtering in case is used an inductive load. With C2 about  $10\text{nF}$  we obtain a good filtering and immunity from input voltage noise. C4 is  $4,7\text{nF}$  according AN495.

R2 is an optional resistor plugged only when the sensor needs to adapt its impedance with the input impedance of device.

**Figure 5. Application circuit for adjustable input hysteresis**



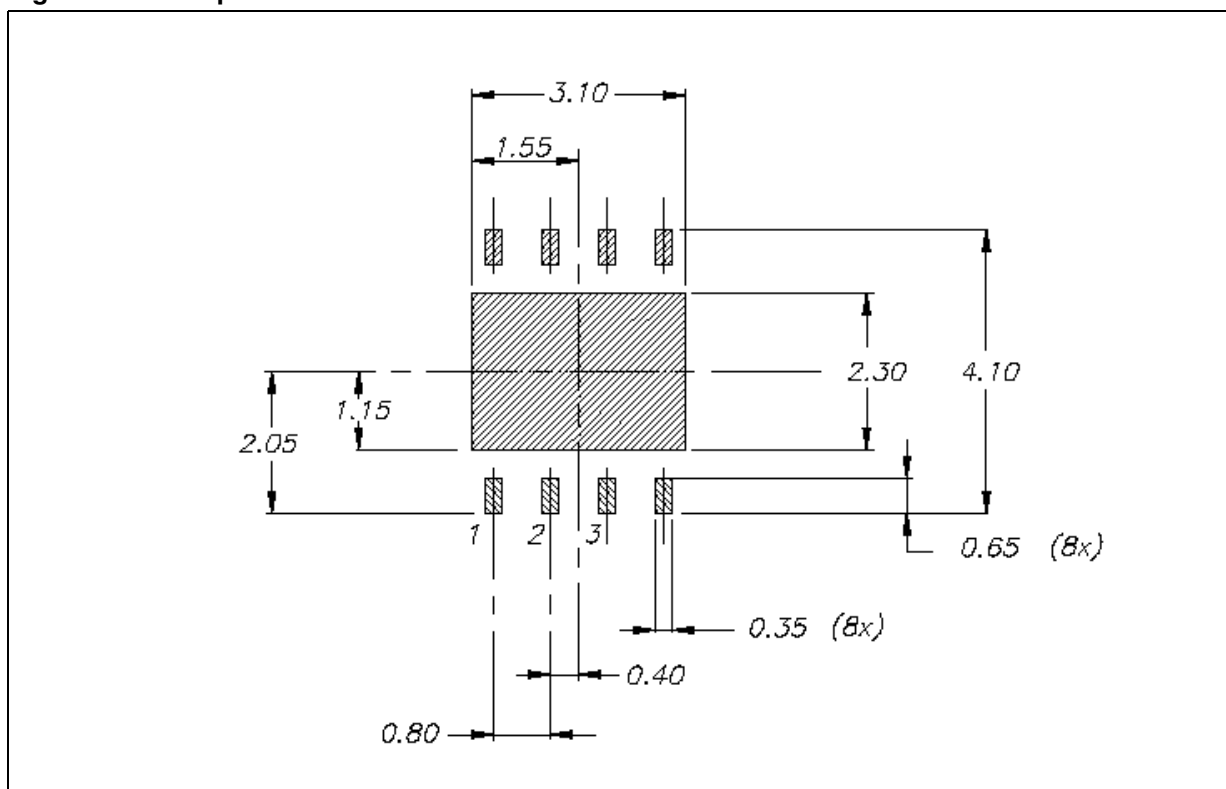
## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com)

## 5 Package information

### 5.1 Foot print recommended

Figure 6. Foot print

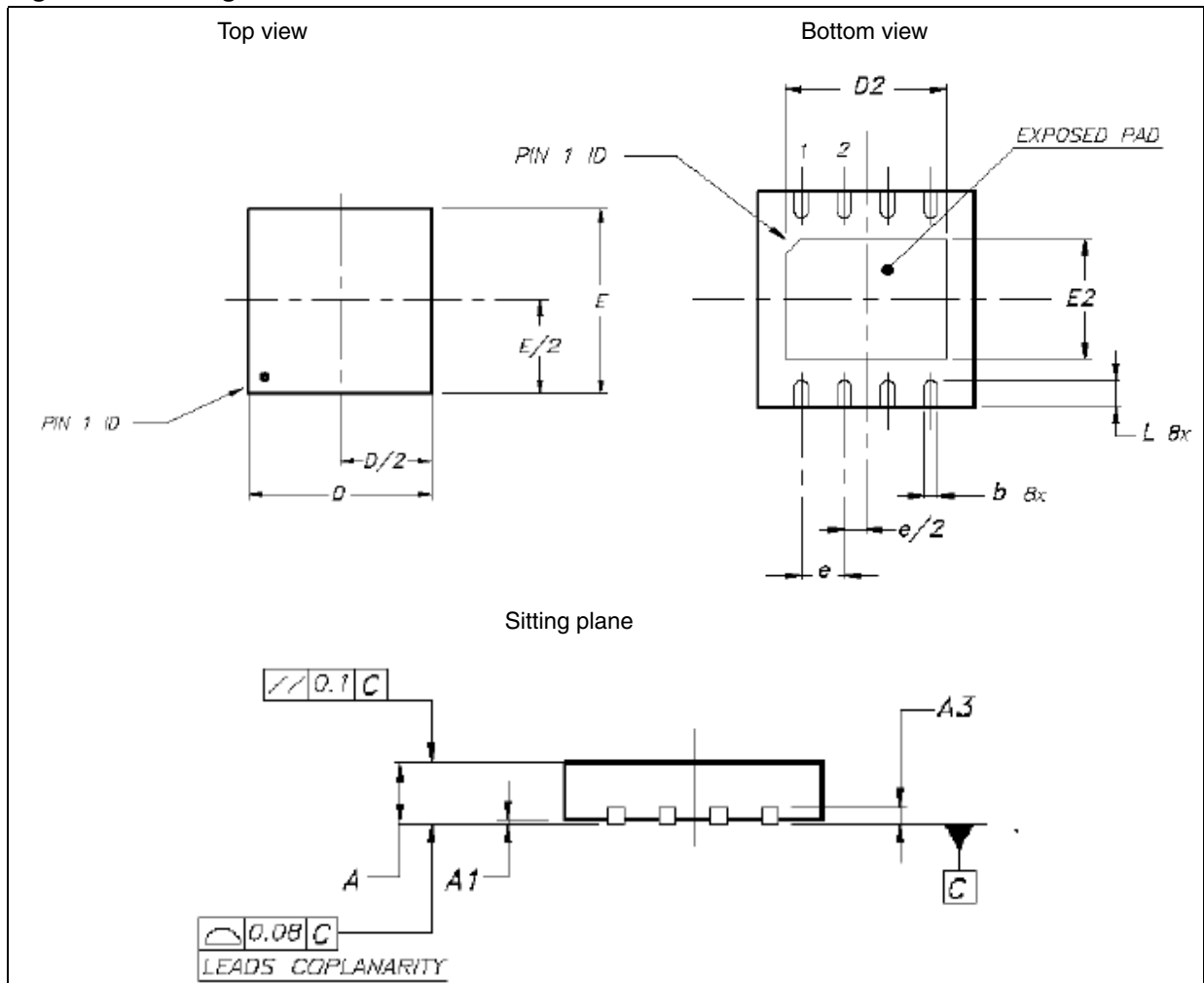


## 5.2 DFN (4x4) Mechanical data & package dimensions

Table 6. Package dimensions

Ref.	Dimensions		
	Millimeters		
	Typ	Min	Max
A	0.90	0.80	1
A1	0.02	0	0.05
A3	0.20		
b	0.30	0.23	0.38
D	4	3.90	4.10
D2	3	2.82	3.23
E	4	3.90	4.10
E2	2.20		2.30
e	0.80		
L	0.50	0.40	0.60

Figure 7. Package dimension



## 6 Revision history

**Table 7. Revision history**

Date	Revision	Changes
26-Jun-2006	1	Initial release.
31-Oct-2006	2	Updated package in cover page, inserted low/high side $I_{SC}$ in <a href="#">Table 4</a> .
09-Jan-2007	3	Updated $I_{SCHS}$ in <a href="#">Table 4 on page 6</a> .

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