TFBS5700

Vishay Semiconductors

VISHAY

Fast Infrared Transceiver Module (MIR, 1.152 Mbit/s) for IrDA® and Remote Control Applications

MEMBER IrDA

Description

The TFBS5700 is a low profile infrared transceiver module compliant to the latest IrDA physical layer standard for fast infrared data communication, supporting IrDA speeds up to 1.152 Mbit/s (MIR) and carrier based remote control modes up to 2 MHz. The transceiver module consists of a PIN photodiode, an infrared emitter (IRED), and a low-power control IC to provide a total font-end solution in a single package.

Features

Pb Pb-free

e4

- IrDA IrPHY 1.4 compliant
  9.6 kbit/s to 1.152 Mbit/s
  range > 50 cm, exceeding the low power standard
- Wide operating voltage range 2.4 V to 3.6 V
- I/O compatible to 1.8 V logic voltage
- Low power consumption
  Supply current in receive mode, Idle: 550 µA
- Small package -
  L 6.8 mm x W 2.8 mm x H 1.6 mm
- Remote control transmitter operation
  - Typical range 12 m
- Emitter wavelength: 886 nm
  - suited for Remote Control
- High immunity to fluorescence light
- High EMI immunity > 200 V/m
  (700 MHz to 2100 MHz)
- Lead (Pb)-free device
- Qualified for lead (Pb)-free and Sn/Pb processing (MSL4)
- Device in accordance with RoHS 2002/95/EC and WEEE 2002/96EC

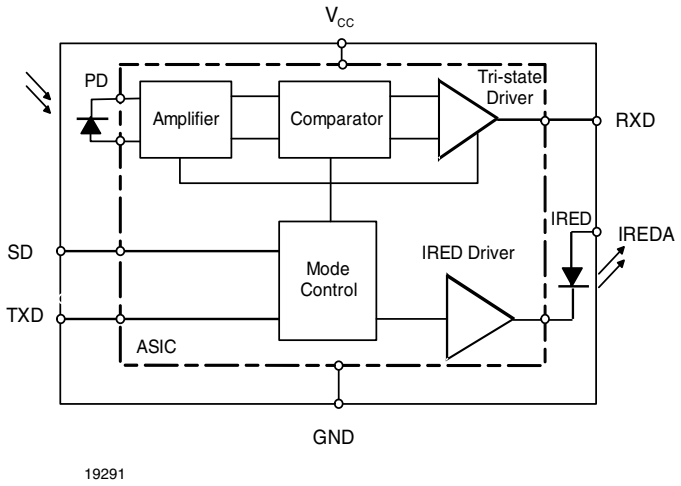
Applications

- Mobile phone
- Smart phone
- PDAs
- POS Terminals/Vending
- Battery Operated IrDA applications

Parts Table

Part	Description	Qty/Reel
TFBS5700-TR3	Oriented in carrier tape for side view surface mounting	2500 pcs

Functional Block Diagram

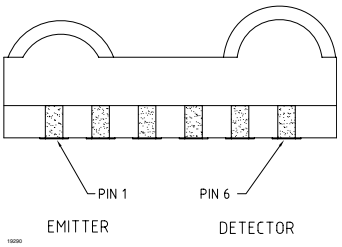


Pin Description

Pin Number	Function	Description	I/O	Active
1	IRED A	IRED anode, V_{CC2}		
2	TXD	This Schmitt-Trigger input is used to transmit serial data when SD is low. An on-chip protection circuit disables the LED driver if the TXD pin is asserted for longer than 80 µs. When used in conjunction with the SD pin, this pin is also used to control receiver output pulse duration. The input threshold voltage adapts to and follows the internal logic voltage reference of 1.8 V	I	HIGH
3	RXD	Received Data Output, push-pull CMOS driver output capable of driving standard CMOS or TTL loads. No external pull-up or pull-down resistor is required. Floating with a weak pull-up of 500 kΩ (typ.) in shutdown mode. The voltage swing is defined by the internal Vlogic voltage of 1.8 V	O	LOW
4	SD	Shutdown. Also used for setting the output pulse duration. Setting this pin active for more than 1.5 ms places the module into shutdown mode. Before that (t < 0.7 ms) on the falling edge of this signal, the state of the TXD pin is sampled and used to set the receiver output to long pulse duration (2 µs) or to short pulse duration (0.4 µs) mode. The input threshold voltage adapts to and follows the internal logic voltage reference of 1.8 V	I	HIGH
5	V_{CC}	Power Supply. Receives power supply 2.4 V to 3.6 V. This pin provides power for the receiver and transmitter drive section.		
6	GND	Ground		

Pinout

TFBS5700, bottom view
weight 33 mg



Definitions:

In the Vishay transceiver data sheets the following nomenclature is used for defining the IrDA operating modes:

SIR: 2.4 kbit/s to 115.2 kbit/s, equivalent to the basic serial infrared standard with the physical layer version IrPhY 1.0

MIR: 576 kbit/s to 1152 kbit/s

FIR: 4 Mbit/s

VFIR: 16 Mbit/s

MIR and FIR were implemented with IrPhY 1.1, followed by IrPhY 1.2, adding the SIR Low Power Standard. IrPhY 1.3 extended the Low Power Option to MIR and FIR and VFIR was added with IrPhY 1.4. A new version of the standard in any case obsoletes the former version.

Absolute Maximum Ratings

Reference point Pin, GND unless otherwise noted.
Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

Parameter	Test Conditions	Symbol	Min	Typ.	Max	Unit
Supply voltage range, transceiver	0 V < V_{CC2} < 6 V	V_{CC1}	- 0.5		6	V
Supply voltage range, transmitter	0 V < V_{CC1} < 6 V	V_{CC2}	- 0.5		6.5	V
Voltage at all I/O pins			- 0.5		5.5	V
Power dissipation	See derating curve	P_D			350	mW
Junction temperature	Note: Internal protection above 125° ASIC temperature	T_J			125	°C
Ambient temperature range (operating)		T_{amb}	- 30		+ 85	°C
Storage temperature range		T_{stg}	- 40		+ 100	°C
Soldering temperature	See section “Recommended Solder Profile”				260	°C
Average output current		I_{IRED} (DC)			125	mA
Repetitive pulse output current	< 90 µs, t_{on} < 20 %	I_{IRED} (RP)			500	mA
Virtual source size	Method: (1-1/e) encircled energy	d	0.8			mm
Maximum Intensity for Class 1	IEC60825-1 or EN60825-1, edition Jan. 2001	I_e			*) (500)**)	mW/sr
ESD protection						
ESD protection on all pins	Method: Human body model	d	1			kV
Latch up		d	|± 100|			mA

*) Due to the internal limitation measures the device is a "class1" device

**) IrDA specifies the max. intensity with 500 mW/sr

Electrical Characteristics

Transceiver

T_{amb} = 25 °C, V_{CC} = 2.4 V to 3.6 V unless otherwise noted.
Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

Parameter	Test Conditions	Symbol	Min	Typ.	Max	Unit
Supply voltage		V_{CC}	2.4		3.6	V
Dynamic Supply current						
Idle, dark ambient	SD = Low (< 0.8 V), E_e = 0 klx	I_{CC}		550	900	µA
Receiving	SD = Low, 1 Mbit/s, E_e = 100 mW/m^2	I_{CC}		0.75		mA
Shutdown supply current Dark ambient	SD = High (> V_{CC1} - 1.3 V), T = 25 °C, E_e = 0 klx T = 25 °C	I_{SD}		 0.01	 1.0	 µA
Shutdown supply current at maximum operating temperature	SD = High, (> V_{CC1} - 1.3 V), T = 85 °C	I_{SD}			5.0	µA
Operating temperature range		T_A	- 25		+ 85	°C
Output voltage low	I_{OL} = 0.5 mA, C_{load} = 15 pF	V_{OL}			0.4	V
Output voltage high	I_{OH} = - 250 µA, C_{load} = 15 pF	V_{OH}	1.44			V
Output voltage high	I_{OH} = 0 µA, C_{load} = 15 pF	V_{OH}			1.98	V
RXD to internal Vlogic impedance	SD = active, pull-up in shutdown	R_{RXD}	400	500	800	kΩ
Input voltage low (TXD, SD)		V_{IL}	- 0.5		0.5	V
Input voltage high (TXD, SD)		V_{IH}	1.3	1.8	2.2	V
Input leakage current (TXD, SD) *)	Vin = 0.9 x V_{CC1}	IS-SD, IIN-SD	- 1.1	4	10	µA
SD mode programming pulse width		t_{SDPW}	0.2		300	µs
Input capacitance (TXD, SD)		C_I			5	pF

*) Decision level 0.9 V

Optoelectronic Characteristics

Receiver

T_{amb} = 25 °C, V_{CC} = 2.4 V to 3.6 V unless otherwise noted.
Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

Parameter	Test Conditions	Symbol	Min	Typ.	Max	Unit
Minimum irradiance E_e in angular range **) SIR mode	9.6 kbit/s to 115.2 kbit/s λ = 850 nm to 900 nm	E_e		50 (5)	81 (8.1)	mW/m² (µW/cm²)
Minimum irradiance E_e in angular range **) MIR mode	1.152 Mbit/s λ = 850 nm to 900 nm	E_e		50 (5)	140 (14)	mW/m² (µW/cm²)
Maximum irradiance E_e in angular range ***)	λ = 850 nm to 900 nm	E_e		5 (500)		kW/m² (mW/cm²)
Logic LOW receiver input irradiance *)	According to IrDA appendix A1, fluorescent light specification	E_e	4 (0.4)			mW/m² (µW/cm²)
RXD pulse width of output signal, dafault mode after power on or reset	Input pulse length T_{Wopt} > 200 ns		300	400	500	ns
Rise time of output signal	10 % to 90 %, C_L = 15 pF	$t_{r\ (RXD)}$	10	27	60	ns
Fall time of output signal	90 % to 10 %, C_L = 15 pF	$t_{f\ (RXD)}$	10	17	60	ns
SIR ENDEC compatility mode [1]): RXD pulse width of output signal	Input pulse length T_{Wopt} > 200 ns, see chapter “Programming”	t_{PW}	1.7	2.0	2.9	µs
Stochastic jitter, leading edge	Input irradiance = 150 mW/m², ≤ 1.152 Mbit/s, 576 kbit/s				70	ns
Stochastic jitter, leading edge	Input irradiance = 150 mW/m², ≤ 115.2 kbit/s				350	ns
Standby/shutdown delay	after shutdown active or (SD low to high transition)		0.6		1.5	ms
Shutdown active time window for programming	During this time the pulse duration of the output can be programmed to the application mode. see chapter “Programming”				600	µs
Receiver start up time, Power on delay Shutdown recovery delay	After shutdown inactive (SD high to low transition) and power-on				250	µs
Latency		t_L		50	200	µs

Note: All timing data measured with 4 Mbit/s are measured using the IrDA® FIR transmission header.
The data given here are valid 5 µs after starting the preamble.

*) This parameter reflects the backlight test of the IrDA physical layer specification to guarantee immunity against light from fluorescent lamps

) IrDA sensitivity definition: **Minimum Irradiance E_e In Angular Range, power per unit area. The receiver must meet the BER specification while the source is operating at the minimum intensity in angular range into the minimum half-angle range at the maximum Link Length.

***) **Maximum Irradiance E_e In Angular Range**, power per unit area. The optical delivered to the detector by a source operating at the maximum intensity in angular range at **Minimum Link Length** must not cause receiver overdrive distortion and possible related link errors. If placed at the Active Output Interface reference plane of the transmitter, the receiver must meet its bit error ratio (BER) specification.

For more definitions see the document “Symbols and Terminology” on the Vishay Website (http://www.vishay.com/docs/82512/82512.pdf).

1) Some ENDECs are not able to decode short pulses as valid SIR pulses. Therefore this additional mode was added in TFBS5700. TFBS5700 is set to the "short output pulse" as default after power on, also after recovering from the shutdown mode (SD must have been longer active than 1.5 ms). For mode changing see the chapter "Programming".

Transmitter

T_{amb} = 25 °C, V_{CC} = 2.4 V to 5.5 V unless otherwise noted.
Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

Parameter	Test Conditions	Symbol	Min	Typ.	Max	Unit
Recommended IRED operating peak current **)	The IRED current must be controlled by an external resistor	I_D		200	600	mA
Output leakage IRED current	TXD = 0 V, T_{amb} = 25 °C TXD = 0 V, T_{amb} = 85 °C	I_{IRED}		200	 1	pA µA
Output radiant intensity, s. figure 3, recommended appl. circuit	a = 0°, 15°, TXD = High, SD = Low, V_{CC1} = 2.5 V, V_{CC2} = 2.9 V, Rs = 4.7 Ω	I_e	25	60	500	mW/sr
Output radiant intensity	V_{CC1} = 5.0 V, α = 0°, 15° TXD = Low, SD = High (Receiver is inactive as long as SD = High)	I_e			0.04	mW/sr
Peak - emission wavelength *)		λ_p	880		900	nm
Optical spectral bandwidth		$\Delta\lambda$		45		nm
Optical rise time, Optical fall time		t_{ropt}, t_{fopt}	10		40	ns
Optical output pulse duration	Input pulse width 217 ns, 1.152 Mbit/s	t_{opt}	180	217	240	ns
	Input pulse width t < 80 µs Input pulse width t ≥ 80 µs	t_{opt} t_{opt}			t_{TXD} 85	µs µs
Optical overshoot					25	%

*) Note: Due to this wavelength restriction compared to the IrDA spec of 850 nm to 900 nm the transmitter is able to operate as source for the standard Remote Control applications with codes as e.g. Philips RC5/RC6® or RECS 80. When operated under IrDA full range conditions (> 120 mW/sr) the RC range to be covered is in the range from 8 m to 12 m, provided that state of the art remote control receivers are used.

**) Typ. conditions for If = 200 mA, V_{CC2} = 2.9 V, Rs = 4.7 Ω

Table 1.
Truth table

Inputs			Outputs		Remark
SD	TXD	Optical input Irradiance mW/m²	RXD	Transmitter	Operation
high < 600 µs	x	x	weakly pulled (500 kΩ) to V_{CC1}	0	Time window for pulse duration setting
high > 1.5 ms	x	x	weakly pulled (500 kΩ) to V_{CC1}	0	Shutdown
low	high	x	low (active)	I_e	Transmitting
low	high > 80 µs	x	high inactive	0	Protection is active
low	low	< 4	high inactive	0	Ignoring low signals below the IrDA defined threshold for noise immunity
low	low	> Min. irradiance*Ee* < Max. irradiance *Ee*	low (active)	0	Response to an IrDA compliant optical input signal
low	low	> Max. irradiance *Ee*	undefined	0	Overload conditions can cause unexpected outputs

Recommended Circuit Diagram

Operated at a clean low impedance power supply the TFBS5700 needs only one additional external component for setting the IRED drive current. However, depending on the entire system design and board layout, additional components may be required (see figure 1).

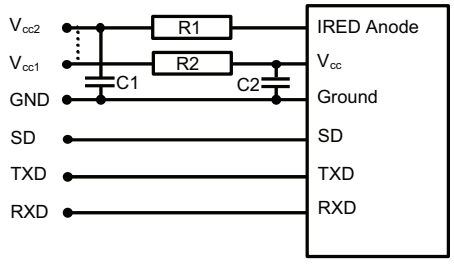


Figure 1. Recommended Application Circuit

The capacitor C1 is buffering the supply voltage and eliminates the inductance of the power supply line. This one should be a small ceramic version or other fast capacitor to guarantee the fast rise time of the IRED current. The resistor R1 is only necessary for setting the IRED drive current.
Vishay transceivers integrate a sensitive receiver and a built-in power driver. The combination of both needs a careful circuit board layout. The use of thin, long, resistive and inductive wiring should be avoided. The inputs (TXD, SD) and the output RXD should be directly (DC) coupled to the I/O circuit.
The capacitor C2 combined with the resistor R2 is the low pass filter for smoothing the supply voltage.
R2, C1 and C2 are optional and dependent on the quality of the supply voltages VCCx and injected noise. An unstable power supply with dropping voltage during transmission may reduce the sensitivity (and transmission range) of the transceiver.
The placement of these parts is critical. It is strongly recommended to position C2 as close as possible to the transceiver power supply pins.
In addition, when connecting the described circuit to the power supply, low impedance wiring should be used.

When extended wiring is used the inductance of the power supply can cause dynamically a voltage drop at V_{CC2}. Often some power supplies are not able to follow the fast current is rise time. In that case another 10 µF (type, see table under C1) at V_{CC2} will be helpful.

Keep in mind that basic RF-design rules for circuit design should be taken into account. Especially longer signal lines should not be used without termination. See e.g. "The Art of Electronics" Paul Horowitz, Wienfield Hill, 1989, Cambridge University Press, ISBN: 0521370957.

Table 2.
Recommended Application Circuit Components

Component	Recommended Value
C1, C2	0.1 µF, Ceramic Vishay part# VJ 1206 Y 104 J XXMT
R1	2.9 V to 5.4 V supply voltage V_{CC2}: add a resistor in series, e.g. 4.7 Ω
R2	47 Ω, 0.125 W ($V_{CC1} \geq 2.5$ V)

I/O and Software

In the description, already different I/Os are mentioned. Different combinations are tested and the function verified with the special drivers available from the I/O suppliers. In special cases refer to the I/O manual, the Vishay application notes, or contact directly Vishay Sales, Marketing or Application.

Programming Pulse duration Switching

After Power-on the TFBS5700 is in the default short pulse duration mode. Some ENDECs are not able to decode short pulses as valid SIR pulses. Therefore an additional mode with an extended pulse duration as in standard SIR transceivers was added in TFBS5700. TFBS5700 is set to the “short output pulse” as default after power on, also after recovering from the shutdown mode (SD must have been longer active than 1.5 ms). For mode changing see the following. To switch the transceivers from the short pulse duration mode to the long pulse duration mode and vice versa, the programming sequences described below are required.

Setting to the ENDEC compatibility mode with an RXD pulse duration of 2 µs

1. Set SD input to logic "HIGH".
2. Set TXD input to logic "LOW". Wait $t_s \geq 200$ ns.
3. Set SD to logic "LOW" (this negative edge latches state of TXD, which determines speed setting).
4. TXD must be held for $t_h \geq 200$ ns. After waiting $t_h \geq 200$ ns TXD.

TXD is now enable as normal TXD input for the longer RXD - pulse duration mode.

Setting back to the default mode with 400 ns RXD-output pulse duration

1. Set SD input to logic "HIGH".
2. Set TXD input to logic "HIGH". Wait $t_s \geq 200$ ns.
3. Set SD to logic "LOW" (this negative edge latches state of TXD, which determines speed setting).
4. After waiting $t_h \geq 200$ ns TXD is limited by the maximum allowed pulse length.

TXD is now enabled as normal TXD input.
The timing of the pulse duration changing procedure is quite uncritical. However, the whole change must not take more than 600 µs. See in the spec. “Shutdown Active Time Window for Programming”

Simplified Method

Setting the device to the long pulse duration is nothing else than a short active SD pulse of less than 600 µs. In any case a short SD pulse will force the device to leave the default mode and go the compatibility mode. Backwards also an active SD can be used to fall back into the default mode by applying that signal for a minimum of 1.5 ms. That causes a power-on-reset and sets the device to the default short pulse mode. This simplified method takes more time but may be easier to handle.

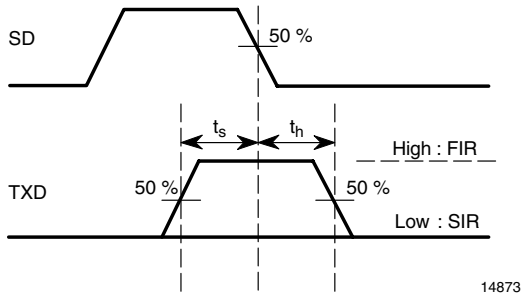


Figure 2. Mode Switching Timing Diagram

Recommended Solder Profiles

Solder Profile for Sn/Pb soldering

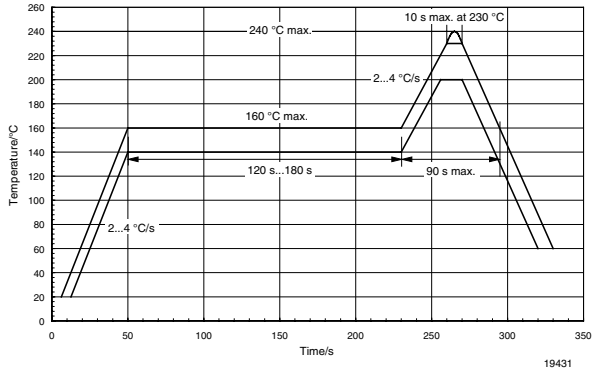


Figure 3. Recommended Solder Profile for Sn/Pb soldering

Lead (Pb)-Free, Recommended Solder Profile

The TFBS5700 is a lead (Pb)-free transceiver and qualified for lead (Pb)-free processing. For lead (Pb)-free solder paste like Sn(3.0-4.0)Ag(0.5-0.9)Cu, there are two standard reflow profiles: Ramp-Soak-Spike (RSS) and Ramp-To-Spike (RTS). The Ramp-Soak-Spike profile was developed primarily for reflow ovens heated by infrared radiation. With widespread use of forced convection reflow ovens the Ramp-To-Spike profile is used increasingly. Shown below in figure 4 is VISHAY's recommended profiles for use with the TFBS5700 transceivers. For more details please refer to Application note: SMD Assembly Instruction (http://www.vishay.com/docs/82602/82602.pdf).

Wave Soldering

For TFDUxxxx and TFBSxxxx transceiver devices wave soldering is not recommended.

Manual Soldering

Manual soldering is the standard method for lab use. However, for a production process it cannot be recommended because the risk of damage is highly dependent on the experience of the operator. Nevertheless, we added a chapter to the above mentioned application note, describing manual soldering and desoldering.

Storage

The storage and drying processes for all VISHAY transceivers (TFDUxxxx and TFBSxxx) are equivalent to MSL4.

The data for the drying procedure is given on labels on the packing and also in the application note "Taping, Labeling, Storage and Packing" (http://www.vishay.com/docs/82601/82601.pdf).

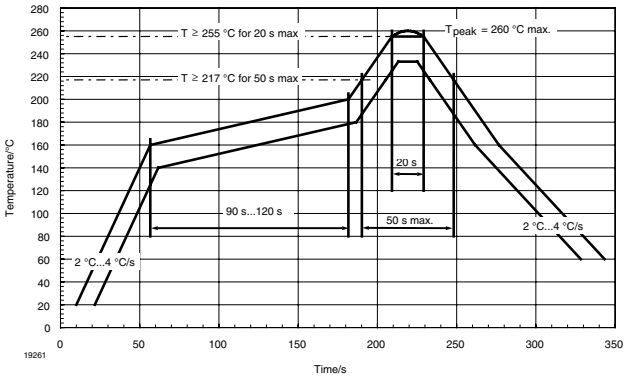


Figure 4. Solder Profile, RSS Recommendation

Package Dimensions in mm

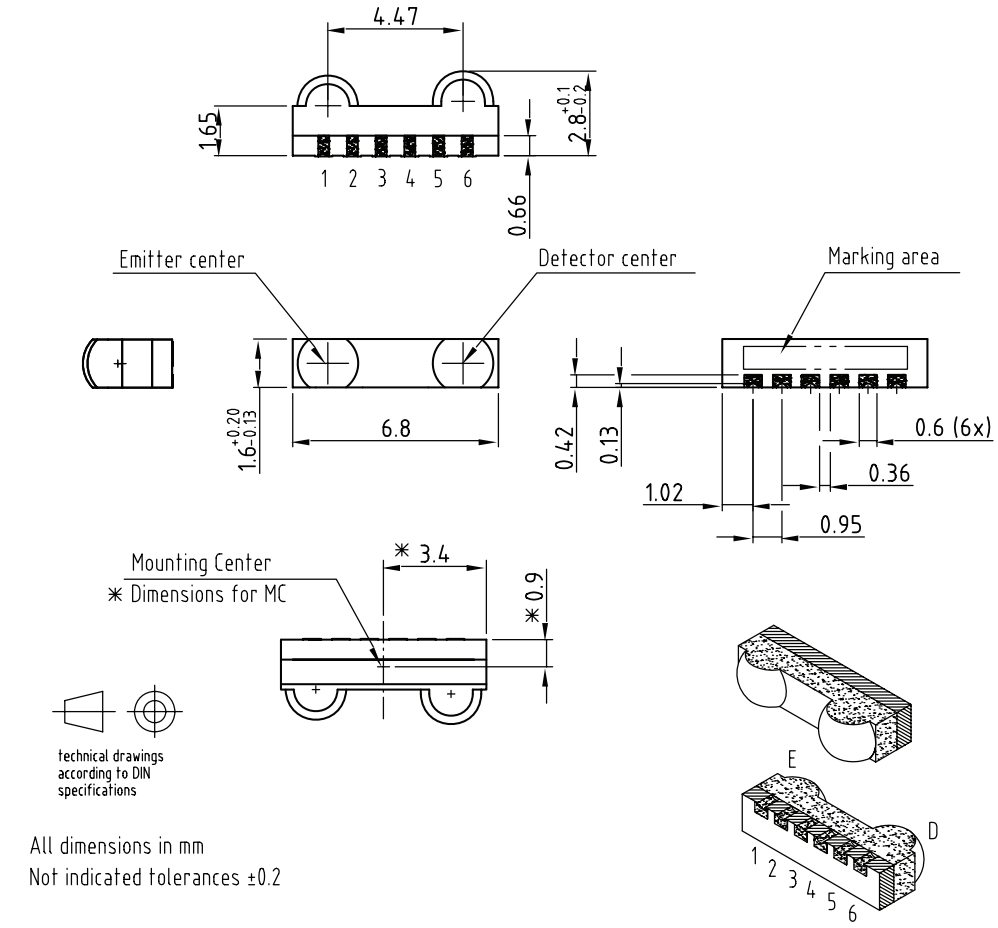


Figure 5. TFBS5700 mechanical dimensions, tolerance ± 0.2 mm if not otherwise mentioned

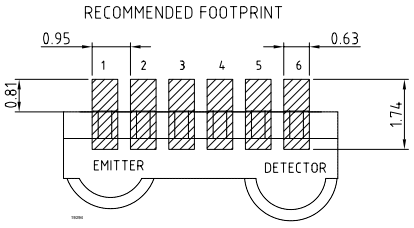
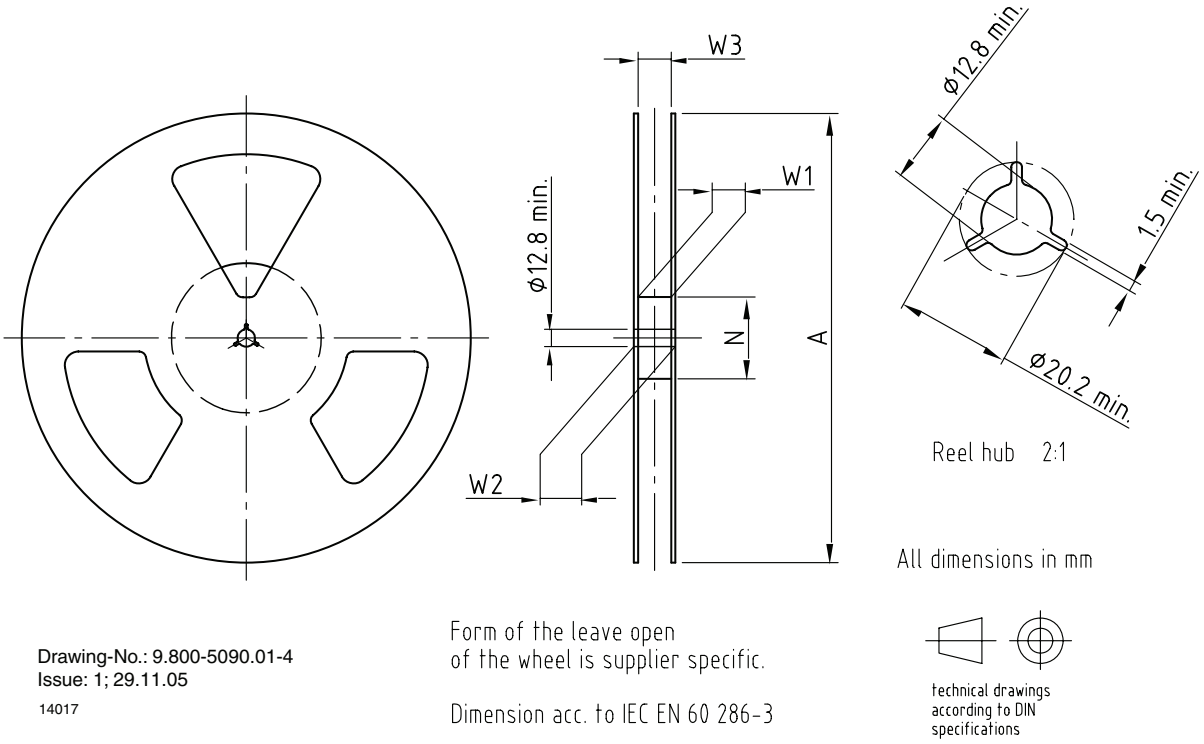


Figure 6. TFBS5700 soldering footprint, tolerance ± 0.2 mm if not otherwise mentioned

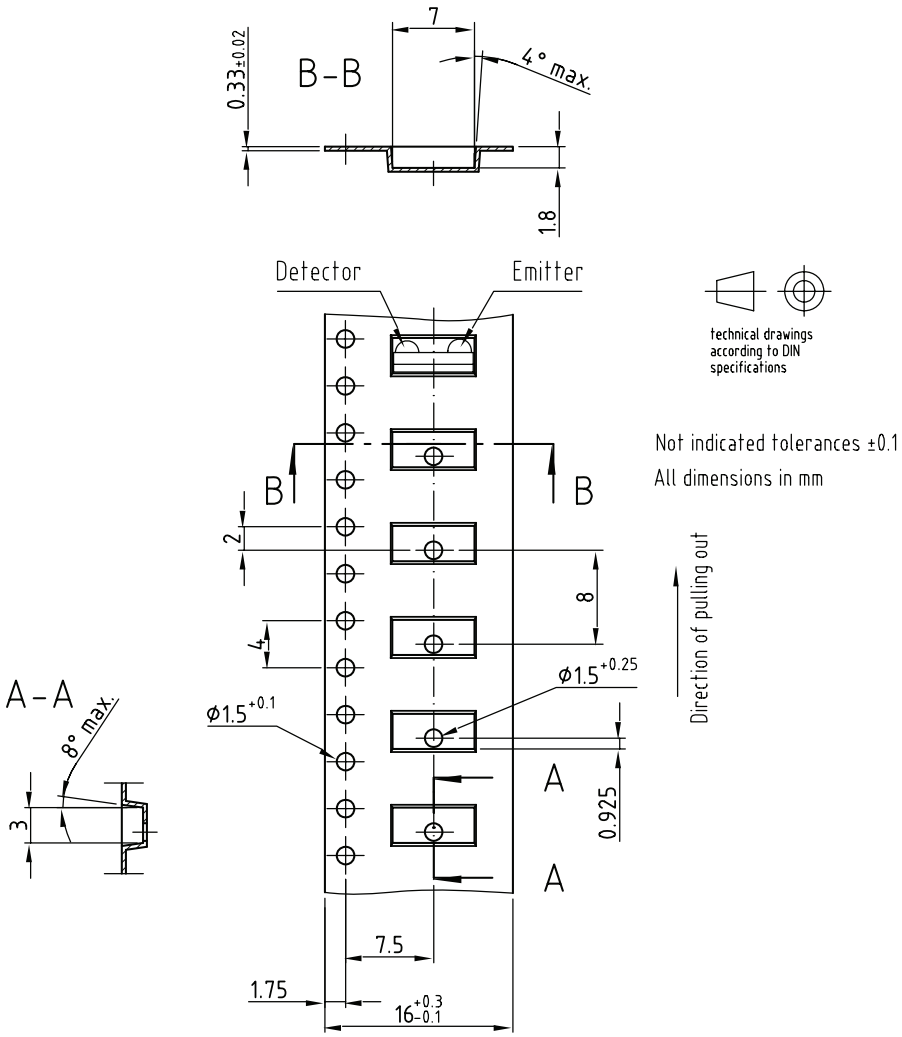
Reel Dimensions



Drawing-No.: 9.800-5090.01-4
Issue: 1; 29.11.05
14017

Tape Width	A max.	N	W_1 min.	W_2 max.	W_3 min.	W_3 max.
mm	mm	mm	mm	mm	mm	mm
16	330	50	16.4	22.4	15.9	19.4

Tape Dimensions in mm



Drawing-No.: 9.700-5296.01-4
Issue: prel. copy; 24.11.04

Drawing refers to following types: TFBS 4650
TFBS 5700

19286

Ozone Depleting Substances Policy Statement

It is the policy of Vishay Semiconductor GmbH to

1. Meet all present and future national and international statutory requirements.
2. Regularly and continuously improve the performance of our products, processes, distribution and operating systems with respect to their impact on the health and safety of our employees and the public, as well as their impact on the environment.

It is particular concern to control or eliminate releases of those substances into the atmosphere which are known as ozone depleting substances (ODSs).

The Montreal Protocol (1987) and its London Amendments (1990) intend to severely restrict the use of ODSs and forbid their use within the next ten years. Various national and international initiatives are pressing for an earlier ban on these substances.

Vishay Semiconductor GmbH has been able to use its policy of continuous improvements to eliminate the use of ODSs listed in the following documents.

1. Annex A, B and list of transitional substances of the Montreal Protocol and the London Amendments respectively
2. Class I and II ozone depleting substances in the Clean Air Act Amendments of 1990 by the Environmental Protection Agency (EPA) in the USA
3. Council Decision 88/540/EEC and 91/690/EEC Annex A, B and C (transitional substances) respectively.

Vishay Semiconductor GmbH can certify that our semiconductors are not manufactured with ozone depleting substances and do not contain such substances.

Vishay Semiconductor GmbH, P.O.B. 3535, D-74025 Heilbronn, Germany

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