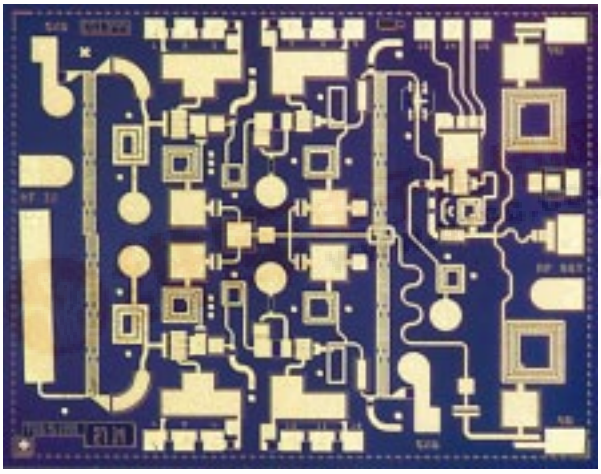
TriQuint SEMICONDUCTOR

Product Data Sheet
October 14, 2005

6-13 GHz Low Noise Amplifier TGA8399B-SCC



Key Features and Performance

- 6-13 GHz Frequency Range
- 1.5 dB Typical Noise Figure Midband
- 26 dB Nominal Gain
- High Input Power Handling: ~ 20dBm
- Balanced Input for Low VSWR
- 5V @ 65mA Self Bias
- 0.25um pHEMT Technology
- Chip Dimensions 3.1 x 2.4 x 0.15 mm

Primary Applications

- Point-to-Point Radio
- X Band Radar, ECM

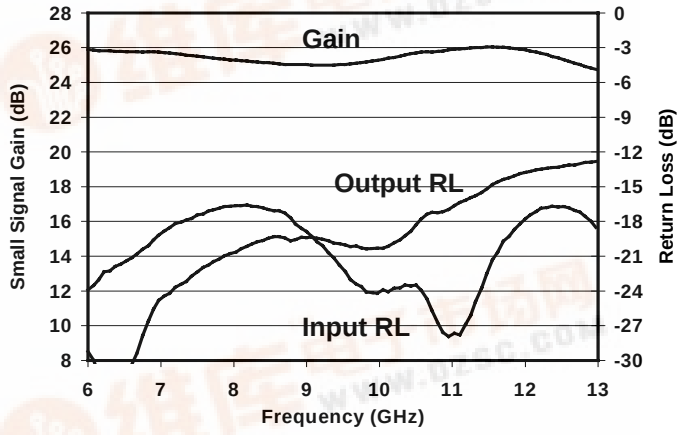
Description

The TriQuint TGA8399B-SCC is a monolithic self-biased low noise amplifier with a balanced input for low VSWR. This LNA operates from 6 to 13 GHz with a typical mid band noise figure of 1.5 dB. The device features high gain of 26 dB across the band, while providing a nominal output power at P1dB gain compression of 11dBm. Typical input and output return loss is 18 dB. Ground is provided to the circuitry through vias to the backside metallization. The TGA8399B-SCC low noise amplifier is suitable for a variety of commercial and high frequency applications, C and X band applications such as radar receivers, electronic counter measures, decoys, jammers and phased array systems. At 5V the drain current is approximately 65 mA and can be increased or decreased by selection of the appropriate source resistors in each stage. For an application note concerning drain current selection see: http://www.triquint.com/company/divisions/millimeter_wave/AppNote_self_bias_of_8399b_c2.pdf

Lead-free and RoHS compliant

Typical Electrical Characteristics

Self Bias, Vd=5V, 65mA



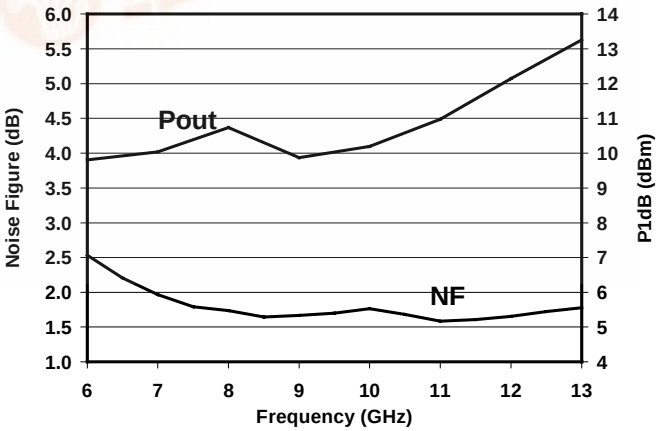


TABLE I
MAXIMUM RATINGS 5/

SYMBOL	PARAMETER	VALUE	NOTES
V^+	Positive Supply Voltage	8 V	4/
V^-	Negative Supply Voltage Range	-5V TO 0V	
I^+	Positive Supply Current (Quiescent)	100 mA	4/
P_{IN}	Input Continuous Wave Power	22 dBm	
P_D	Power Dissipation	1.95W	3/ 4/
T_{CH}	Operating Channel Temperature	150 ^{0}C	1/ 2/
T_M	Mounting Temperature (30 Seconds)	320 ^{0}C	
T_{STG}	Storage Temperature	-65 to 150 ^{0}C	

1/ These ratings apply to each individual FET.

2/ Junction operating temperature will directly affect the device median time to failure (T_M). For maximum life, it is recommended that junction temperatures be maintained at the lowest possible levels.

3/ When operated at this bias condition with a base plate temperature of 70 ^{0}C, the median life is reduced from 9.2E+8 to 2.5E+6 hours.

4/ Combinations of supply voltage, supply current, input power, and output power shall not exceed P_D.

5/ These ratings represent the maximum operable values for this device.

TABLE II
DC PROBE TEST
(TA = 25 °C ± 5 °C)

NOTES	SYMBOL	LIMITS		UNITS
		MIN	MAX	
	I_{DSS1}	Information Only		mA
	I_{MAX}	169	290	mS
	Gm1	99	239	mS
1/	$\|V_{P1,2,3,4,5}\|$	0.5	1.5	V
1/	$\|V_{BVGD1}\|$	8	30	V
1/	$\|V_{BVGS1}\|$	8	30	V

1/ V_P, V_{BVGD}, and V_{BVGS} are negative.

TABLE III
RF CHARACTERISTICS
(T_A = 25°C ± 5°C)

NOTE	TEST	MEASUREMENT CONDITIONS Self Bias, Vd=5V	VALUE			UNITS
			MIN	TYP	MAX	
1/	Small Signal Gain	F = 6 - 13 GHz	23	26		dB
	Power Output @ 1 dB Gain Compression	F = 6 - 13 GHz		11		dBm
2/	Noise Figure	F = 6 - 13 GHz F = 10 GHz		2.0	 2.5	dB dB
1/	Input Return Loss Magnitude	F = 6 - 13 GHz		-18	-9.5	dB
1/	Output Return Loss Magnitude	F = 6 - 13 GHz		-18	-9.5	dB

1/ RF probe data is taken at 1 GHz steps

2/ RF probe data is taken at 10 GHz.

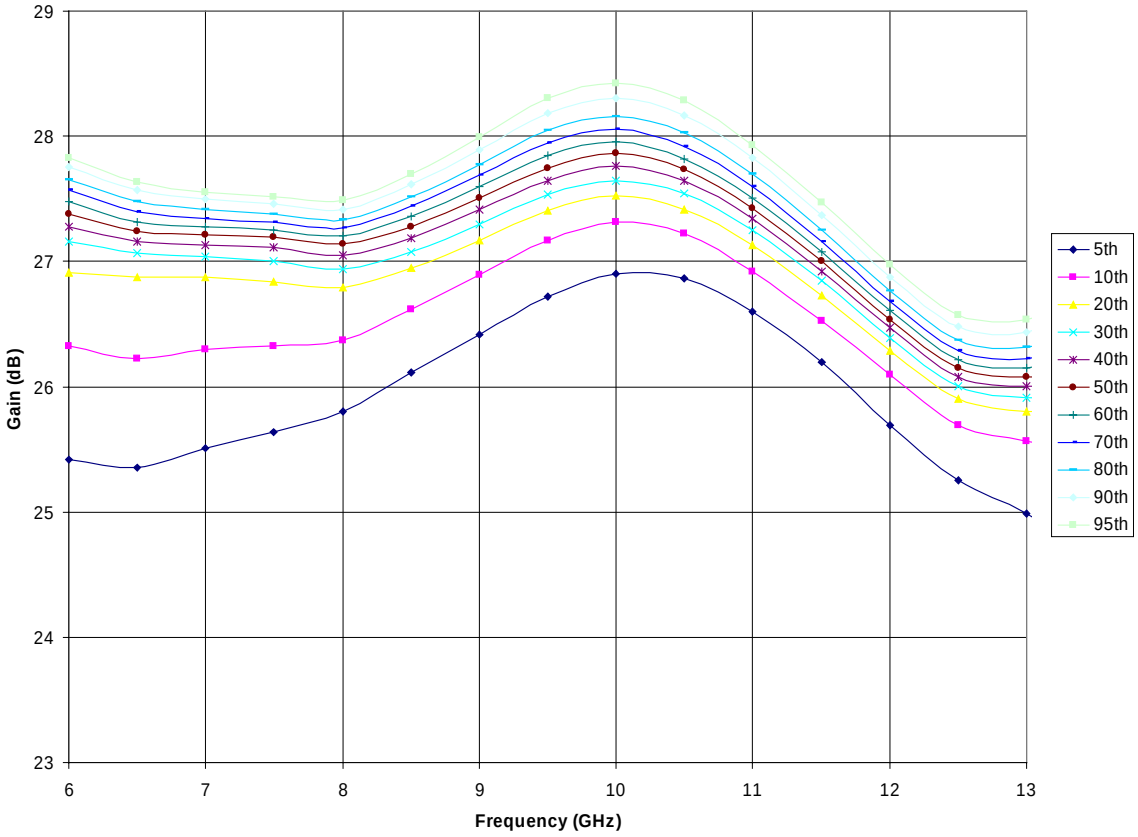
TABLE IV
THERMAL INFORMATION

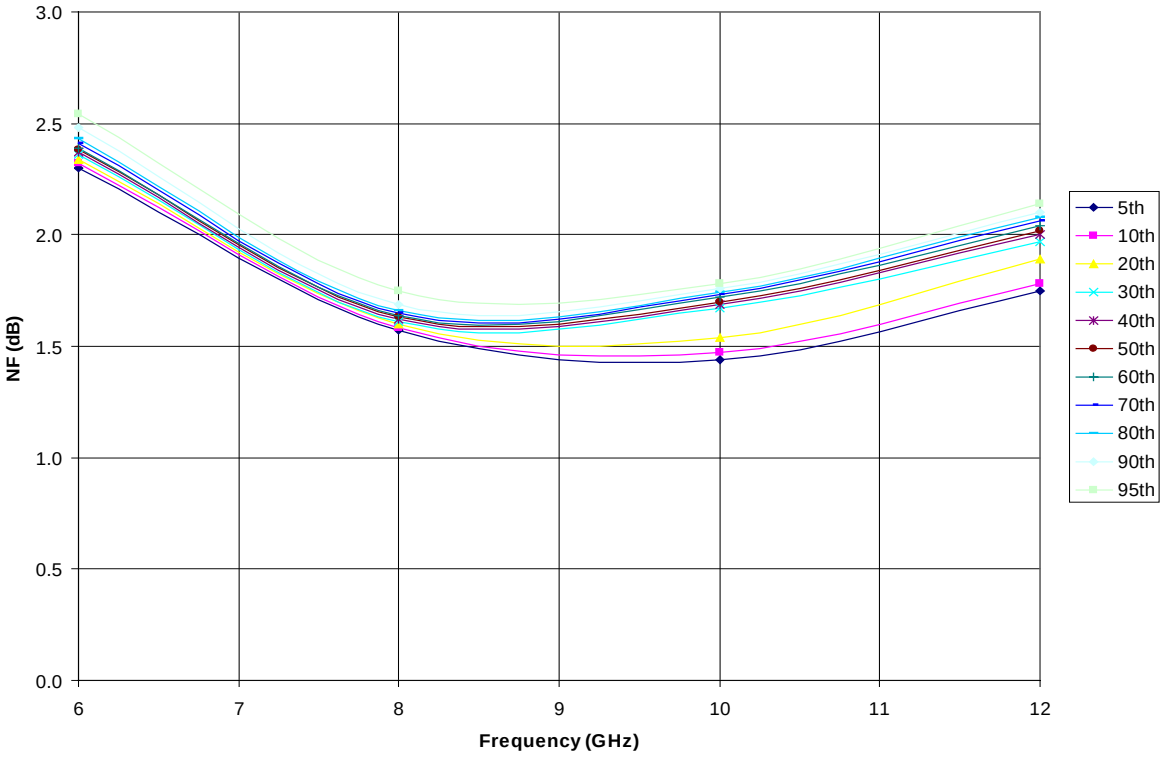
PARAMETER	TEST CONDITIONS	T_{CH} (°C)	$R_{\theta JC}$ (°C/W)	T_M (HRS)
$R_{\theta JC}$ Thermal Resistance (channel to backside of carrier)	Vd = 5 V I_D = 65 mA Pdiss = 0.325 W	82.14	37.354	9.2E+8

Note: Assumes eutectic attach using 1.5 mil 80/20 AuSn mounted to a 20 mil CuMo Carrier at 70°C baseplate temperature. Worst case condition with no RF applied, 100% of DC power is dissipated.

Typical On-Wafer Electrical Characteristics

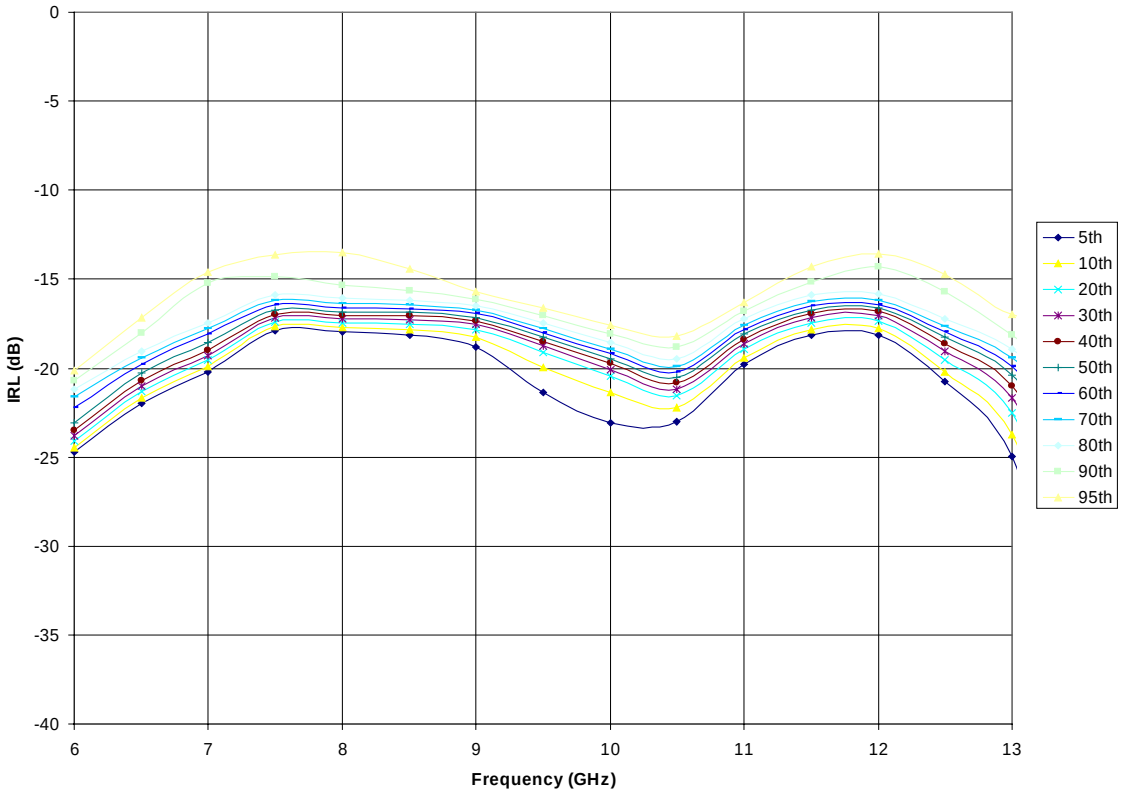
Sefl Bias, Vd=5V, Room Temperature

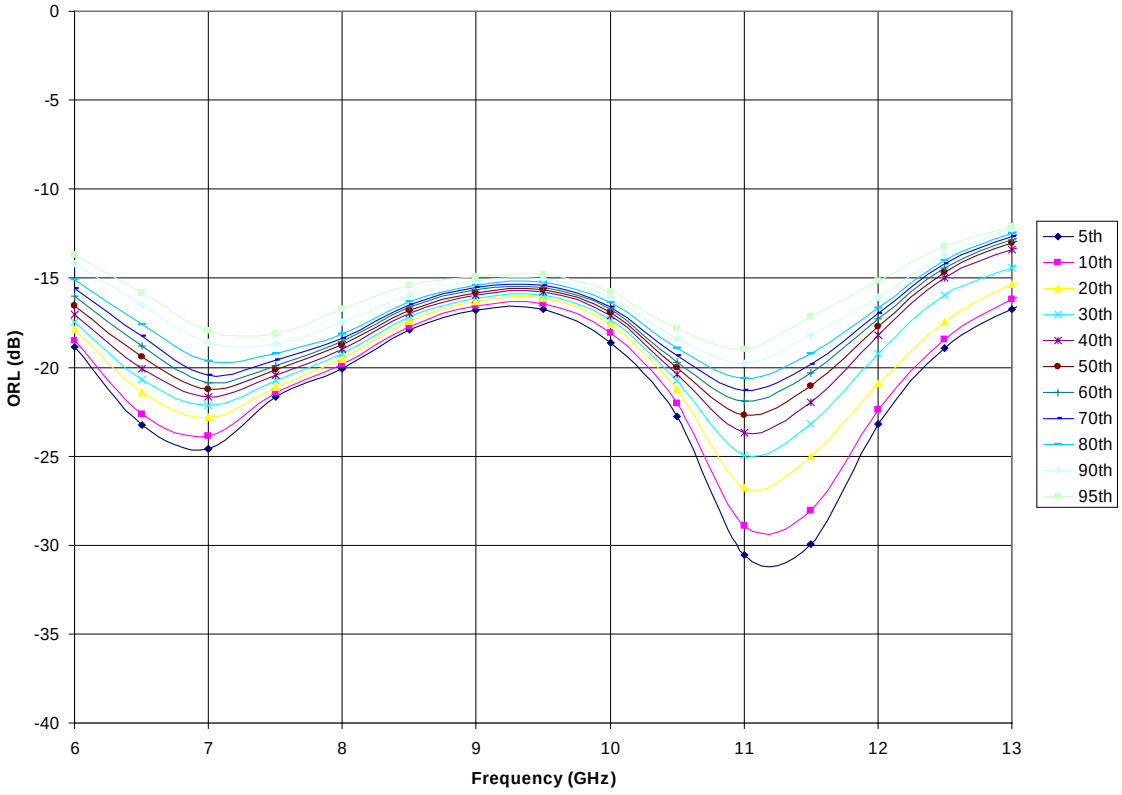




Typical On-Wafer Electrical Characteristics

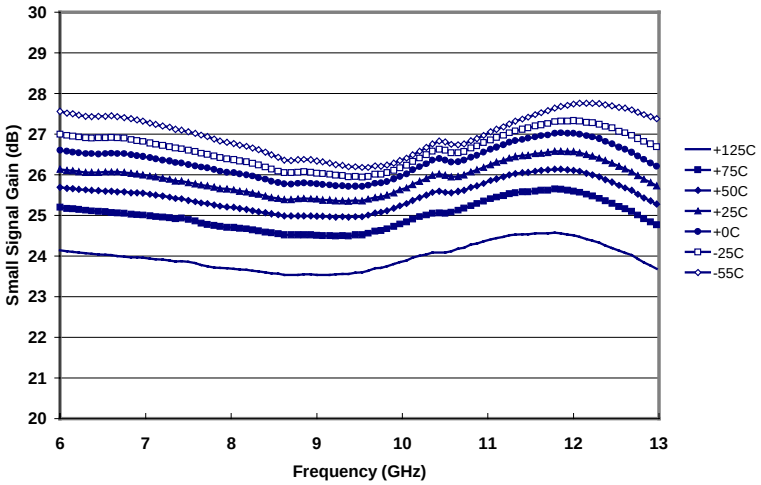
Sefl Bias, Vd=5V, Room Temperature

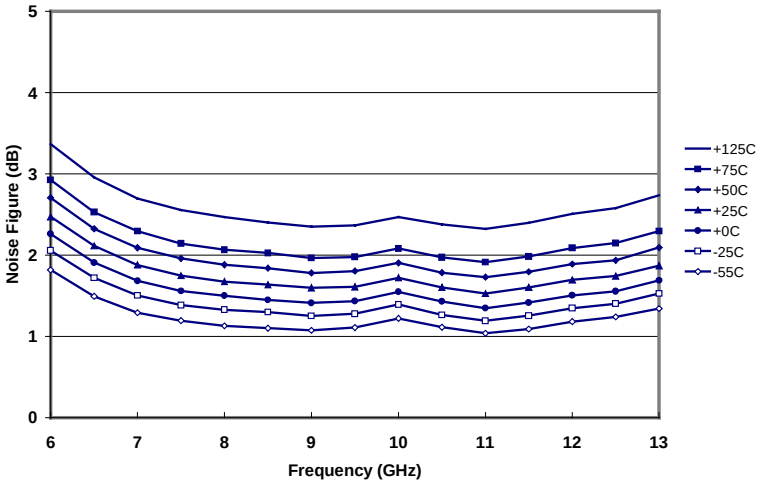


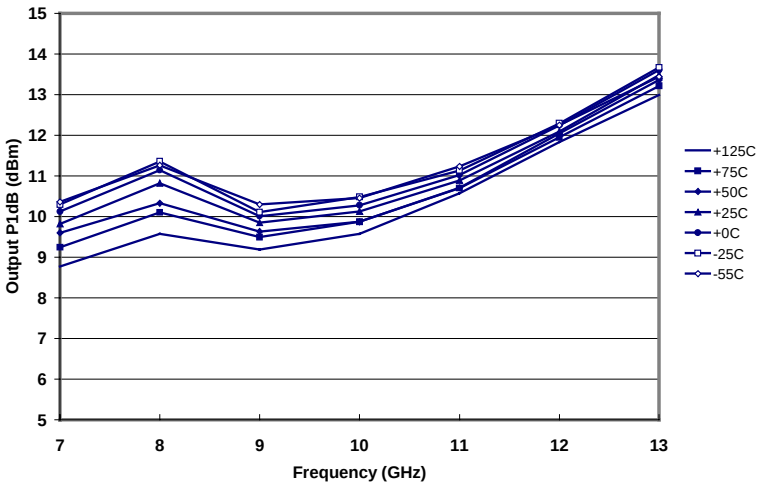


Typical Performance vs Temperature

Sefl Bias, Vd=5V, Room Temperature







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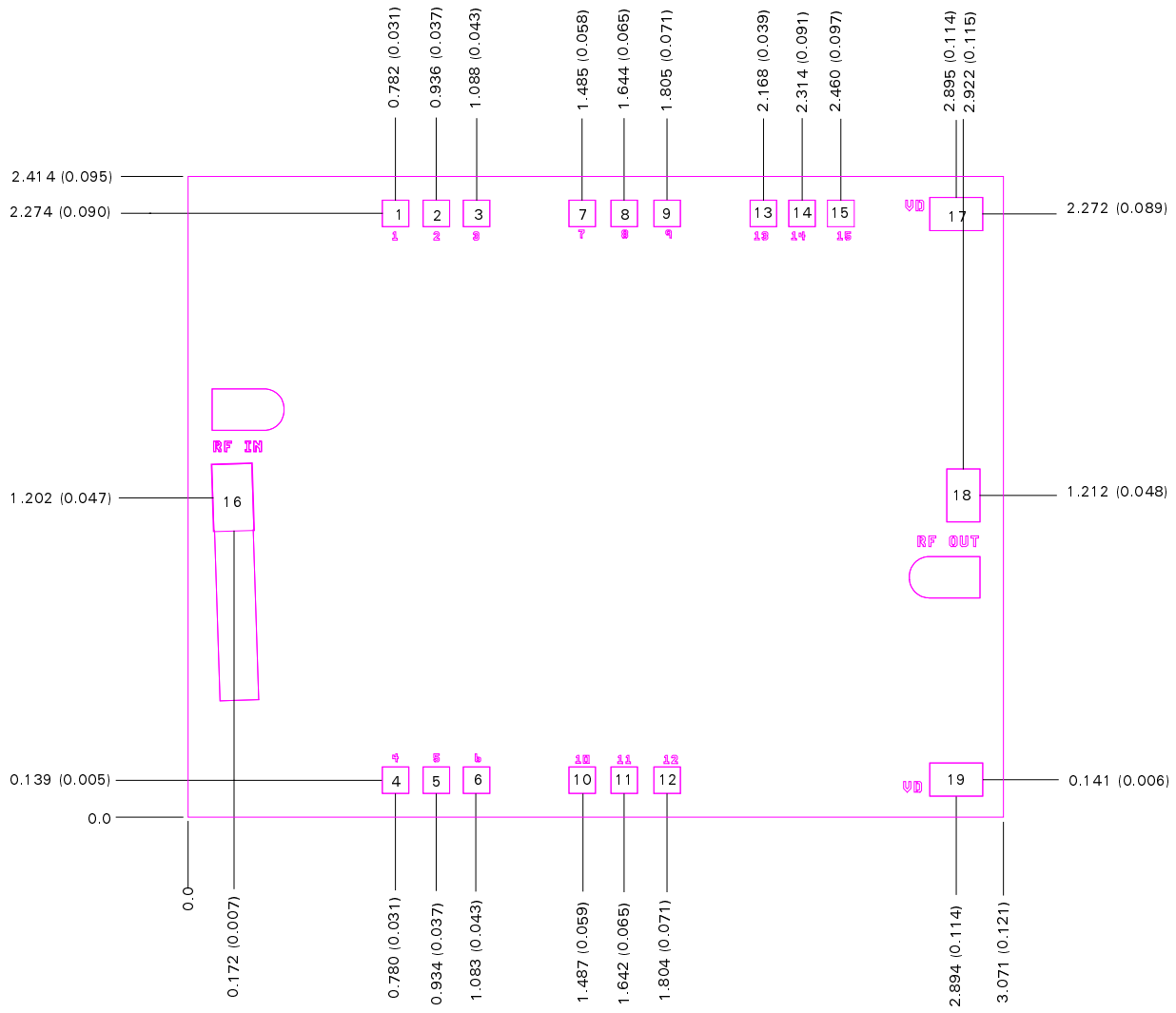
Mechanical Drawing

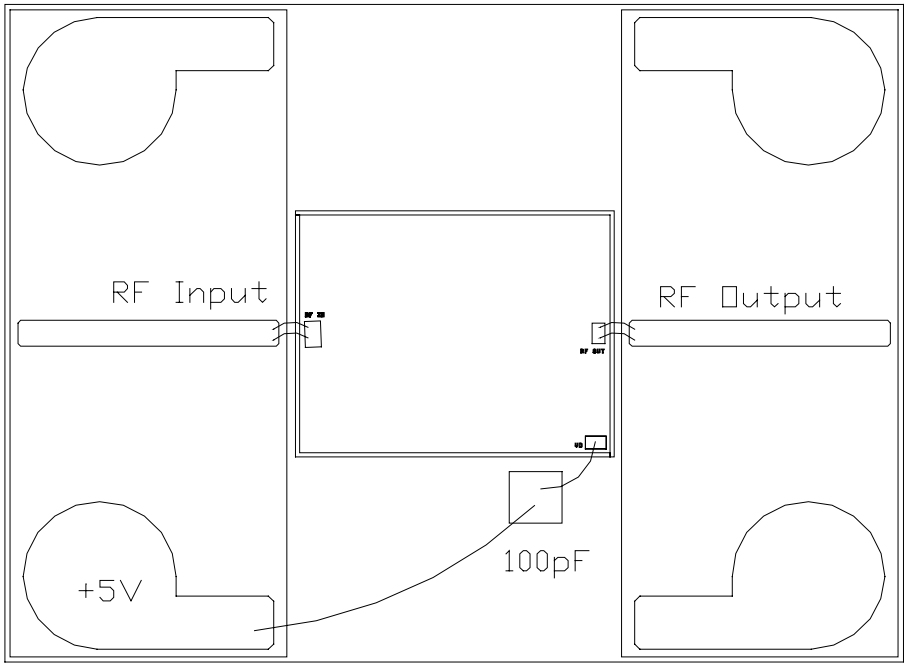


Units: millimeters (inches)
Thickness: 0.150 (0.006)
Chip edge to bond pad dimensions are shown to center of bond pad
Chip size tolerance: +/- 0.05 (0.002)

Bond Pad #1 ~ #15 (R1 ~ R15)	0.100 x 0.100 (0.004 x 0.004)
Bond Pad #16 (RF Input)	0.152 x 0.252 (0.006 x 0.010)
Bond Pad #17 (VD)	0.125 x 0.200 (0.005 x 0.008)
Bond Pad #18 (RF Output)	0.125 x 0.200 (0.005 x 0.008)
Bond Pad #19 (VD)	0.125 x 0.200 (0.005 x 0.008)

GaAs MMIC devices are susceptible to damage from Electrostatic Discharge. Proper precautions should be observed during handling, assembly and test.

Recommended Assembly Layout



Assembly Process Notes

Reflow process assembly notes:

- Use AuSn (80/20) solder with limited exposure to temperatures at or above 300 °C.
- An alloy station or conveyor furnace with reducing atmosphere should be used.
- No fluxes should be utilized.
- Coefficient of thermal expansion matching is critical for long-term reliability.
- Devices must be stored in a dry nitrogen atmosphere.

Component placement and adhesive attachment assembly notes:

- Vacuum pencils and/or vacuum collets are the preferred method of pick up.
- Air bridges must be avoided during placement.
- The force impact is critical during auto placement.
- Organic attachment can be used in low-power applications.
- Curing should be done in a convection oven; proper exhaust is a safety concern.
- Microwave or radiant curing should not be used because of differential heating.
- Coefficient of thermal expansion matching is critical.

Interconnect process assembly notes:

- Thermosonic ball bonding is the preferred interconnect technique.
- Force, time, and ultrasonics are critical parameters.
- Aluminum wire should not be used.
- Discrete FET devices with small pad sizes should be bonded with 0.0007-inch wire.
- Maximum stage temperature is 200 °C.

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