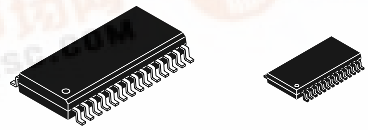


SLAS289B – OCTOBER 2001 – REVISED FEBRUARY 2002

# 10-Bit, 40-MSPS ANALOG-TO-DIGITAL CONVERTER WITH PGA AND CLAMP

## FEATURES

- **Analog Supply 3 V**
- **Digital Supply 3 V**
- **Configurable Input Functions:**
  - **Single-Ended**
  - **Single-Ended With Analog Clamp**
  - **Single-Ended With Programmable Digital Clamp**
  - **Differential**
- **Built-In Programmable Gain Amplifier (PGA)**
- **Differential Nonlinearity: ±0.45 LSB**
- **Signal-to-Noise: 60 dB Typ at 4.8 MHz**
- **Spurious Free Dynamic Range: 72 dB**
- **Adjustable Internal Voltage Reference**
- **Unsigned Binary/2s Complement Output**
- **Out-of-Range Indicator**
- **Power-Down Mode**

## APPLICATIONS

- **Video/CCD Imaging**
- **Communications**
- **Set-Top-Box**
- **Medical**

## DESCRIPTION

The THS1041 is a CMOS, low power, 10-bit, 40 MSPS analog-to-digital converter (ADC) that operates from a single 3-V supply. The THS1041 has been designed to give circuit developers flexibility. The analog input to the THS1041 can be either single-ended or differential. This device has a built-in clamp amplifier whose clamp input level can be driven from an external dc source or from an internal high-precision 10-bit digital clamp level programmable via an internal CLAMP register. A 3-bit PGA is included to maintain SNR for small signals. The THS1041 provides a wide selection of voltage references to match the user's design requirements. For more design flexibility, the internal reference can be bypassed to use an external reference to suit the dc accuracy and temperature drift requirements of the application. The out-of-range output indicates any out-of-range condition in THS1041's input signal. The format of the digital output can be coded in either unsigned binary or 2s complement.

The speed, resolution, and single-supply operation of the THS1041 are suited to applications in set-top-box (STB), video, multimedia, imaging, high-speed acquisition, and communications. The built-in clamp function allows dc restoration of a video signal and is suitable for video applications. The speed and resolution ideally suit charge-couple device (CCD) input systems such as color scanners, digital copiers, digital cameras, and camcorders. A wide input voltage range allows the THS1041 to be applied in both imaging and communications systems.

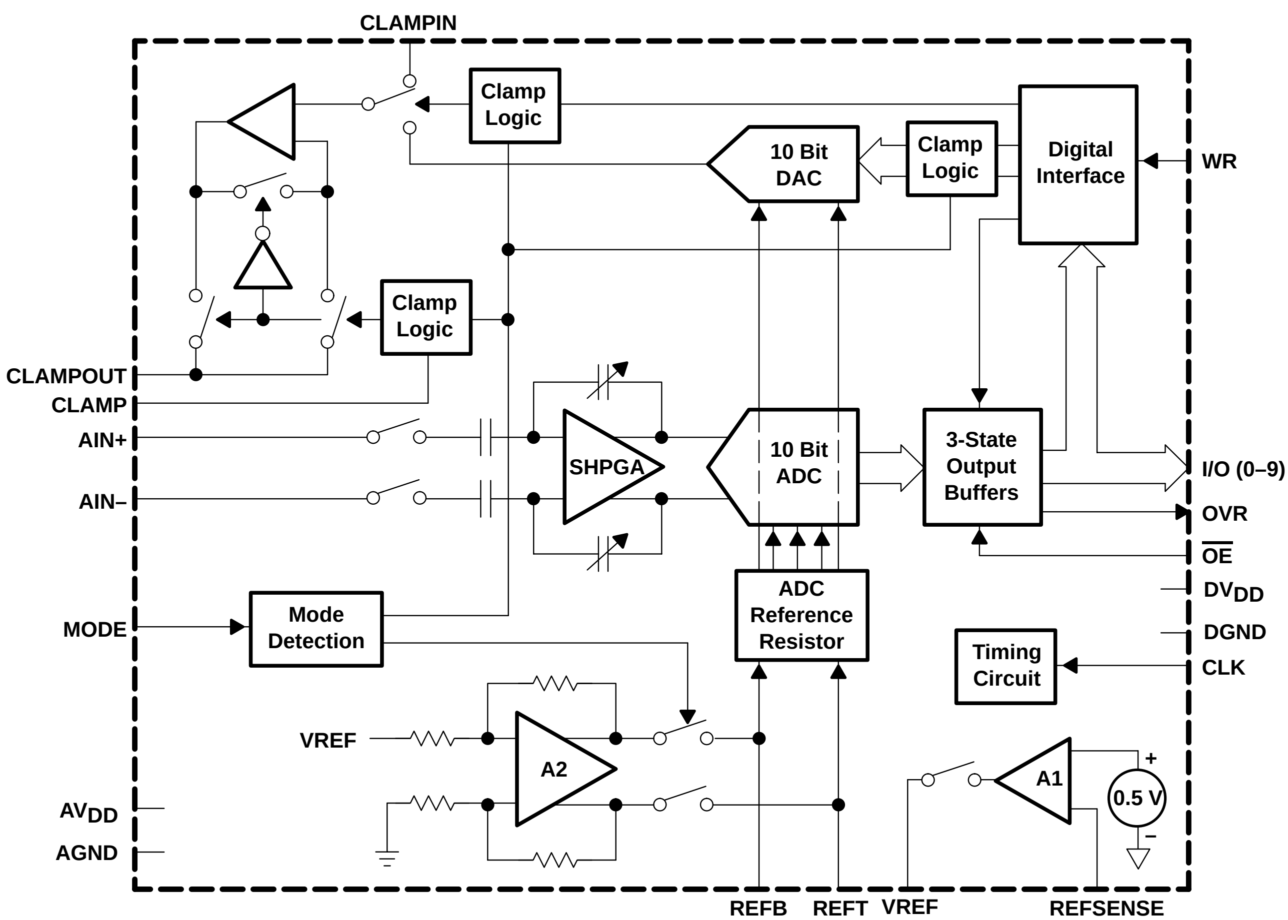
The THS1041C is characterized for operation from 0°C to 70°C, while the THS1041I is characterized for operation from –40°C to 85°C.

**28-PIN TSSOP/SOIC PACKAGE (TOP VIEW)**

**AVAILABLE OPTIONS**

| $T_A$ | PACKAGED DEVICES | |
|---|---|---|
| | 28-TSSOP (PW) | 28-SOIC (DW) |
| 0°C to 70°C | THS1041CPW | THS1041CDW |
| –40°C to 85°C | THS1041IPW | THS1041IDW |

## functional block diagram




NOTE: A1 – Internal bandgap reference
A2 – Internal ADC reference generator

## Terminal Functions

| TERMINAL NAME | TERMINAL NO. | I/O | DESCRIPTION |
|---|---|---|---|
| AGND | 1 | I | Analog ground |
| AIN+ | 27 | I | Positive analog input |
| AIN– | 25 | I | Negative analog input |
| $AV_{DD}$ | 28 | I | Analog supply |
| CLAMP | 19 | I | High to enable clamp mode, low to disable clamp mode |
| CLAMPIN | 20 | I | Connect to an external analog clamp reference input. |
| CLAMPOUT | 21 | O | The CLAMPOUT pin can provide a dc restoration or a bias source function (see AC reference generation section). If neither function is required then the clamp can be disabled to save power (see power management section). |
| CLK | 15 | I | Clock input |
| DGND | 14 | I | Digital ground |
| $DV_{DD}$ | 2 | I | Digital supply |
| I/O0<br>I/O1<br>I/O2<br>I/O3<br>I/O4<br>I/O5<br>I/O6<br>I/O7<br>I/O8<br>I/O9 | 3<br>4<br>5<br>6<br>7<br>8<br>9<br>10<br>11<br>12 | I/O | Digital I/O bit 0 (LSB)<br>Digital I/O bit 1<br>Digital I/O bit 2<br>Digital I/O bit 3<br>Digital I/O bit 4<br>Digital I/O bit 5<br>Digital I/O bit 6<br>Digital I/O bit 7<br>Digital I/O bit 8<br>Digital I/O bit 9 (MSB) |
| MODE | 23 | I | Operating mode select (AGND, $AV_{DD}/2$, $AV_{DD}$) |
| $\overline{OE}$ | 16 | I | High to high-impedance state the data bus, low to enable the data bus |
| OVR | 13 | O | Out-of-range indicator |
| REFB | 24 | I/O | Bottom ADC reference voltage |
| REFSENSE | 18 | I | VREF mode control |
| REFT | 22 | I/O | Top ADC reference voltage |
| VREF | 26 | I/O | Internal or external reference |
| WR | 17 | I | Write strobe |

## absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range: $AV_{DD}$ to AGND, $DV_{DD}$ to DGND . . . . . . . . . . –0.3 V to 4 V
AGND to DGND . . . . . . . . . . –0.3 V to 0.3 V
$AV_{DD}$ to $DV_{DD}$ . . . . . . . . . . –4 V to 4 V
MODE input voltage range, MODE to AGND . . . . . . . . . . –0.3 V to $AV_{DD}$ + 0.3 V
Reference voltage input range, REFT, REFB, to AGND . . . . . . . . . . –0.3 V to $AV_{DD}$ + 0.3 V
Analog input voltage range, AIN to AGND . . . . . . . . . . –0.3 V to $AV_{DD}$ + 0.3 V
Reference input voltage range, VREF to AGND . . . . . . . . . . –0.3 V to $AV_{DD}$ + 0.3 V
Reference output voltage range, VREF to AGND . . . . . . . . . . –0.3 V to $AV_{DD}$ + 0.3 V
Clock input voltage range, CLK to AGND . . . . . . . . . . –0.3 V to $AV_{DD}$ + 0.3 V
Digital input voltage range, digital input to DGND . . . . . . . . . . –0.3 V to $DV_{DD}$ + 0.3 V
Digital output voltage range, digital output to DGND . . . . . . . . . . –0.3 V to $DV_{DD}$ + 0.3 V
Operating junction temperature range, $T_J$ . . . . . . . . . . 0°C to 150°C
Storage temperature range, $T_{stg}$ . . . . . . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 in) from case for 10 seconds . . . . . . . . . . 300°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## recommended operating conditions

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Supply voltage, $AV_{DD}$, $DV_{DD}$ | | 3 | 3 | 3.6 | V |
| High-level digital input, $V_{IH}$ | | $DV_{DD}$ | | $DV_{DD}$ | V |
| Low-level digital input, $V_{IL}$ | | DGND | | DGND | V |
| Minimum digital output load resistance, $R_L$ | | 100 | | | kΩ |
| Maximum digital output load capacitance, $C_L$ | | | | 10 | pF |
| Clock frequency, $f_{clk}$ | | 5 | | 40 | MHz |
| Clock duty cycle | | 45% | 50% | 55% | |
| Operating free-air temperature | THS1041C | 0 | 25 | 70 | °C |
| | THS1041I | –40 | 25 | 85 | |

## electrical characteristics over recommended operating conditions, $AV_{DD}$ = 3 V, $DV_{DD}$ = 3 V, $f_S$ = 40 MSPS/50% duty cycle, MODE = $AV_{DD}$ (internal reference), differential input range = 1 Vpp and 2 Vpp, PGA = 1X, $T_A$ = $T_{min}$ to $T_{max}$ (unless otherwise noted)

### dc accuracy

| PARAMETER | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| | Resolution | | 10 | | Bits |
| INL | Integral nonlinearity (see definitions) | | ±0.75 | ±1.5 | LSB |
| DNL | Differential nonlinearity (see definitions) | | ±0.3 | ±1 | LSB |
| | Zero error (see definitions) | | 0.7 | 1.5 | %FSR |
| | Full-scale error (see definitions) | | 2.2 | 3 | %FSR |
| | Missing code | No missing code assured | | | |

## electrical characteristics over recommended operating conditions, $AV_{DD}$ = 3 V, $DV_{DD}$ = 3 V, $f_s$ = 40 MSPS/50% duty cycle, MODE = $AV_{DD}$ (internal reference), differential input range = 1 Vpp and 2 Vpp, PGA = 1X, $T_A$ = $T_{min}$ to $T_{max}$ (unless otherwise noted) (continued)

### power supply

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $AV_{DD}$ | Supply voltage | | 3 | 3 | 3.6 | V |
| $DV_{DD}$ | Supply voltage | | 3 | 3 | 3.6 | V |
| $I_{CC}$ | Operating supply current | All circuits active, See Note 1 | | 34 | 42 | mA |
| $P_D$ | Power dissipation | All circuits active | | 103 | 125 | mW |
| $P_{D(STBY)}$ | Standby power | | | 75 | | μW |
| | Power up time for all references from standby, $t_{(PU)}$ | | | 770 | | μs |
| | Wake-up time, $t_{(WU)}$ | See Note 2 | | 45 | | μs |

NOTES: 1. Actual values will vary slightly depending on application clamp load, VREF load, etc.
2. Wake-up time is from the power-down state to accurate ADC samples being taken and is specified for MODE = AGND with external reference sources applied to the device at the time of release of power-down and an applied 40-MHz clock. Circuits that need to power up are the bandgap, bias generator, ADC, and SHPGA.

### analog inputs

| | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|
| Differential analog input voltage, $V_{I(AIN)}$ = AIN+ – AIN– | –1 | | 1 | V |
| Reference input voltage, $V_{I(VREF)}$ | 0.5 | | 1 | V |
| Clamp input voltage, $V_{I(CLAMPIN)}$ | 0.1 | | $AV_{DD}$–0.1 | V |

### REFT, REFB external ADC reference voltages inputs (MODE = AGND)

| PARAMETER | TEST CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Reference input voltage, REFT–REFB | | 0.5 | | 1 | V |
| Reference common mode voltage, (REFT + REFB)/2 | $AV_{DD}$ = 3 | | 1.5 | | V |
| Input resistance between REFT and REFB | | | 1.9 | | kΩ |

### REFT, REFB internal ADC reference voltages outputs (MODE = $AV_{DD}$ or $AV_{DD}$/2)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| Reference voltage top, REFT | VREF = 0.5 V | $AV_{DD}$ = 3 V | | 1.75 | | V |
| | VREF = 1 V | | | 2 | | |
| Refence voltage bottom, REFB | VREF = 0.5 V | $AV_{DD}$ = 3 V | | 1.25 | | V |
| | VREF = 1 V | | | 1 | | |

### VREF (on-chip voltage reference generator)

| PARAMETER | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|
| Internal 0.5-V reference voltage (REFSENSE = VREF) | 0.45 | 0.5 | 0.55 | V |
| Internal 1-V reference voltage (REFSENSE = AGND) | 0.95 | 1 | 1.05 | V |
| External reference voltage (REFSENSE = $AV_{DD}$) | 0.5 | | 1 | V |
| Reference input resistance (REFSENSE = $AV_{DD}$, MODE = $AV_{DD}$/2 or $AV_{DD}$) | | 14 | | kΩ |

## electrical characteristics over recommended operating conditions, $AV_{DD}$ = 3 V, $DV_{DD}$ = 3 V, $f_S$ = 40 MSPS/50% duty cycle, MODE = $AV_{DD}$ (internal reference), differential input range = 1 Vpp and 2 Vpp, PGA = 1X, $T_A$ = $T_{min}$ to $T_{max}$ (unless otherwise noted) (continued)

### dynamic performance (ADC and PGA)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| ENOB | Effective number of bits | f = 4.8 MHz, –0.5 dBFS | 8.8 | 9.6 | | Bits |
| | | f = 20 MHz, –0.5 dBFS | | 9.5 | | |
| SFDR | Spurious free dynamic range | f = 4.8 MHz, –0.5 dBFS | 60.5 | 72 | | dB |
| | | f = 20 MHz, –0.5 dBFS | | 70 | | |
| THD | Total harmonic distortion | f = 4.8 MHz, –0.5 dBFS | | –72.5 | –61.3 | dB |
| | | f = 20 MHz, –0.5 dBFS | | –71.6 | | |
| SNR | Signal-to-noise ratio | f = 4.8 MHz, –0.5 dBFS | 55.7 | 60 | | dB |
| | | f = 20 MHz, –0.5 dBFS | | 57 | | |
| SINAD | Signal-to-noise and distortion | f = 4.8 MHz, –0.5 dBFS | 55.6 | 59.7 | | dB |
| | | f = 20 MHz, –0.5 dBFS | | 59.6 | | |
| BW | Full power bandwidth (–3 dB) | | | 900 | | MHz |

### PGA

| PARAMETER | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|
| Gain range (linear scale) | 0.5 | | 4 | V/V |
| Gain step size (linear scale) | | 0.5 | | V/V |
| Gain error (deviation from ideal, all gain settings) | –3% | | 3% | |
| Number of control bits | | 3 | | Bits |

### clamp amplifier and clamp DAC

| PARAMETER | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|
| Resolution | | 10 | | Bits |
| DAC output range | REFB | | REFT | V |
| DAC differential nonlinearity | –1 | | 1 | LSB |
| DAC integral nonlinearity | | ±1 | | LSB |
| Clamping analog output voltage range | 0.1 | | $AV_{DD}$–0.1 | V |
| Clamping analog output voltage error | –40 | | 40 | mV |

NOTE: The CLAMPOUT pin must see a load capacitance of at least 10 nF to ensure stability of the on-chip clamp buffer. When using the clamp for dc restoration, the signal coupling capacitor should be at least 10 nF. When using the clamp buffer as a dc biasing reference, CLAMPOUT should be decoupled to analog ground through at least a 10-nF capacitor.

## electrical characteristics over recommended operating conditions, $AV_{DD}$ = 3 V, $DV_{DD}$ = 3 V, $f_s$ = 40 MSPS/50% duty cycle, MODE = $AV_{DD}$ (internal reference), differential input range = 1 Vpp and 2 Vpp, PGA = 1X, $T_A = T_{min}$ to $T_{max}$ (unless otherwise noted) (continued)

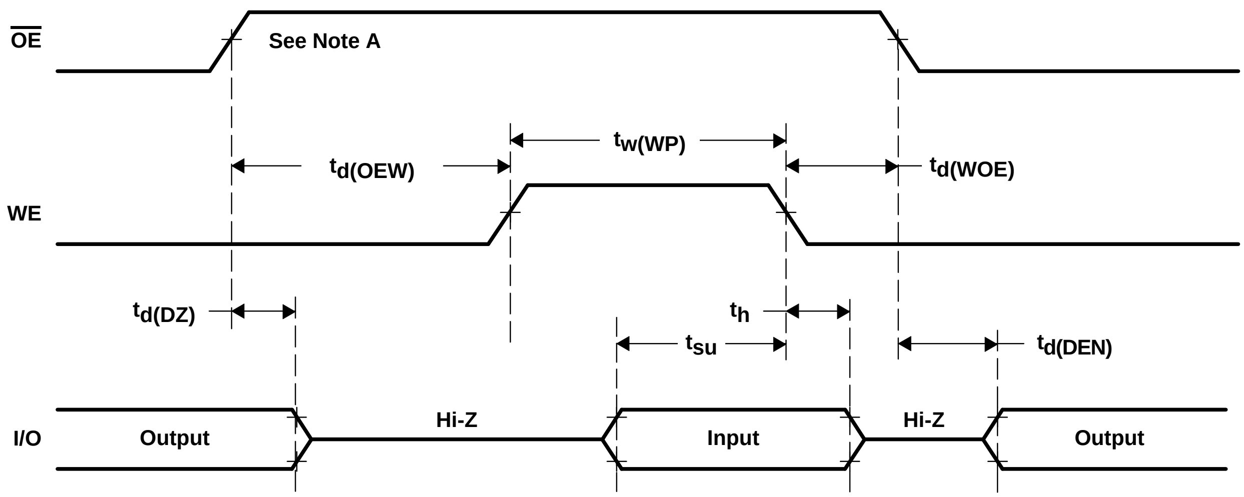
### digital specifications

| PARAMETER | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| **Digital Inputs** | | | | | | |
| $V_{IH}$ | High-level input voltage | Clock input | $0.8 \times AV_{DD}$ | | | V |
| | | All other inputs | $0.8 \times DV_{DD}$ | | | |
| $V_{IL}$ | Low-level input voltage | Clock input | | | $0.2 \times AV_{DD}$ | V |
| | | All other inputs | | | $0.2 \times DV_{DD}$ | |
| $I_{IH}$ | High-level input current | | | | 1 | µA |
| $I_{IL}$ | Low-level input current | | | | \|–1\| | µA |
| $C_i$ | Input capacitance | | | 5 | | pF |
| **Digital Outputs** | | | | | | |
| $V_{OH}$ | High-level output voltage | $I_{load}$ = 50 µA | $DV_{DD}$–0.4 | | | V |
| $V_{OL}$ | Low-level output voltage | $I_{load}$ = 50 µA | | | 0.4 | V |
| | High impedance output current | | | | ±1 | µA |
| | Rise/fall time | $C_{load}$ = 15 pF | | 3.5 | | ns |
| **Clock Input** | | | | | | |
| $t_c$ | Clock cycle | | 25 | | 200 | ns |
| $t_{w(CKH)}$ | Pulse duration, clock high | | 11.25 | | 110 | ns |
| $t_{w(CKL)}$ | Pulse duration, clock low | | 11.25 | | 110 | ns |
| | Clock duty cycle | | 45% | 50% | 55% | |
| $t_{d(o)}$ | Clock to data valid, delay time | | | 9.5 | 16 | ns |
| | Pipeline latency | | | 4 | | Cycles |
| $t_{d(AP)}$ | Aperture delay time | | | 0.1 | | ns |
| | Aperture uncertainty (jitter) | | | 1 | | ps |

### timing

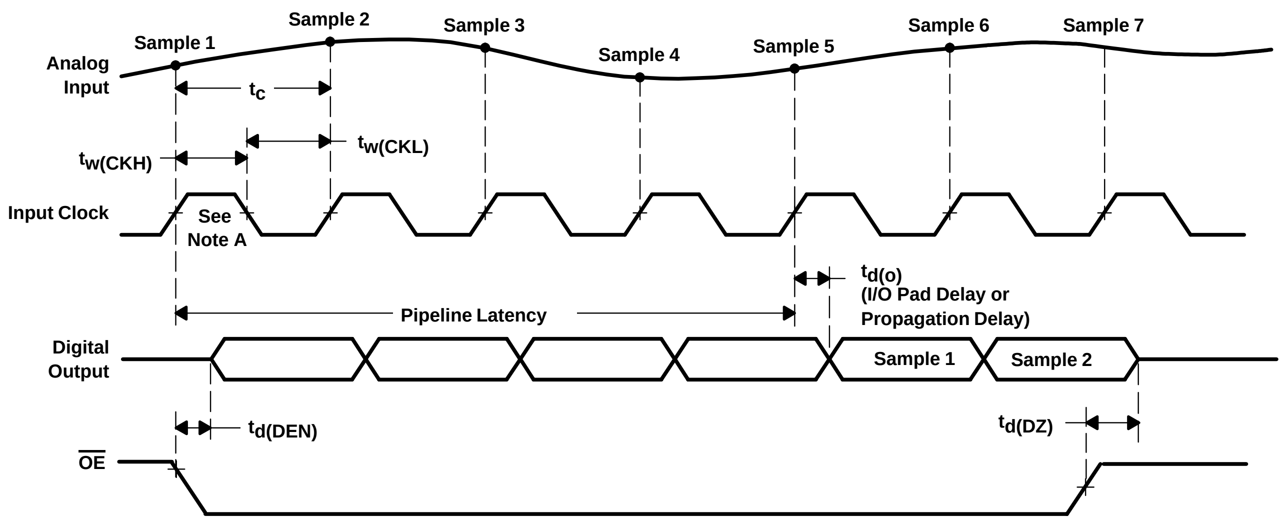
| PARAMETER | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $t_{d(DZ)}$ | Output disable to Hi-Z output, delay time | 0 | | 10 | ns |
| $t_{d(DEN)}$ | Output enable to output valid, delay time | 0 | | 10 | ns |
| $t_{d(OEW)}$ | Output disable to write enable, delay time | 12 | | | ns |
| $t_{d(WOE)}$ | Write disable to output enable, delay time | 12 | | | ns |
| $t_{w(WP)}$ | Write pulse duration | 15 | | | ns |
| $t_{su}$ | Input data setup time | 5 | | | ns |
| $t_h$ | Input data hold time | 5 | | | ns |

## PARAMETER MEASUREMENT INFORMATION




NOTE A: All timing measurements are based on 50% of edge transition.

**Figure 1. Write Timing Diagram**




NOTE A: All timing measurements are based on 50% of edge transition.

**Figure 2. Digital Output Timing Diagram**

## TYPICAL CHARACTERISTICS

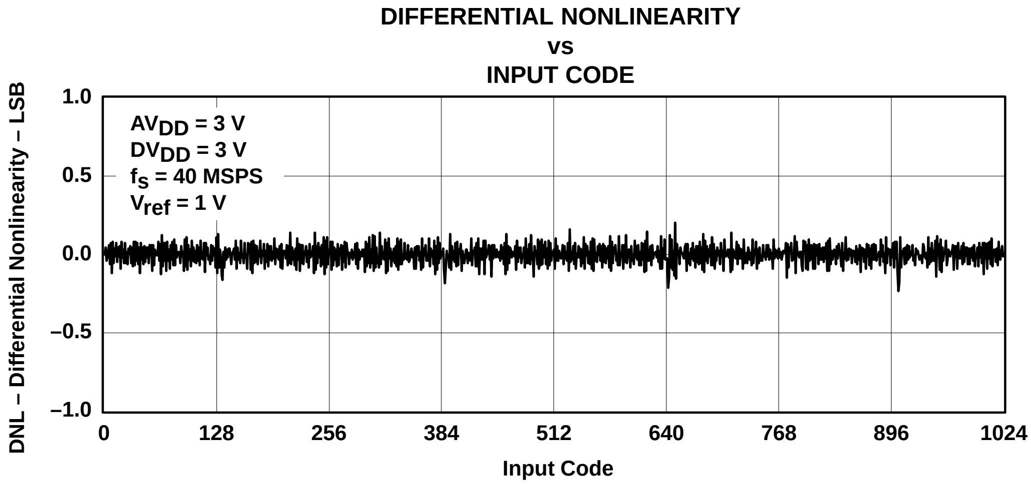



Figure 3

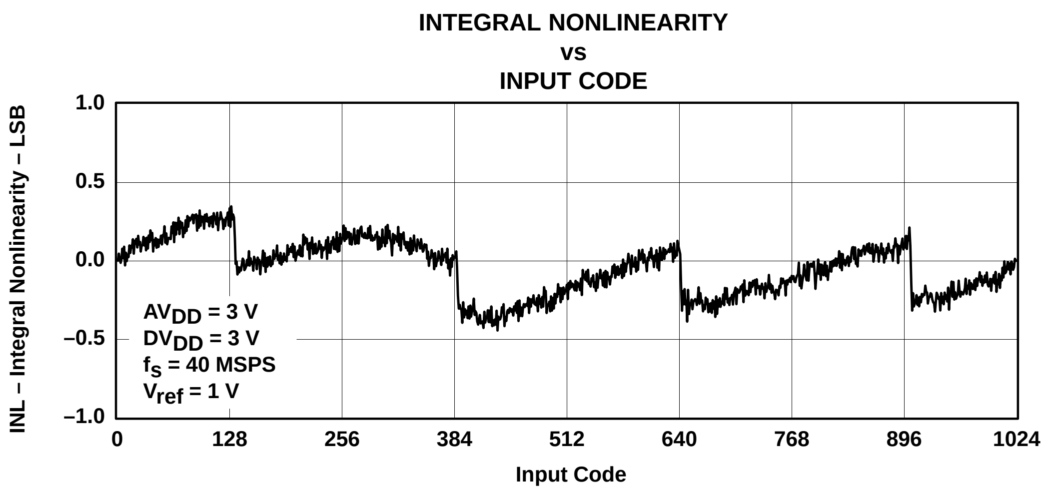



Figure 4

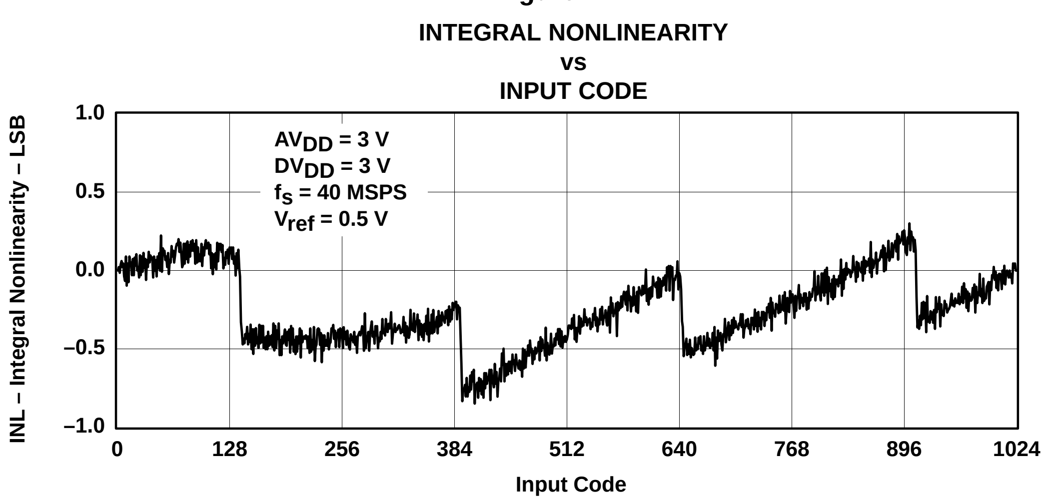



Figure 5

## TYPICAL CHARACTERISTICS

**TOTAL HARMONIC DISTORTION vs INPUT FREQUENCY**

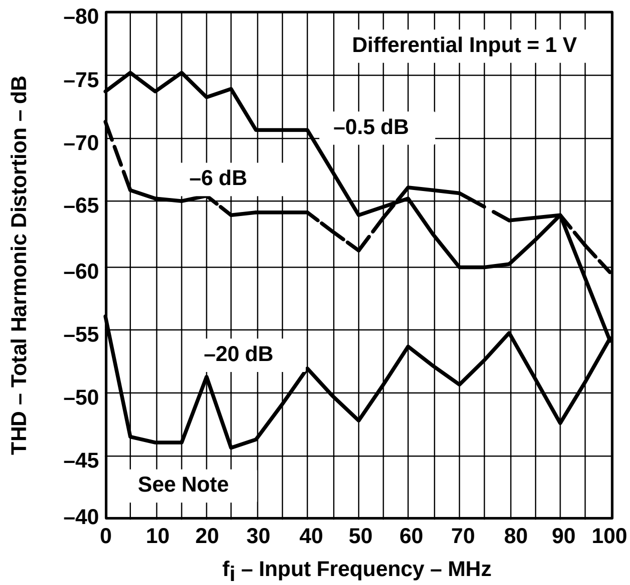



**Figure 6**

**TOTAL HARMONIC DISTORTION vs INPUT FREQUENCY**

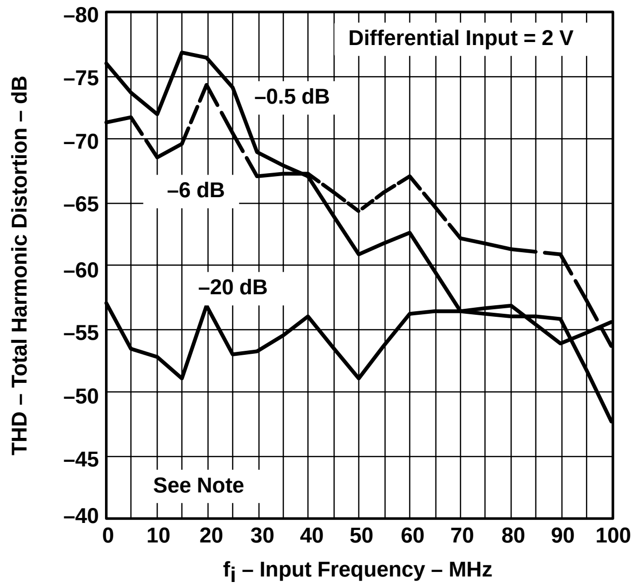



**Figure 7**

**SIGNAL-TO-NOISE RATIO vs INPUT FREQUENCY**

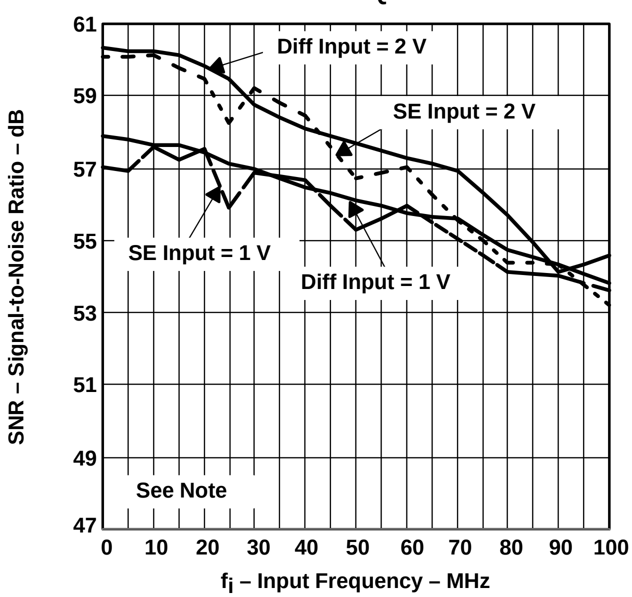



**Figure 8**

**SPURIOUS FREE DYNAMIC RANGE vs INPUT FREQUENCY**

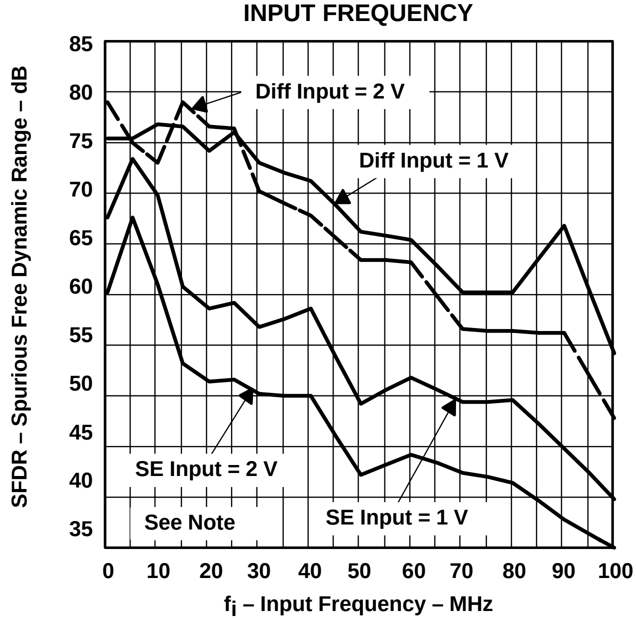



**Figure 9**

NOTE: $AV_{DD} = DV_{DD} = 3$ V, CLK = 40 MSPS, PGA = 1, 20-pF capacitors AIN+ to AGND and AIN– to AGND,
Input series resistor = 25 Ω,
2-V Input: Ext Ref, REFT = 2 V, REFB = 1 V
1-V Input: Ext Ref, REFT = 1.75 V, REFB = 1.25 V

## TYPICAL CHARACTERISTICS

**SIGNAL-TO-NOISE PLUS DISTORTION vs INPUT FREQUENCY**

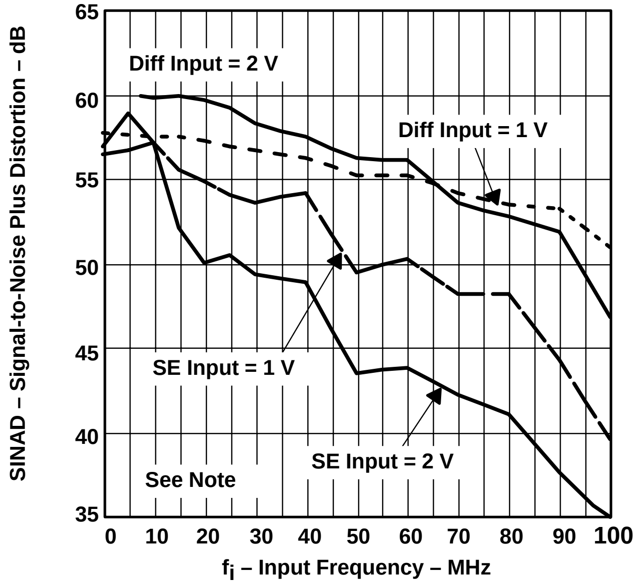



**Figure 10**

**TOTAL HARMONIC DISTORTION vs INPUT FREQUENCY**

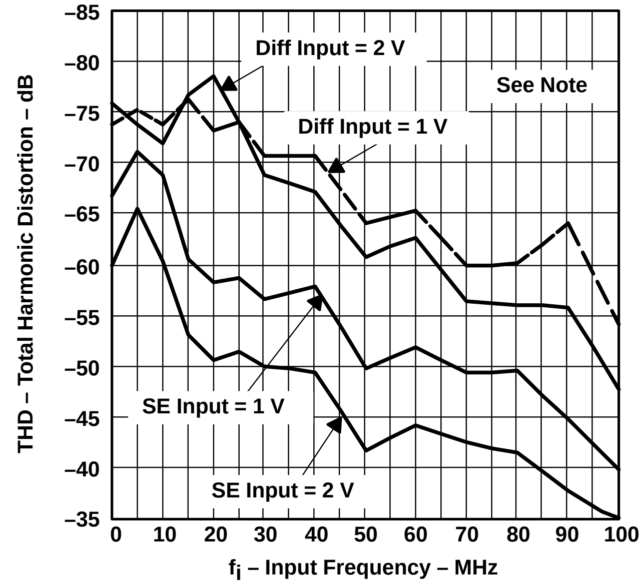



**Figure 11**

NOTE: $AV_{DD} = DV_{DD}$ = 3 V, CLK = 40 MSPS, PGA = 1, 20-pF capacitors AIN+ to AGND and AIN– to AGND, Input series resistor = 25 Ω,
2-V Input: Ext Ref, REFT = 2 V, REFB = 1 V
1-V Input: Ext Ref, REFT = 1.75 V, REFB = 1.25 V

**TOTAL HARMONIC DISTORTION vs SAMPLE RATE**

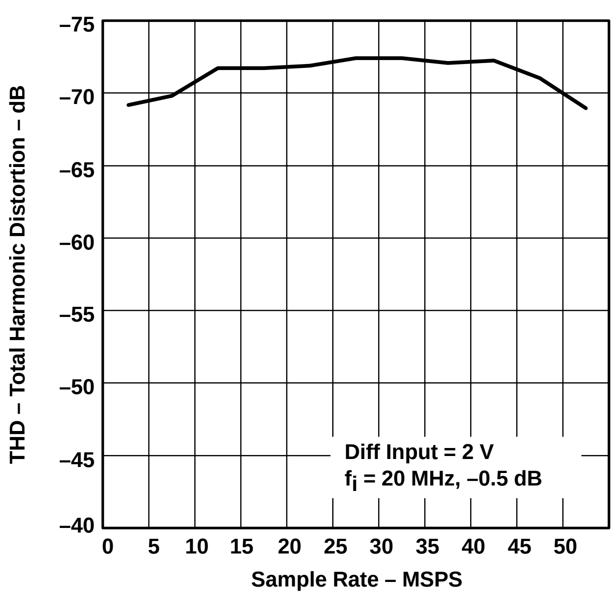



**Figure 12**

**SIGNAL-TO-NOISE RATIO vs SAMPLE RATE**

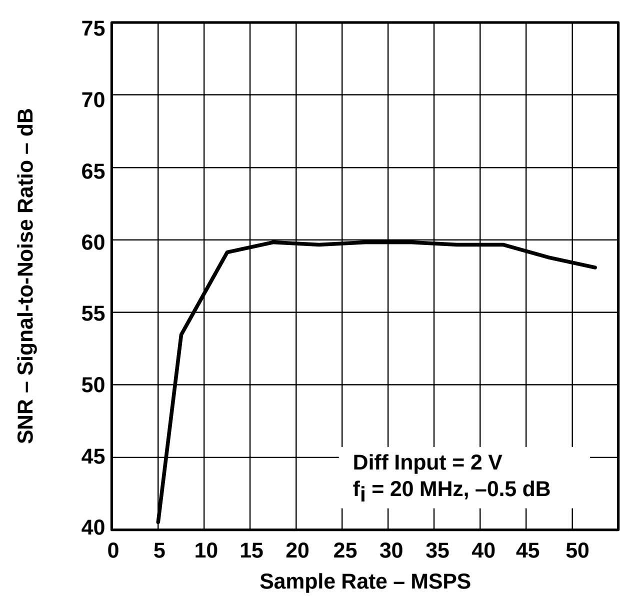



**Figure 13**

# TYPICAL CHARACTERISTICS

**SPURIOUS FREE DYNAMIC RANGE**
**vs**
**SUPPLY VOLTAGE**

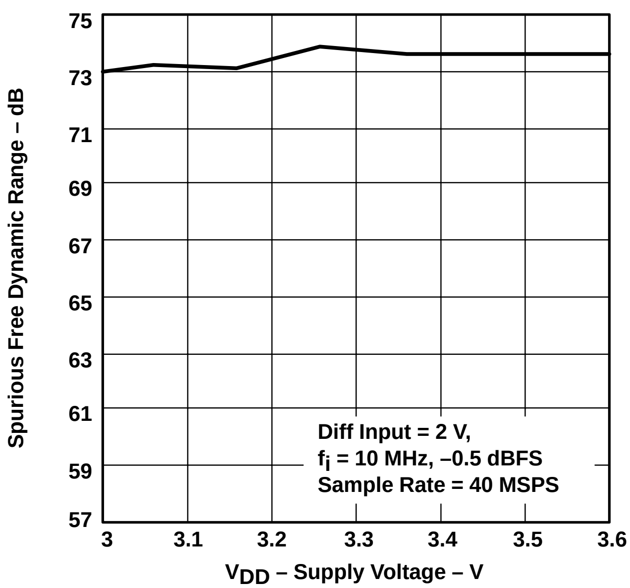



**Figure 14**

**TOTAL HARMONIC DISTORTION**
**vs**
**SUPPLY VOLTAGE**

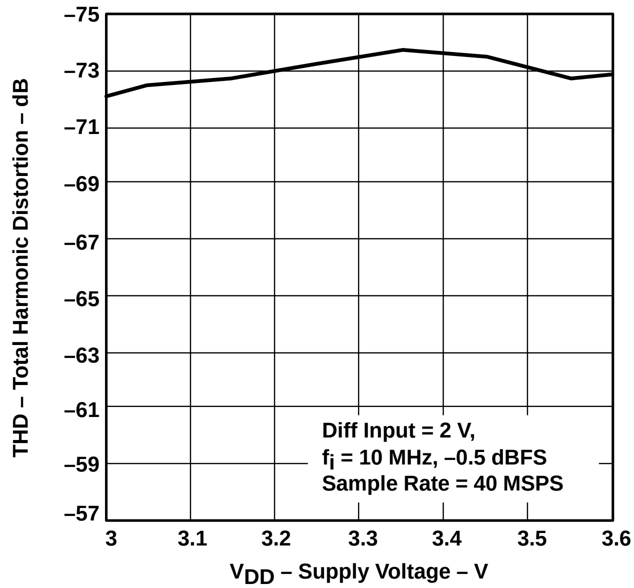



**Figure 15**

**SIGNAL-TO-NOISE RATIO**
**vs**
**SUPPLY VOLTAGE**

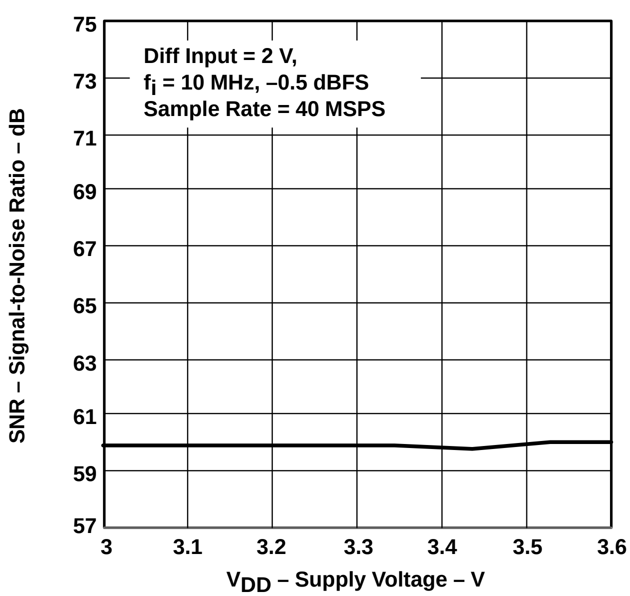



**Figure 16**

**SIGNAL-TO-NOISE PLUS DISTORTION**
**vs**
**SUPPLY VOLTAGE**

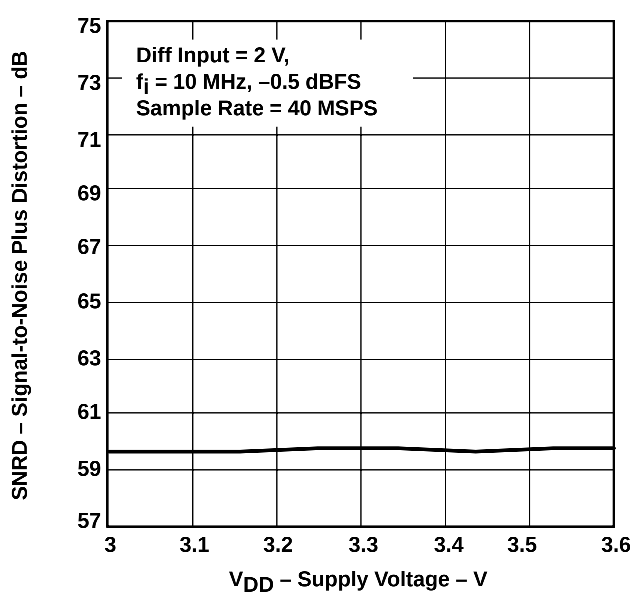



**Figure 17**

## TYPICAL CHARACTERISTICS

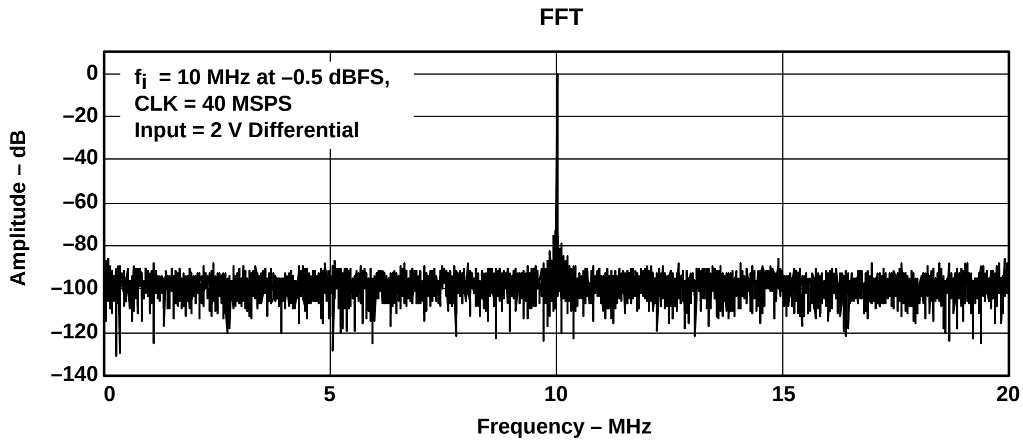



Figure 18

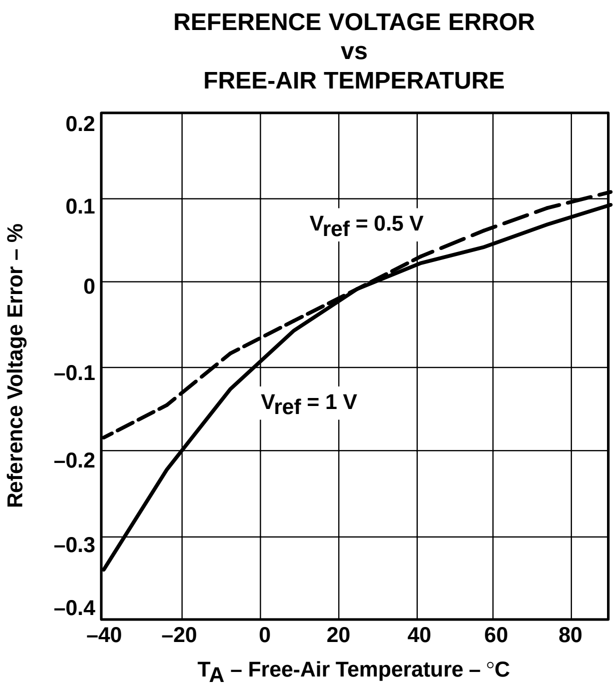



Figure 19

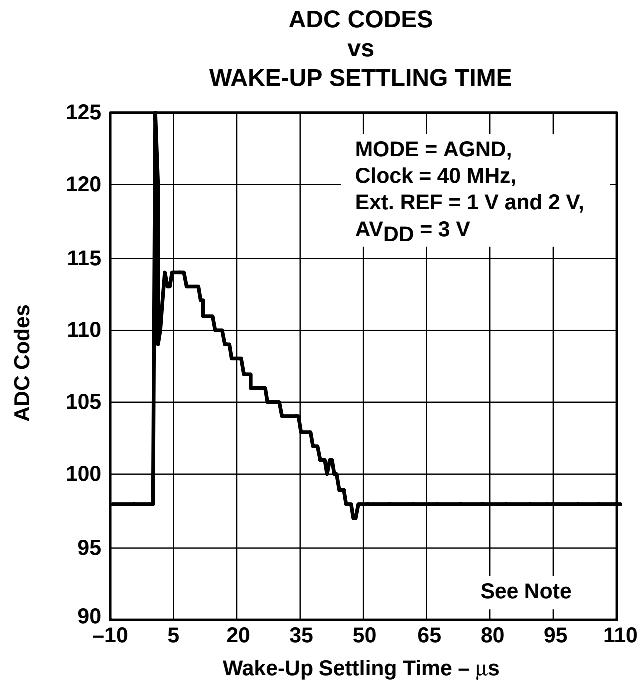



Figure 20

NOTE: See wake-up time in definitions at the end of this data sheet.

## TYPICAL CHARACTERISTICS

POWER-UP TIME FOR INTERNAL REFERENCE VOLTAGE FROM STANDBY

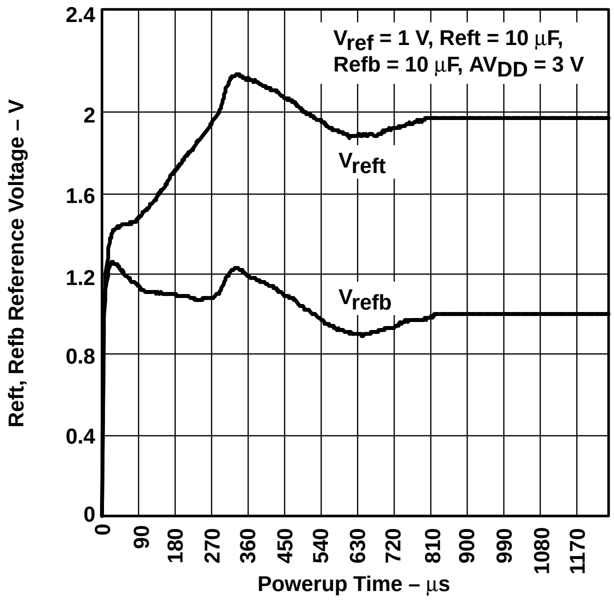



Figure 21

POWER DISSIPATION vs SAMPLE RATE

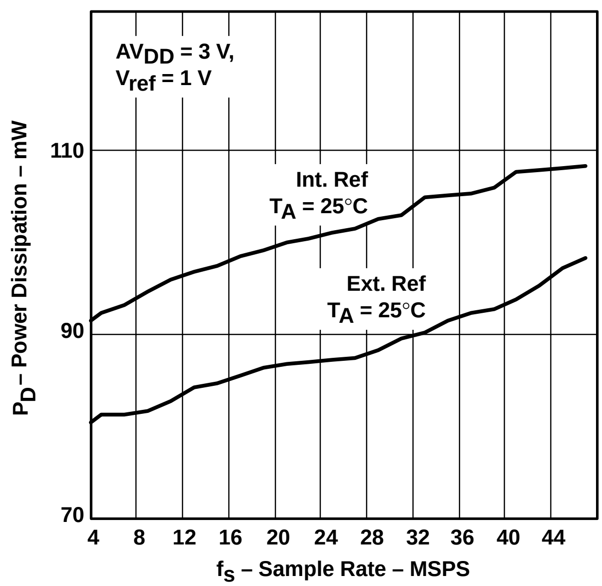



Figure 22

INPUT BANDWIDTH

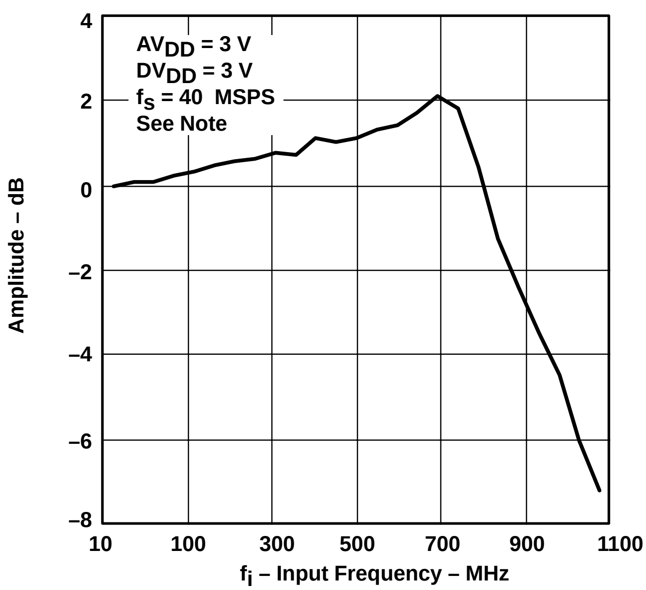



Figure 23

EFFECTIVE NUMBER OF BITS vs FREE-AIR TEMPERATURE

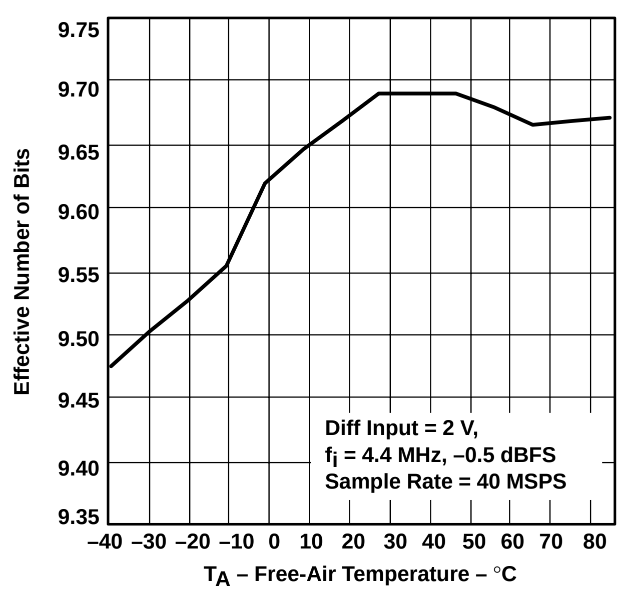



Figure 24

NOTE: No series resistors and no bypass capacitors at AIN+ and AIN– inputs

## PRINCIPLES OF OPERATION

### functional overview

Refer to functional block diagram. A single-ended, sample rate clock is required at pin CLK for device operation. Analog inputs AIN+ and AIN– are sampled on each rising edge of CLK in a switched capacitor sample and hold unit, the output of which feeds a programmable gain amplifier (PGA) to the ADC core, where analog-to-digital conversion is performed against the ADC reference voltages REFT and REFB.

Internal or external ADC reference voltage configurations are selected by connecting the MODE pin appropriately. When MODE = AGND, the user must provide external sources at pins REFB and REFT. When MODE = $AV_{DD}$ or MODE = $AV_{DD}/2$, an internal ADC references generator (A2) is enabled, which drives the REFT and REFB pins using the voltage at pin VREF as its input. The user can choose to drive VREF from the internal bandgap reference, or they can disable A1 and provide their own reference voltage at pin VREF.

On the fourth rising CLK edge following the edge that sampled AIN+ and AIN–, the conversion result is output via data pins I/O0 to I/O9. The output buffers can be disabled by pulling pin $\overline{\text{OE}}$ high, allowing the user to place device configuration data on the data pins, which are then latched into the internal control registers by strobing the WR pin high then low. The internal registers control the data output format (unsigned or twos complement), the PGA gain, device powerdown, and the clamp functions.

The THS1041 offers a clamp circuit suitable for dc restoration of ac-coupled signals. The clamp voltage level can be set using an external reference applied to the CLAMPIN pin, or it can be set to a reference level provided by an on-chip 10-bit DAC. The CLAMPOUT pin must be connected externally to AIN+ or AIN– in applications requiring the clamp function.

The following sections explain further:

- How signals flow from AIN+ and AIN– to the ADC core, and how the reference voltages at REFT and REFB set the ADC input range and hence the input range at AIN+ and AIN–
- How to set the ADC references REFT and REFB using external sources or the internal ADC reference buffer (A2) to match the device input range to the input signal
- How to set the output of the internal bandgap reference (A1) if required
- How to use the clamp and device control registers

### signal processing chain (sample and hold, PGA, ADC)

Figure 25 shows the signal flow through the sample and hold unit and the PGA to the ADC core.

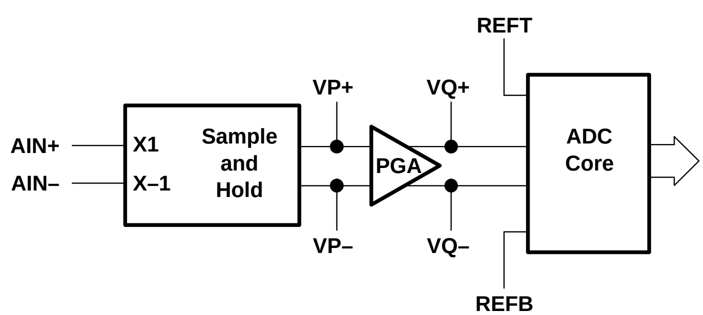



**Figure 25. Analog Input Signal Flow**

# PRINCIPLES OF OPERATION

## sample-and-hold

Differential input signal sources can be connected directly to the AIN+ and AIN– pins using either dc- or ac-coupling.

For single-ended sources, the signal can be dc- or ac-coupled to one of AIN+ or AIN–, and a suitable reference voltage (usually the midscale voltage, see *operating configuration examples*) must be applied to the other pin. Note that connecting the signal to AIN– results in it being inverted during sampling.

The sample and hold differential output voltage VP = VP+ – VP– is given by

$$VP = (AIN+) - (AIN-) \tag{1}$$

A clamp is available for dc restoration of ac-coupled single-ended inputs (see *clamp operation*).

## programmable gain amplifier

VP is amplified by the PGA and fed to the ADC as a voltage VQ = VQ+ – VQ– where

$$VQ = Gain \times VP = Gain \times [(AIN+) - (AIN-)] \tag{2}$$

## analog-to-digital converter

VQ is digitized by the ADC, using the voltages at pins REFT and REFB to set the ADC zero-scale (code 0) and full-scale (code 1023) input voltages.

$$VQ\ (ZS) = -\ (REFT - REFB) \tag{3}$$

$$VQ\ (FS) = (REFT - REFB) \tag{4}$$

Any inputs at AIN+ and AIN– that give VQ voltages less than VQ(ZS) or greater than VQ(FS) lie outside the ADC's conversion range and attempts to convert such voltages are signalled by driving pin OVR high when the conversion result is output. VQ voltages less than VQ(ZS) digitize to give ADC output code 0, and VQ voltages greater than VQ(FS) give ADC output code 1023.

### complete system and system input range

Combining the above equations to find the input voltages [(AIN+) – (AIN–)] that correspond to the limits of the ADC's valid input range gives:

$$\frac{(REFB - REFT)}{Gain} \le [(AIN+) - (AIN-)] \le \frac{(REFT - REFB)}{Gain} \tag{5}$$

For both single-ended and differential inputs, the ADC can thus handle signals with a peak-to-peak input range [(AIN+) – (AIN–)] of:

$$[(AIN+) - (AIN-)]\ \text{pk–pk input range} = 2 \times \frac{(REFT - REFB)}{Gain} \tag{6}$$

The next sections describe the options available to the user for setting the REFT and REFB voltages to obtain the desired input range and performance in their THS1041 applications.

## PRINCIPLES OF OPERATION

### ADC reference generation

The THS1041 ADC references REFT and REFB can be driven from external (off-chip) sources or from the internal A2 reference buffer. The voltage at the MODE pin determines the ADC references source.

Connecting MODE to AGND enables external ADC references mode. In this mode the internal buffer A2 is powered down and the user must provide the REFT and REFB voltages by connecting external sources directly to these pins. This mode is useful where several THS1041 devices must share common references for best matching of their ADC input ranges, or when the application requires better accuracy and temperature stability than the on-chip reference source can provide.

Connecting MODE to $AV_{DD}$ or $AV_{DD}/2$ enables internal ADC references mode. In this mode the buffer A2 is powered up and drives the REFT and REFB pins. External reference sources should not be connected in this mode. Using internal ADC references mode when possible helps to reduce the component count and hence the system cost.

When MODE is connected to $AV_{DD}$, a buffered $AV_{DD}/2$ voltage is also available at the CLAMPOUT pin. This voltage can be used as a dc bias level for any ac-coupling networks connecting the input signal sources to the AIN+ and AIN– pins.

| MODE PIN | REFERENCE SELECTION | CLAMPOUT PIN FUNCTION |
|---|---|---|
| AGND | External | Clamp |
| $AV_{DD}/2$ | Internal | Clamp |
| $AV_{DD}$ | Internal | $AV_{DD}/2$ for AIN± bias |

### external reference mode (MODE = AGND)

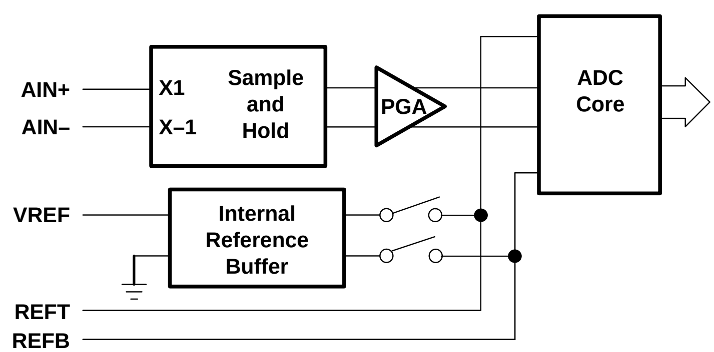



**Figure 26. ADC Reference Generation, MODE = AGND**

Connecting pin MODE to AGND powers-down the internal references buffer A2 and disconnects its outputs from the REFT and REFB pins. The user must connect REFT and REFB to external sources to provide the ADC reference voltages required to match the THS1041 input range to their application requirements. The common-mode reference voltage must be $AV_{DD}/2$ for correct THS1041 operation:

$$\frac{(REFT + REFB)}{2} = \frac{AV_{DD}}{2} \tag{7}$$

## PRINCIPLES OF OPERATION

### internal reference mode (MODE = $AV_{DD}$ or $AV_{DD}/2$)

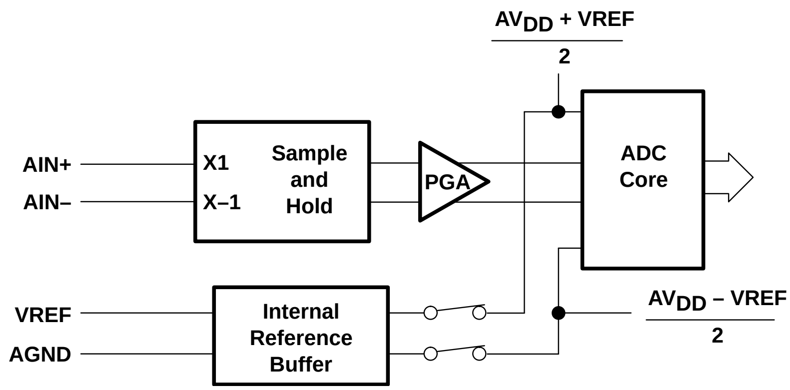



**Figure 27. ADC Reference Generation, MODE = $AV_{DD}/2$**

Connecting MODE to $AV_{DD}$ or $AV_{DD}/2$ enables the internal ADC references buffer A2. The outputs of A2 are connected to the REFT and REFB pins and its inputs are connected to pins VREF and AGND. The resulting voltages at REFT and REFB are:

$$REFT = \frac{\left(AV_{DD} + VREF\right)}{2} \quad (8)$$

$$REFB = \frac{\left(AV_{DD} - VREF\right)}{2} \quad (9)$$

Depending on the connection of the REFSENSE pin, the voltage on VREF may be driven by an off-chip source or by the internal bandgap reference (A1) (see *onboard reference generator configuration*) to match the THS1041 input range to their application requirements.

When MODE = $AV_{DD}$ the CLAMPOUT pin provides a buffered, stabilized $AV_{DD}/2$ output voltage that can be used as a bias reference for ac coupling networks connecting the signal sources to the AIN+ or AIN– inputs. This removes the need for the user to provide a stabilized external bias reference.

## PRINCIPLES OF OPERATION

### internal reference mode (MODE = $AV_{DD}$ or $AV_{DD}/2$) (continued)

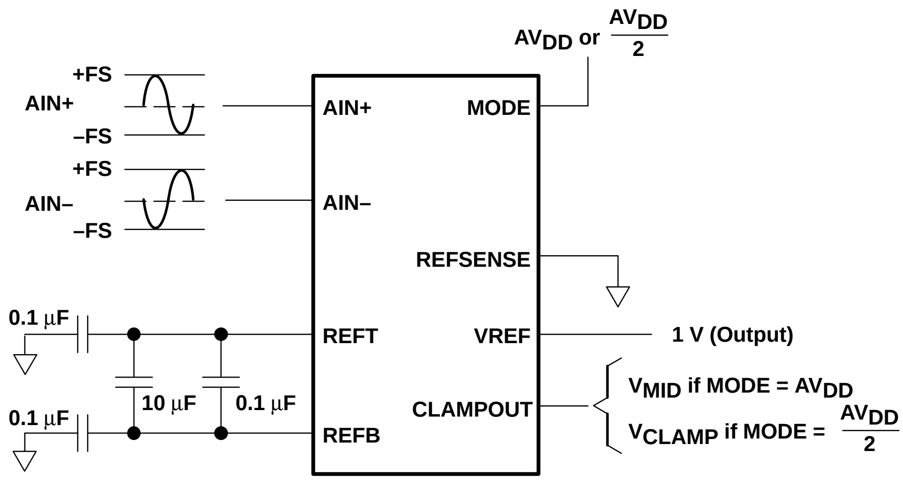



**Figure 28. Internal Reference Mode, 1-V Reference Span**

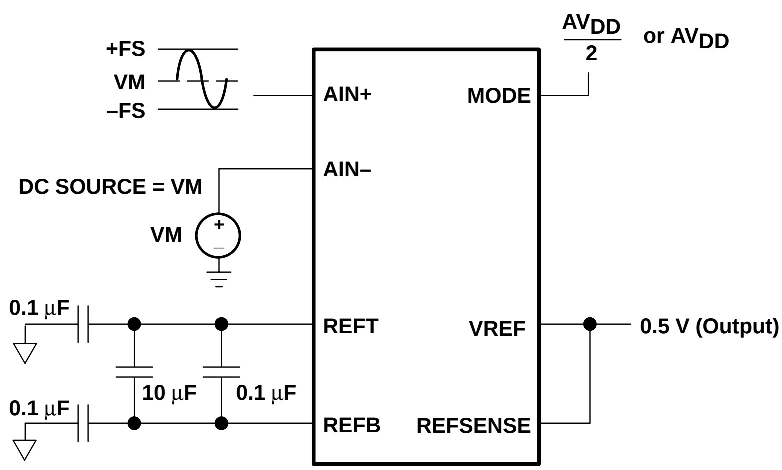



**Figure 29. Internal Reference Mode, 0.5-V Reference Span, Single-Ended Input**

## PRINCIPLES OF OPERATION

### onboard reference generator configuration

The internal bandgap reference A1 can provide a supply-voltage-independent and temperature-independent voltage on pin VREF.

External connections to REFSENSE control A1's output to the VREF pin as shown in Table 1.

**Table 1. Effect of REFSENSE Connection on VREF Value**

| REFSENSE CONNECTION | A1 OUTPUT TO VREF | REFER TO: |
|---|---|---|
| VREF pin | 0.5 V | Figure 30 |
| AGND | 1 V | Figure 31 |
| External divider junction | $(1 + R_a/R_b)/2$ V | Figure 32 |
| $AV_{DD}$ | Open circuit | Figure 33 |

REFSENSE = $AV_{DD}$ powers the internal bandgap reference A1 down, saving power when A1 is not required. If MODE is connected to $AV_{DD}$ or $AV_{DD}/2$, then the voltage at VREF determines the ADC reference voltages:

$$REFT = \frac{AV_{DD}}{2} + \frac{VREF}{2} \quad (10)$$

$$REFB = \frac{AV_{DD}}{2} - \frac{VREF}{2} \quad (11)$$

$$REFT–REFB = VREF \quad (12)$$

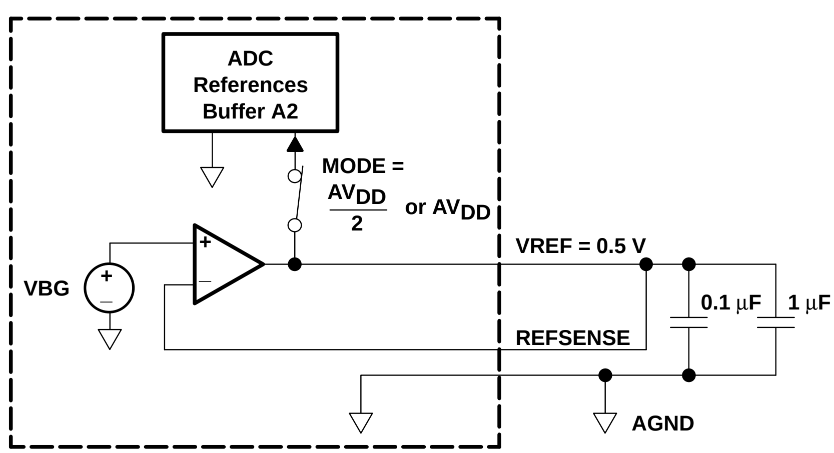



**Figure 30. 0.5-V VREF Using the Internal Bandgap Reference A1**

## PRINCIPLES OF OPERATION

### onboard reference generator configuration (continued)

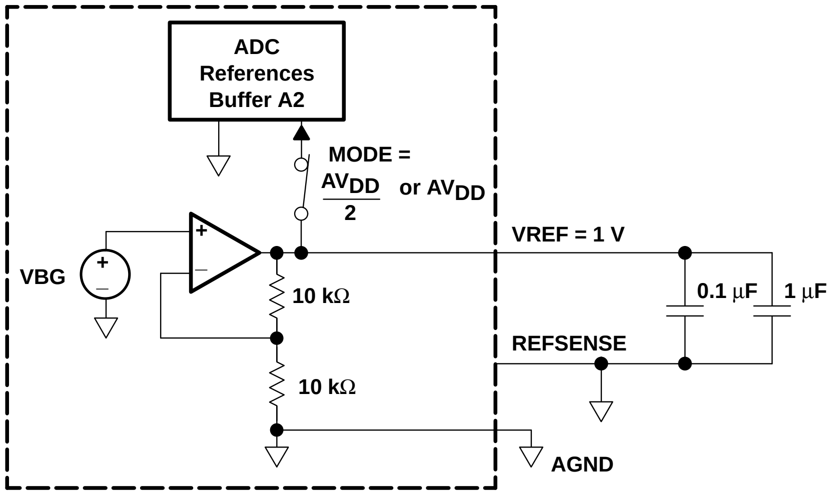



**Figure 31. 1-V VREF Using the Internal Bandgap Reference A1**

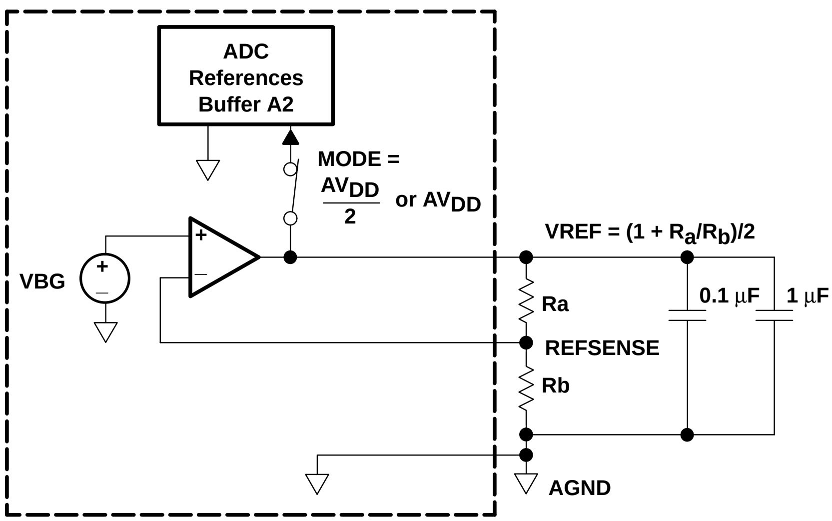



**Figure 32. External Divider Mode**

## PRINCIPLES OF OPERATION

### onboard reference generator configuration (continued)

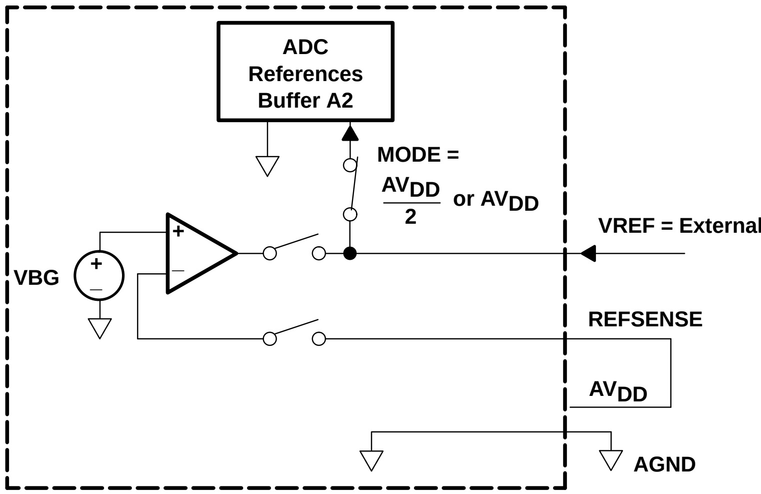



**Figure 33. Drive VREF Mode**

### operating configuration examples

Figure 34 shows a configuration using the internal ADC references for digitizing a single-ended signal with span 0 V to 2 V. Tying REFSENSE to ground gives 1 V at pin VREF. Tying MODE to $AV_{DD}/2$ then sets the REFT and REFB voltages via the internal reference generator for a 2-$V_{p-p}$ ADC input range and the CLAMPOUT pin also provides the midscale 1-V bias for the AIN– input. Using the clamp to drive AIN– rather than connecting AIN– directly to VREF helps to prevent kickback from the AIN– pin corrupting VREF. AIN– can be connected to VREF, provided that VREF is well-decoupled to analog ground. Internal PGA gain setting is 1.

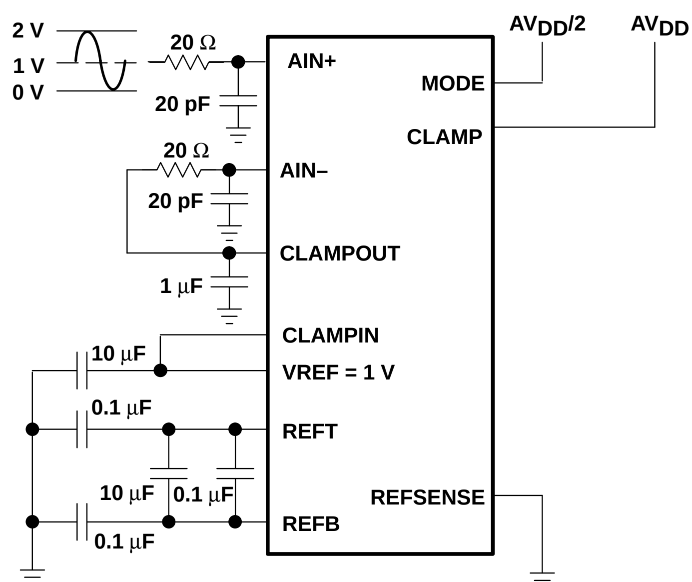



**Figure 34. Operating Configuration: 2-V Single-Ended Input, Internal ADC References**

## PRINCIPLES OF OPERATION

### operating configuration examples (continued)

Figure 35 shows a configuration using the internal ADC references for digitizing a dc-coupled differential input with 1.5-$V_{p\text{-}p}$ span and 1.5-V common-mode voltage. External resistors are used to set the internal bandgap reference output at VREF to 0.75 V. Tying MODE to $AV_{DD}$ then sets the REFT and REFB voltages via the internal reference generator for a 1.5-$V_{p\text{-}p}$ ADC input range.

If a transformer is used to generate the differential ADC input from a single-ended signal, then the CLAMPOUT pin provides a suitable bias voltage for the secondary windings center tap when MODE = $AV_{DD}$.

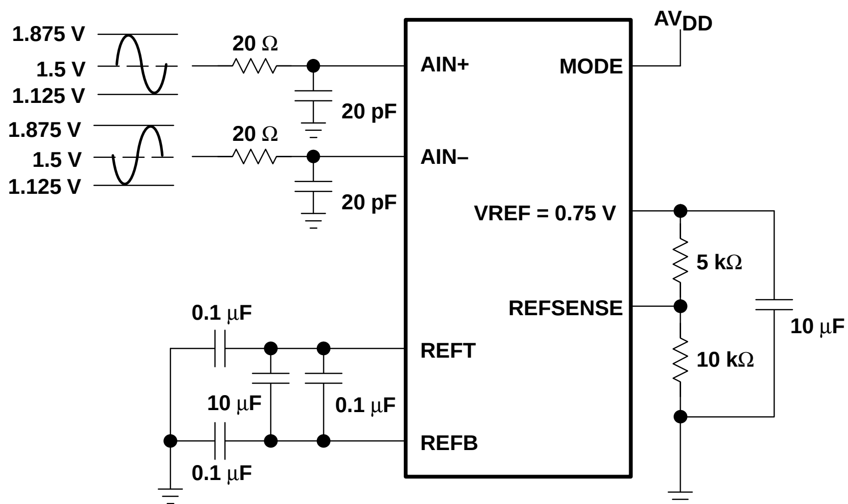



**Figure 35. Operating Configuration: 1.5-V Differential Input, Internal ADC References**

Figure 36 shows a configuration using the internal ADC references and an external VREF source for digitizing a dc coupled single-ended input with span 0.5 V to 2 V. A 1.25-V external source provides the bias voltage for the AIN– pin and also, via a buffered potential divider; the 0.75 VREF voltage required to set the input range to 1.5 $V_{p\text{-}p}$ MODE is tied to $AV_{DD}$ to set internal ADC references configuration.

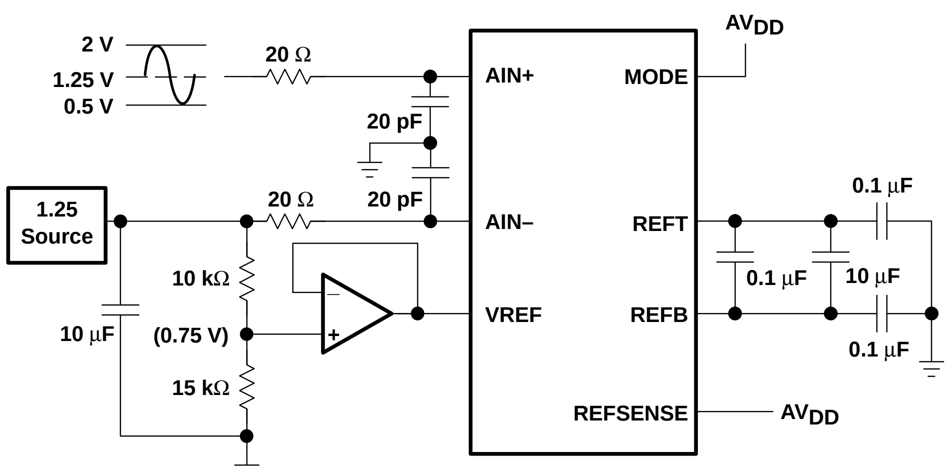



**Figure 36. Operating Configuration: 1.5-V Single-Ended Input, External VREF Source**

## PRINCIPLES OF OPERATION

### operating configuration examples (continued)

Figure 37 shows a configuration using external ADC references for digitizing a differential input with span 0.8 V. To maximize the signal swing at the ADC core, the PGA gain is set to 2.5 to give a 2-$V_{p-p}$ output from the PGA. MODE is tied to ground to disable the internal reference buffer. The external ADC reference sources must set REFT 1 V higher than REFB to set the ADC input span to 2 $V_{p-p}$, and the voltages provided by the external sources must be centered near $AV_{DD}/2$ for best ADC operation. REFSENSE is shown tied to $AV_{DD}$ to disable the internal bandgap refence (A1), though other components in the system may use the VREF output if desired.

External ADC references are best suited to applications which require the tighter reference voltage tolerance and temperature coefficient than the internal bandgap reference (A1) can provide, or where the references are to be shared among several THS1041 ADCs for best matching of their ADC channels.

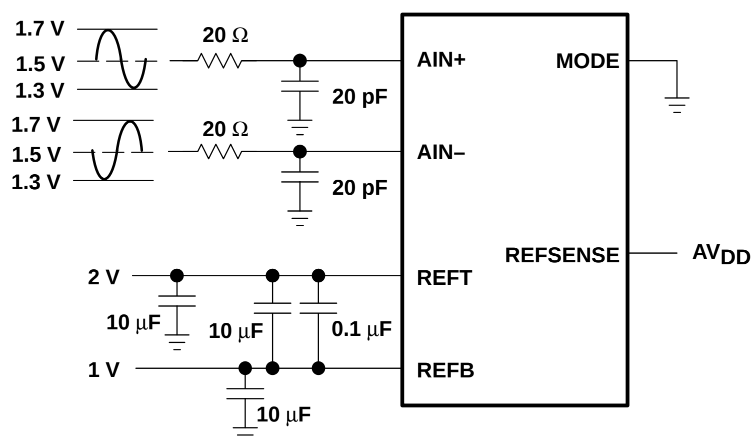



**Figure 37. Operating Configuration: 0.8-V Differential Input and External ADC References**

### clamp operation

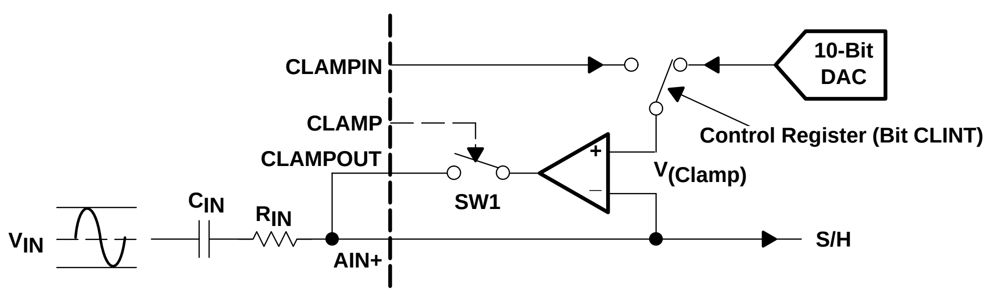



**Figure 38. Schematic of Clamp Circuitry**

The THS1041 provides a clamp function for restoring a dc reference level to the signal at AIN+ or AIN– which has been lost through ac-coupling from the signal source to this pin.

Figure 38 and Figure 39 show an example of using the clamp to restore the black level of a composite video input ac-coupled to AIN+. While the clamp pin is held high, the clamp amplifier forces the voltage at AIN+ to equal the clamp reference voltage, setting the dc voltage at AIN+ for the video black level.

After power up, the clamp reference voltage is the voltage on the CLAMPIN pin. This reference can instead be taken from the internal CLAMP DAC by suitably programming the THS1041 clamp and control registers.

Clamp acquisition and clamp droop design calculations are discussed later.

## PRINCIPLES OF OPERATION

### clamp operation (continued)

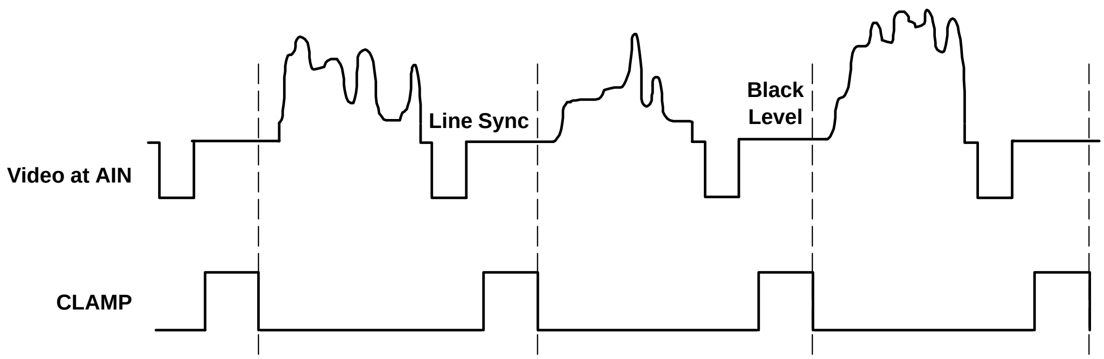



**Figure 39. Example Waveforms for Line-Clamping to a Video Input Black Level**

### clamp DAC output voltage range and limits

When using the internal clamp DAC, the user must ensure that the desired dc clamp level at AIN+/– lies within the voltage range $V_{REFB}$ to $V_{REFT}$. This is because the clamp DAC voltage is constrained to lie within this range $V_{REFB}$ to $V_{REFT}$. Specifically:

$$VDAC = V_{REFB} + (V_{REFT} - V_{REFB}) \times (0.006 + 0.988 \times (\text{DAC code})/1024) \quad (13)$$

DAC codes can range from 0 to 1023. Figure 40 graphically shows the clamp DAC output voltage versus the DAC code.

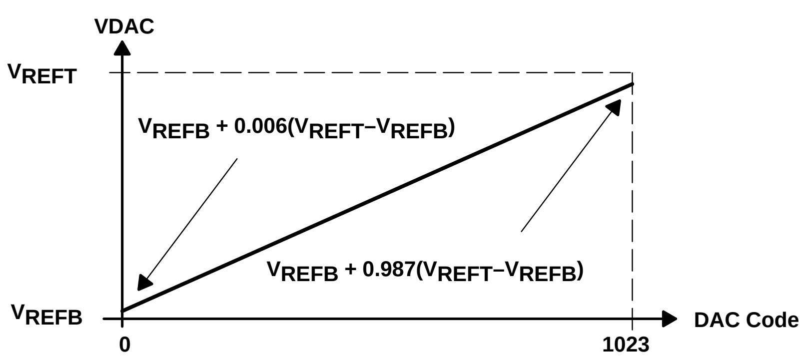



**Figure 40. Clamp DAC Output Voltage Versus DAC Register Code Value**

If the desired dc level at AIN+/– does not lie within the voltage range $V_{REFT}$ to $V_{REFB}$, then either the CLAMPIN pin can be used instead to provide a suitable reference voltage, or it may be possible to redesign the application to move the AIN+/– input range into the CLAMP DAC voltage range.

# PRINCIPLES OF OPERATION

## power management

In power-sensitive applications (such as battery-powered systems) where the THS1041 ADC is not required to convert continuously, power can be saved between conversion intervals by placing the THS1041 into power-down mode. This is achieved by setting bit 3 (PWDN) of the control register to 1. In power-down mode, the device typically consumes less than 0.1 mW. Power-down mode is exited by resetting control register bit 3 to 0. On power up, typical wake-up and power-up times apply. See *power supply* section.

In systems where the ADC must run continuously, but where the clamp is not required, the supply current can be reduced by approximately 1.2 mA by setting the control register bit 6 (CLDIS) to 1, which disables the clamp circuit. Similarly, when REFSENSE is tied to $AV_{DD}$, the reference generator is disabled and supply current reduced by approximately 1.2 mA.

## output format and digital I/O

While the $\overline{OE}$ pin is held low, ADC conversion results are output at pins I/O0 (LSB) to I/O9 (MSB). The ADC input over-range indicator is output at pin OVR. OVR is also disabled when $\overline{OE}$ is held high.

The default ADC output data format is unsigned binary (output codes 0 to 1023). The output format can be switched to 2s complement (output codes –512 to 511) by setting control register bit 5 (TWOC) to 1.

### writing to the internal registers through the digital I/O bus

Pulling pin $\overline{OE}$ high disables the I/O and OVR pin output drivers, placing the driver outputs in a high impedance state. This allows control register data to be loaded into the THS1041 by presenting it on the I/O0 to I/O9 pins and pulsing the WR pin high then low to latch the data into the chosen control or DAC register.

Figure 41 shows an example register write cycle where the clamp DAC code is set to 10F (hex) by writing to clamp registers 1 and 2 (see the register map in Table 2). Pins I/O0 to I/O7 are driven to the clamp DAC code lower byte (0F hex), and pins I/08 and I/O9 are both driven to 0 to select clamp register 1 as the data destination. The clamp low-byte data is then loaded into this register by pulsing WR high. The top 2 bits of the DAC word are then loaded by driving 01(hex) on pins I/O0 to I/O7 and by driving pin I/O8 to 1 and pin I/O9 to 0 to select clamp register 2 as the data destination. WR is pulsed a second time to latch this second control word into clamp register 2. Interface timing parameters are given in Figures 1 and 2.

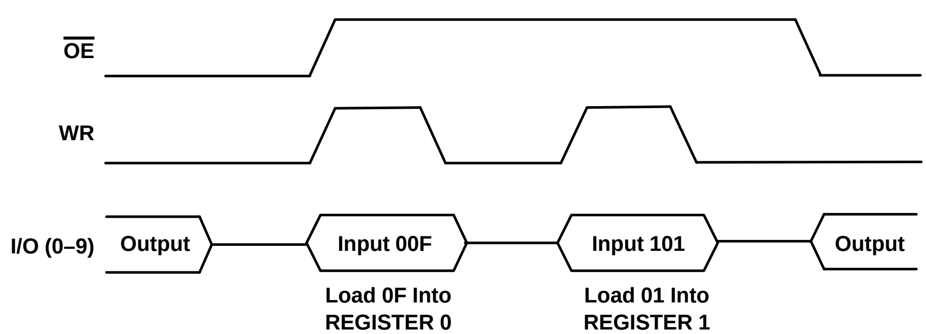



**Figure 41. Example Register Write Cycle to Clamp DAC Register**

## PRINCIPLES OF OPERATION

### digital control registers

The THS1041 contains two clamp registers and a control register for user programming of THS1041 operation. Binary data can be written into these registers by using pins I/O0 to I/O9 and the WR and $\overline{OE}$ pins (see the previous section). In input mode, the two I/O bus MSBs are address bits, 00 addressing clamp register 1, 01 clamp register 2, and 10 the control register.

**Table 2. Register Map**

| ADDRESS I/O[9:8] | DESCRIPTION | DEF (HEX) | RW | BIT | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
| 00 | Clamp register 1 | 00 | RW | DAC[7] | DAC[6] | DAC[5] | DAC[4] | DAC[3] | DAC[2] | DAC[1] | DAC[0] |
| 01 | Clamp register 2 | 00 | RW | | | | | | | DAC[9] | DAC[8] |
| 10 | Control register | 01 | RW | | CLDIS | TWOC | CLINT | PDWN | PGA[2] | PGA[1] | PGA[0] |
| 11† | Reserved† | | | | | | | | | | |

† Do not write to register 11

**Table 3. Register Contents**

| REGISTER | BIT NO | BIT NAME(S) | DEFAULT | DESCRIPTION |
|---|---|---|---|---|
| Control register I/O[9:8] = 10 | 2:0 | PGA[2:0] | 001 | PGA gain:<br>000 = 0.5<br>001 = 1.0 (default value)<br>010 = 1.5<br>011 = 2.0<br>100 = 2.5<br>101 = 3.0<br>110 = 3.5<br>111 = 4.0 |
| | 3 | PDWN | 0 | Power down<br>0 = THS1041 powered up<br>1 = THS1041 powered down |
| | 4 | CLINT | 0 | Clamp voltage internal/external<br>0 = external analog clamp voltage from CLAMPIN pin<br>1 = from onboard DAC (see clamp register) |
| | 5 | TWOC | 0 | Output format<br>0 = unsigned binary<br>1 = twos complement |
| | 6 | CLDIS | 0 | CLAMPOUT pin disable (for power saving)<br>0 = Enable<br>1 = Disable |
| | 7 | | | Unused |
| Clamp register 1 I/O[9:8] = 00 | 7:0 | DAC[7:0] | 0 | Clamp DAC voltage<br>(DAC[0] = LSB.)<br>DAC[9:0] = 00h: Clamp voltage = REFB<br>DAC[9:0] = 3Fh: Clamp voltage = REFT |
| Clamp register 2 I/O[9:8] = 01 | 7:2 | | | Unused |
| | 1:0 | DAC[9:8] | 0 | Clamp DAC voltage<br>(DAC[9] = MSB) |

## APPLICATION INFORMATION

### driving the THS1041 analog inputs

#### driving the clock input

Obtaining good performance from the THS1041 requires care when driving the clock input.

Different sections of the sample-and-hold and ADC operate while the clock is low or high. The user should ensure that the clock duty cycle remains near 50% to ensure that all internal circuits have as much time as possible in which to operate.

The CLK pin should also be driven from a low jitter source for best dynamic performance. To maintain low jitter at the CLK input, any clock buffers external to the THS1041 should have fast rising edges. Use a fast logic family such as AC or ACT to drive the CLK pin, and consider powering any clock buffers separately from any other logic on the PCB to prevent digital supply noise appearing on the buffered clock edges as jitter.

As the CLK input threshold is nominally around $AV_{DD}/2$, any clock buffers need to have an appropriate supply voltage to drive above and below this level.

#### driving the sample and hold inputs

***driving the AIN+ and AIN– pins***

Figure 42 shows an equivalent circuit for the THS1041 AIN+ and AIN– pins. The load presented to the system at the AIN pins comprises the switched input sampling capacitor, $C_{Sample}$, and various stray capacitances, $C_1$ and $C_2$.

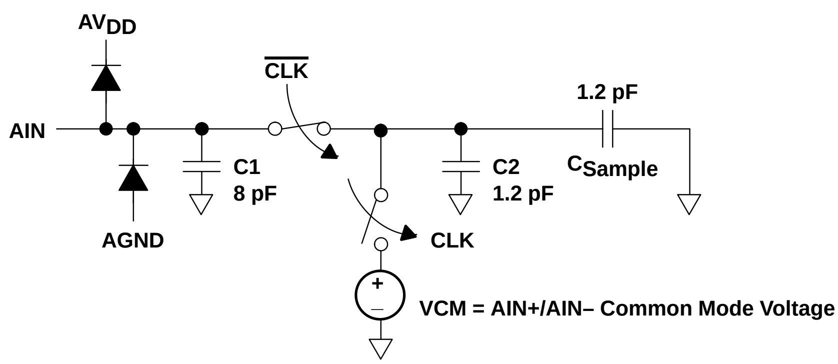



**Figure 42. Equivalent Circuit for Analog Input Pins AIN+ and AIN–**

The input current pulses required to charge $C_{Sample}$ and $C_2$ can be time averaged and the switched capacitor circuit modelled as an equivalent resistor:

$$R_{IN2} = \frac{1}{C_S \times f_{CLK}} \quad (14)$$

where $C_S$ is the sum of $C_{Sample}$ and $C_2$. This model can be used to approximate the input loading versus source resistance for high impedance sources.

## APPLICATION INFORMATION

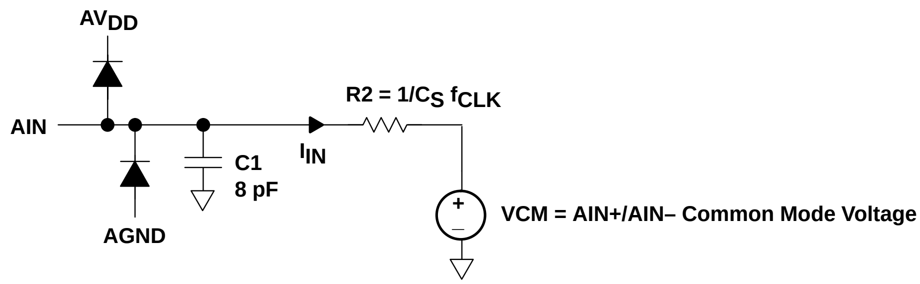



**Figure 43. Equivalent Circuit for the AIN Switched Capacitor Input**

### *AIN input damping*

The charging current pulses into AIN+ and AIN– can make the signal sources jump or ring, especially if the sources are slightly inductive at high frequencies. Inserting a small series resistor of 20 Ω or less and a small capacitor to ground of 20 pF or less in the input path can damp source ringing (see Figure 44). The resistor and capacitor values can be made larger than 20 Ω and 20 pF if reduced input bandwidth and a slight gain error (due to potential division between the external resistors and the AIN equivalent resistors) are acceptable.

Note that the capacitors should be soldered to a clean analog ground with a common ground point to prevent any voltage drops in the ground plane appearing as a differential voltage at the ADC inputs.

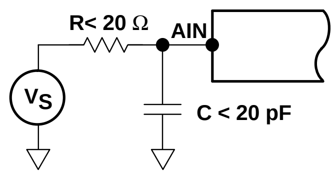



**Figure 44. Damping Source Ringing Using a Small Resistor and Capacitor**

### driving the VREF pin

Figure 45 shows the equivalent load on the VREF pin when driving the ADC internal references buffer via this pin (MODE = $AV_{DD}/2$ or $AV_{DD}$ and REFSENSE = $AV_{DD}$).

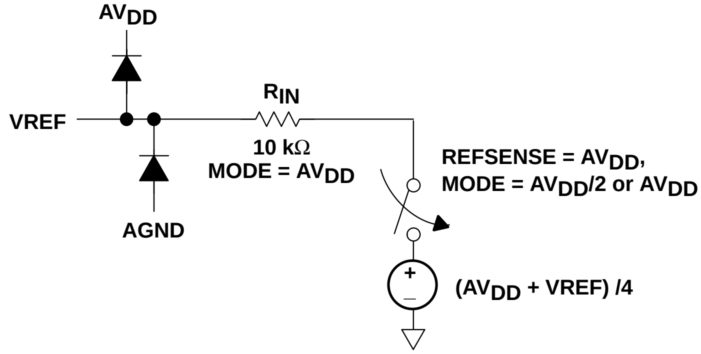



**Figure 45. Equivalent Circuit of VREF**

The nominal input current $I_{REF}$ is given by:

$$I_{REF} = \frac{3\,V_{REF} - AV_{DD}}{4 \times R_{IN}} \tag{15}$$

## APPLICATION INFORMATION

### driving the VREF pin (continued)

Note that the maximum current may be up to 30% higher. The user should ensure that VREF is driven from a low noise, low drift source, well decoupled to analog ground and capable of driving the maximum $I_{REF}$.

### *driving REFT and REFB (external ADC references, MODE = AGND)*

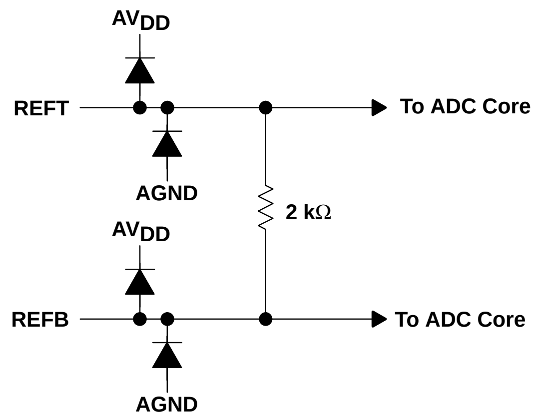



**Figure 46. Equivalent Circuit of REFT and REFB Inputs**

### designing the dc clamp

Figure 38 shows the basic operation of the clamp circuit with the analog input AIN+ coupled via an RC circuit. AIN– must be connected to a dc source whose voltage level keeps the THS1041 differential input within the ADC input range. The clamp voltage output level may be established by an analog voltage on the CLAMPIN pin or by programming the on-chip clamp DAC.

(Note that it is possible to reverse the AIN+ and AIN– connections if signal inversion is also required. The following section assumes that the signal is coupled to AIN+ and that AIN– is connected to a suitable dc bias level).

### *initial clamp acquisition time*

Acquisition time is the time required to reach the target clamp voltage at AIN+ when the clamp switch SW1 is closed for the first time. The acquisition time is given by

$$T_{ACQ} = C_{IN} \times R_{IN} \times \ln\left(\frac{V_C}{V_E}\right) \qquad (16)$$

where $V_C$ is the difference between the dc level of the input $V_{IN}$ and the target clamp output voltage, $V_{Clamp}$. $V_E$ is the difference between the ideal $V_C$ and the actual $V_C$ obtained during the acquisition time. The maximum tolerable error depends on the application requirements.

For example, consider clamping an incoming video signal that has a black level near 0.3 V to a black level of 1.3 V at the THS1041 AIN+ input. The voltage $V_C$ required across the input coupling capacitor is thus 1.3 – 0.3 = 1 V. If a 10 mV or less clamp voltage error $V_E$ gives acceptable system operation, the source resistance $R_{IN}$ is 20 Ω and the coupling capacitor $C_{IN}$ is 1 µF, then the total clamp pulse duration required to reach this error is:

$T_{ACQ} = 1\ \mu F \times 20\ \Omega \times \ln(1/0.01) = 92\ \mu s$ (approximate)

## APPLICATION INFORMATION

### *initial clamp acquisition time (continued)*

Initial acquisition can be performed in two ways:

- Pulsing the CLAMP pin as in normal operation. Provided that clamp droop (see below) is negligible, initial acquisition is complete when the total clamped (CLAMP = high) time equals $T_{ACQ}$.
- Pulling the CLAMP pin high for the required acquisition time before starting normal operation. This method is faster, though possibly less convenient for the user to implement.

### *clamp droop*

The charging currents drawn by the sample-and-hold switched capacitor input can charge or discharge $C_{IN}$, causing the dc voltage at AIN+ to drift towards the dc bias voltage at AIN– during the time between clamp pulses. This effect is called clamp droop.

Voltage droop is a function of the AIN+ and AIN– input currents to the THS1041, $I_{IN}$, and the time between clamp intervals, $t_D$:

$$V_{DROOP} \approx \left(\frac{I_{IN}}{C_{IN}}\right) \times t_d \text{ (approximate)} \tag{17}$$

Worst case droop between clamping intervals occurs for maximum input bias current. Maximum input current is $I_{INFS}$, which occurs when the input level is at its maximum or minimum.

For example, at 40 MSPS $I_{INFS}$ is approximately 20 µA for a 2-V input range at AIN (assuming 2 V appear across RIN2—see *driving the sample and hold reference inputs* to calculate $R_{IN2}$). Note that $I_{INFS}$ may vary from this by ±30% because of processing variations and voltage dependencies. Designs should allow for this variation. If the time $t_d$ between clamping intervals is 63.5 µs and $C_{IN}$ is 1 µF, then the maximum clamp level droop between clamp pulses is

$$\begin{aligned} V_{DROOP}(\text{max}) &= 20\ \mu\text{A}/1\ \mu\text{F} \times 63.5\ \mu\text{s} = 1.25\ \text{mV (approximate, ignoring 30\% tolerance)} \\ &= 0.62\ \text{LSB at PGA gain} = 1,\ 2\ \text{V ADC references} \end{aligned} \tag{18}$$

If this droop is greater than can be tolerated in the application, then increase $C_{IN}$ to slow the droop and hence reduce the voltage change between clamp pulses.

If a high leakage capacitor is used for coupling the input source to the AIN pin then the droop may be significantly worse than calculated above. Avoid using electrolytic and tantalum coupling capacitors as these have higher leakage currents than nonpolarized capacitor types. Electrolytic and tantalum capacitors also tend to have higher parasitic inductance, which can cause problems at high input frequencies.

### *steady-state clamp voltage error*

During the clamp pulse (CLAMP = high), the dc voltage on AIN is refreshed from the clamp voltage. Provided that droop is not excessive, clamping fully reverses the effect of droop. However, using very short clamp pulses with long intervals between pulses ($t_d$) can result in a steady-state voltage difference, $V_{COS}$, between the dc voltage at AIN and $V_{(Clamp)}$.

Figure 47 shows the approximate voltage waveform at AIN resulting from a a large clamp droop during $t_d$ and clamp voltage reacquisition during the clamp pulse time, $t_c$.

## APPLICATION INFORMATION

***steady-state clamp voltage error (continued)***

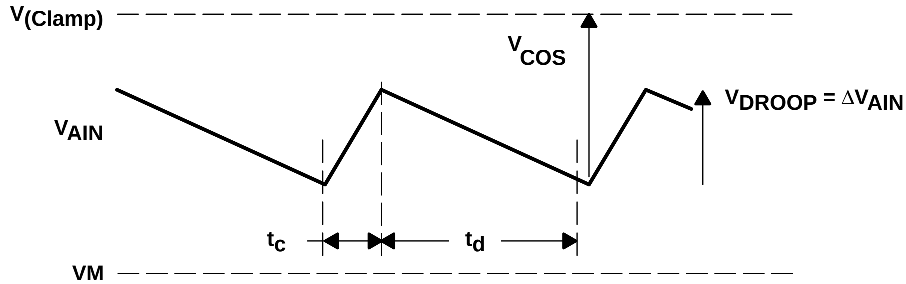



**Figure 47. Approximate Waveforms at AIN During Droop and Clamping**

The voltage change at AIN during acquisition has been approximated as a linear charging ramp by assuming that almost all of $V_{COS}$ appears across $R_{IN}$, giving a charging current $V_{COS}/R_{IN}$ (this is a reasonable approximation when $V_{COS}$ is large enough to be of concern). The voltage change at AIN during clamp acquisition is then:

$$\Delta V_{AIN} = \frac{V_{COS} \times t_d}{R_{IN} \times C_{IN}} \tag{19}$$

The peak-to-peak voltage variation at AIN must equal the clamp droop voltage at steady state. Equating the droop voltage to the clamp acquisition voltage change gives:

$$V_{COS} = \frac{R_{IN} \times I_{IN} \times t_d}{t_c} \tag{20}$$

Thus for low offset voltage, keep $R_{IN}$ low, design for low droop and ensure that the ratio $t_d/t_c$ is not unreasonably large.

**reference decoupling**

***VREF pin***

When the on-chip reference generator is enabled, the VREF pin should be decoupled to the circuit board's analog ground plane close to the THS1041 AGND pin via a 1-μF capacitor and a 0.1-μF ceramic capacitor.

***REFT and REFB pins***

In any mode of operation, the REFT and REFB pins should be decoupled as shown in Figure 48. Use short board traces between the THS1041 and the capacitors to minimize parasitic inductance.

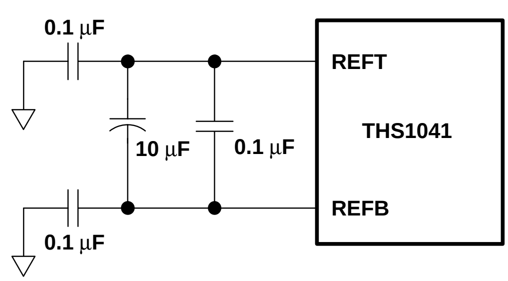



**Figure 48. Recommended Decoupling for the ADC Reference Pins REFT and REFB**

## APPLICATION INFORMATION

### CLAMPOUT decoupling (when used as dc bias source)

When using CLAMPOUT as a dc biasing reference (e.g., MODE = $AV_{DD}$), the CLAMPOUT pin should be decoupled to the circuit board’s analog ground plane close to the THS1041 AGND pin via a 1-µF capacitor and a 0.1-µF ceramic capacitor.

### supply decoupling

The analog ($AV_{DD}$, AGND) and digital ($DV_{DD}$, DGND) power supplies to the THS1041 should be separately decoupled for best performance. Each supply needs at least a 10-µF electrolytic or tantalum capacitor (as a charge reservoir) and a 100-nF ceramic type capacitor placed as close as possible to the respective pins (to suppress spikes and supply noise).

### digital output loading and circuit board layout

The THS1041 outputs are capable of driving rail-to-rail with up to 10 pF of load per pin at 40-MHz clock frequency and 3-V digital supply. Minimizing the load on the outputs improves THS1041 signal-to-noise performance by reducing the switching noise coupling from the THS1041 output buffers to the internal analog circuits. The output load capacitance can be minimized by buffering the THS1041 digital outputs with a low input capacitance buffer placed as close to the output pins as physically possible, and by using the shortest possible tracks between the THS1041 and this buffer. Inserting small resistors in the range 100 Ω to 300 Ω between the THS1041 I/O outputs and their loads can help minimize the output-related noise in noise-critical applications.

Noise levels at the output buffers, which may affect the analog circuits within THS1041, increase with the digital supply voltage. Where possible, consider using the lowest $DV_{DD}$ that the application can tolerate.

Use good layout practices when designing the application PCB to ensure that any off-chip return currents from the THS1041 digital outputs (and any other digital circuits on the PCB) do not return via the supplies to any sensitive analog circuits. The THS1041 should be soldered directly to the PCB for best performance. Socketing the device degrades performance by adding parasitic socket inductance and capacitance to all pins.

### user tips for obtaining best performance from the THS1041

- Choose differential input mode for best distortion performance.
- Choose a 2-V ADC input span for best noise performance.
- Choose a 1-V ADC input span for best distortion performance.
- Drive the clock input CLK from a low-jitter, fast logic stage, with a well-decoupled power supply and short PCB traces.
- Use a small RC filter (typically 20 Ω and 20 pF) between the signal source(s) the AIN+ (and AIN–) input(s) when the systems bandwidth requirements allow this.

## APPLICATION INFORMATION

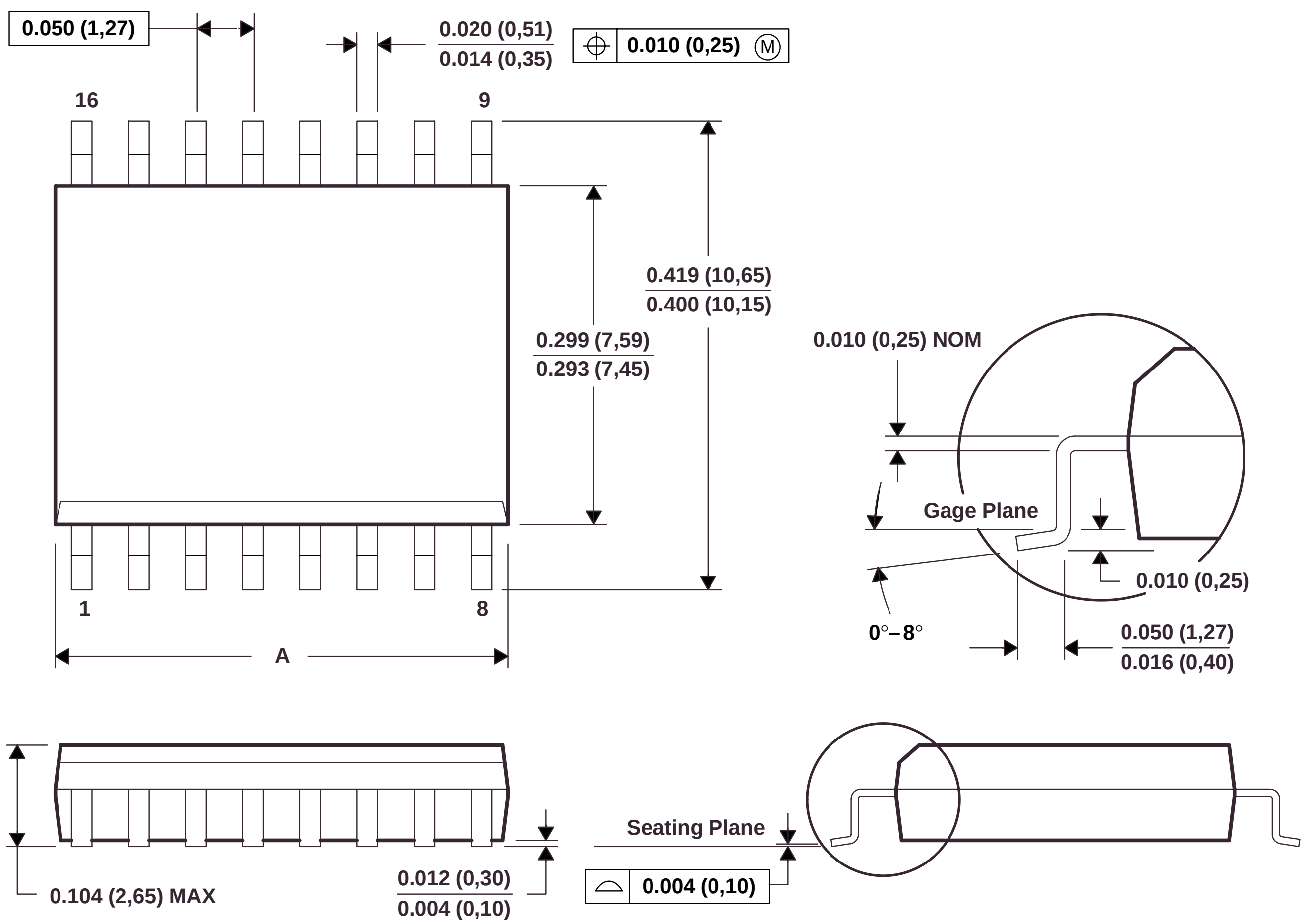
### definitions

- Integral nonlinearity (INL)—Integral nonlinearity refers to the deviation of each individual code from a line drawn from zero to full scale. The point used as zero occurs 1/2 LSB before the first code transition. The full-scale point is defined as a level 1/2 LSB beyond the last code transition. The deviation is measured from the center of each particular code to the true straight line between these two endpoints.
- Differential nonlinearity (DNL)—An ideal ADC exhibits code transitions that are exactly 1 LSB apart. DNL is the deviation from this ideal value. Therefore this measure indicates how uniform the transfer function step sizes are. The ideal step size is defined here as the step size for the device under test (i.e., (last transition level – first transition level) ÷ ($2^n$ – 2)). Using this definition for DNL separates the effects of gain and offset error. A minimum DNL better than –1 LSB ensures no missing codes.
- Zero-error—Zero-error is defined as the difference in analog input voltage—between the ideal voltage and the actual voltage—that switches the ADC output from code 0 to code 1. The ideal voltage level is determined by adding the voltage corresponding to 1/2 LSB to the bottom reference level. The voltage corresponding to 1 LSB is found from the difference of top and bottom references divided by the number of ADC output levels (1024).
- Full-scale error—Full-scale error is defined as the difference in analog input voltage—between the ideal voltage and the actual voltage—that will switch the ADC output from code 1022 to code 1023. The ideal voltage level is determined by subtracting the voltage corresponding to 1.5 LSB from the top reference level. The voltage corresponding to 1 LSB is found from the difference of top and bottom references divided by the number of ADC output levels (1024).
- Wake-up time—Wake-up time is from the power-down state to accurate ADC samples being taken and is specified for MODE = AGND with external reference sources applied to the device at the time of release of power-down, and an applied 40-MHz clock. Circuits that need to power up are the bandgap, bias generator, SHPGA, and ADC.
- Power-up time—Power-up time is from the power-down state to accurate ADC samples being taken and is specified for MODE = $AV_{DD}/2$ or $AV_{DD}$ and an applied 40-MHz clock. Circuits that need to power up include VREF reference generation (A1), bias generator, ADC, the SHPGA, and the on-chip ADC reference generator (A2).
- Aperture delay—The delay between the 50% point of the rising edge of the clock and the instant at which the analog input is sampled.
- Aperture uncertainty (Jitter)—The sample-to-sample variation in aperture delay.

## MECHANICAL DATA

**DW (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE**

**16 PINS SHOWN**




| PINS ** / DIM | 16 | 20 | 24 | 28 |
|---|---|---|---|---|
| A MAX | 0.410 (10,41) | 0.510 (12,95) | 0.610 (15,49) | 0.710 (18,03) |
| A MIN | 0.400 (10,16) | 0.500 (12,70) | 0.600 (15,24) | 0.700 (17,78) |

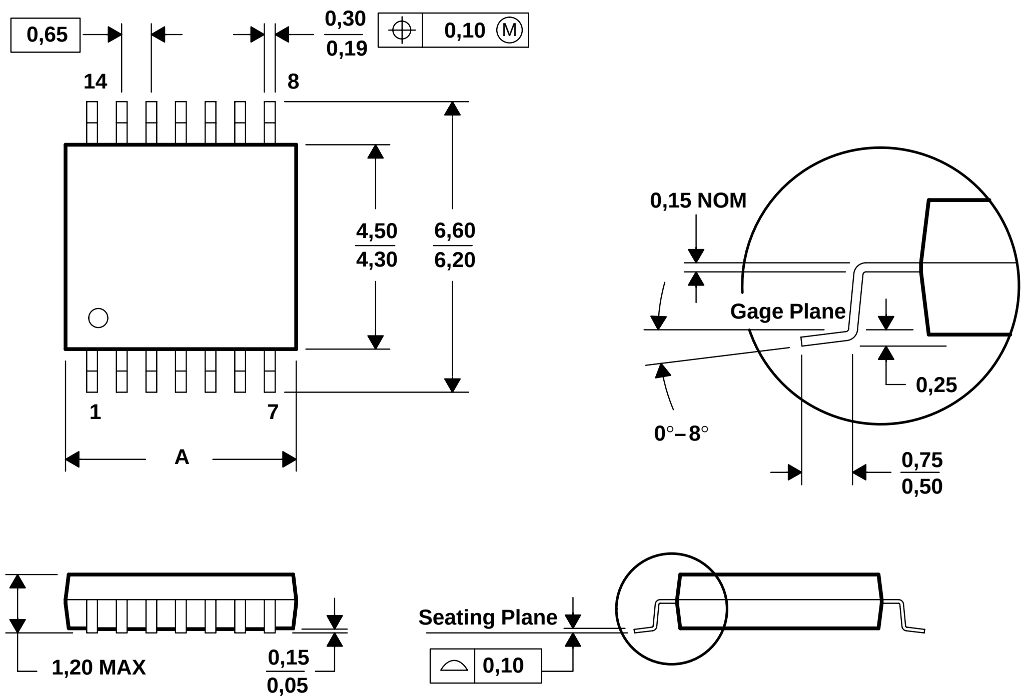
4040000/C 07/96

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-013

## MECHANICAL DATA

**PW (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE**

**14 PINS SHOWN**




| PINS ** / DIM | 8 | 14 | 16 | 20 | 24 | 28 |
|---|---|---|---|---|---|---|
| A MAX | 3,10 | 5,10 | 5,10 | 6,60 | 7,90 | 9,80 |
| A MIN | 2,90 | 4,90 | 4,90 | 6,40 | 7,70 | 9,60 |

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NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
- D. Falls within JEDEC MO-153

## IMPORTANT NOTICE



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