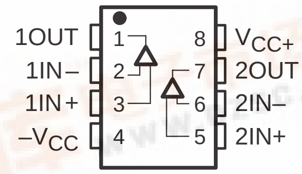
- **ADSL Differential Receiver**
- **Low 1.6 nV/√Hz Voltage Noise**
- **High Speed**
  - **100 MHz Bandwidth [–3 dB, G = 2 (–1)]**
  - **100 V/μs Slew Rate**
- **90 mA Output Drive (Typ)**
- **Very Low Distortion**
  - **THD = –72 dBc (f = 1 MHz, R_L = 150 Ω)**
  - **THD = –90 dBc (f = 1 MHz, R_L = 1 kΩ)**
- **5 V, ±5 V to ±15 V Typical Operation**
- **Available in Standard SOIC or MSOP PowerPAD™ Package**

D AND DGN PACKAGE (TOP VIEW)



Cross Section View Showing PowerPAD

description

The THS6062 is a high-speed differential receiver designed for ADSL data communication systems. Its very low 1.6 nV/√Hz voltage noise provides the high signal-to-noise ratios necessary for the long transmission lengths of ADSL systems over copper telephone lines. In addition, this receiver operates with a very low distortion of –90 dBc (f = 1 MHz, R_L = 1 kΩ), exceeding the distortion requirements of ADSL CODECs. The THS6062 is a voltage feedback amplifier offering a high 100-MHz bandwidth and 100-V/μs slew rate and is stable at gains of 2(–1) or greater. It operates over a wide range of power supply voltages including 5 V and ±5 V to ±15 V. This device is available in standard SOIC or MSOP PowerPAD package. The small, surface-mount, thermally-enhanced MSOP PowerPAD package is fully compatible with automated surface-mount assembly procedures.

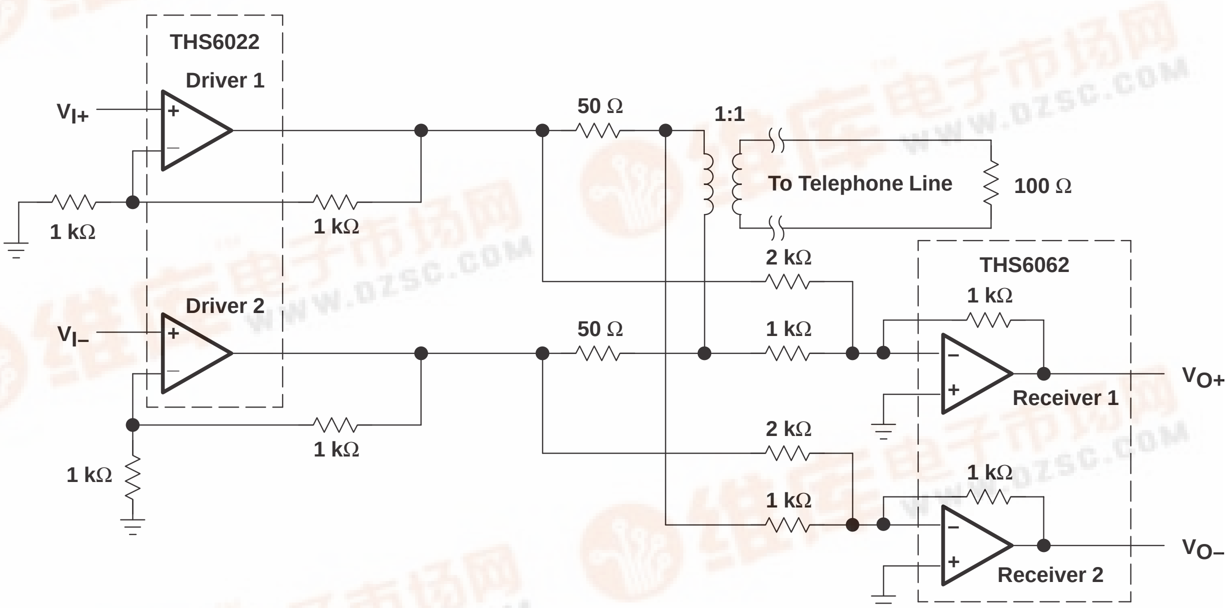


Figure 1. Typical Client-Side ADSL Application

CAUTION: The THS6062 provides ESD protection circuitry. However, permanent damage can still occur if this device is subjected to high-energy electrostatic discharges. Proper ESD precautions are recommended to avoid any performance degradation or loss of functionality.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PowerPAD is a trademark of Texas Instruments Incorporated.

HIGH-SPEED xDSL LINE DRIVER/RECEIVER FAMILY

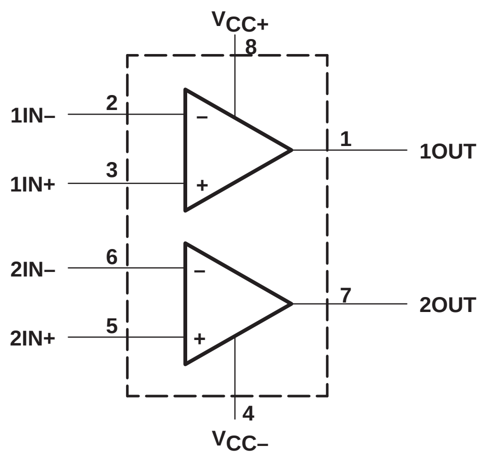
DEVICE	DRIVER	RECEIVER	5 V	±5 V	±15 V	BW (MHz)	SR (V/μs)	THD f = 1 MHz (dB)	I_O (mA)	V_n (nV/$\sqrt{Hz}$)
THS6002	•	•		•	•	140	1000	–62	500	1.7
THS6012	•			•	•	140	1300	–65	500	1.7
THS6022	•			•	•	210	1900	–66	250	1.7
THS6062		•	•	•	•	100	100	–72	90	1.6
THS7002		•		•	•	70	100	–84	25	2.0

AVAILABLE OPTIONS

T_A	PACKAGED DEVICES			
	PLASTIC SMALL OUTLINE† (D)	PowerPAD PLASTIC MSOP† (DGN)	MSOP SYMBOL	EVALUATION MODULE
0°C to 70°C	THS6062CD	THS6062CDGN	TIABE	THS6062EVM
–40°C to 85°C	THS6062ID	THS6062IDGN	TIABH	—

† The D and DGN packages are available taped and reeled. Add an R suffix to the device type (i.e., THS6062CDGNR).

functional block diagram



absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, V_{CC+} to V_{CC-} 33V
Input voltage, V_I . . . . . $\pm V_{CC}$
Output current, I_O . . . . . 150 mA
Differential input voltage, V_{IO} . . . . . ±4 V
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature, T_A: C–suffix . . . . . 0°C to 70°C
I-suffix . . . . . –40°C to 85°C
Maximum junction temperature, T_J . . . . . 150°C
Storage temperature, T_{stg} . . . . . –65°C to 150°C
Lead temperature, 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 300°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	θ_{JA} (°C/W)	θ_{JC} (°C/W)	T_A = 25°C POWER RATING
D	167†	38.3	740 mW
DGN‡	58.4	4.7	2.14 W

† This data was taken using the JEDEC standard Low-K test PCB. For the JEDEC Proposed High-K test PCB, the θ_{JA} is 95°C/W with a power rating at T_A = 25°C of 1.32 W.
‡ This data was taken using 2 oz. trace and copper pad that is soldered directly to a 3 in. × 3 in. PC. For further information, refer to *Application Information* section of this data sheet.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC+} and V_{CC-}	Dual supply	±2.5		±16	V
	Single supply	5		32	
Operating free-air temperature, T_A	C-suffix	0		70	°C
	I-suffix	–40		85	

electrical characteristics at T_A = 25°C, V_{CC} = ±15 V, R_L = 150 Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage operating range	Dual supply		±2.25		±16.5	V
		Single supply		4.5		33	
I_{CC}	Supply current (per amplifier)	V_{CC} = ±15 V	T_A = 25°C		8.5	10	mA
			T_A = full range			11	
		V_{CC} = ±5 V	T_A = 25°C		7.5	9	
			T_A = full range			10.5	
		V_{CC} = ±2.5 V	T_A = 25°C		7.3	9	
			T_A = full range			10.5	
V_O	Output voltage swing	V_{CC} = ±15 V	R_L = 1 kΩ	±13	±13.6		V
		V_{CC} = ±5 V		±3.4	±3.8		
		V_{CC} = ±2.5 V		±1	±1.3		
		V_{CC} = ±15 V	R_L = 250 Ω	±12	±12.9		
		V_{CC} = ±5 V	R_L = 150 Ω	±3	±3.5		
		V_{CC} = ±2.5 V		±0.9	±1.2		
I_O	Output current (see Note 1)	V_{CC} = ±15 V	R_L = 20 Ω	60	90		mA
		V_{CC} = ±5 V		50	70		
		V_{CC} = ±2.5 V		40	55		
I_{SC}	Short-circuit current (see Note 1)	V_{CC} = ±15 V			150		mA
V_{IO}	Input offset voltage	V_{CC} = ±5 V or ±15 V	T_A = 25°C		1.5	6	mV
			T_A = full range			8	
	Offset drift	V_{CC} = ±5 V or ±15 V	T_A = full range		20		µV/°C
I_{IB}	Input bias current	V_{CC} = ±5 V or ±15 V	T_A = 25°C		3	6	µA
			T_A = full range			8	
I_{OS}	Input offset current	V_{CC} = ±5 V or ±15 V	T_A = 25°C		30	250	nA
			T_A = full range			400	
	Offset current drift	V_{CC} = ±5 V or ±15 V	T_A = full range		0.3		nA/°C
CMRR	Common mode rejection ratio	V_{CC} = ±15 V, V_{ICR} = ±12 V	T_A = 25°C	85	95		dB
			T_A = full range	80			
		V_{CC} = ±5 V, V_{ICR} = ±2.5 V	T_A = 25°C	90	100		
			T_A = full range	85			
PSRR	Power supply rejection ratio	V_{CC} = ±5 V or ±15 V	T_A = 25°C	85	95		dB
			T_A = full range	80			

† Full range = 0°C to 70°C for the THS6062C and –40°C to 85°C for the THS6062I.

NOTE 1: Observe power dissipation ratings to keep the junction temperature below absolute maximum ratings when the output is heavily loaded or shorted. See the absolute maximum ratings section for more information.

electrical characteristics at T_A = 25°C, V_{CC} = ±15 V, R_L = 150 Ω (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{ICR}	Common-mode input voltage range	V_{CC} = ±15 V		±13.5	±14.3		V
		V_{CC} = ±5 V		±3.8	±4.3		
		V_{CC} = ±2.5 V		±1.4	±1.8		
R_I	Input resistance				2		MΩ
C_i	Input capacitance				1.5		pF
R_O	Output resistance	Open loop			13		Ω
	Open loop gain	V_{CC} = ±15 V, V_O = ±10 V, R_L = 1 kΩ	T_A = 25°C	40	70		V/mV
			T_A = full range	35			
		V_{CC} = ±5 V, V_O = ±2.5 V, R_L = 1 kΩ	T_A = 25°C	35	50		V/mV
			T_A = full range	30			

† Full range = 0°C to 70°C for the THS6062C and –40°C to 85°C for the THS6062I.

operating characteristics at T_A = 25°C, V_{CC} = ±15 V, R_L = 150 Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP	MAX	UNIT
SR	Slew rate (see Note 2)	V_{CC} = ±15 V	Gain = –1		100		V/µs
		V_{CC} = ±5 V			80		
		V_{CC} = ±2.5 V			70		
t_s	Settling time to 0.1%	V_{CC} = ±15 V, 5-V step	Gain = –1		60		ns
		V_{CC} = ±5 V, 2.5-V step			45		
		V_{CC} = ±2.5 V, 1-V step			35		
	Settling time to 0.01%	V_{CC} = ±15 V, 5-V step	Gain = –1		90		ns
		V_{CC} = ±5 V, 2.5-V step			80		
		V_{CC} = ±2.5 V, 1-V step			75		
THD	Total harmonic distortion	V_{CC} = ±5 V or ±15 V, $V_{O(pp)}$ = 2 V, f = 1 MHz, Gain = 2	R_L = 150 Ω		–72		dBc
			R_L = 1 kΩ		–90		
V_n	Input voltage noise	V_{CC} = ±5 V or ±15 V, f = 10 kHz			1.6		nV/√Hz
I_n	Input current noise	V_{CC} = ±5 V or ±15 V, f = 10 kHz			1.2		pA/√Hz
BW	Dynamic performance small-signal bandwidth (–3 dB)	V_{CC} = ±15 V	$V_{O(pp)}$ = 0.4 V, Gain = 2, –1		100		MHz
		V_{CC} = ±5 V			90		
		V_{CC} = ±2.5 V			85		
	Bandwidth for 0.1 dB flatness	V_{CC} = ±15 V	$V_{O(pp)}$ = 0.4 V, Gain = 2, –1		50		
		V_{CC} = ±5 V			45		
		V_{CC} = ±2.5 V			40		
	Full power bandwidth (see Note 3)	$V_{O(pp)}$ = 20 V, V_{CC} = ±15 V	R_L = 1 kΩ		1.6		MHz
		$V_{O(pp)}$ = 5 V, V_{CC} = ±5 V			5		
	Channel-to-channel crosstalk	V_{CC} = ±5 V or ±15 V, f = 1 MHz, Gain = 2			–61		dBc

† Full range = 0°C to 70°C for the THS6062C and –40°C to 85°C for the THS6062I.

NOTES: 2. Slew rate is measured from an output level range of 25% to 75%.

3. Full power bandwidth = slew rate /2 π $V_{(peak)}$

PARAMETER MEASUREMENT INFORMATION

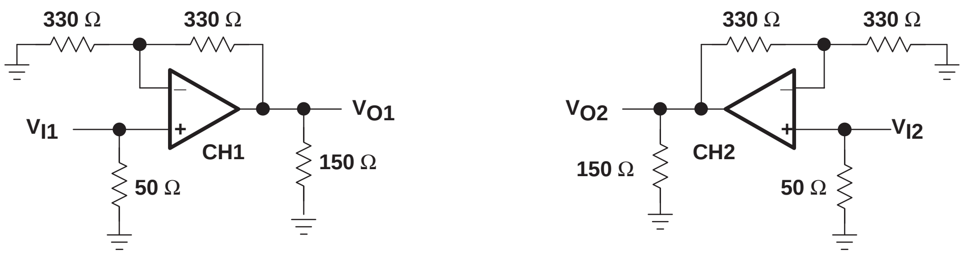


Figure 2. THS6062 Crosstalk Test Circuit

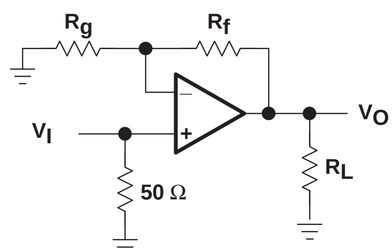


Figure 3. Step Response Test Circuit

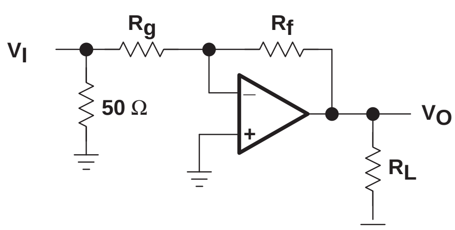


Figure 4. Step Response Test Circuit

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
V_{IO}	Input offset voltage	vs Free-air temperature	5
I_{IB}	Input bias current	vs Free-air temperature	6
V_O	Output voltage	vs Supply voltage	7
	Maximum output voltage swing	vs Free-air temperature	8
I_O	Maximum output current	vs Free-air temperature	9
I_{CC}	Supply current	vs Free-air temperature	10
V_{IC}	Common-mode input voltage	vs Supply voltage	11
Z_O	Closed-loop output impedance	vs Frequency	12
	Open-loop gain		13
	Phase response		13
PSRR	Power-supply rejection ratio	vs Frequency	14
CMRR	Common-mode rejection ratio	vs Frequency	15
	Crosstalk	vs Frequency	16
	Harmonic distortion	vs Frequency	17, 18
	Harmonic distortion	vs Peak-to-peak output voltage	19, 20
SR	Slew rate	vs Free-air temperature	21
	0.1% settling time	vs Output voltage step size	22
	Output amplitude	vs Frequency	23–29
	Small and large frequency response		30–33
	1-V step response		34, 35
	4-V step response		36
	20-V step response		37

TYPICAL CHARACTERISTICS

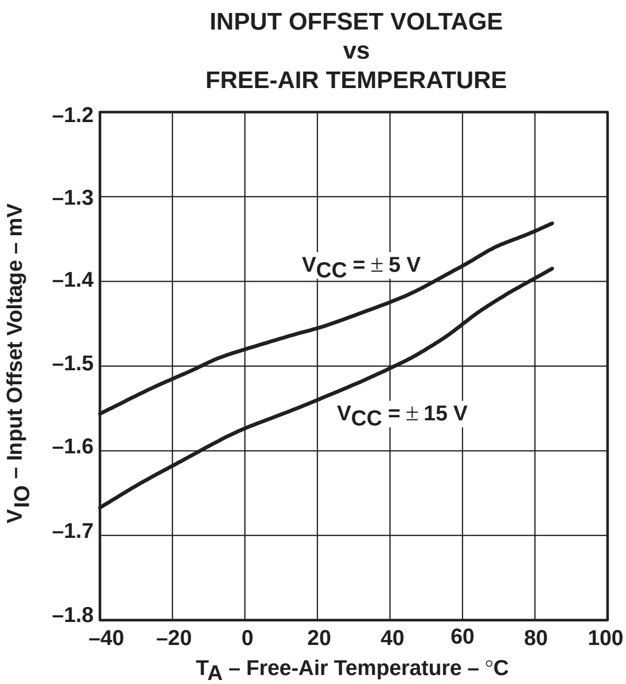


Figure 5

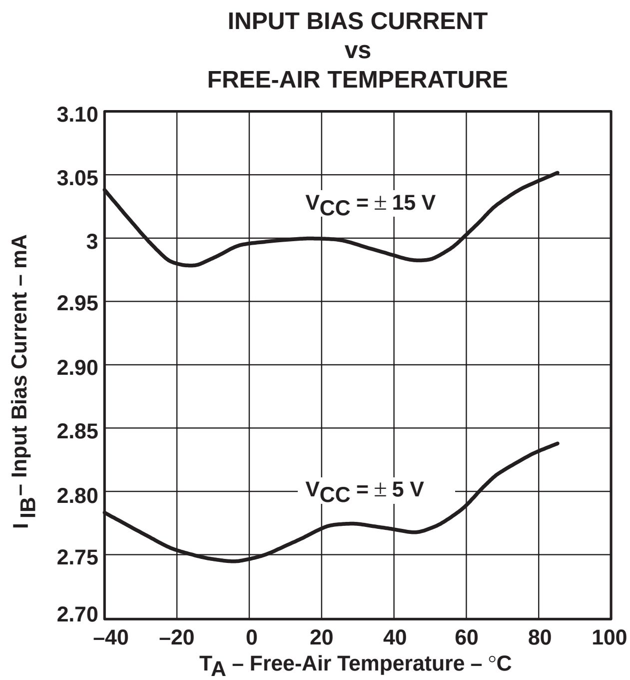


Figure 6

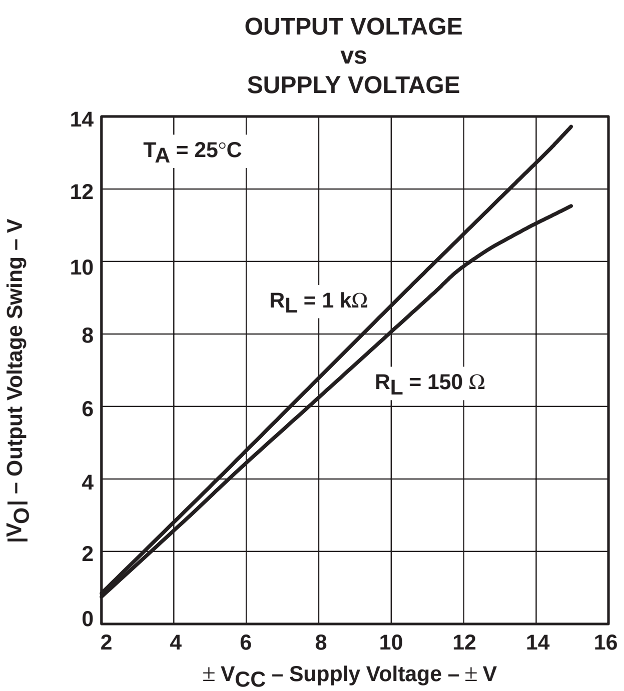


Figure 7

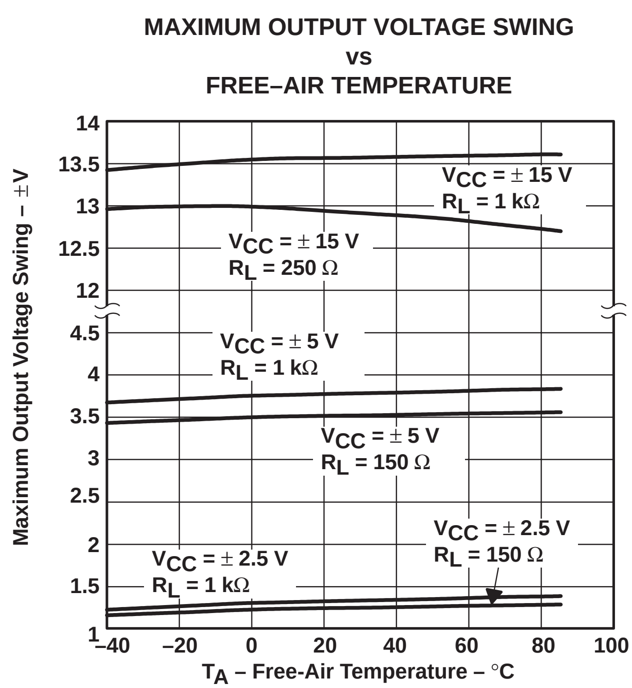


Figure 8

TYPICAL CHARACTERISTICS

MAXIMUM OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

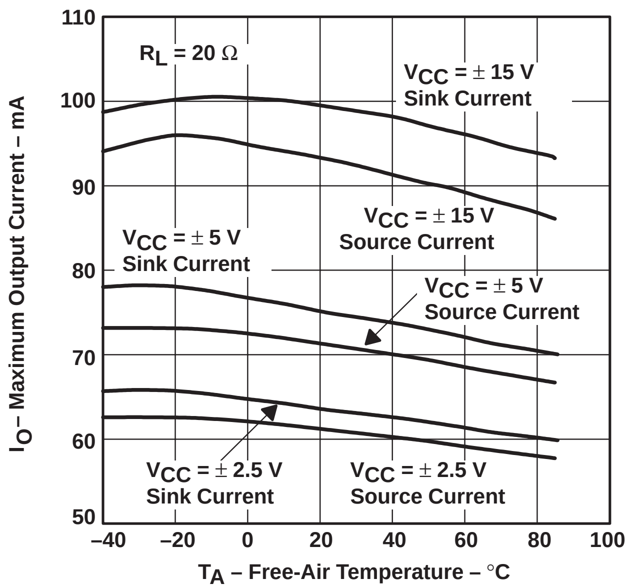


Figure 9

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

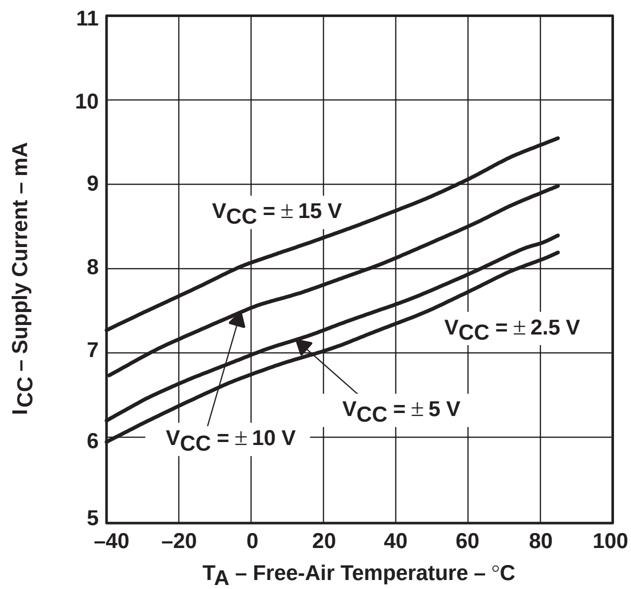


Figure 10

COMMON-MODE INPUT VOLTAGE
vs
SUPPLY VOLTAGE

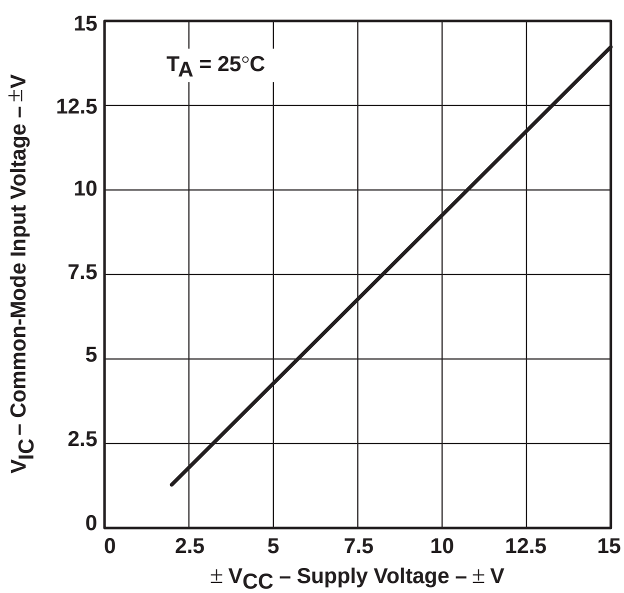


Figure 11

CLOSED-LOOP OUTPUT IMPEDANCE
vs
FREQUENCY

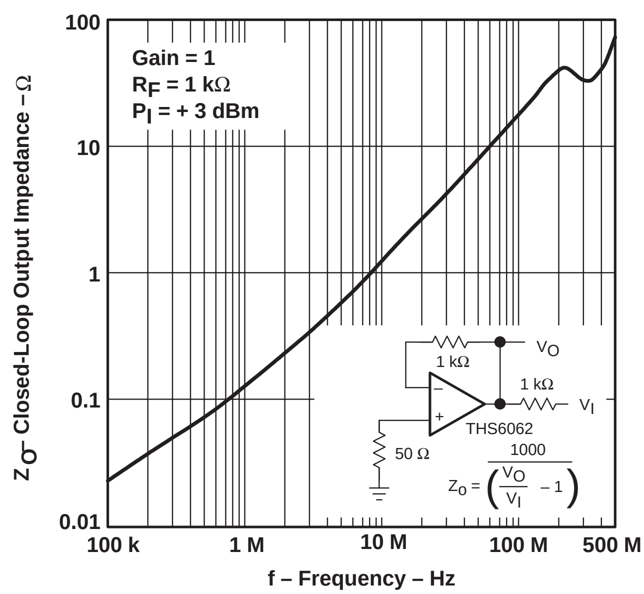


Figure 12

TYPICAL CHARACTERISTICS

OPEN-LOOP GAIN AND PHASE RESPONSE

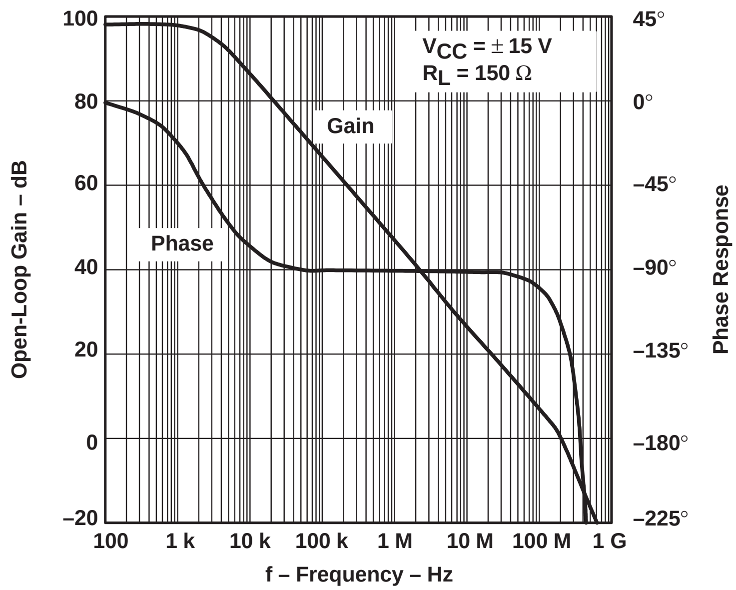


Figure 13

POWER-SUPPLY REJECTION RATIO
vs
FREQUENCY

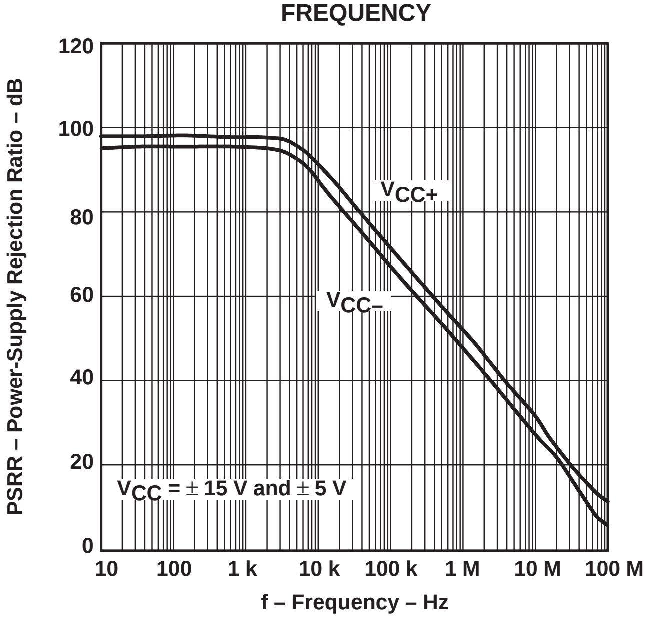


Figure 14

COMMON-MODE REJECTION RATIO
vs
FREQUENCY

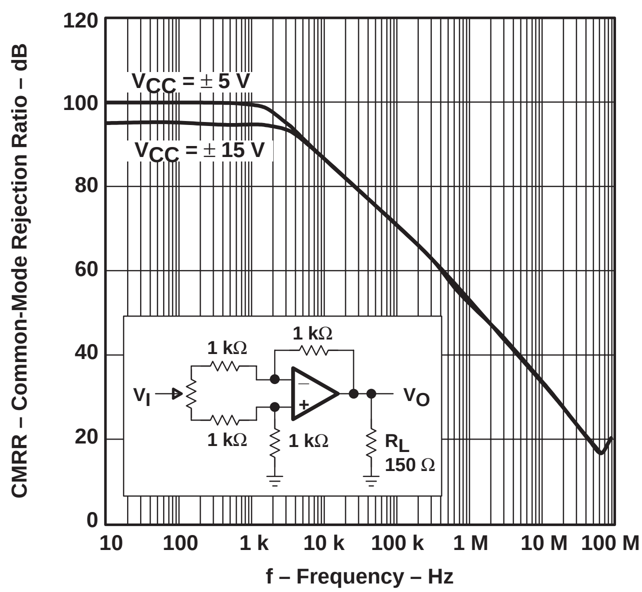


Figure 15

TYPICAL CHARACTERISTICS

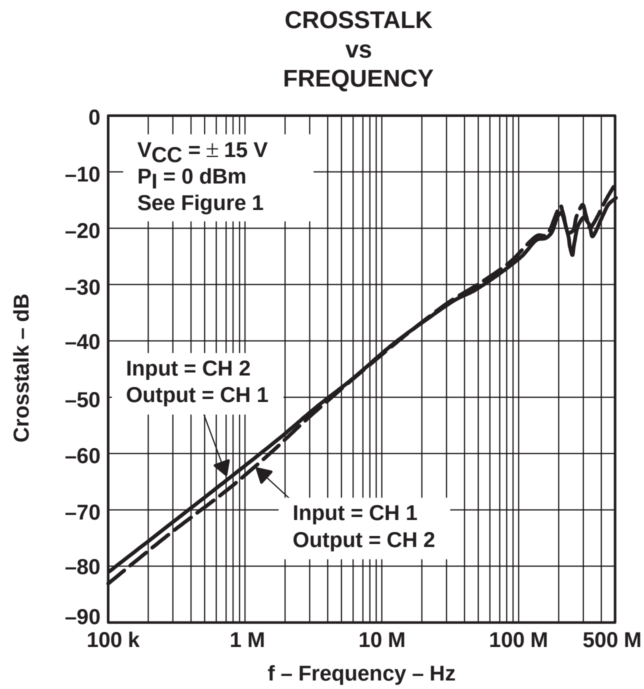


Figure 16

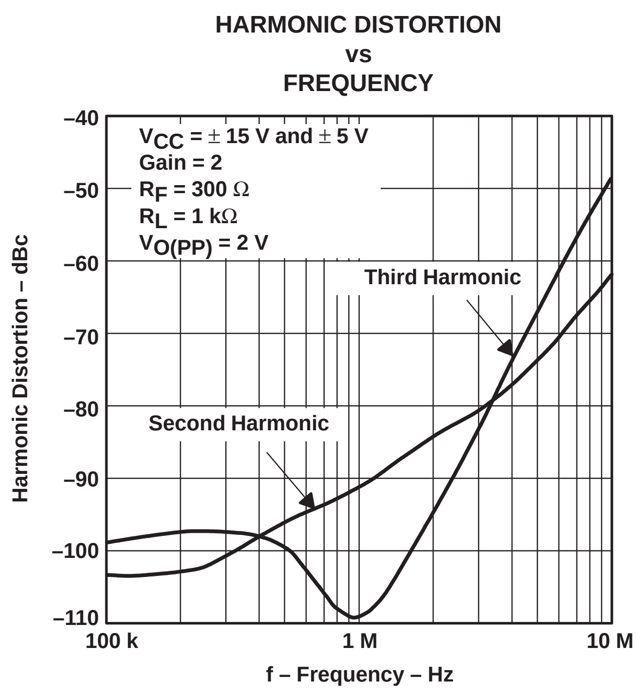


Figure 17

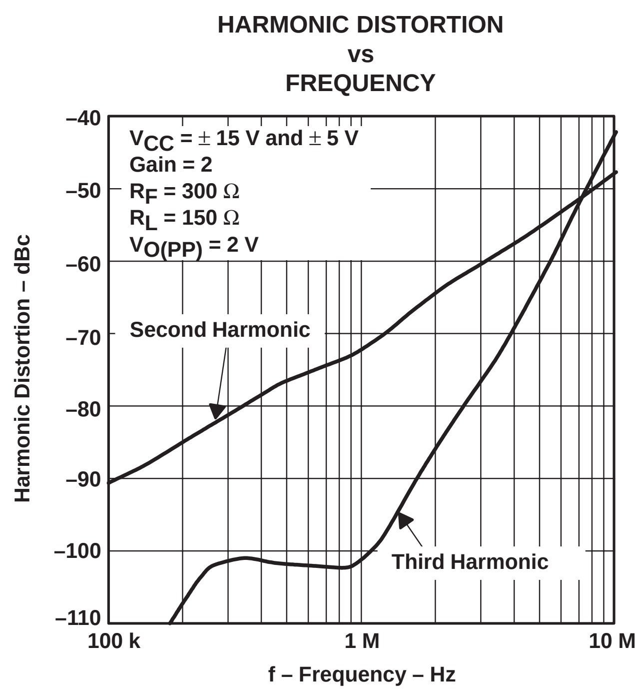


Figure 18

TYPICAL CHARACTERISTICS

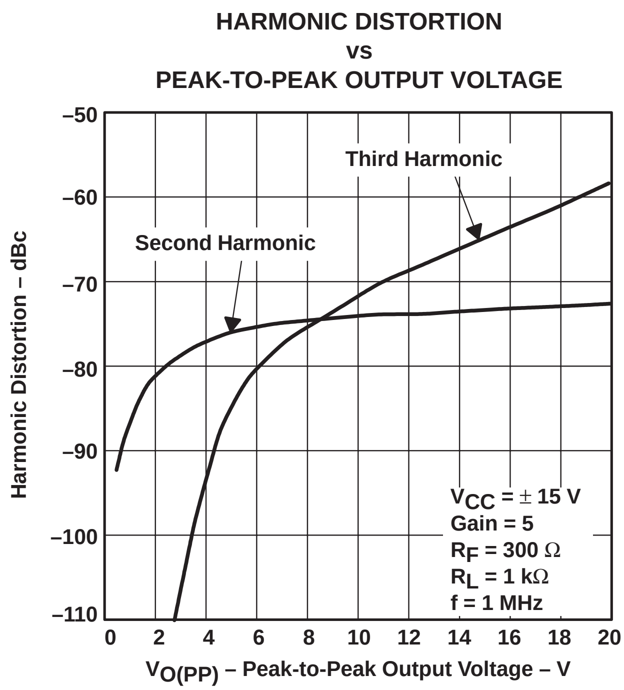


Figure 19

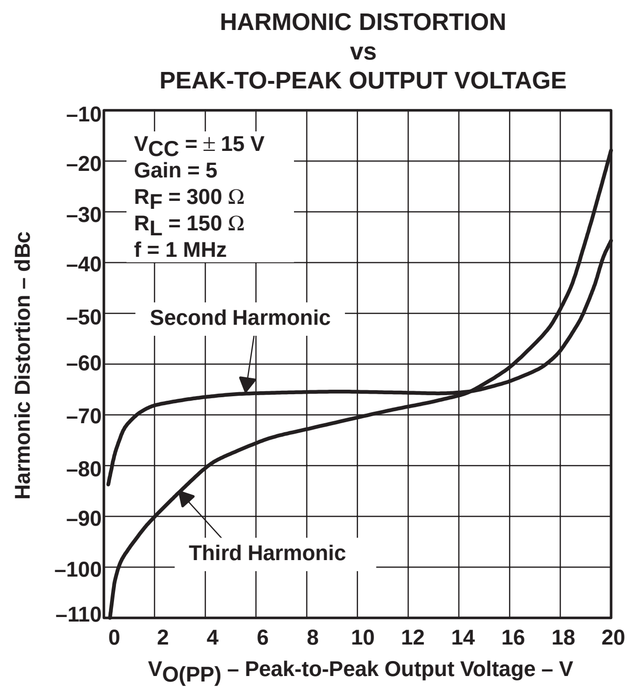


Figure 20

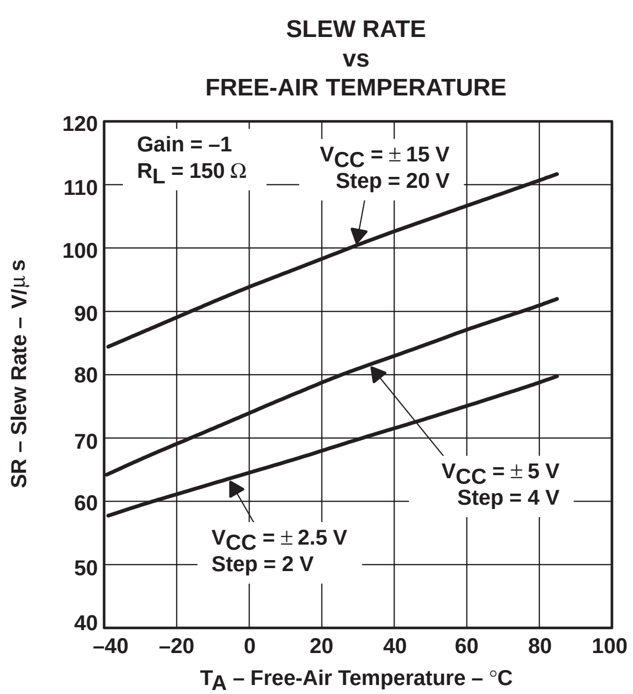


Figure 21

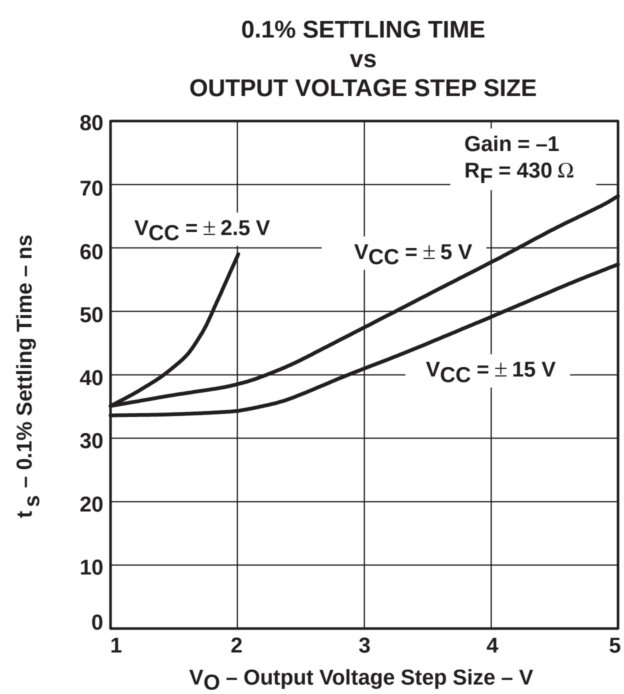


Figure 22

TYPICAL CHARACTERISTICS

OUTPUT AMPLITUDE vs FREQUENCY

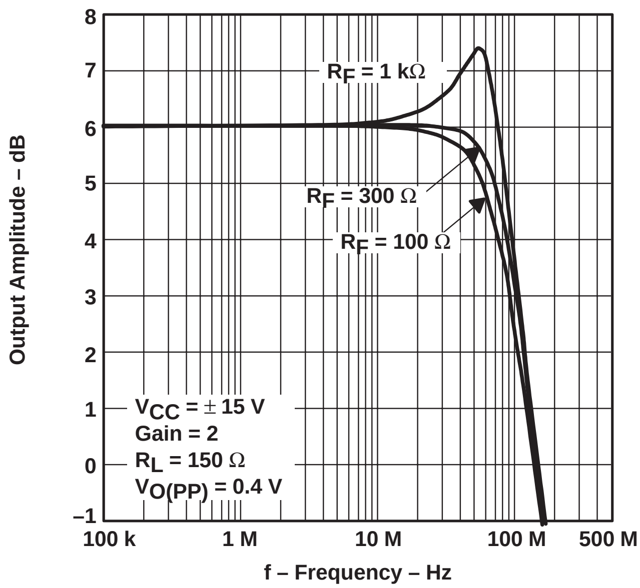


Figure 23

OUTPUT AMPLITUDE vs FREQUENCY

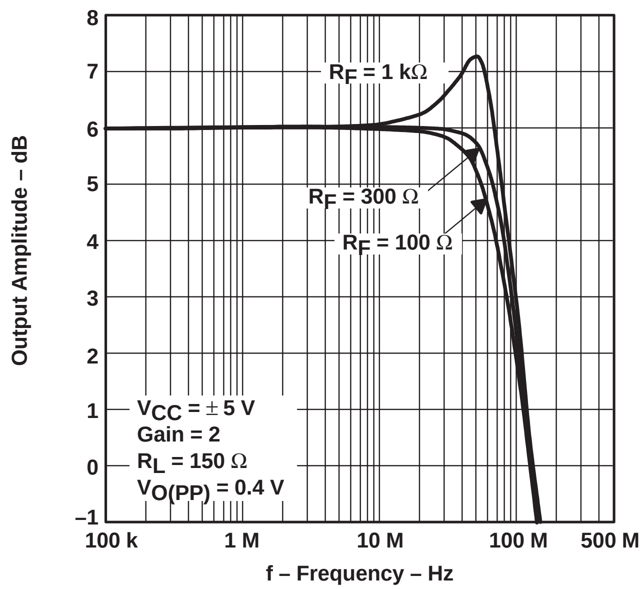


Figure 24

OUTPUT AMPLITUDE vs FREQUENCY

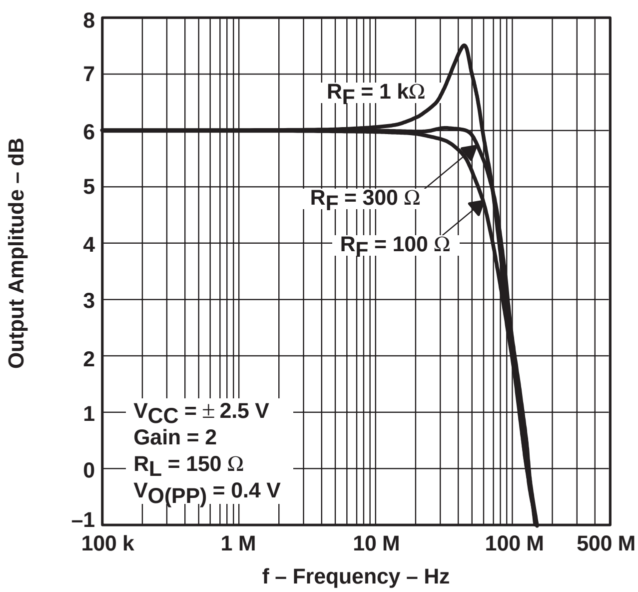


Figure 25

OUTPUT AMPLITUDE vs FREQUENCY

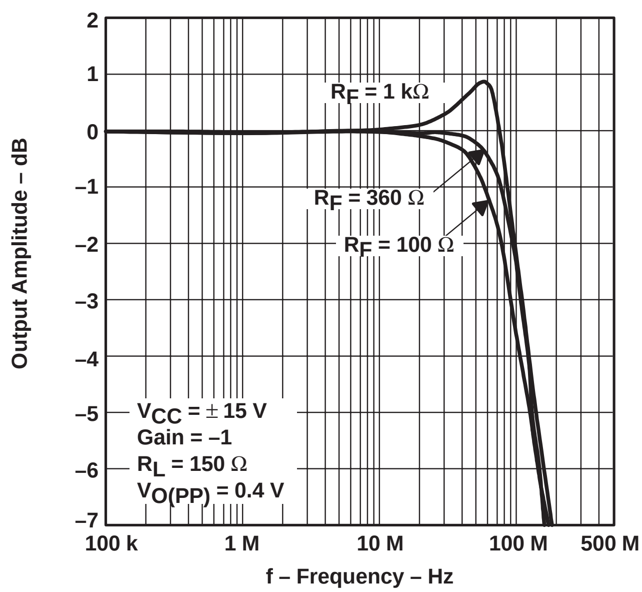


Figure 26

TYPICAL CHARACTERISTICS

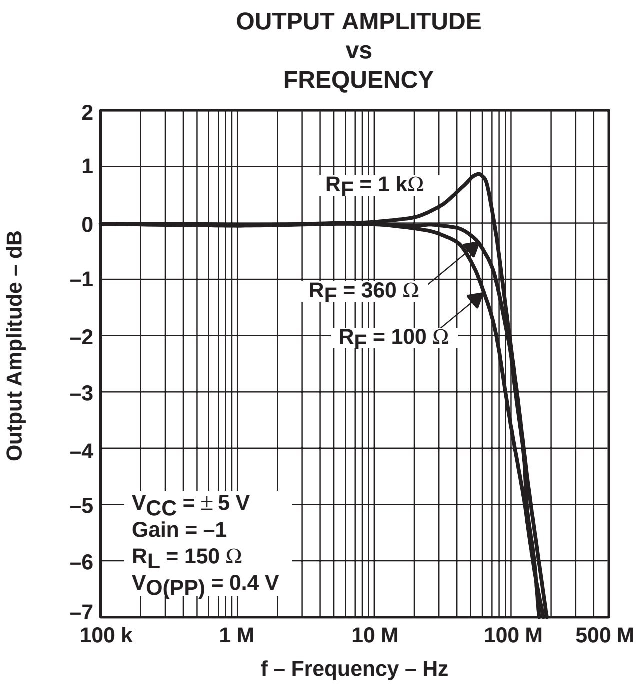


Figure 27

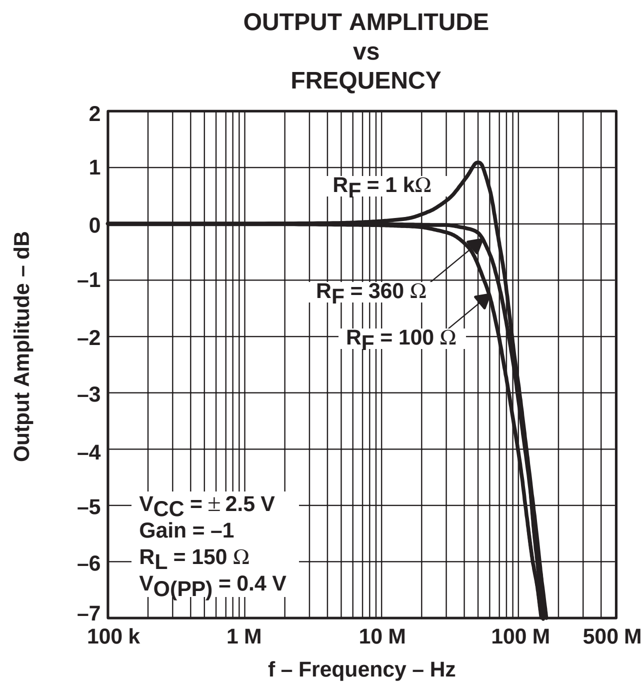


Figure 28

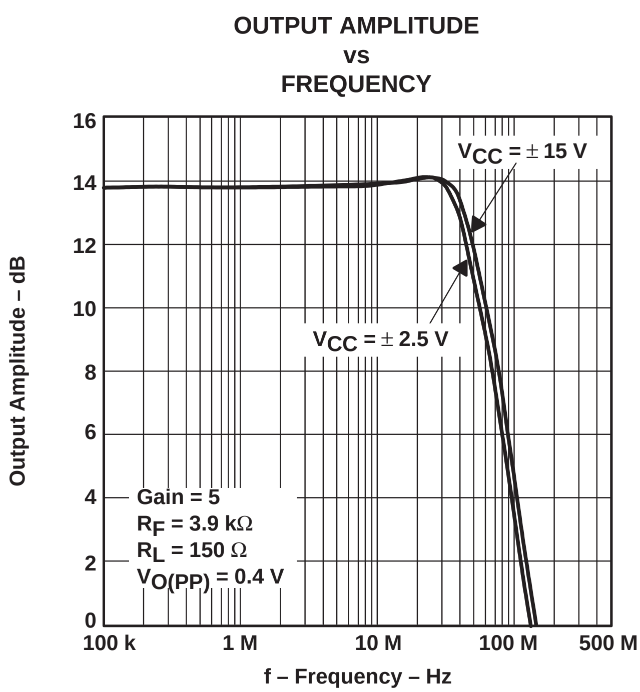


Figure 29

TYPICAL CHARACTERISTICS

SMALL AND LARGE SIGNAL
FREQUENCY RESPONSE

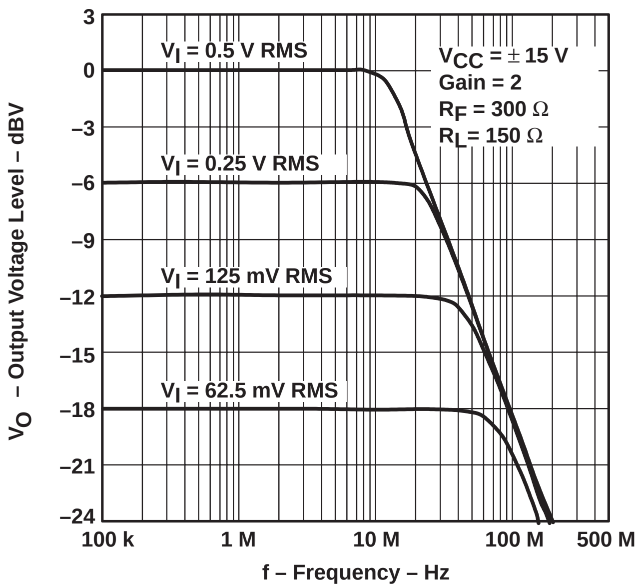


Figure 30

SMALL AND LARGE SIGNAL
FREQUENCY RESPONSE

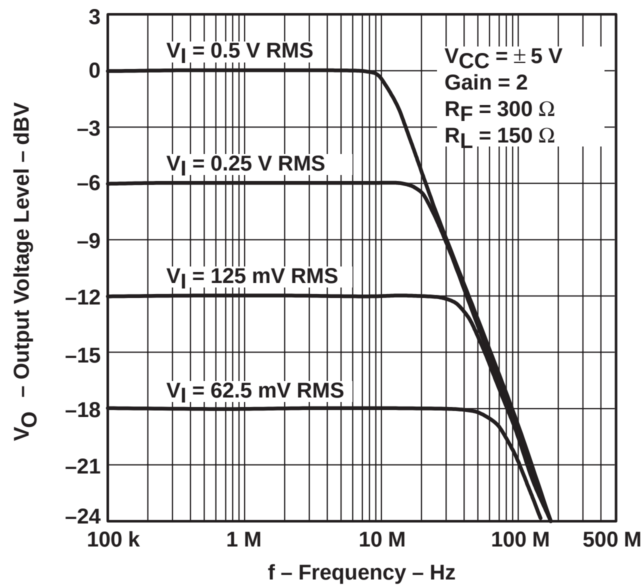


Figure 31

SMALL AND LARGE SIGNAL
FREQUENCY RESPONSE

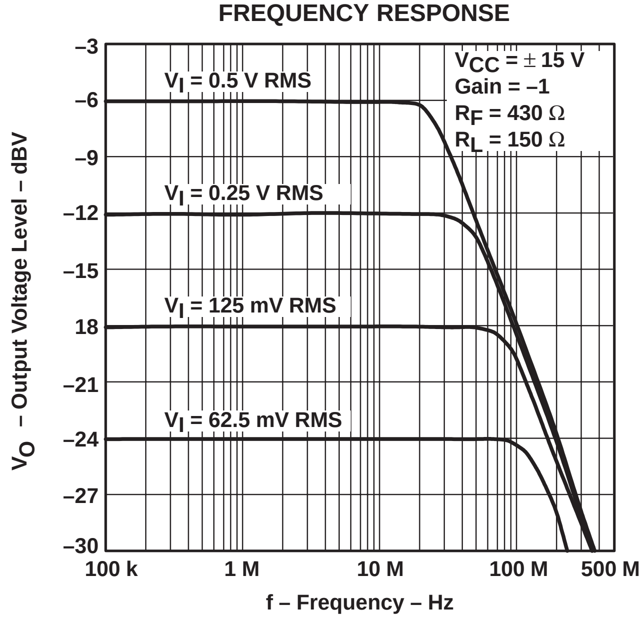


Figure 32

SMALL AND LARGE SIGNAL
FREQUENCY RESPONSE

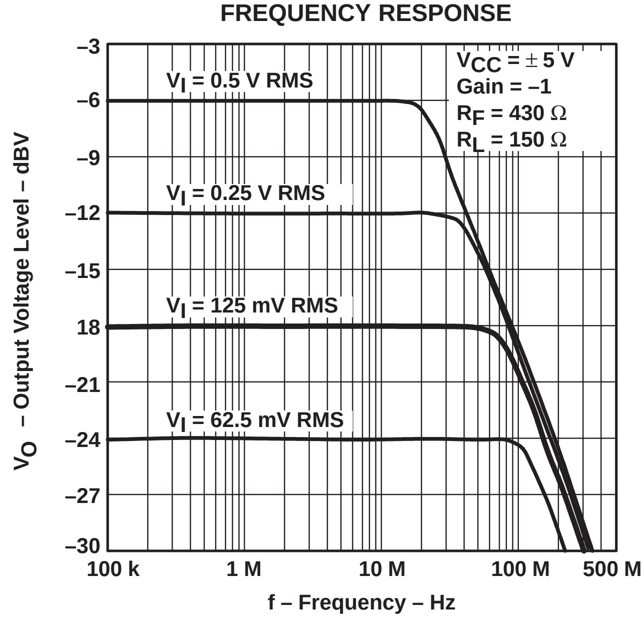


Figure 33

TYPICAL CHARACTERISTICS

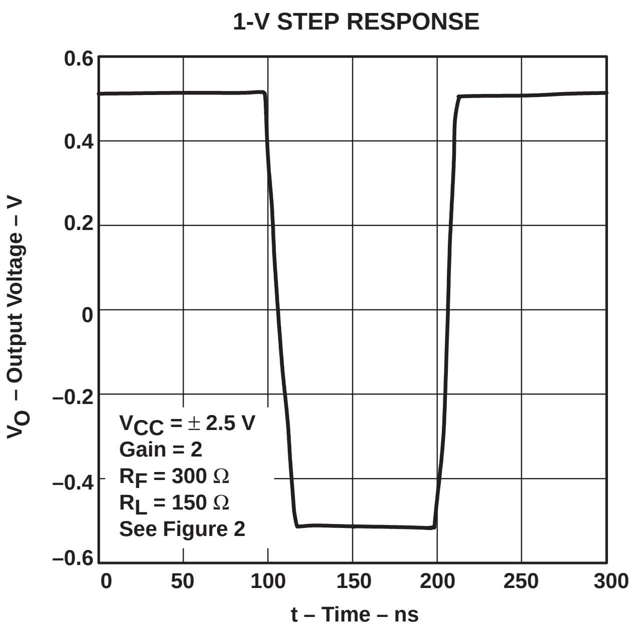


Figure 34

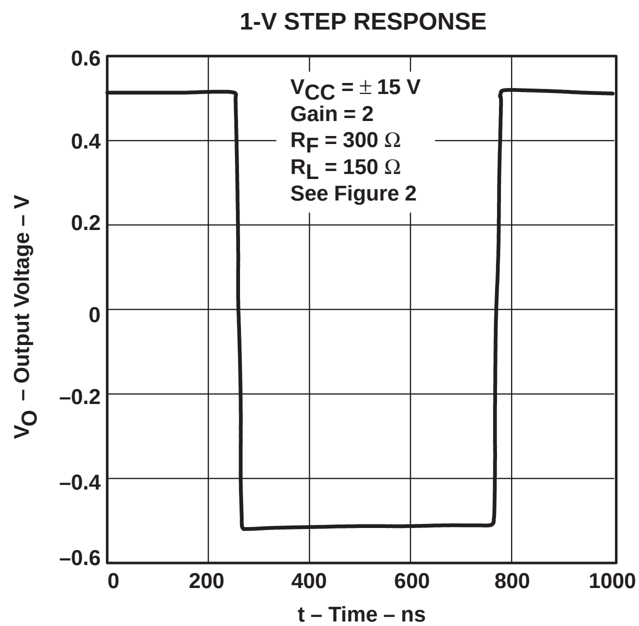


Figure 35

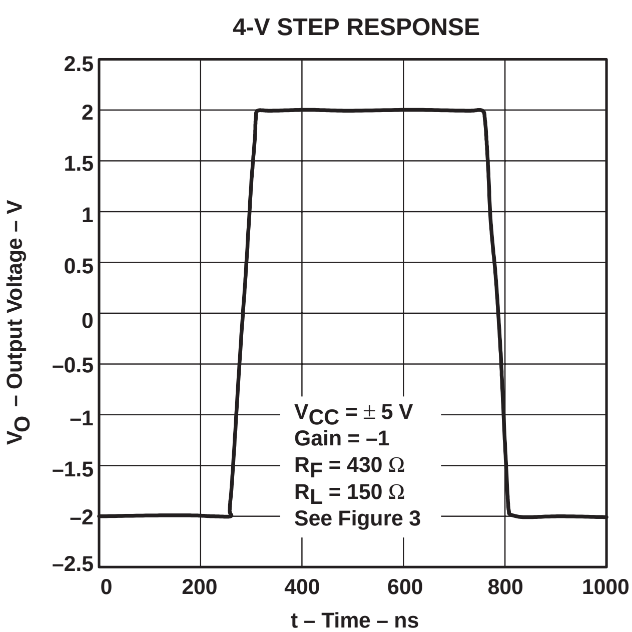


Figure 36

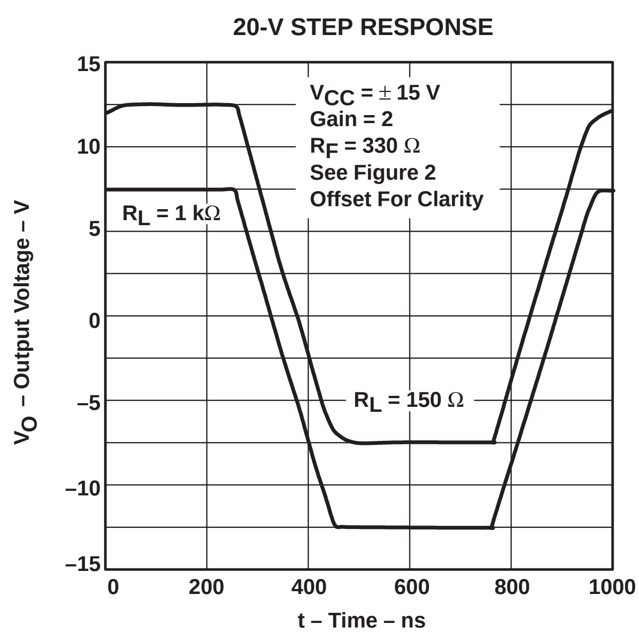


Figure 37

APPLICATION INFORMATION

theory of operation

The THS6062 is a high-speed, operational amplifier configured in a voltage feedback architecture. It is built using a 30-V, dielectrically isolated, complementary bipolar process with NPN and PNP transistors possessing f_Ts of several GHz. This results in an exceptionally high-performance amplifier that has a wide bandwidth, high slew rate, fast settling time, and low distortion. A simplified schematic is shown in Figure 38.

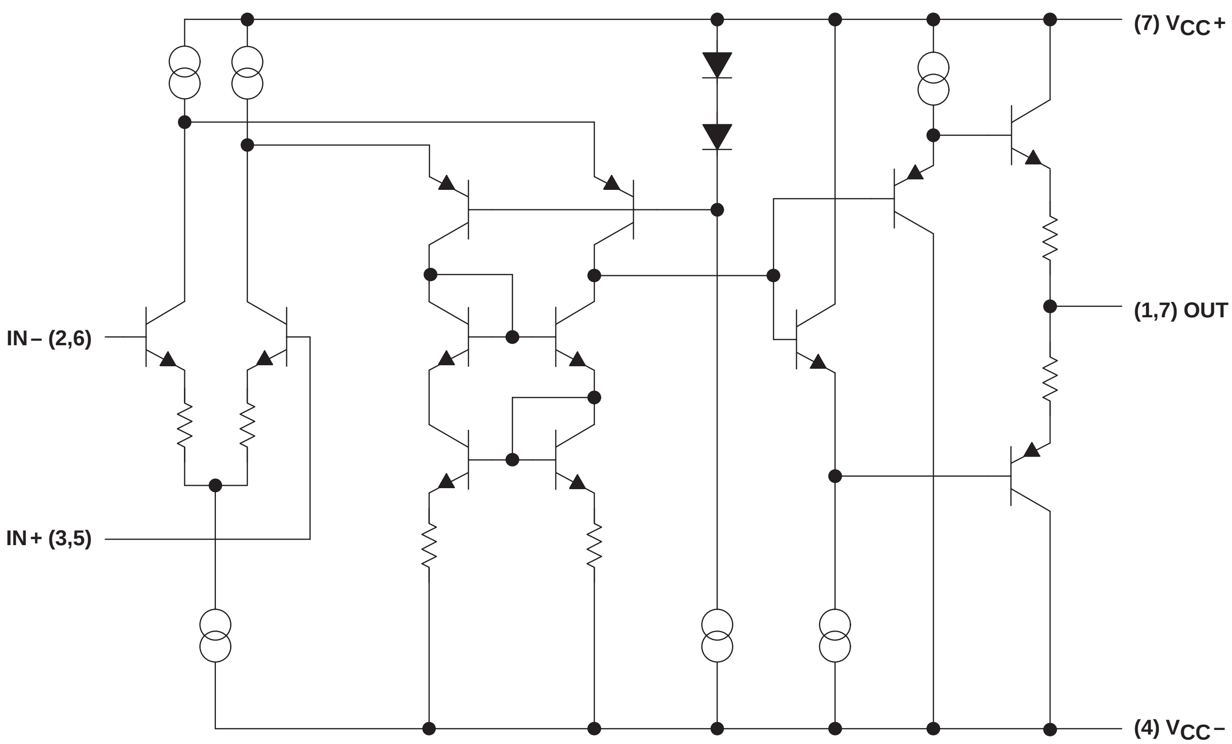


Figure 38. THS6062 Simplified Schematic

APPLICATION INFORMATION

The ADSL remote terminal receive band consists of 255 separate carrier frequencies each with its own modulation and amplitude level. With such an implementation, it is imperative that signals received off the telephone line have as high a signal-to-noise ratio (SNR) as possible. This is because of the numerous sources of interference on the line. The best way to accomplish this high SNR is to have a low-noise receiver on the front-end. It is also important to have the lowest distortion possible to help minimize against interference within the ADSL carriers. The THS6062 was designed with these two priorities in mind.

By taking advantage of the superb characteristics of the complimentary bipolar process (BICOM), the THS6062 offers extremely low noise and distortion while maintaining a high bandwidth. There are some aspects that help minimize distortion in any amplifier. The first is to extend the bandwidth of the amplifier as high as possible without peaking. This allows the amplifier to eliminate any nonlinearities in the output signal. Another thing that helps to minimize distortion is to increase the load impedance seen by the amplifier, thereby reducing the currents in the output stage. This will help keep the output transistors in their linear amplification range and will also reduce the heating effects. This can be seen in Figures 17 to 20, which show a 1-kΩ load distortion is much better than a 150 Ω load.

One client side terminal circuit implementation, shown in Figure 39, uses a 1:2 transformer ratio. While creating a power and output voltage advantage for the line drivers, the 1:2 transformer ratio reduces the SNR for the received signals. The ADSL standard, ANSI T1.413, stipulates a noise power spectral density of –140 dBm/Hz, which is equivalent to 31.6 $nV/\sqrt{Hz}$ for a 100 Ω system. Although many amplifiers can reach this level of performance, actual ADSL system testing has indicated that the noise power spectral density may typically be ≤ –150 dBm/Hz, or ≤ 10 $nV/\sqrt{Hz}$. With a transformer ratio of 1:2, this number reduces to less than 5 $nV/\sqrt{Hz}$. The THS6062, with an equivalent input noise of 1.6 $nV/\sqrt{Hz}$, is an excellent choice for this application. Coupled with a very low 1.2 $pA/\sqrt{Hz}$ equivalent input current noise and low value resistors, the THS6062 will ensure that the received signal SNR will be as high as possible.

APPLICATION INFORMATION

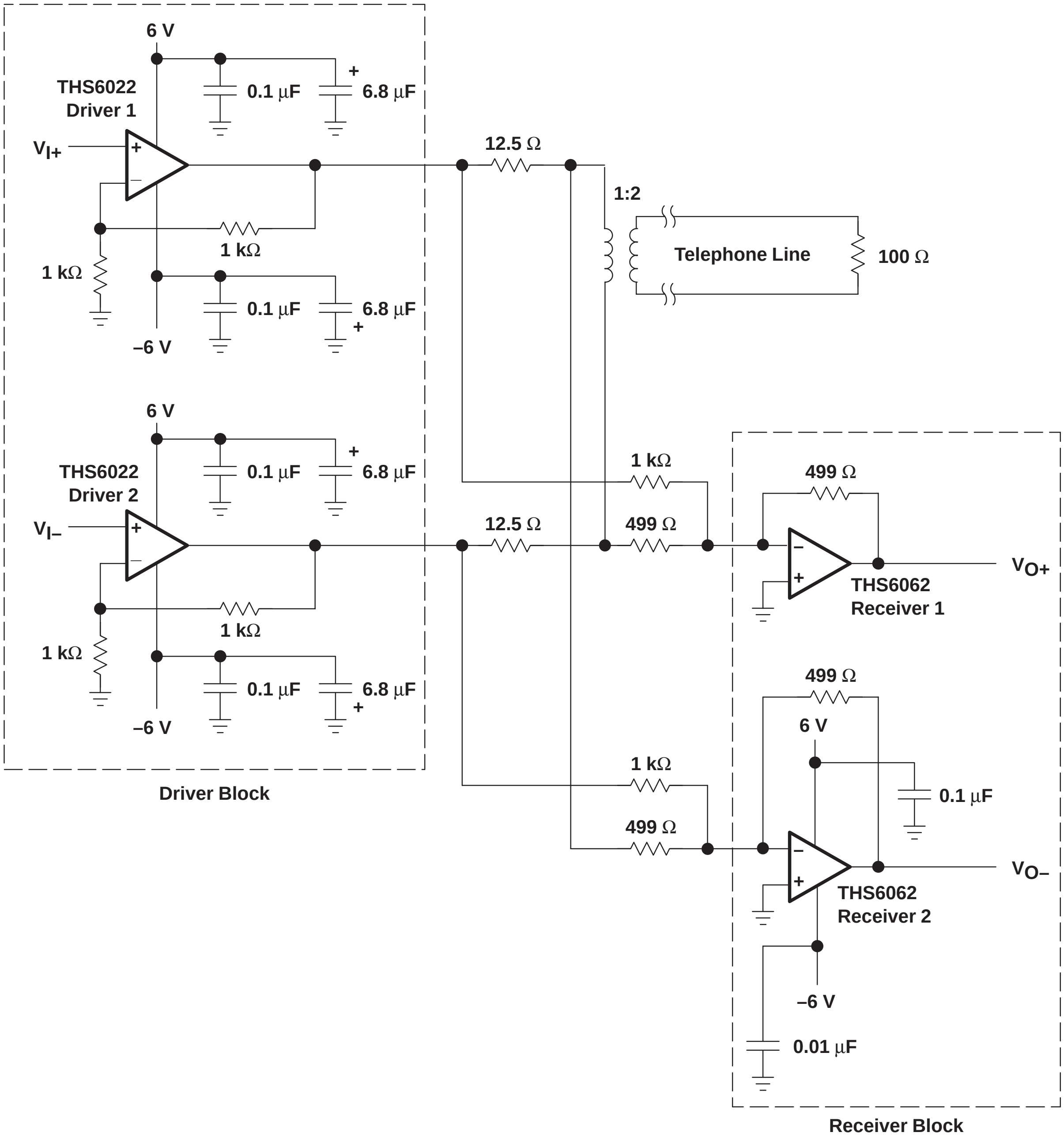


Figure 39. THS6062 Client-Side ADSL Application

APPLICATION INFORMATION

noise calculations and noise figure

Noise can cause errors on very small signals. This is especially true for the amplifying small signals. The noise model for current feedback amplifiers (CFB) is the same as voltage feedback amplifiers (VFB). The only difference between the two is that the CFB amplifiers generally specify different current noise parameters for each input, while VFB amplifiers usually only specify one noise current parameter. The noise model is shown in Figure 40. This model includes all of the noise sources as follows:

- e_n = amplifier internal voltage noise (nV/$\sqrt{Hz}$)
- IN+ = noninverting current noise (pA/$\sqrt{Hz}$)
- IN– = inverting current noise (pA/$\sqrt{Hz}$)
- e_{Rx} = thermal voltage noise associated with each resistor (e_{Rx} = 4 kTR_x)

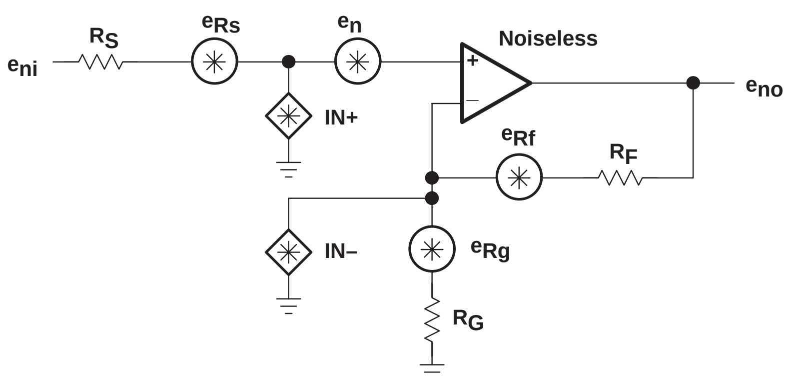


Figure 40. Noise Model

The total equivalent input noise density (e_{ni}) is calculated by using the following equation:

$$e_{ni} = \sqrt{\left(e_n\right)^2 + \left(IN+ \times R_S\right)^2 + \left(IN- \times \left(R_F \parallel R_G\right)\right)^2 + 4\ kTR_S + 4\ kT\left(R_F \parallel R_G\right)}$$

Where:

k = Boltzmann’s constant = 1.380658×10^{-23}
T = temperature in degrees Kelvin (273 +°C)
R_F || R_G = parallel resistance of R_F and R_G

To get the equivalent output noise of the amplifier, just multiply the equivalent input noise density (e_{ni}) by the overall amplifier gain (A_V).

$$e_{no} = e_{ni}\ A_V = e_{ni}\left(1 + \frac{R_F}{R_G}\right) \text{ (Noninverting Case)}$$

As the previous equations show, to keep noise at a minimum, small value resistors should be used. As the closed-loop gain is increased (by reducing R_G), the input noise is reduced considerably because of the parallel resistance term. This leads to the general conclusion that the most dominant noise sources are the source resistor (R_S) and the internal amplifier noise voltage (e_n). Because noise is summed in a root-mean-squares method, noise sources smaller than 25% of the largest noise source can be effectively ignored. This can greatly simplify the formula and make noise calculations much easier to calculate.

APPLICATION INFORMATION

noise calculations and noise figure (continued)

For more information on noise analysis, please refer to the *Noise Analysis* section in *Operational Amplifier Circuits Applications Report* (literature number SLVA043).

This brings up another noise measurement usually preferred in RF applications, the noise figure (NF). Noise figure is a measure of noise degradation caused by the amplifier. The value of the source resistance must be defined and is typically 50 Ω in RF applications.

$$NF = 10\log\left[\frac{{e_{ni}}^2}{\left(e_{Rs}\right)^2}\right]$$

Because the dominant noise components are generally the source resistance and the internal amplifier noise voltage, we can approximate the noise figure as:

$$NF = 10\log\left[1 + \frac{\left[\left(e_n\right)^2 + \left(IN + \times R_S\right)^2\right]}{4\ kTR_S}\right]$$

Figure 40 shows the noise figure graph for the THS6062.

NOISE FIGURE
vs
SOURCE RESISTANCE

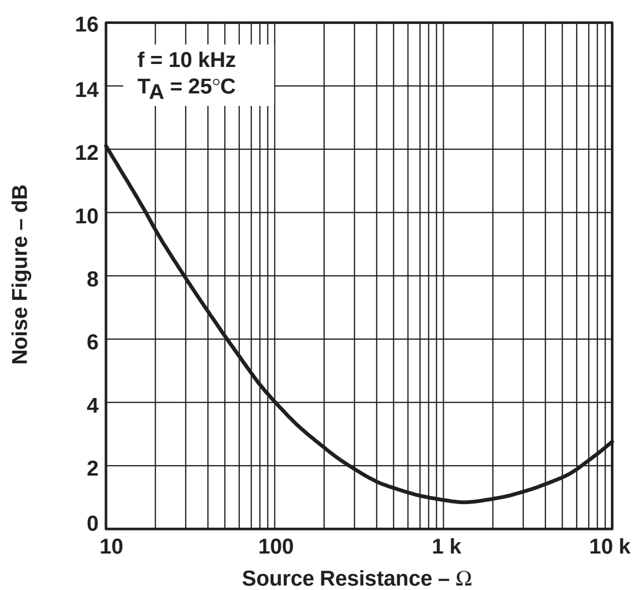


Figure 41. Noise Figure vs Source Resistance

APPLICATION INFORMATION

optimizing frequency response

Internal frequency compensation of the THS6062 was selected to provide very wide bandwidth performance and still maintain a very low noise floor. In order to meet these performance requirements, the THS6062 must have a minimum gain of 2 (–1). Because everything is referred to the noninverting terminal of an operational amplifier, the noise gain in a G = –1 configuration is the same as in a G = 2 configuration.

One of the keys to maintaining a smooth frequency response, and hence, a stable pulse response, is to pay particular attention to the inverting terminal. Any stray capacitance at this node causes peaking in the frequency response (see Figure 42 and Figure 43). There are two things that can be done to help minimize this effect. The first is to simply remove any ground planes under the inverting terminal of the amplifier. This also includes the trace that connects to this terminal. Additionally, the length of this trace should be minimized. The capacitance at this node causes a lag in the voltage being fed back due to the charging and discharging of the stray capacitance. If this lag becomes too long, the amplifier will not be able to correctly keep the noninverting terminal voltage at the same potential as the inverting terminal's voltage. Peaking and possibly oscillations will then occur.

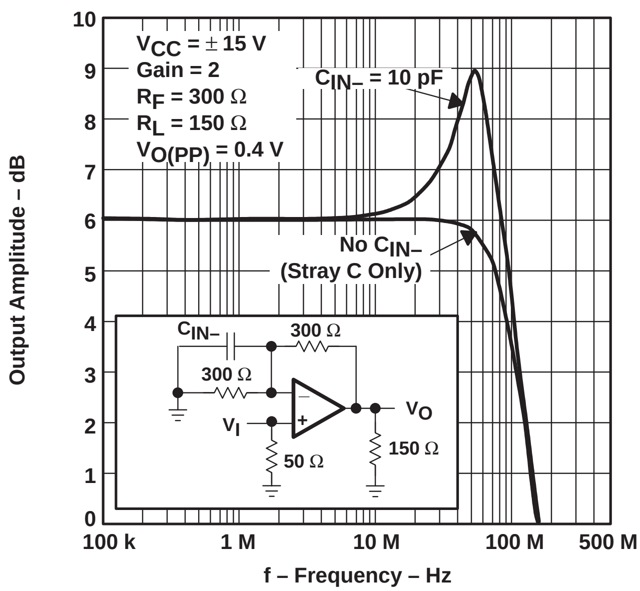


Figure 42

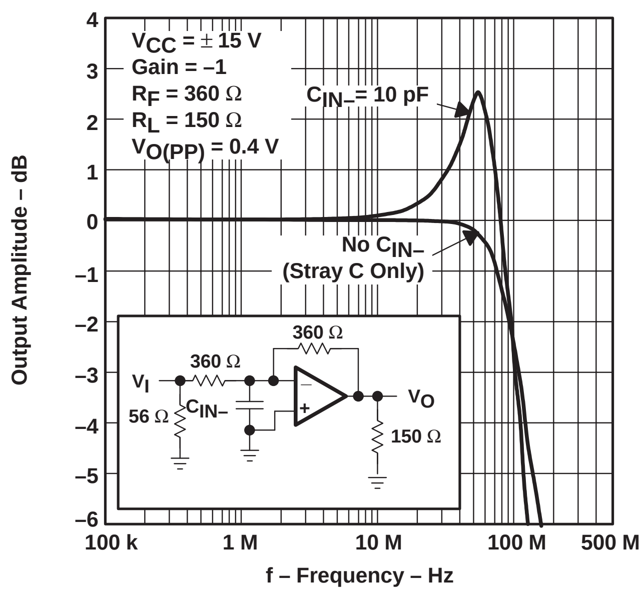


Figure 43

APPLICATION INFORMATION

optimizing frequency response (continued)

The next thing that helps to maintain a smooth frequency response is to keep the feedback resistor (R_f) and the gain resistor (R_g) values fairly low. These two resistors are effectively in parallel when looking at the ac small-signal response. This is why in Figure 29, a feedback resistor of 3.9 kΩ with a gain resistor of 1 kΩ only shows a small peaking in the frequency response. The parallel resistance is only 800 Ω. This value, in conjunction with a very small stray capacitance test PCB, forms a zero on the edge of the amplifier's natural frequency response. To eliminate this peaking, all that needs to be done is to reduce the feedback and gain resistances. One other way to compensate for this stray capacitance is to add a small capacitor in parallel with the feedback resistor. This helps to neutralize the effects of the stray capacitance. To keep this zero out of the operating range, the stray capacitance and resistor value's time constant must be kept low. But, as can be seen in Figures 23 – 28, a value too low starts to reduce the bandwidth of the amplifier. Table 1 shows some recommended feedback resistors to be used with the THS6062.

Table 1. Recommended Feedback Resistors

GAIN	R_f for V_{CC} = ±15 V, ± 5 V, 5 V
2	300 Ω
–1	360 Ω
5	3.3 kΩ (low stray-c PCB only)

driving a capacitive load

Driving capacitive loads with high performance amplifiers is not a problem as long as certain precautions are taken. The first is to realize that the THS6062 has been internally compensated to maximize its bandwidth and slew rate performance. When the amplifier is compensated in this manner, capacitive loading directly on the output will decrease the device's phase margin leading to high frequency ringing or oscillations. Therefore, for capacitive loads of greater than 10 pF, it is recommended that a resistor be placed in series with the output of the amplifier, as shown in Figure 44. A minimum value of 20 Ω should work well for most applications. For example, in 75-Ω transmission systems, setting the series resistor value to 75 Ω both isolates any capacitance loading and provides the proper line impedance matching at the source end.

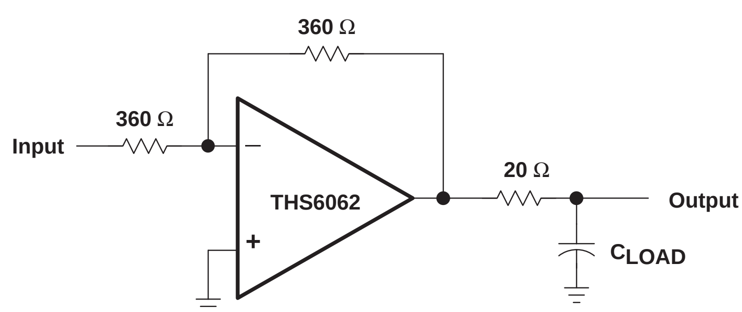
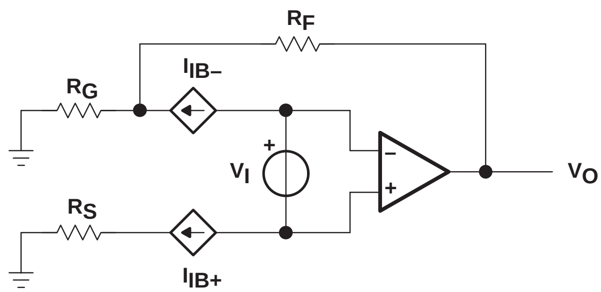


Figure 44. Driving a Capacitive Load

APPLICATION INFORMATION

offset voltage

The output offset voltage, (V_{OO}) is the sum of the input offset voltage (V_{IO}) and both input bias currents (I_{IB}) times the corresponding gains. The following schematic and formula are used to calculate the output offset voltage:



$$V_{OO} = V_{IO}\left(1 + \left(\frac{R_F}{R_G}\right)\right) \pm I_{IB+}\, R_S \left(1 + \left(\frac{R_F}{R_G}\right)\right) \pm I_{IB-}\, R_F$$

Figure 45. Output Offset Voltage Model

circuit layout considerations

In order to achieve the high-frequency performance of the THS6062, it is essential that proper printed-circuit board high frequency design techniques be followed. A general set of guidelines is given below. In addition, a THS6062 evaluation board is available to use as a guide for layout or for evaluating the device performance.

- Ground planes – It is highly recommended that a ground plane be used on the board to provide all components with a low inductive ground connection. However, in the areas of the amplifier inputs and output, the ground plane can be removed to minimize the stray capacitance.
- Proper power supply decoupling – Use a 6.8-µF tantalum capacitor in parallel with a 0.1-µF ceramic capacitor on each supply terminal. It may be possible to share the tantalum among several amplifiers depending on the application, but a 0.1-µF ceramic capacitor should always be used on the supply terminal of every amplifier. In addition, the 0.1-µF capacitor should be placed as close as possible to the supply terminal. As this distance increases, the inductance in the connecting trace makes the capacitor less effective. The designer should strive for distances of less than 0.1 inches between the device power terminals and the ceramic capacitors.
- Sockets – Sockets are not recommended for high-speed operational amplifiers. The additional lead inductance in the socket pins will often lead to stability problems. Surface-mount packages soldered directly to the printed-circuit board is the best implementation.
- Short trace runs/compact part placements – Optimum high frequency performance is achieved when stray series inductance has been minimized. To realize this, the circuit layout should be made as compact as possible, thereby minimizing the length of all trace runs. Particular attention should be paid to the inverting input of the amplifier. Its length should be kept as short as possible. This will help to minimize stray capacitance at the input of the amplifier.
- Surface-mount passive components – Using surface-mount passive components is recommended for high frequency amplifier circuits for several reasons. First, because of the extremely low lead inductance of surface-mount components, the problem with stray series inductance is greatly reduced. Second, the small size of surface-mount components naturally leads to a more compact layout, thereby minimizing both stray inductance and capacitance. If leaded components are used, it is recommended that the lead lengths be kept as short as possible.

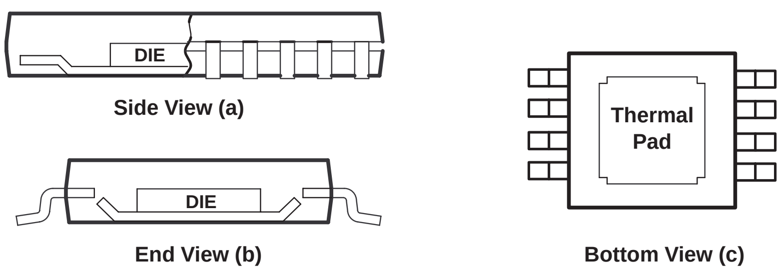
APPLICATION INFORMATION

general PowerPAD design considerations

The THS6062 is available packaged in a thermally-enhanced DGN package, which is a member of the PowerPAD family of packages. This package is constructed using a downset leadframe upon which the die is mounted [see Figure 46(a) and Figure 46(b)]. This arrangement results in the lead frame being exposed as a thermal pad on the underside of the package [see Figure 45(c)]. Because this thermal pad has direct thermal contact with the die, excellent thermal performance can be achieved by providing a good thermal path away from the thermal pad.

The PowerPAD package allows for both assembly and thermal management in one manufacturing operation. During the surface-mount solder operation (when the leads are being soldered), the thermal pad can also be soldered to a copper area underneath the package. Through the use of thermal paths within this copper area, heat can be conducted away from the package into either a ground plane or other heat dissipating device.

The PowerPAD package represents a breakthrough in combining the small area and ease of assembly of surface mount with the, heretofore, awkward mechanical methods of heatsinking.



NOTE A: The thermal pad is electrically isolated from all terminals in the package.

Figure 46. Views of Thermally Enhanced DGN Package

Although there are many ways to properly heatsink this device, the following steps illustrate the recommended approach.

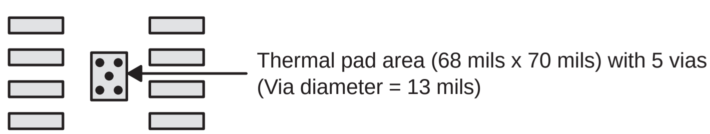


Figure 47. PowerPAD PCB Etch and Via Pattern

APPLICATION INFORMATION

general PowerPAD design considerations

1. Prepare the PCB with a top side etch pattern as shown in Figure 47. There should be etch for the leads as well as etch for the thermal pad.
2. Place five holes in the area of the thermal pad. These holes should be 13 mils in diameter. They are kept small so that solder wicking through the holes is not a problem during reflow.
3. Additional vias may be placed anywhere along the thermal plane outside of the thermal pad area. This helps dissipate the heat generated by the THS6062DGN IC. These additional vias may be larger than the 13-mil diameter vias directly under the thermal pad. They can be larger because they are not in the thermal pad area to be soldered so that wicking is not a problem.
4. Connect all holes to the internal ground plane.
5. When connecting these holes to the ground plane, **do not** use the typical web or spoke via connection methodology. Web connections have a high thermal resistance connection that is useful for slowing the heat transfer during soldering operations. This makes the soldering of vias that have plane connections easier. In this application, however, low thermal resistance is desired for the most efficient heat transfer. Therefore, the holes under the THS6062DGN package should make their connection to the internal ground plane with a complete connection around the entire circumference of the plated-through hole.
6. The top-side solder mask should leave the terminals of the package and the thermal pad area with its five holes exposed. The bottom-side solder mask should cover the five holes of the thermal pad area. This prevents solder from being pulled away from the thermal pad area during the reflow process.
7. Apply solder paste to the exposed thermal pad area and all of the IC terminals.
8. With these preparatory steps in place, the THS6062DGN IC is simply placed in position and run through the solder reflow operation as any standard surface-mount component. This results in a part that is properly installed.

The actual thermal performance achieved with the THS6062DGN in its PowerPAD package depends on the application. In the example above, if the size of the internal ground plane is approximately 3 inches $\times$ 3 inches, then the expected thermal coefficient, θ_{JA}, is about 58.4°C/W. For comparison, the non-PowerPAD version of the THS6062 IC (SOIC) is shown. For a given θ_{JA}, the maximum power dissipation is shown in Figure 48 and is calculated by the following formula:

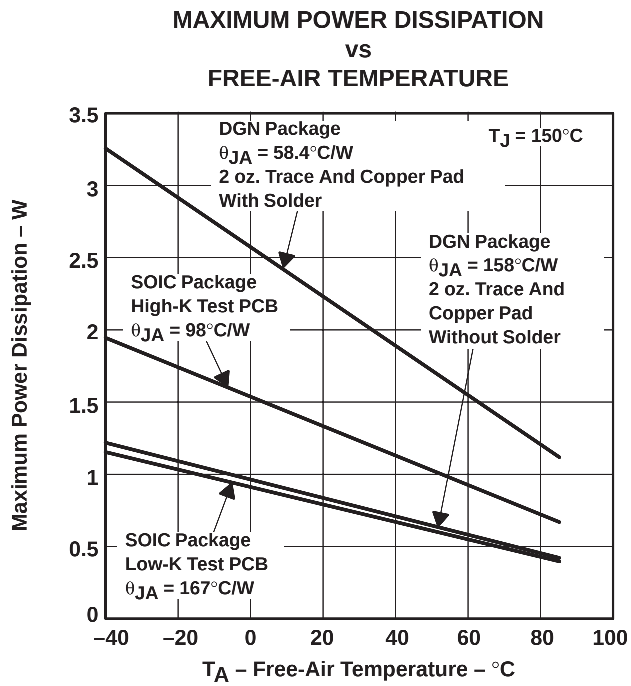
$$P_D = \left(\frac{T_{MAX} - T_A}{\theta_{JA}} \right)$$

Where:

P_D = Maximum power dissipation of THS6062 IC (watts)
T_{MAX} = Absolute maximum junction temperature (150°C)
T_A = Free-ambient air temperature (°C)
θ_{JA} = $\theta_{JC} + \theta_{CA}$
θ_{JC} = Thermal coefficient from junction to case
θ_{CA} = Thermal coefficient from case to ambient air (°C/W)

APPLICATION INFORMATION

general PowerPAD design considerations (continued)



NOTE A: Results are with no air flow and PCB size = 3”× 3”

Figure 48. Maximum Power Dissipation vs Free-Air Temperature

More complete details of the PowerPAD installation process and thermal management techniques can be found in the Texas Instruments Technical Brief, *PowerPAD Thermally Enhanced Package.* This document can be found at the TI web site (www.ti.com) by searching on the key word PowerPAD. The document can also be ordered through your local TI sales office. Refer to literature number SLMA002 when ordering.

The next thing that should be considered is the package constraints. The two sources of heat within an amplifier are quiescent power and output power. The designer should never forget about the quiescent heat generated within the device, especially a multiamplifier device. Because these devices have linear output stages (Class A-B), most of the heat dissipation is at low output voltages with high output currents. Figure 49 and Figure 50 show this effect, along with the quiescent heat, with an ambient air temperature of 50°C. When using V_{CC} = 5 V or ±5 V, there is generally not a heat problem, even with SOIC packages. But, when using V_{CC} = ±15 V, the SOIC package is severely limited in the amount of heat it can dissipate. The other key factor when looking at these graphs is how the devices are mounted on the PCB. The PowerPAD devices are extremely useful for heat dissipation. But the device should always be soldered to a copper plane to fully use the heat dissipation properties of the PowerPAD. The SOIC package, on the other hand, is highly dependent on how it is mounted on the PCB. As more trace and copper area is placed around the device, θ_{JA} decreases and the heat dissipation capability increases. The currents and voltages shown in these graphs are for the total package. Because the THS6062 is a dual amplifier, the sum of the RMS output currents and voltages should be used to choose the proper package.

APPLICATION INFORMATION

general PowerPAD design considerations (continued)

MAXIMUM RMS OUTPUT CURRENT
vs
RMS OUTPUT VOLTAGE DUE TO THERMAL LIMITS

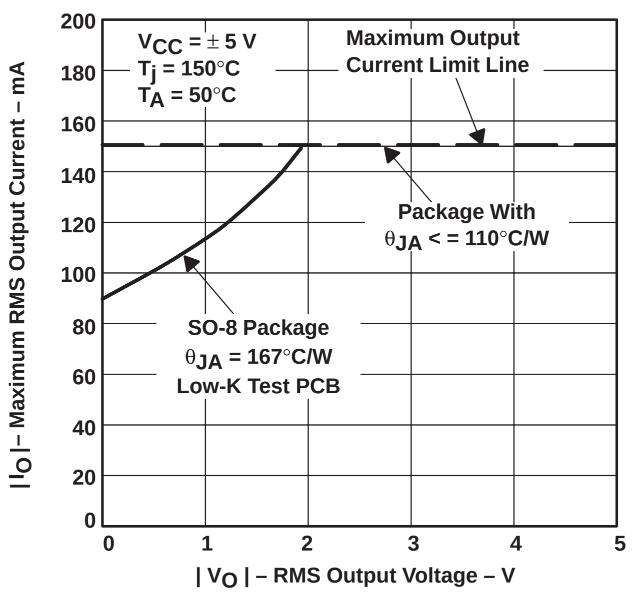


Figure 49

MAXIMUM RMS OUTPUT CURRENT
vs
RMS OUTPUT VOLTAGE DUE TO THERMAL LIMITS

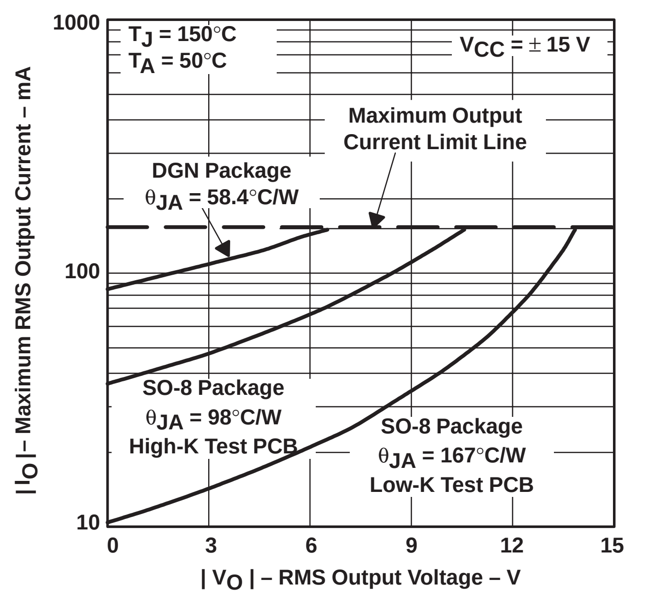


Figure 50

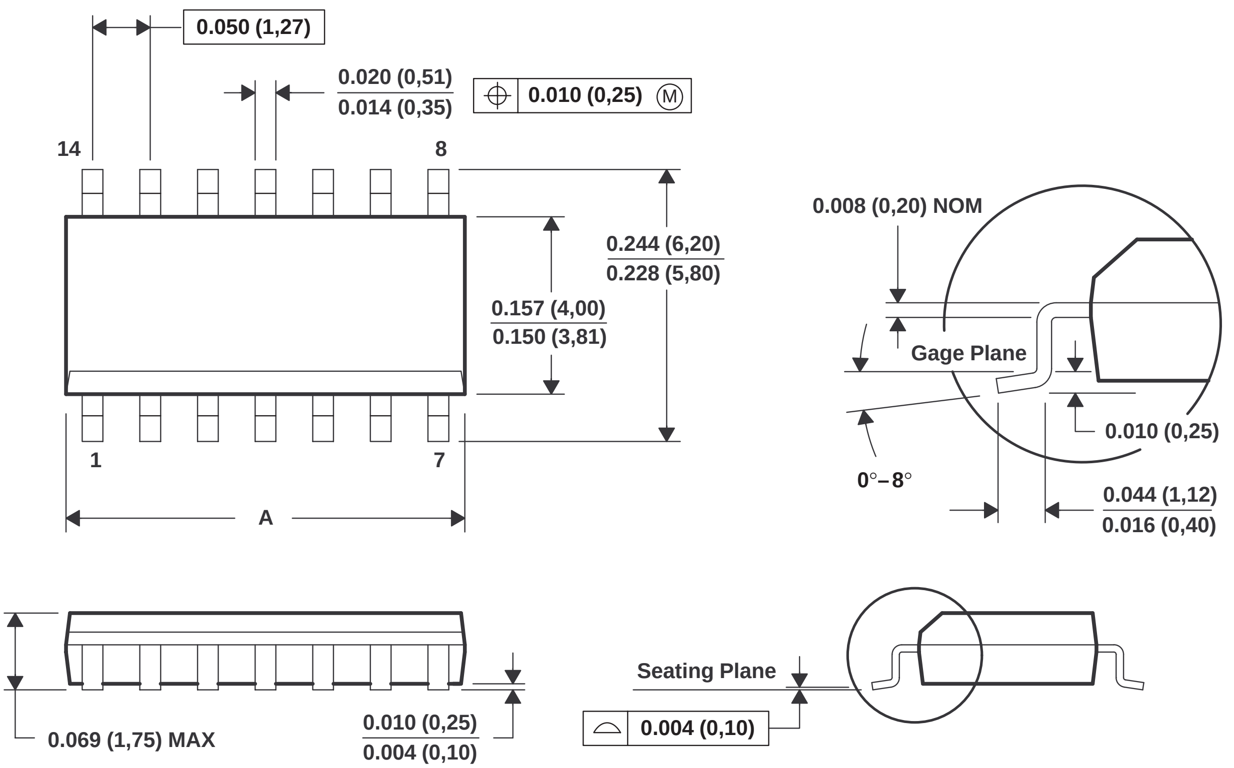
evaluation board

An evaluation board is available for the THS6062 (literature number SLOP221). This board has been configured for very low parasitic capacitance in order to realize the full performance of the amplifier. For more information, refer to the *THS6062 EVM User's Guide* (literature number SLOU036) To order the evaluation board contact your local TI sales office or distributor.

MECHANICAL DATA

D (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PIN SHOWN



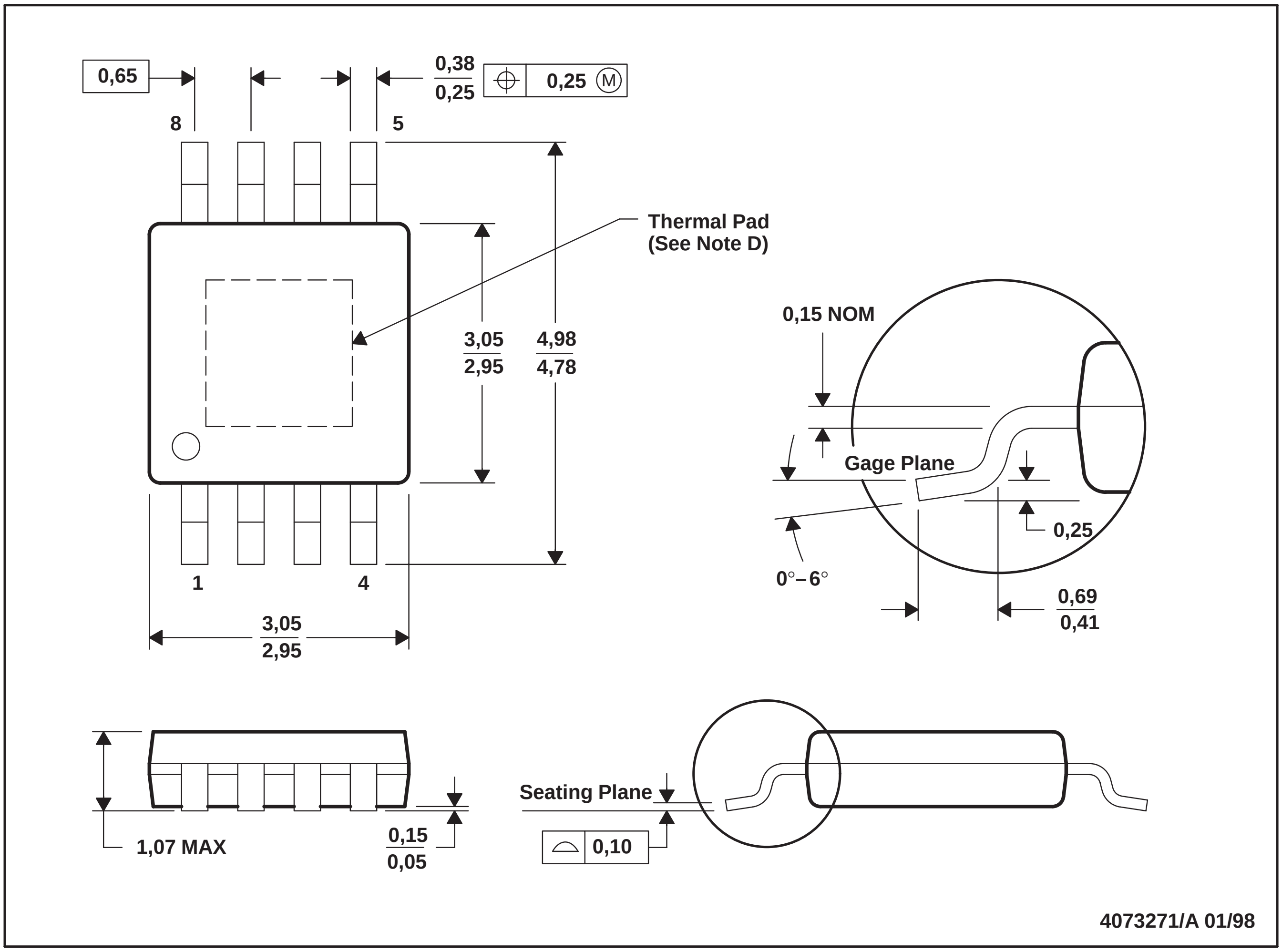
PINS ** / DIM	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

4040047/D 10/96

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-012

MECHANICAL DATA

DGN (S-PDSO-G8) **PowerPAD™ PLASTIC SMALL-OUTLINE PACKAGE**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions include mold flash or protrusions.
D. The package thermal performance may be enhanced by attaching an external heat sink to the thermal pad. This pad is electrically and thermally connected to the backside of the die and possibly selected leads.
E. Falls within JEDEC MO-187

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