3-Channel RGBHV Video Buffer with I²C™ Control, 2:1 Input Mux, Monitor Pass-Through, and Selectable Input Bias Modes

FEATURES

- 3-Video Amplifiers for CVBS, S-Video, EDTV, HDTV $Y'P'_BP'_R$, G'B'R', and R'G'B' Video
- H/V Sync Paths with Adjustable Schmitt Trigger
- 2:1 Input Mux
- I²C Control of All Functions on Each Channel
- Unity-Gain Buffer Path for ADC Buffering:
  - 500-MHz Bandwidth, 1200-V/µs Slew Rate
- Monitor Pass-Through Function:
  - 500-MHz Bandwidth, 1300-V/µs Slew Rate
  - 6-dB Gain with SAG Correction Capable
  - High Output Impedance in Disable State
- Selectable Input Bias Modes:
  - AC-Coupled with Sync-Tip Clamp
  - AC-Coupled with Bias
  - DC-Coupled with Offset Shift
  - DC-Coupled
- +2.7-V to +5-V Single-Supply Operation
- Total Power Consumption: 265 mW at 3.3 V
- Disable Function Reduces Current to 0.1 µA
- Rail-to-Rail Output:
- Output Swings Within 0.1 V of the Rails, Allowing AC- or DC-Output Coupling
- Lead-free, RoHS TQFP Package

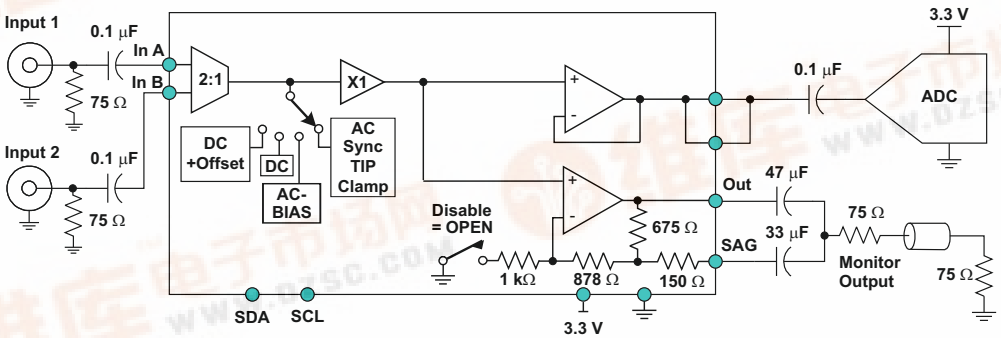
APPLICATIONS

- Projectors
- Professional Video Systems
- LCD/DLP®/LOCS Input Buffering

DESCRIPTION

Fabricated using the revolutionary complementary silicon-germanium (SiGe) BiCom3 process, the THS7347 is a low-power, single-supply 2.7-V to 5-V 3-channel integrated video buffer with horizontal (H) and vertical (V) sync signal paths. It incorporates a 500-MHz bandwidth, 1200-V/µs unity-gain buffer ideal for driving analog-to-digital converters (ADCs) and video decoders. In parallel with the unity-gain buffer, a monitor pass-through path allows for passing the input signal on to other systems. This path has a 6-dB gain, 500-MHz bandwidth, 1300V/µs slew rate, SAG correction capability, and high output impedance while disabled.

Each channel of the THS7347 is individually I²C-configurable for all functions, including controlling the 2:1 input mux. Its rail-to-rail output stage allows for both ac- and dc-coupling applications.



3.3 V Single-Supply Projector Input System with Monitor Pass-Through (1 of 3 R'G'B' Channels Shown)

DESCRIPTION, CONTINUED

As part of the THS7347 flexibility, the device input can be selected for ac- or dc-coupled inputs. The ac-coupled modes include a sync-tip clamp option for CVBS/Y'/G'B'R' with sync or a fixed bias for the C'/P'$_B$/P'$_R$/R'G'B' channels without sync. The dc input options include a dc input or a dc+Offset shift to allow for a full sync dynamic range at the output with 0 V input.

The THS7347 is available in a lead-free, RoHS-compliant TQFP package.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGING/ORDERING INFORMATION(1)

PACKAGED DEVICES	PACKAGE TYPE	TRANSPORT MEDIA, QUANTITY
THS7347IPHP	HTQFP-48 PowerPAD™	Tray, 250
THS7347IPHPR		Tape and reel, 1000

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature range (unless otherwise noted)(1)

			THS7347	UNIT
V_{SS}	Supply voltage, GND to V_A or GND to V_{DD}		5.5	V
V_I	Input voltage		–0.4 to V_A or V_{DD}	V
I_O	Continuous output current		±80	mA
	Continuous power dissipation		See Dissipation Rating Table	
T_J	Maximum junction temperature, any condition(2)		+150	°C
T_J	Maximum junction temperature, continuous operation, long term reliability(3)		+125	°C
T_{stg}	Storage temperature range		–65 to +150	°C
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		300	°C
	ESD ratings	HBM	1500	V
		CDM	1500	V
		MM	100	V

(1) Stresses above those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied Exposure to absolute maximum rated conditions for extended periods may degrade device reliability.
(2) The absolute maximum junction temperature under any condition is limited by the constraints of the silicon process.
(3) The absolute maximum junction temperature for continuous operation is limited by the package constraints. Operation above this temperature may result in reduced reliability and/or lifetime of the device.

DISSIPATION RATINGS

PACKAGE	θ_{JC} (°C/W)	θ_{JA} (°C/W)	POWER RATING(1)(2) (T_J = +125°C)	
			T_A = +25°C	T_A = +85°C
HTQFP-48 with PowerPAD (PHP)	1.2	35	2.85 W	1.14 W

(1) This data was taken with a PowerPAD standard 3-inch by 3-inch, 4-layer printed circuit board (PCB) with internal ground plane connections to the PowerPAD.
(2) Power rating is determined with a junction temperature of +125°C. This temperature is the point where distortion starts to substantially increase and long-term reliability starts to be reduced. Thermal management of the final PCB should strive to keep the junction temperature at or below +125°C for best performance and reliability.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
V_{DD}	Digital supply voltage	2.7		5	V
V_A	Analog supply voltage. Must be equal to or greater than V_{DD}	VDD		5	V
T_A	Ambient temperature	–40		+85	°C

ELECTRICAL CHARACTERISTICS, $V_A = V_{DD} = 3.3$ V

R_L = 150 Ω‖ 5 pF to GND for Monitor Output, 19 kΩ || 8 pF Load to GND for Buffer Output, SAG pin shorted to Monitor Output Pin, unless otherwise noted.

PARAMETER		TEST CONDITIONS	TYP	OVER TEMPERATURE				
			+25°C	+25°C	0°C to +70°C	–40°C to +85°C	UNIT	MIN/MAX/ TYP
AC PERFORMANCE								
Small-signal bandwidth (–3 dB)	Buffer output	V_O = 0.2 V_{PP}	500				MHz	Typ
	Monitor output		450				MHz	Typ
–1 dB Flatness	Buffer output	V_O = 0.2 V_{PP}	425				MHz	Typ
	Monitor output		375				MHz	Typ
Large-signal bandwidth (–3 dB)	Buffer output	V_O = 1 V_{PP}	475				MHz	Typ
	Monitor output	V_O = 2 V_{PP}	240				MHz	Typ
Slew rate	Buffer output	V_O = 1 V_{PP}	1050				V/µs	Typ
	Monitor output	V_O = 2 V_{PP}	1050				V/µs	Typ
Group delay at 100 kHz	Buffer output		1.2				ns	Typ
	Monitor output		1.2				ns	Typ
Differential gain	Buffer output	NTSC/PAL	0.05/0.05				%	Typ
	Monitor output		0.1/0.1				%	Typ
Differential phase	Buffer output	NTSC/PAL	0.1/0.15				degrees	Typ
	Monitor output		0.15/0.2				degrees	Typ
Total harmonic distortion f = 1 MHz	Buffer output	V_O = 1 V_{PP}	–58				dB	Typ
	Monitor output	V_O = 2 V_{PP}	–57				dB	Typ
Signal-to-noise ratio	Buffer output	No weighting, up to 100 MHz	63				dB	Typ
	Monitor output		65				dB	Typ
Channel-to-channel crosstalk	Buffer output	f = 100 MHz	–40				dB	Typ
	Monitor output		–36				dB	Typ
MUX Isolation	Buffer output	f = 100 MHz	64				dB	Typ
	Monitor output		66				dB	Typ
Gain	Buffer output	f = 100 kHz; V_O = 1 V_{PP}	0				dB	Typ
	Monitor output	f = 100 kHz; V_O = 2 V_{PP}	6	5.8/6.25	5.75/6.3	5.75/6.35	dB	Min/Max
Settling time	Buffer output	V_{IN} = 1 V_{PP}; 0.5% Settling	6				ns	Typ
	Monitor output		6				ns	Typ
Output impedance	Buffer output	f = 10 MHz	0.3				Ω	Typ
	Monitor output		0.4				Ω	Typ
DC PERFORMANCE								
Output offset voltage	Buffer output	Bias = dc	15	±80	±85	±85	mV	Max
	Monitor output		20	±120	±125	±125	mV	Max
Average offset voltage drift	Buffer output	Bias = dc				20	µV/°C	Typ
	Monitor output					20	µV/°C	Typ
Bias output voltage	Buffer output	Bias = dc + shift, V_{IN} = 0 V	255	175/335	165/345	160/350	mV	Min/Max
		Bias = ac	1.0	0.85/1.15	0.8/1.2	0.8/1.2	V	Min/Max
	Monitor output	Bias = dc + shift, V_{IN} = 0 V	235	145/325	135/335	130/340	mV	Min/Max
		Bias = ac	1.7	1.55/1.85	1.5/1.9	1.5/1.9	V	Min/Max
Sync tip clamp voltage	Buffer output	Bias = ac STC, clamp voltage	290	200/380	195/385	190/390	mV	Min/Max
	Monitor output		300	200/400	195/405	190/410	mV	Min/Max

ELECTRICAL CHARACTERISTICS, $V_A = V_{DD} = 3.3$ V (continued)

R_L = 150 Ω‖ 5 pF to GND for Monitor Output, 19 kΩ || 8 pF Load to GND for Buffer Output, SAG pin shorted to Monitor Output Pin, unless otherwise noted.

PARAMETER		TEST CONDITIONS	TYP	OVER TEMPERATURE				
			+25°C	+25°C	0°C to +70°C	–40°C to +85°C	UNIT	MIN/MAX/ TYP
DC PERFORMANCE, continued								
Input bias current		Bias = dc; (–) implies I_B out of the pin	–1.3	–3.0	–3.5	–3.5	µA	Max
Average bias current drift		Bias = dc				10	nA/°C	Typ
Sync tip clamp bias current		Bias = ac STC, low bias	2.3	0.9/3.6	0.8/3.8	0.7/3.9	µA	Min/Max
		Bias = ac STC, mid bias	5.8	3.8/8.0	3.7/8.2	3.6/8.3	µA	Min/Max
		Bias = ac STC, high bias	8.1	5.7/10.8	5.6/11.0	5.5/11.1	µA	Min/Max
INPUT CHARACTERISTICS								
Input voltage range		Bias = dc	0 to 2				V	Typ
Input resistance		Bias = ac bias mode	25				kΩ	Typ
		Bias = dc, dc + shift, ac STC	3				MΩ	Typ
Input capacitance			1.5				pF	Typ
OUTPUT CHARACTERISTICS: MONITOR OUTPUT								
High output voltage swing		R_L = 150 Ω to 1.65 V	3.15	2.9	2.8	2.8	V	Min
		R_L = 150 Ω to GND	3.05	2.85	2.75	2.75	V	Min
		R_L = 75 Ω to 1.65 V	3.05				V	Typ
		R_L = 75 Ω to GND	2.9				V	Typ
Low output voltage swing		R_L = 150 Ω to 1.65 V	0.15	0.25	0.28	0.29	V	Max
		R_L = 150 Ω to GND	0.1	0.18	0.21	0.22	V	Max
		R_L = 75 Ω to 1.65 V	0.25				V	Typ
		R_L = 75 Ω to GND	0.08				V	Typ
Output current	Sourcing	R_L = 10 Ω to 1.65 V	80	50	47	45	mA	Min
	Sinking		75	50	47	45	mA	Min
OUTPUT CHARACTERISTICS: BUFFER OUTPUT								
High output voltage swing (Limited by input range and G = 0 dB)		Load = 19 kΩ‖ 8 pF to 1.65 V	2	1.8	1.75	1.75	V	Min
Low Output voltage swing (Limited by input range and G = 0 dB)			0.05	0.12	0.13	0.14	V	Max
Output Current	Sourcing	R_L = 10 Ω to GND	80	50	47	45	mA	Min
	Sinking	R_L = 10 Ω to 1.65 V	75	50	47	45	mA	Min
POWER SUPPLY: ANALOG								
Maximum operating voltage		V_A	3.3	5.5	5.5	5.5	V	Max
Minimum operating voltage		V_A	3.3	2.7	2.7	2.7	V	Min
Maximum quiescent current		V_A, dc + shift mode, V_{IN} = 100 mV	80	100	103	105	mA	Max
Minimum quiescent current		V_A, dc + shift mode, V_{IN} = 100 mV	80	60	57	55	mA	Min
Power supply rejection (+PSRR)		Buffer output	50				dB	Typ
POWER SUPPLY: DIGITAL								
Maximum operating voltage		V_{DD}	3.3	5.5	5.5	5.5	V	Max
Minimum operating voltage		V_{DD}	3.3	2.7	2.7	2.7	V	Min
Maximum quiescent current		V_{DD}, V_{IN} = 0 V	0.65	1.2	1.3	1.4	mA	Max
Minimum quiescent current		V_{DD}, V_{IN} = 0 V	0.65	0.35	0.3	0.25	mA	Min
DISABLE CHARACTERISTICS: ALL CHANNELS DISABLED								
Quiescent current		All channels disabled	0.1				µA	Typ
Turn-on time delay (t_{ON})		Time for I_S to reach 50% of final value after I^2C control is initiated	5				µs	Typ
Turn-on time delay (t_{OFF})			2				µs	Typ

ELECTRICAL CHARACTERISTICS, $V_A = V_{DD} = 3.3$ V (continued)

R_L = 150 Ω‖ 5 pF to GND for Monitor Output, 19 kΩ || 8 pF Load to GND for Buffer Output, SAG pin shorted to Monitor Output Pin, unless otherwise noted.

PARAMETER	TEST CONDITIONS	TYP	OVER TEMPERATURE				
		+25°C	+25°C	0°C to +70°C	–40°C to +85°C	UNIT	MIN/MAX/ TYP
H/V SYNC CHARACTERISTICS: R_{Load} = 1 kΩ To GND(1)							
Schmitt trigger adjust pin voltage	Reference for Schmitt trigger	1.47	1.35/1.6	1.3/1.65	1.27/1.68	V	Min/Max
Schmitt trigger threshold range	Allowable range for Schmitt trigger adjust	0.9 to 2				V	Typ
Schmitt trigger VT+	Positive-going input voltage threshold relative to Schmitt trigger threshold	0.25				V	Typ
Schmitt trigger VT–	Negative-going input voltage threshold relative to Schmitt trigger threshold	–0.3				V	Typ
Schmitt trigger threshold pin input resistance	Input resistance into Control pin	10				kΩ	Typ
H/V Sync input impedance		10				MΩ	Typ
H/V Sync high output voltage	1 kΩ to GND	3.15	3.05	3.0	3.0	V	Min
H/V Sync low output voltage	1 kΩ to GND	0.01	0.05	0.1	0.1	V	Max
H/V Sync source current	10 Ω to GND	50	35	30	30	mA	Min
H/V Sync sink current	10 Ω to 3.3 V	35	25	23	21	mA	Min
H/V Delay	Delay from Input to output	6.5				ns	Typ
H/V to buffer output skew		5				ns	Typ

(1) Schmitt trigger threshold is defined by (VT+ – VT–)/2.

ELECTRICAL CHARACTERISTICS, $V_A = V_{DD} = 5$ V

R_L = 150Ω || 5pF to GND for Monitor Output, 19kΩ || 8pF Load to GND for Buffer Output, SAG pin shorted to Monitor Output Pin, unless otherwise noted.

PARAMETER		TEST CONDITIONS	TYP	OVER TEMPERATURE				
			+25°C	+25°C	0°C to +70°C	–40°C to +85°C	UNIT	MIN/MAX/ TYP
AC PERFORMANCE								
Small-signal bandwidth (–3 dB)	Buffer output	V_O = 0.2 V_{PP}	550				MHz	Typ
	Monitor output		500				MHz	Typ
–1 dB Flatness	Buffer output	V_O = 0.2 V_{PP}	450				MHz	Typ
	Monitor output		400				MHz	Typ
Large-signal bandwidth (–3 dB)	Buffer output	V_O = 1 V_{PP}	525				MHz	Typ
	Monitor output	V_O = 2 V_{PP}	325				MHz	Typ
Slew rate	Buffer output	V_O = 1 V_{PP}	1200				V/µs	Typ
	Monitor output	V_O = 2 V_{PP}	1350				V/µs	Typ
Group delay at 100 kHz	Buffer output		1.15				ns	Typ
	Monitor output		1.15				ns	Typ
Differential gain	Buffer output	NTSC/PAL	0.05/0.05				%	Typ
	Monitor output		0.1/0.1				%	Typ
Differential phase	Buffer output	NTSC/PAL	0.05/0.05				degrees	Typ
	Monitor output		0.05/0.05				degrees	Typ
Total harmonic distortion f = 1 MHz	Buffer output	V_O = 1 V_{PP}	–71				dB	Typ
	Monitor output	V_O = 2 V_{PP}	–67				dB	Typ
Signal-to-noise ratio	Buffer output	No weighting, up to 100 MHz	63				dB	Typ
	Monitor output		65				dB	Typ
Channel-to-channel crosstalk	Buffer output	f = 100 MHz	–40				dB	Typ
	Monitor output		–36				dB	Typ
MUX Isolation	Buffer output	f = 100 MHz	64				dB	Typ
	Monitor output		66				dB	Typ
Gain	Buffer output	f = 100 kHz; V_O = 1 V_{PP}	0				dB	Typ
	Monitor output	f = 100 kHz; V_O = 2 V_{PP}	6	5.8/6.25	5.75/6.3	5.75/6.35	dB	Min/Max
Settling time	Buffer output	V_{IN} = 1 V_{PP}; 0.5% Settling	6				ns	Typ
	Monitor output		6				ns	Typ
Output impedance	Buffer output	f = 10 MHz	0.3				Ω	Typ
	Monitor output		0.4				Ω	Typ
DC PERFORMANCE								
Output offset voltage	Buffer output	Bias = dc	15	±80	±85	±85	mV	Max
	Monitor output		20	±120	±125	±125	mV	Max
Average offset voltage drift	Buffer output	Bias = dc				20	µV/°C	Typ
	Monitor output					20	µV/°C	Typ
Bias output voltage	Buffer output	Bias = dc + shift, V_{IN} = 0 V	265	185/345	175/355	170/360	mV	Min/Max
		Bias = ac	1.5	1.3/1.65	1.25/1.7	1.25/1.7	V	Min/Max
	Monitor output	Bias = dc + shift, V_{IN} = 0 V	235	145/325	135/335	130/340	mV	Min/Max
		Bias = ac	2.65	2.5/2.8	2.45/2.85	2.45/2.85	V	Min/Max
Sync tip clamp voltage	Buffer output	Bias = ac STC, clamp voltage	295	205/385	200/390	195/395	mV	Min/Max
	Monitor output		300	200/400	195/405	190/410	mV	Min/Max
Input bias current		Bias = dc; (–) implies I_B out of the pin	–1.4	–3.0	–3.5	–3.5	µA	Max
Average bias current drift		Bias = dc				10	nA/°C	Typ
Sync tip clamp bias current		Bias = ac STC, low bias	2.4	0.9/3.9	0.8/4.0	0.7/4.1	µA	Min/Max
		Bias = ac STC, mid bias	6.2	3.9/8.4	3.8/8.6	3.7/8.7	µA	Min/Max
		Bias = ac STC, high bias	8.6	6/11.2	5.8/11.4	5.7/11.5	µA	Min/Max

ELECTRICAL CHARACTERISTICS, $V_A = V_{DD} = 5$ V (continued)

R_L = 150Ω || 5pF to GND for Monitor Output, 19kΩ || 8pF Load to GND for Buffer Output, SAG pin shorted to Monitor Output Pin, unless otherwise noted.

PARAMETER		TEST CONDITIONS	TYP	OVER TEMPERATURE				
			+25°C	+25°C	0°C to +70°C	–40°C to +85°C	UNIT	MIN/MAX/ TYP
INPUT CHARACTERISTICS								
Input voltage range		Bias = dc	0 to 3.4				V	Typ
Input resistance		Bias = ac bias mode	25				kΩ	Typ
		Bias = dc, dc + shift, ac STC	3				MΩ	Typ
Input capacitance			1.5				pF	Typ
OUTPUT CHARACTERISTICS: MONITOR OUTPUT								
High output voltage swing		R_L = 150 Ω to 2.5 V	4.8	4.65	4.6	4.6	V	Min
		R_L = 150 Ω to GND	4.7	4.55	4.5	4.5	V	Min
		R_L = 75 Ω to 2.5 V	4.7				V	Typ
		R_L = 75 Ω to GND	4.6				V	Typ
Low output voltage swing		R_L = 150 Ω to 2.5 V	0.2	0.25	0.28	0.30	V	Max
		R_L = 150 Ω to GND	0.1	0.19	0.23	0.24	V	Max
		R_L = 75 Ω to 2.5 V	0.24				V	Typ
		R_L = 75 Ω to GND	0.085				V	Typ
Output current	Sourcing	R_L = 10 Ω to 2.5 V	110	85	80	75	mA	Min
	Sinking		110	85	80	75	mA	Min
OUTPUT CHARACTERISTICS: BUFFER OUTPUT								
High output voltage swing (Limited by input range and G = 0 dB)		Load = 19 kΩ‖ 8 pF to 2.5 V	3.4	3.1	3.0	3.0	V	Min
Low output voltage swing (Limited by input range and G = 0 dB)			0.05	0.12	0.13	0.14	V	Max
Output current	Sourcing	R_L = 10 Ω to GND	110	85	80	75	mA	Min
	Sinking	R_L = 10 Ω to 2.5 V	110	85	80	75	mA	Min
POWER SUPPLY: ANALOG								
Maximum operating voltage		V_A	5.0	5.5	5.5	5.5	V	Max
Minimum operating voltage		V_A	5.0	2.7	2.7	2.7	V	Min
Maximum quiescent current		V_A, dc + shift mode, V_{IN} = 100 mV	90	112	115	117	mA	Max
Minimum quiescent current		V_A, dc + shift mode, V_{IN} = 100 mV	90	68	65	63	mA	Min
Power supply rejection (+PSRR)		Buffer Output	46				dB	Typ
POWER SUPPLY: DIGITAL								
Maximum operating voltage		V_{DD}	5.0	5.5	5.5	5.5	V	Max
Minimum operating voltage		V_{DD}	5.0	2.7	2.7	2.7	V	Min
Maximum quiescent current		V_{DD}, V_{IN} = 0 V	1	2	3	3	mA	Max
Minimum quiescent current		V_{DD}, V_{IN} = 0 V	1	0.5	0.4	0.4	mA	Min
DISABLE CHARACTERISTICS: ALL CHANNELS DISABLED								
Quiescent current		All channels disabled	1				µA	Typ
Turn-on time delay (t_{ON})		Time for I_S to reach 50% of final value after I^2C control is initiated	5				µs	Typ
Turn-on time delay (t_{OFF})			2				µs	Typ

ELECTRICAL CHARACTERISTICS, $V_A = V_{DD} = 5$ V (continued)

R_L = 150Ω || 5pF to GND for Monitor Output, 19kΩ || 8pF Load to GND for Buffer Output, SAG pin shorted to Monitor Output Pin, unless otherwise noted.

PARAMETER	TEST CONDITIONS	TYP	OVER TEMPERATURE				
		+25°C	+25°C	0°C to +70°C	–40°C to +85°C	UNIT	MIN/MAX/ TYP
H/V SYNC CHARACTERISTICS: R_{Load} = 1 kΩ To GND(1)							
Schmitt trigger adjust pin voltage	Reference for Schmitt trigger	1.54	1.43/1.65	1.38/1.7	1.35/1.73	V	Min/Max
Schmitt trigger threshold range	Allowable range for Schmitt trigger adjust	0.9 to 2				V	Typ
Schmitt trigger VT+	Positive-going input voltage threshold relative to Schmitt trigger threshold	0.25				V	Typ
Schmitt trigger VT–	Negative-going input voltage threshold relative to Schmitt trigger threshold	–0.3				V	Typ
Schmitt trigger threshold pin input resistance	Input resistance into Control pin	10				kΩ	Typ
H/V Sync input impedance		10				MΩ	Typ
H/V Sync high output voltage	1 kΩ to GND	4.8	4.7	4.6	4.6	V	Min
H/V Sync low output voltage	1 kΩ to GND	0.01	0.05	0.1	0.1	V	Max
H/V Sync source current	10 Ω to GND	90	60	55	55	mA	Min
H/V Sync sink current	10 Ω to 5 V	50	30	27	25	mA	Min
H/V Delay	Delay from input to output	6.5				ns	Typ
H/V to buffer output skew		5				ns	Typ

(1) Schmitt trigger threshold is defined by (VT+ – VT–)/2.

TIMING REQUIREMENTS FOR I²C INTERFACE(1)(2)

At V_{DD} = 2.7 V to 5 V.

PARAMETER		STANDARD MODE		FAST MODE		UNIT
		MIN	MAX	MIN	MAX	
f_{SCL}	Clock frequency, SCL	0	100	0	400	kHz
$t_{w(H)}$	Pulse duration, SCL high	4		0.6		µs
$t_{w(L)}$	Pulse duration, SCL low	4.7		1.3		µs
t_r	Rise time, SCL and SDA		1000		300	ns
t_f	Fall time, SCL and SDA		300		300	ns
$t_{su(1)}$	Setup time, SDA to SCL	250		100		ns
$t_{h(1)}$	Hold time, SCL to SDA	0		0		ns
$t_{(buf)}$	Bus free time between stop and start conditions	4.7		1.3		µs
$t_{su(2)}$	Setup time, SCL to start condition	4.7		0.6		µs
$t_{h(2)}$	Hold time, start condition to SCL	4		0.6		µs
$t_{su(3)}$	Setup time, SCL to stop condition	4		0.6		µs
C_b	Capacitive load for each bus line		400		400	pF

(1) The THS7347 I²C address = 01011(A1)(A0)(R/$\overline{W}$). See the *Applications Information* section for more information.
(2) The THS7347 was designed to comply with version 2.1 of the I²C specification.

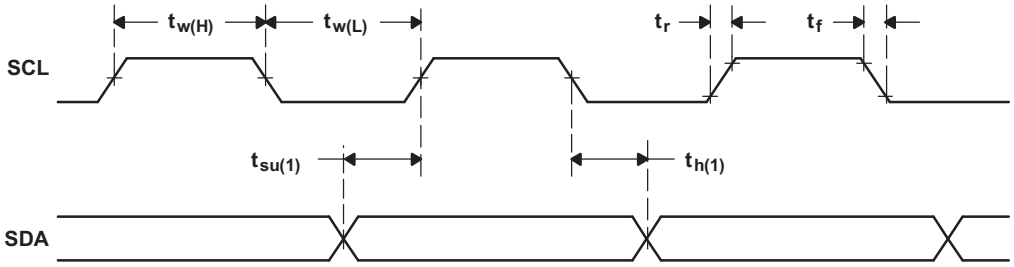


Figure 1. SCL and SDA Timing

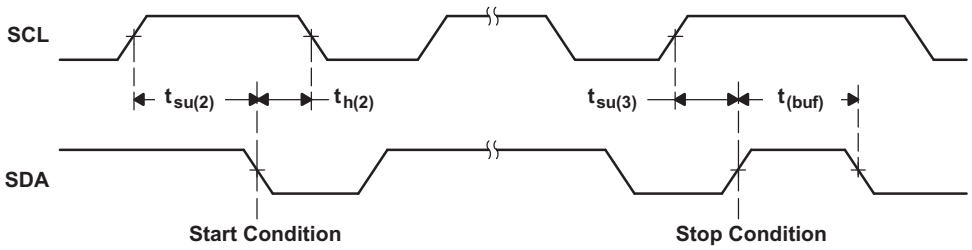
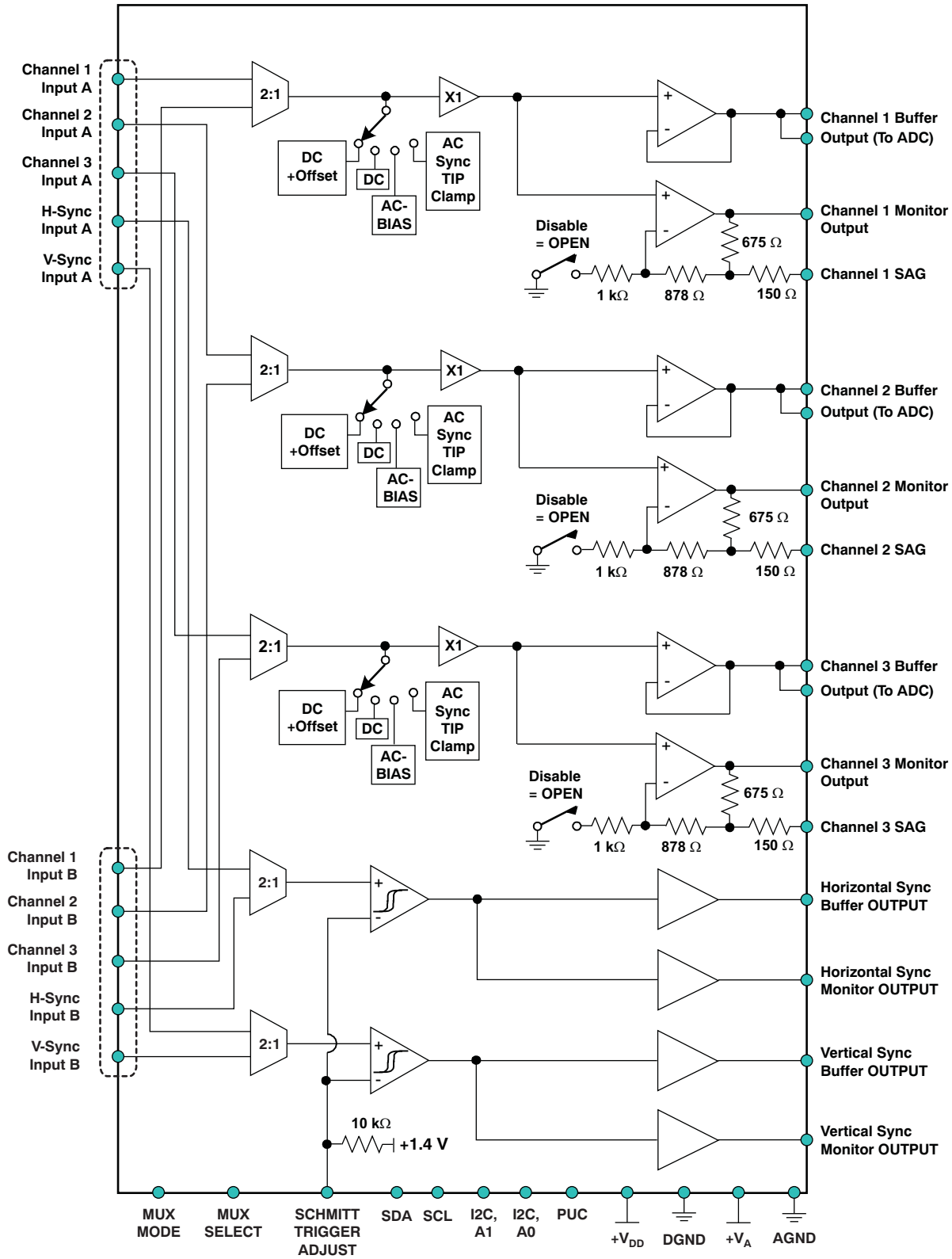


Figure 2. Start and Stop Conditions

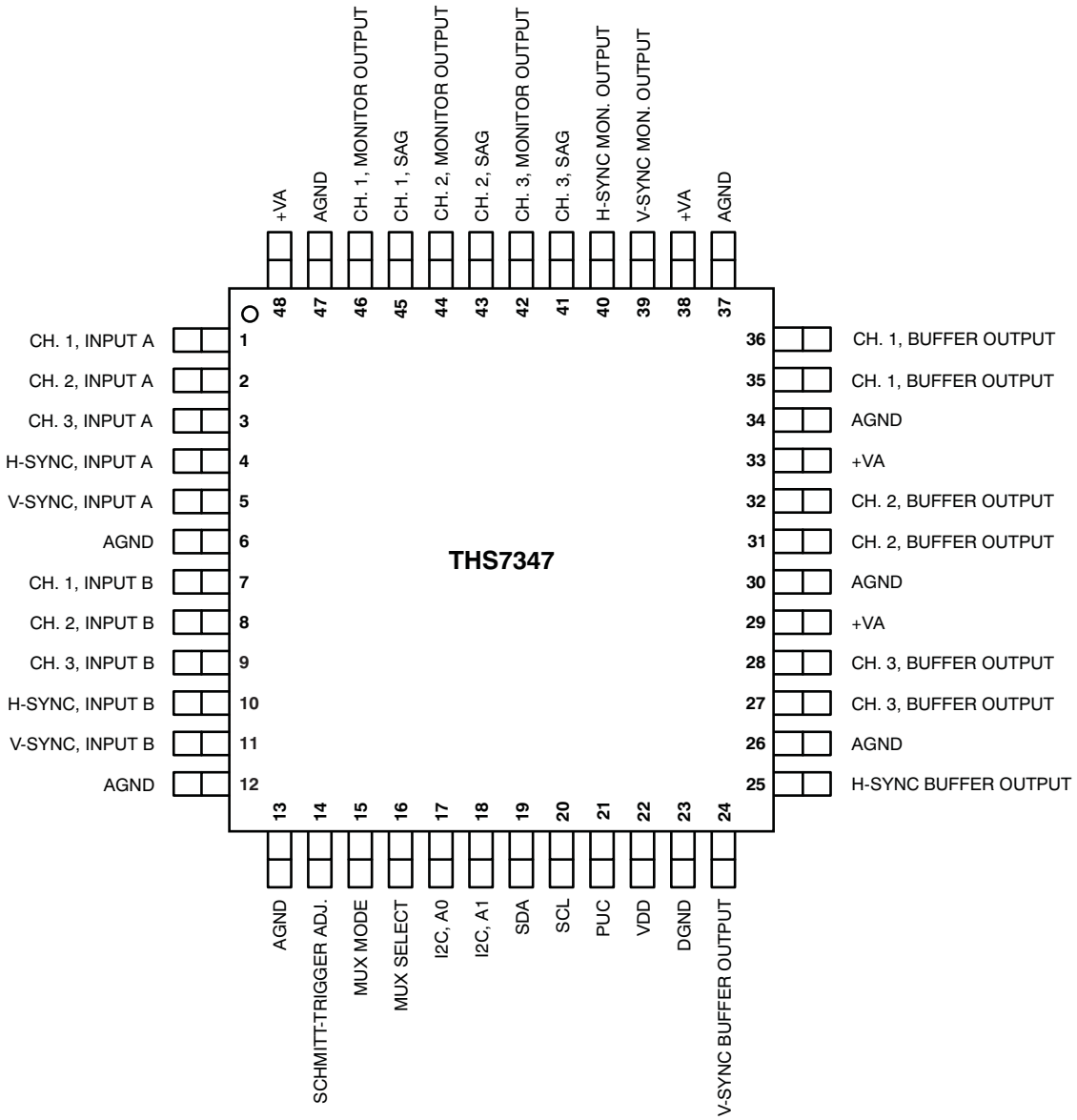
FUNCTIONAL BLOCK DIAGRAM



NOTE: The I²C address of the THS7347 is 01011(A1)(A0)(R/$\overline{W}$).

PIN CONFIGURATION

THS7347IPHP
HTQFP-48 (PHP)
(Top View)



PIN CONFIGURATION (continued)

TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
CH. 1, INPUT A	1	I	Video Input Channel 1, Input A
CH. 2, INPUT A	2	I	Video Input Channel 2, Input A
CH. 3, INPUT A	3	I	Video Input Channel 3, Input A
H-SYNC, INPUT A	4	I	Horizontal Sync, Input A
V-SYNC, INPUT A	5	I	Vertical Sync, Input A
CH. 1, INPUT B	7	I	Video Input Channel 1, Input B
CH. 2, INPUT B	8	I	Video Input Channel 2, Input B
CH. 3, INPUT B	9	I	Video Input Channel 3, Input B
H-SYNC, INPUT B	10	I	Horizontal Sync, Input B
V-SYNC, INPUT B	11	I	Vertical Sync, Input B
I^2C, A1	17	I	I^2C Slave Address Control Bit A1. Connect to V_{DD} for a logic 1 preset value or GND for a logic 0 preset value.
I^2C, A0	18	I	I^2C Slave Address Control Bit A0. Connect to V_{DD} for a logic 1 preset value or GND for a logic 0 preset value.
SDA	19	I/O	Serial data line of the I^2C bus. Pull-up resistor should have a minimum value = 2 kΩ and a maximum value = 19 kΩ. Pull up to V_{DD}.
SCL	20	I	I^2C bus clock line. Pull-up resistor should have a minimum value = 2 kΩ and a maximum value = 19 -kΩ. Pull up to V_{DD}.
PUC	21	I	Power-Up Condition. Connect to GND for all channels disabled upon power-up. Connect to V_{DD} (logic high) to set buffer outputs to OFF and monitor outputs ON with ac-bias configuration on Channels 1 to 3 and both H-Sync/V-Sync enabled.
MUX MODE	15	I	Sets the MUX configuration control. Connect to logic low for MUX Select (pin 16) control of the MUX. Connect to logic high for I^2C control of the MUX.
MUX Select	16	I	Controls the MUX selection when MUX MODE (pin 15) is set to logic low. Connect to logic low for MUX selector set to Input A. Connect to logic high for MUX selector set to Input B.
CH. 1, BUFFER OUTPUT	35, 36	O	Output Channel 1 from either CH. 1, INPUT A or CH. 1, INPUT B. Connect to ADC/Scalar/Decoder. Both pins should be connected together on the PCB.
CH. 2, BUFFER OUTPUT	31, 32	O	Output Channel 2 from either CH. 2, INPUT A or CH. 2, INPUT B. Connect to ADC/Scalar/Decoder. Both pins should be connected together on the PCB.
CH. 3, BUFFER OUTPUT	27, 28	O	Output Channel 3 from either CH. 3, INPUT A or CH. 3, INPUT B. Connect to ADC/Scalar/Decoder. Both pins should be connected together on the PCB.
H-SYNC BUFFER OUTPUT	25	O	Horizontal Sync Buffer Output. Connect to ADC/Scalar H-sync input.
V-SYNC BUFFER OUTPUT	24	O	Vertical Sync Buffer Output. Connect to ADC/Scalar V-sync input.
CH. 1, SAG	45	O	Video Monitor Pass-Through Output Channel 1 SAG Correction pin. If SAG is not used, connect Directly to CH. 1, OUTPUT pin 46.
CH. 1, OUTPUT	46	O	Video Monitor Pass-Through Output Channel 1 from either CH. 1, INPUT A or CH. 1, INPUT B.
CH. 2, SAG	43	O	Video Monitor Pass-Through Output Channel 2 SAG Correction pin. If SAG is not used, connect Directly to CH. 2, OUTPUT pin 44.
CH. 2, OUTPUT	44	O	Video Monitor Pass-Through Output Channel 2 from either CH. 2, INPUT A or CH. 2, INPUT B.
CH. 3, SAG	41	O	Video Monitor Pass-Through Output Channel 3 SAG Correction pin. If SAG is not used, connect Directly to CH. 3, OUTPUT pin 42.
CH. 3, OUTPUT	42	O	Video Monitor Pass-Through Output Channel 3 from either CH. 3, INPUT A or CH. 3, INPUT B.
H-SYNC MONITOR OUTPUT	40	O	Horizontal Sync Monitor Pass-Through Output.
V-SYNC MONITOR OUTPUT	39	O	Vertical Sync Monitor Pass-Through Output.
AGND	6, 12, 13, 26, 30, 34, 37, 47	I	Ground Reference pin for analog signals. Internally, these pins connect to DGND, although it is recommended to have the AGND and DGND connected to the proper signals for best results.
+VA	29, 33, 38, 48	I	Analog Positive Power Supply Input pins. Connect to 2.7 V to 5 V. Must be equal to or greater than VDD.
VDD	22	I	Digital Positive Supply pin for I^2C circuitry and H-Sync/V-Sync outputs. Connect to 2.7 V to 5 V.
DGND	23	I	Digital GND pin for HV circuitry and I^2C circuitry.
Schmitt Trigger Adjust	14	I	Defaults to 1.45 V (TTL compatible). Connect to external voltage reference to adjust H-Sync/V-Sync input thresholds from 0.9 V to 2 V range.

APPLICATIONS INFORMATION

The THS7347 is targeted for RGB+HV video buffer applications. Although it can be used for numerous other applications, the needs and requirements of the video signal were the most important design parameters of the THS7347. Built on the revolutionary complementary silicon-germanium (SiGe) BiCom3 process, the THS7347 incorporates many features not typically found in integrated video parts while consuming very low power. Each channel configuration is completely independent of the other channels. This architecture allows for any configuration for each channel to be dictated by the end user, rather than the part dictating what the configuration must be—resulting in a highly flexible system.

The THS7347 has the following features:

- I^2C interface for easy interfacing to the system.
- Single-supply 2.7-V to 5-V operation with low quiescent current of 80 mA at 3.3 V.
- 2:1 input mux.
- Input configuration accepts dc, dc + shift, ac bias, or ac sync-tip clamp selection.
- 500-MHz unity-gain buffer amplifier to drive ADC/Scalar/Decoder.
- Monitor Pass-Through path has an internal fixed gain of 2 V/V (+6 dB) amplifier that can drive two video lines per channel with dc coupling, traditional ac coupling, or SAG-corrected ac coupling.
- While disabled, the Monitor Pass-Through path has a very high output impedance (> 500 kΩ || 8 pF)
- Power-Up Control (PUC) allows the THS7347 to be fully disabled or have the Monitor Pass-Through function (with ac-bias mode on all channels) enabled upon initial device power-up.
- Mux is controlled by either I^2C or a general-purpose input/output (GPIO) pin, based on the MUX Mode pin logic.
- H-Sync and V-Sync paths have an externally-adjustable Schmitt trigger threshold
- Disable mode reduces quiescent current to as low as 0.1-µA.

OPERATING VOLTAGE

The THS7347 is designed to operate from 2.7 V to 5 V over a -40°C to +85°C temperature range. The impact on performance over the entire temperature range is negligible because of the implementation of thin film resistors and high-quality, low temperature coefficient capacitors.

A 0.1-µF to 0.01-µF capacitor should be placed as close as possible to the power-supply pins. Failure to do so may result in the THS7347 outputs ringing or oscillating. Additionally, a large capacitor, such as 100 µF, should be placed on the power-supply line to minimize issues with 50-Hz/60-Hz line frequencies.

INPUT VOLTAGE

The THS7347 input range allows for an input signal range from ground to approximately (V_S+ – 1.6 V). However, because of the internal fixed gain of 2 V/V (+6 dB), the output is generally the limiting factor for the allowable linear input range. For example, with a 5-V supply, the linear input range is from GND to 3.4 V. As a result of the gain, the linear output range limits the allowable linear input range from GND to 2.5 V at most.

APPLICATIONS INFORMATION (continued)

INPUT OVERVOLTAGE PROTECTION

The THS7347 is built using a very high-speed complementary bipolar and CMOS process. The internal junction breakdown voltages are relatively low for these very small geometry devices. These breakdowns are reflected in the Absolute Maximum Ratings table. All input and output device pins are protected with internal ESD protection diodes to the power supplies, as shown in Figure 3.

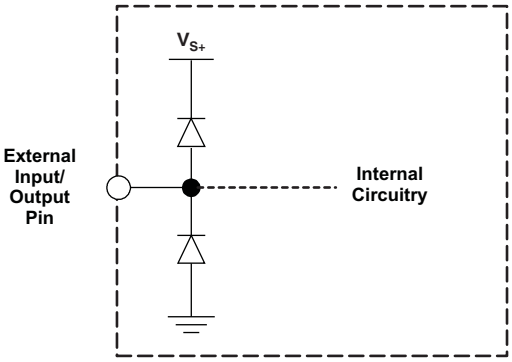


Figure 3. Internal ESD Protection

These diodes provide moderate protection to input overdrive voltages above and below the supplies. The protection diodes can typically support 30 mA of continuous current when overdriven.

TYPICAL CONFIGURATION

A typical application circuit usng the THS7347 as an ac-coupled input video buffer is shown in Figure 4. It shows the THS7347 driving a video ADC (such as the TVP7000) with 0-dB gain and also driving an output line with 6-dB gain. The Horizontal and Vertical Sync signals are also driven to the ADC and the Monitor Output separately. Although the computer resolution R'G'B'HV signals are shown, these channels can easily be the high-definition video (HD), enhanced-definition (ED), or standard-definition (SD) $Y'P'_BP'_R$ (sometimes labeled Y'U'V' or incorrectly labeled $Y'C'_BC'_R$) channels. These channels could also be S-Video Y'/C' channels and the composite video baseband signal (CVBS). Note that the R'G'B' channels could be professional/broadcast G'B'R' signals or other R'G'B' variations based on the placement of the sync signals that are commonly called R'G'sB' (sync on Green) or R'sG'sB's (sync on all signals).

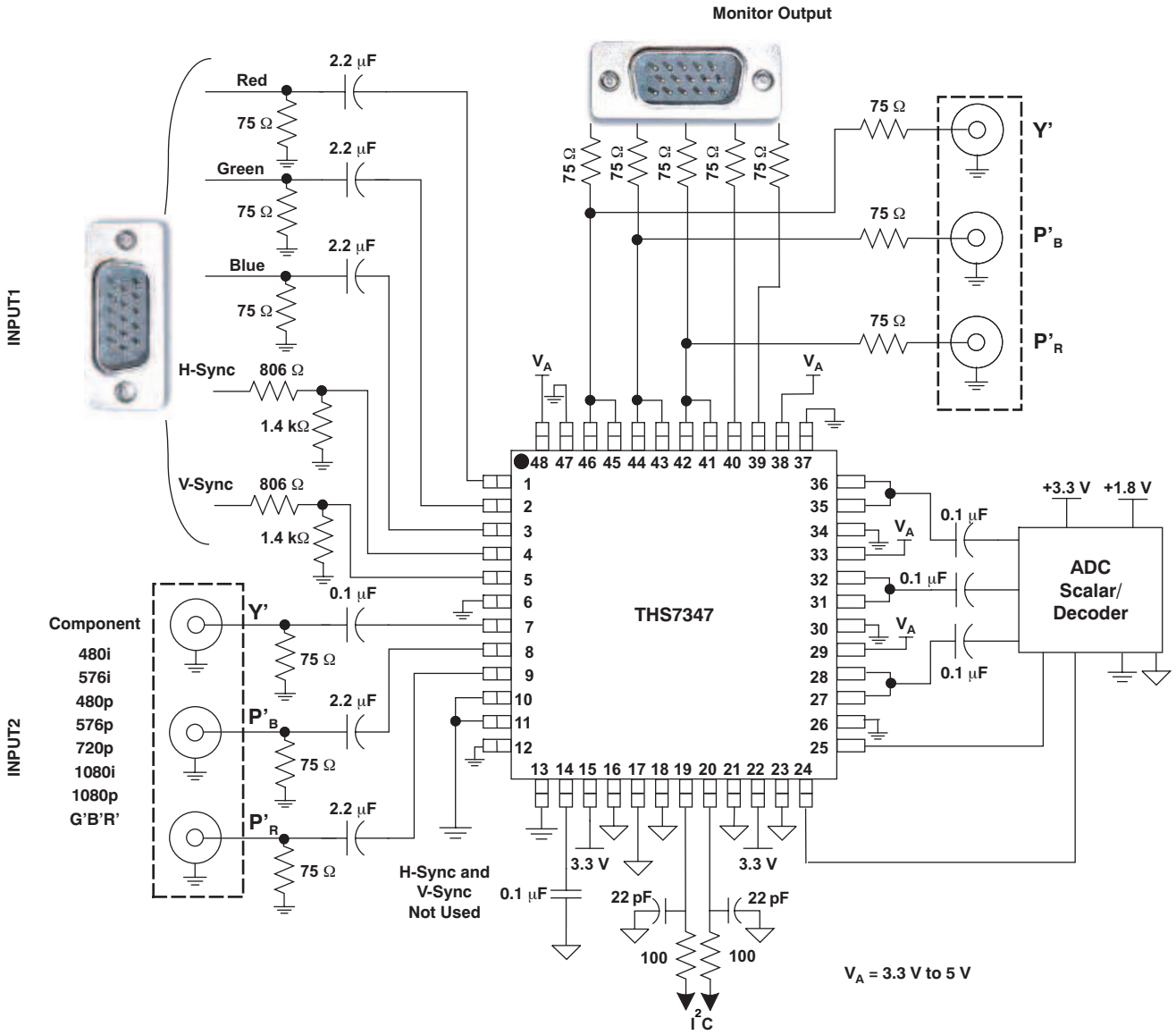
The second set of inputs (B-Channels) shown are connected to another set of inputs. Again, these inputs can be either HD, ED, SD, or R'G'B'/G'B'R' video signals. The THS7347 flexibility allows for virtually any input signal to be driven into the THS7347 regardless of the other set of inputs. Simple control of the I^2C configures the THS7347 for any conceivable combination. For example, the THS7347 can be configured to have Channel 1 Input connected to input A while Channel 2 and Channel 3 are connected to input B. See the multiple application notes sections explaining the I^2C interface later in this document for details on configuring these options.

Note that the Y' term is used for the luma channels throughout this document, rather than the more common luminance (Y) term. The reason for this usage is to account for the true definition of luminance as stipulated by the CIE (International Commission on Illumination). Video departs from true luminance because a nonlinear term, gamma, is added to the true RGB signals to form R'G'B' signals. These R'G'B' signals are then utilized to mathematically create luma (Y'). Therefore, true luminance (Y) is not maintained, and thus the difference in terminology arises.

This rationale is also utilized for the chroma (C') term. Chroma is derived from the nonlinear R'G'B' terms and therefore it is also nonlinear. True chominance (C) is derived from linear RGB, and thus the difference between chroma (C') and chrominance (C) exists. The color difference signals (P'_B/ P'_R/U'/V') are also referenced this way to denote the nonlinear (gamma-corrected) signals.

APPLICATIONS INFORMATION (continued)

R'G'B' (commonly labeled RGB) is also called G'B'R' (again commonly labeled as GBR) in professional video systems. The SMPTE component standard stipulates that the luma information is placed on the first channel, the blue color difference is placed on the second channel, and the red color difference signal is placed on the third channel. This approach is consistent with the $Y'P'_BP'_R$ nomenclature. Because the luma channel (Y') carries the sync information and the green channel (G') also carries the sync information, it makes logical sense that G' be placed first in the system. Since the blue color difference channel (P'_B) is next and the red color difference channel (P'_R) is last, then it also makes logical sense to place the B' signal on the second channel and the R' signal on the third channel, respectively. Thus, hardware compatibility is better achieved when using G'B'R' rather than R'G'B'. Note that for many G'B'R' systems, sync is embedded on all three channels; this configuration may not always be the case for all systems.



(1) Inputs and/or outputs can be ac- or dc-coupled if desired.

(2) H-Sync and V-Sync input resistance as shown above = 2.2kΩ, but may be changed to any desired resistance.

(3) If the Monitor or Buffer PCB trace is >25 mm, it is recommended to place at least a 10-Ω resistor in series with each signal to reduce PCB parasitic issues

Figure 4. Typical R'G'B'HV and $Y'P'_BP'_R$ AC-Coupled Inputs and DC-Coupled Output Configuration

APPLICATIONS INFORMATION (continued)

I²C INTERFACE NOTES

The I²C interface is used to access the internal registers of the THS7347. I²C is a two-wire serial interface developed by Philips Semiconductor (see the I2C Bus Specification, Version 2.1, January 2000). The THS7347 was designed in compliance with version 2.1 specifications. The bus consists of a data line (SDA) and a clock line (SCL) with pull-up structures. When the bus is idle, both SDA and SCL lines are pulled high. All the I²C-compatible devices connect to the I²C bus through open-drain I/O pins, SDA and SCL. A *master* device, usually a microcontroller or a digital signal processor, controls the bus. The master is responsible for generating the SCL signal and device addresses. The master also generates specific conditions that indicate the START and STOP of data transfer. A *slave* device receives and/or transmits data on the bus under control of the master device. The THS7347 works as a slave and supports the standard mode transfer (100 kbps) and fast mode transfer (400 kbps) as defined in the I²C Bus Specification. The THS7347 has been tested to be fully functional with the high-speed mode (3.4 Mbps) but it is not specified at this time.

Figure 5 shows the basic I²C start and stop access cycles.

The basic access cycle consists of the following:

- A start condition
- A slave address cycle
- Any number of data cycles
- A stop condition

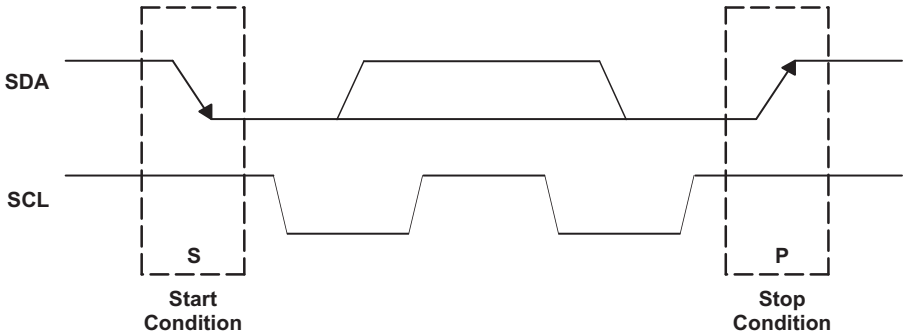


Figure 5. I²C Start and Stop Conditions

GENERAL I²C PROTOCOL

- The *master* initiates data transfer by generating a *start condition*. The *start condition* exists when a high-to-low transition occurs on the SDA line while SCL is high, as shown in Figure 5. All I²C-compatible devices should recognize a *start condition*.
- The master then generates the SCL pulses and transmits the 7-bit address and the *read/write direction bit* R/$\overline{W}$ on the SDA line. During all transmissions, the master ensures that data is *valid*. A *valid data* condition requires the SDA line to be stable during the entire high period of the clock pulse (see Figure 6). All devices recognize the address sent by the master and compare it to the respective internal fixed addresses. Only the slave device with a matching address generates an *acknowledge* (see Figure 7) by pulling the SDA line low during the entire high period of the ninth SCL cycle. On detecting this acknowledge, the master knows that a communication link with a slave has been established.

APPLICATIONS INFORMATION (continued)

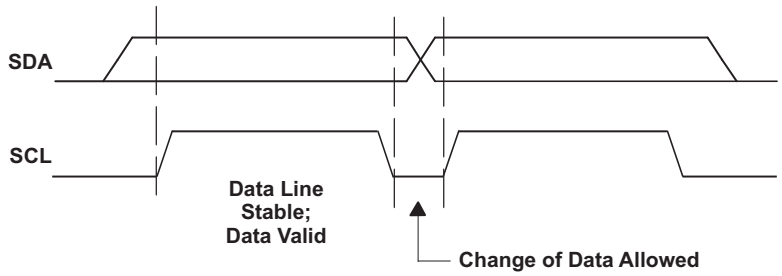


Figure 6. I²C Bit Transfer

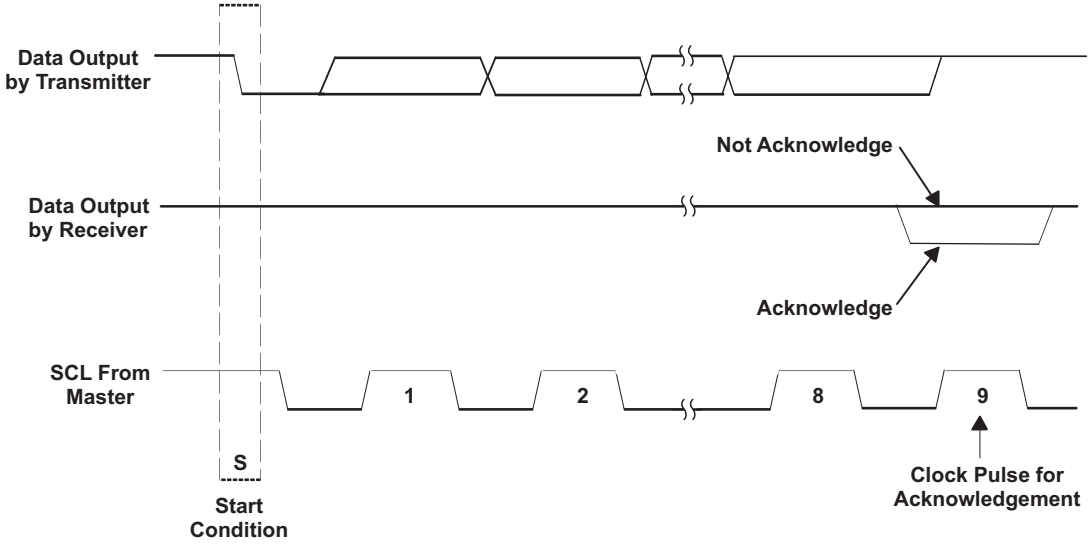


Figure 7. I²C Acknowledge

- The master generates further SCL cycles to either *transmit* data to the slave (R/$\overline{W}$ bit 1) or *receive* data from the slave (R/$\overline{W}$ bit 0). In either case, the *receiver* must acknowledge the data sent by the *transmitter*. So, an acknowledge signal can either be generated by the master or by the slave, depending on which one is the receiver. The 9-bit valid data sequences consisting of 8-bit data and 1-bit acknowledge can continue as long as necessary (see Figure 8).

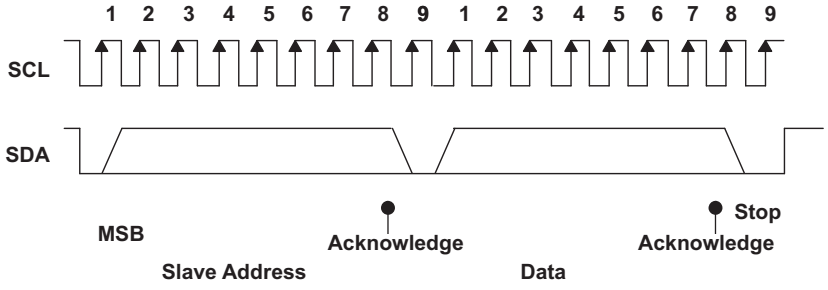


Figure 8. I²C Address and Data Cycles

- To signal the end of the data transfer, the master generates a *stop condition* by pulling the SDA line from low to high while the SCL line is high (see Figure 5). This transaction releases the bus and stops the communication link with the addressed slave. All I²C-compatible devices must recognize the *stop condition*. Upon the receipt of a stop condition, all devices know that the bus is released, and they wait for a *start condition* followed by a matching address.

APPLICATIONS INFORMATION (continued)

During a write cycle, the transmitting device must not drive the SDA signal line during the acknowledge cycle, so that the receiving device may drive the SDA signal low. After each byte transfer following the address byte, the receiving device pulls the SDA line low for one SCL clock cycle. A stop condition is initiated by the transmitting device after the last byte is transferred. Figure 9 and Figure 10 show an example of a write cycle. Note that the THS7347 does not allow multiple write transfers to occur. See the example, **Writing to the THS7347**, in Section 12 for more information.

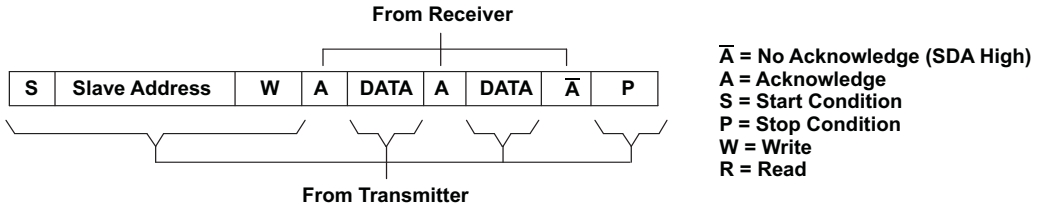


Figure 9. I²C Write Cycle

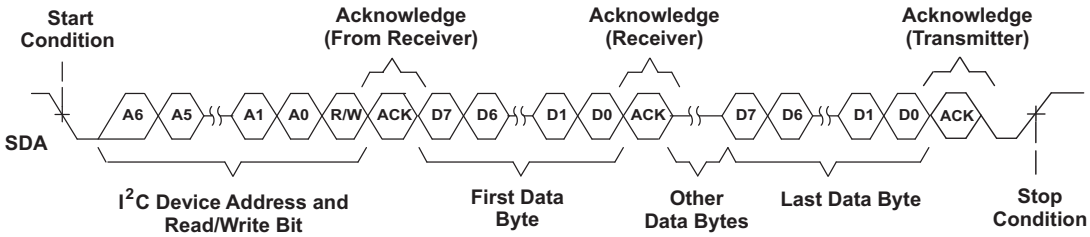


Figure 10. Multiple Byte Write Transfer

During a read cycle, the slave receiver acknowledges the initial address byte if it decodes the address as its address. Following this initial acknowledge by the slave, the master device becomes a receiver and acknowledges data bytes sent by the slave. When the master has received all of the requested data bytes from the slave, the not acknowledge ($\overline{A}$) condition is initiated by the master by keeping the SDA signal high just before it asserts the stop (P) condition. This sequence terminates a read cycle, as shown in Figure 11 and Figure 12. Note that the THS7347 does not allow multiple read transfers to occur. See the example, **Reading from the THS7347**, in Section 12 for more information.

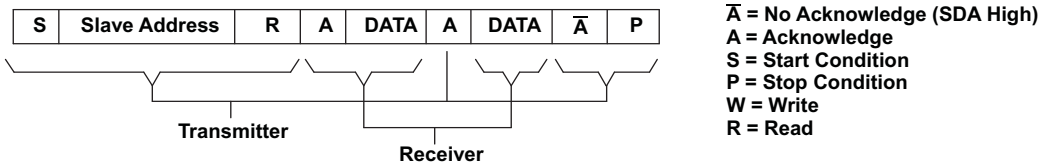


Figure 11. I²C Read Cycle

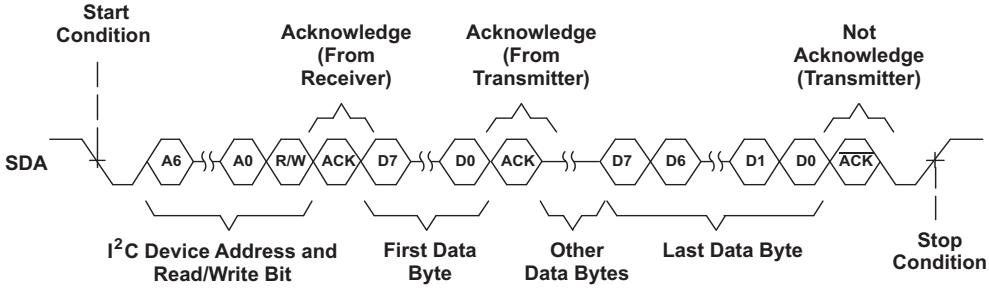


Figure 12. Multiple Byte Read Transfer

APPLICATIONS INFORMATION (continued)

Slave Address

Both the SDA and the SCL must be connected to a positive supply voltage via a pull-up resistor. These resistors should range from 2 kΩ to 19 kΩ in order to comply with the I^2C specification. When the bus is free, both lines are high. The address byte is the first byte received following the START condition from the master device. The first five bits (MSBs) of the address are factory-preset to 01011. The next two bits of the THS7347 address are controlled by the logic levels appearing on the I^2C, A1 and I^2C, A0 pins. The I^2C, A1 and I^2C, A0 address inputs can be connected to V_{DD} for logic 1, GND for logic 0, or actively driven by TTL/CMOS logic levels. The device address is set by the state of these pins and is not latched. Thus, a dynamic address control system could be used to incorporate several devices on the same system. Up to four THS7347 devices can be connected to the same I^2C bus without requiring additional *glue* logic. Table 1 lists the possible addresses for the THS7347.

Table 1. THS7347 Slave Addresses

FIXED ADDRESS					SELECTABLE WITH ADDRESS PINS		READ/WRITE BIT
Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2 (A1)	Bit 1 (A0)	Bit 0 (R/$\overline{W}$)
0	1	0	1	1	0	0	0
0	1	0	1	1	0	0	1
0	1	0	1	1	0	1	0
0	1	0	1	1	0	1	1
0	1	0	1	1	1	0	0
0	1	0	1	1	1	0	1
0	1	0	1	1	1	1	0
0	1	0	1	1	1	1	1

Channel Selection Register Description (Subaddress) and Power-Up Condition (PUC) Pin

The THS7347 operates using only a single-byte transfer protocol similar to that illustrated in Figure 9 and Figure 11. The internal subaddress registers and the functionality of each are given in Table 2. When writing to the device, it is required to send one byte of data to the corresponding internal subaddress. If control of all three channels is desired, then the master must cycle through all the subaddresses (channels) one at a time; see the example, **Writing to the THS7347** (in Section 12) for the proper procedure of writing to the THS7347.

During a read cycle, the THS7347 sends the data in its selected subaddress (or channel) in a single transfer to the master device requesting the information. See the **Reading from the THS7347** example (in Section 12) for the proper procedure on reading from the THS7347.

On power-up, the THS7347 registers are dictated by the Power-Up Control (PUC) pin. If the PUC pin is tied to GND, the THS7347 powers up in a fully disabled state. If the PUC pin is tied to VDD, upon power-up the THS7347 is configured in the following state: ADC buffers disabled, monitor pass-through enabled, and ac-bias on, for all three input channels. It remains in the state dictated by the PUC unti a valid write sequence is completed.

Table 2. THS7347 Channel Selection Register Bit Assignments

REGISTER NAME	BIT ADDRESS ($b_7b_6b_5....b_0$)
Channel 1	0000 0001
Channel 2	0000 0010
Channel 3	0000 0011
Channel H Sync, Channel V Sync, and Disable Controls	0000 0100

Channel Register Bit Descriptions

Each bit of the subaddress (channel selection) control register as described in the previous section allows the user to individually control the THS7347 functionality. This process allows the user to control the functionality of each channel independently with regard to the other channels. The bit description for Channel 1 through Channel 3 is shown in Table 3, while the H/V sync channels and the analog channel states are described in Table 4.

Table 3. THS7347 Channel Register (Channel 1 through Channel 3) Bit Decoder Table. Use with Register Bit Codes (0000 0001), (0000 0010), and (0000 0011)

BIT	FUNCTION	BIT VALUE(S)	RESULT
(MSB) 7	Sync-Tip Clamp Filter	0	500-kHz filter on the STC circuit
		1	5-MHz filter on the STC circuit
6, 5, 4, 3	MUX Selection	0 0 0 0	MUX Input A
		0 0 0 1	MUX Input A
		0 0 1 0	MUX Input A
		0 0 1 1	MUX Input A
		0 1 0 0	MUX Input A
		0 1 0 1	MUX Input B
		0 1 1 0	MUX Input B
		0 1 1 1	MUX Input B
		1 0 0 0	MUX Input B
		1 0 0 1	MUX Input B
		1 0 1 0	Reserved; do not care
		1 0 1 1	Reserved; do not care
		1 1 0 0	Reserved; do not care
		1 1 0 1	Reserved; do not care
		1 1 1 0	Reserved; do not care
		1 1 1 1	Reserved; do not care
2, 1, 0 (LSB)	Input Mode + Operation	0 0 0	Disables both monitor and buffer paths of the respective channel/register
		0 0 1	Channel Mute
		0 1 0	Input Mode = dc
		0 1 1	Input Mode = dc + Shift
		1 0 0	Input Mode = ac-bias
		1 0 1	Input Mode = ac-STC with low bias
		1 1 0	Input Mode = ac-STC with mid bias
		1 1 1	Input Mode = ac-STC with high bias

Bit 7 (MSB): Controls the sync-tip clamp filter. Useful only when AC-STC input mode is selected.

Bits 6, 5, 4, 3: Selects the Input MUX channel.

Bits 2, 1, and 0 (LSB): Configures the channel mode and operation. See Table 4, Bits 6 and 5, for more information with respect to the enable/disable state.

Table 4. THS7347 Channel Register (H/V Sync Channel + Analog Channels State) Bit Decoder Table. Use in Conjunction With Register Bit Code (0000 0100)

BIT	FUNCTION	BIT VALUE(S)	RESULT
(MSB) 7	Reserved; Do not care	X	Reserved; do not care
6	Monitor Pass-Through Path Disable Mode (Use in Conjunction with Table 3)	0	Disables all monitor channels regardless of bits 2:0 of Register 1 through Register 3
		1	Enables monitor channels functions dictated by each programmed register code
5	Buffer Path Disable Mode (Use in Conjunction with Table 3)	0	Disables all buffer channels regardless of bits 2:0 of Register 1 through Register 3
		1	Enables buffer channel functions dictated by each programmed register code
4, 3	Vertical Sync Channel MUX Selection	0 0	MUX Input A
		0 1	MUX Input B
		1 0	Reserved; do not care
		1 1	Reserved; do not care
2, 1	Horizontal Sync Channel MUX Selection	0 0	MUX Input A
		0 1	MUX Input B
		1 0	Reserved; do not care
		1 1	Reserved; do not care
0 (LSB)	H/V Sync Paths Disable Mode	0	Disable H-Sync and V-Sync Channels
		1	Enable H-Sync and V-Sync Channels

Bit (MSB) 7: Reserved; do not care.

Bit 6: Master Monitor Path Disable. Disables all monitor channels regardless of what is programmed into each register channel (1 to 3).

Bit 5: Master Buffer Path Disable. Disables all buffer channels regardless of what is programmed into each register channel (1 to 3).

Bits 4, 3: Selects the Input MUX channel for the Vertical Sync.

Bits 2, 1: Selects the Input MUX channel for the Horizontal Sync.

Bit 0 (LSB): Enables or disables the H-Sync and V-Sync Channels.

WRITE AND READ EXAMPLES

These examples illustrate the proper way to write to and read from the THS7347.

WRITING TO THE THS7347

An I^2C master initiates a write operation to the THS7347 by generating a start condition (S) followed by the THS7347 I^2C address, in MSB-first order, followed by a '0' to indicate a write cycle. After receiving an acknowledge from the THS7347, the master presents the subaddress (channel) it wants to write, consisting of one byte of data, MSB first. The THS7347 acknowledges the byte after completion of the transfer. Finally, the master presents the data it wants to write to the register (channel) and the THS7347 acknowledges the byte. The I^2C master then terminates the write operation by generating a stop condition (P). Note that the THS7347 does not support multi-byte transfers. To write to all three channels (or registers), this procedure must be repeated for each register, one series at a time (that is, repeat steps 1 through 8 for each channel).

Step 1	0
I^2C Start (Master)	S

Step 2	7	6	5	4	3	2	1	0
I^2C General Address (Master)	0	1	0	1	1	X	X	0

Where each *X* logic state is defined by I^2C-A1 and I^2C-A0 pins being tied to either V_{DD} or GND.

Step 3	9
I^2C Acknowledge (Slave)	A

Step 4	7	6	5	4	3	2	1	0
I^2C Write Channel Address (Master)	0	0	0	0	0	Addr	Addr	Addr

Where *Addr* is determined by the values shown in Table 2.

Step 5	9
I^2C Acknowledge (Slave)	A

Step 6	7	6	5	4	3	2	1	0
I^2C Write Data (Master)	Data	Data	Data	Data	Data	Data	Data	Data

Where *Data* is determined by the values shown in Table 3.

Step 7	9
I^2C Acknowledge (Slave)	A

Step 8	0
I^2C Stop (Master)	P

READING FROM THE THS7347

The read operation consists of two phases. The first phase is the address phase. In this phase, an I^2C master initiates a write operation to the THS7347 by generating a start condition (S) followed by the THS7347 I^2C address, in MSB-first order, followed by a '0' to indicate a write cycle. After receiving an acknowledge from the THS7347, the master presents the subaddress (channel) of the register it wants to read. After the cycle is acknowledged (A), the master terminates the cycle immediately by generating a stop condition (P).

The second phase is the data phase. In this phase, an I^2C master initiates a read operation to the THS7347 by generating a start condition followed by the THS7347 I^2C address, in MSB-first order, followed by a '1' to indicate a read cycle. After an acknowledge from the THS7347, the I^2C master receives one byte of data from the THS7347. After the data byte has been transferred from the THS7347 to the master, the master generates a not-acknowledge ($\overline{A}$) followed by a stop. As with the Write function, to read all channels, steps 1 through 11 must be repeated for each channel desired.

THS7347 Read Phase 1:

Step 1	0
I^2C Start (Master)	S

Step 2	7	6	5	4	3	2	1	0
I^2C General Address (Master)	0	1	0	1	1	X	X	0

Where each *X* logic state is defined by I^2C-A1 and I^2C-A0 pins being tied to either V_{DD} or GND.

Step 3	9
I^2C Acknowledge (Slave)	A

Step 4	7	6	5	4	3	2	1	0
I^2C Read Channel Address (Master)	0	0	0	0	0	Addr	Addr	Addr

Where *Addr* is determined by the values shown in Table 2.

Step 5	9
I^2C Acknowledge (Slave)	A

Step 6	0
I^2C Start (Master)	P

THS7347 Read Phase 2:

Step 7	0
I^2C Start (Master)	S

Step 8	7	6	5	4	3	2	1	0
I^2C General Address (Master)	0	1	0	1	1	X	X	1

Where each *X* Logic state is defined by I^2C-A1 and I^2C-A0 pins being tied to either V_{DD} or GND.

Step 9	9
I^2C Acknowledge (Slave)	A

Step 10	7	6	5	4	3	2	1	0
I^2C Read Data (Slave)	Data	Data	Data	Data	Data	Data	Data	Data

Where *Data* is determined by the logic values contained in the Channel Register.

Step 11	9
I^2C Not-Acknowledge (Master)	$\overline{A}$

Step 12	0
I^2C Stop (Master)	P

PACKAGE OPTION ADDENDUM

29-May-2007

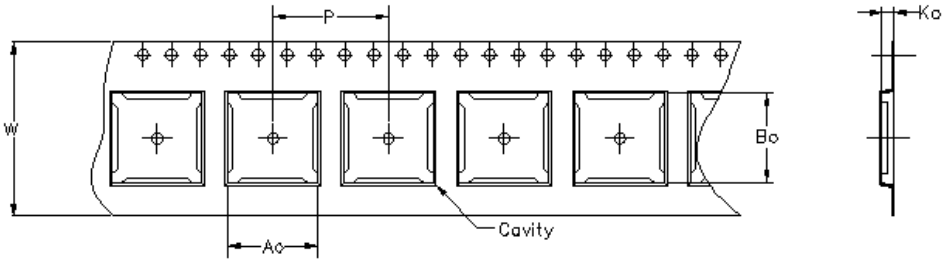
PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
THS7347IPHP	ACTIVE	HTQFP	PHP	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
THS7347IPHPR	ACTIVE	HTQFP	PHP	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

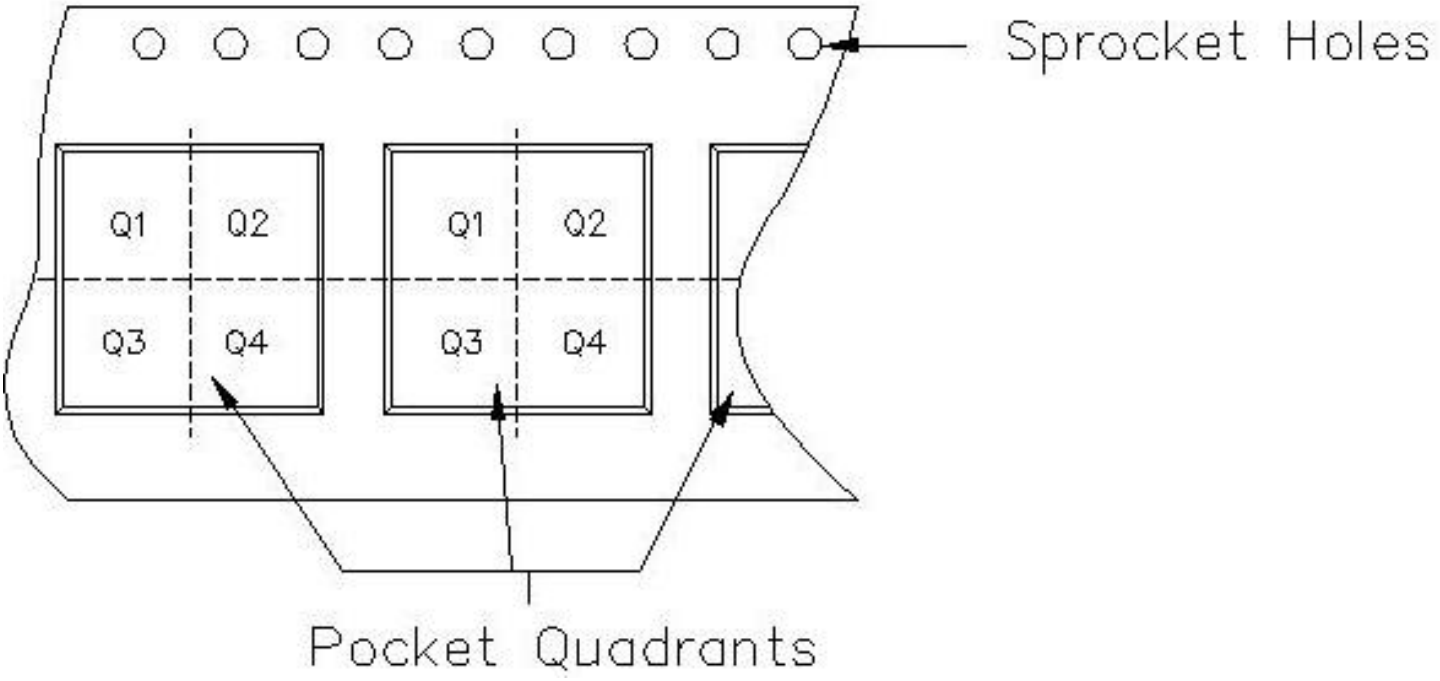
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.



Carrier tape design is defined largely by the component lentgh, width, and thickness.

Ao = Dimension designed to accommodate the component width.
Bo = Dimension designed to accommodate the component length.
Ko = Dimension designed to accommodate the component thickness.
W = Overall width of the carrier tape.
P = Pitch between successive cavity centers.

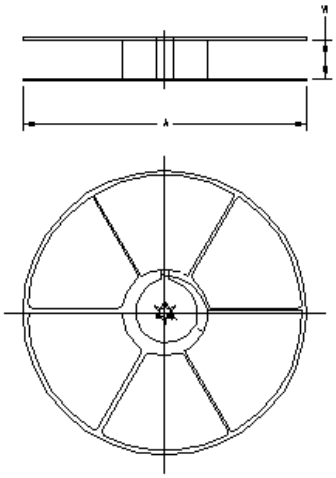


TAPE AND REEL INFORMATION

PACKAGE MATERIALS INFORMATION

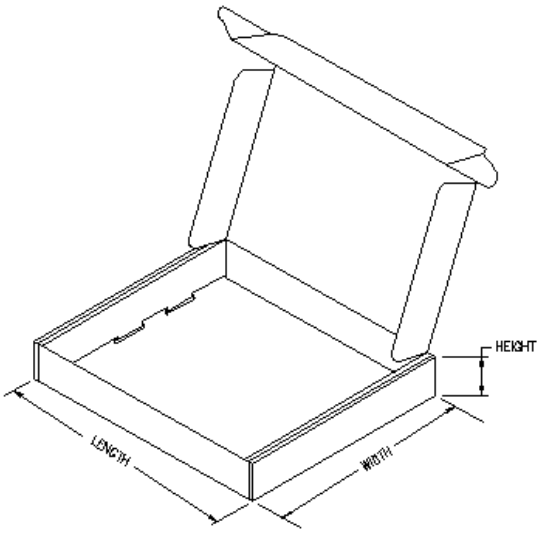
26-May-2007

Device	Package	Pins	Site	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
THS7347IPHPR	PHP	48	TAI	330	16	9.6	9.6	1.5	12	16	Q2

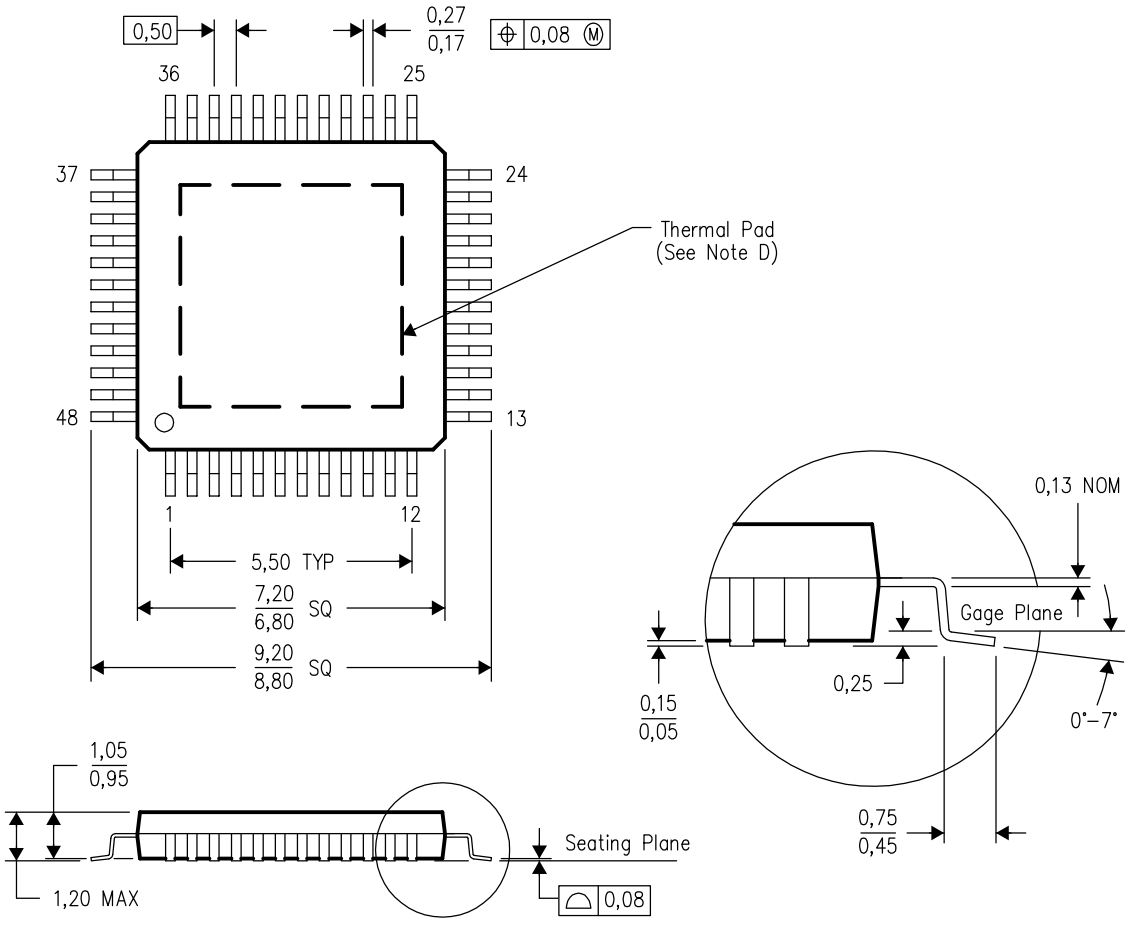


TAPE AND REEL BOX INFORMATION

Device	Package	Pins	Site	Length (mm)	Width (mm)	Height (mm)
THS7347IPHPR	PHP	48	TAI	346.0	346.0	33.0



PHP (S–PQFP–G48) PowerPAD™ PLASTIC QUAD FLATPACK



4146927/B 08/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. Falls within JEDEC MS–026

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