

- LinEPIC™ 1-μm CMOS Process
- 125-MHz Pipelined Architecture
- Available Clock Rate . . . 110 MHz
- Dual-Port Color RAM
256 Words x 24 Bits
- Bit-Plane Read and Blink Masks
- EIA RS-343-A Compatible Outputs
- Functionally Interchangeable With
Brooktree® Bt458
- Direct Interface to SMJ340xx Graphics Processors
- Standard Microprocessor Unit (MPU) Palette Interface
- Multiplexed-TTL Pixel Ports
- Triple Digital-to-Analog Converters (DACs)
- Dual-Port Overlay Registers . . . 4 × 24 Bits
- 5-V Power Supply

description

The TLC34058-110M color-palette integrated circuit is specifically developed for high-resolution color graphics in such applications as CAE/CAD/CAM, image processing, and video reconstruction. The architecture provides for the display of 1280 × 1024 bit-mapped color graphics (up to eight bits per pixel resolution) with two bits of overlay information. The TLC34058-110M has a 256-word × 24-bit RAM used as a lookup table with three 8-bit video D/A converters.

On-chip features such as high-speed pixel clock logic minimize costly ECL interface. Multiple pixel ports and internal multiplexing provide TTL-compatible interface (up to 32 MHz) to the frame buffer while maintaining sophisticated color graphic data rates (up to 135 MHz). Programmable blink rates, bit plane masking and blinking, color overlay capability, and a dual-port palette RAM are other key features. The TLC34058-110M generates red, green, and blue signals compatible with EIA RS-343-A and can drive 75-Ω coaxial cables terminated at each end without external buffering.

AVAILABLE OPTIONS

T _A	SPEED	DAC RESOLUTION	PACKAGE	
			84-PIN CERAMIC GRID ARRAY	84-PIN QUAD FLAT PACKAGE
-55°C to 125°C	110 MHz	8 Bits	TLC34058-110MGA	TLC34058-110MHFG

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Brooktree is a registered trademark of Brooktree Corporation.

PRODUCTION DATA information is current as of publication date.
Products conform to specifications per the terms of Texas Instruments
standard warranty. Production processing does not necessarily include
testing of all parameters.

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84-PIN GA PACKAGE (TOP VIEW)

12	COMP	GND	V _{DD}	P7D	P7B	P6E	P6C	P6B	P5E	P5C	P5B	P4E
11	IOB	GND	V _{DD}	P7E	P7C	P7A	P6D	P6A	P5D	P5A	P4C	P4A
10	IOG	FS ADJ	REF						P4D	P4B	SYNC	
9	V _{DD}	IOR								BLK	LD	
8	C1	R/W								CLK	CLK	
7	V _{DD}	C0								V _{DD}	V _{DD}	
6	GND	GND								P3E	GND	
5	CE	D7								P3C	P3D	
4	D6	D5								P3A	P3B	
3	D4	D2	D0							P2A	P2C	P2E
2	D3	D1	OL0B	OL0E	OL1B	OL1E	P0B	P0D	P1A	P1D	P1E	P2D
1	OL0A	OL0C	OL0D	OL1A	OL1C	OL1D	P0A	P0C	P0E	P1B	P1C	P2B
	A	B	C	D	E	F	G	H	J	K	L	M

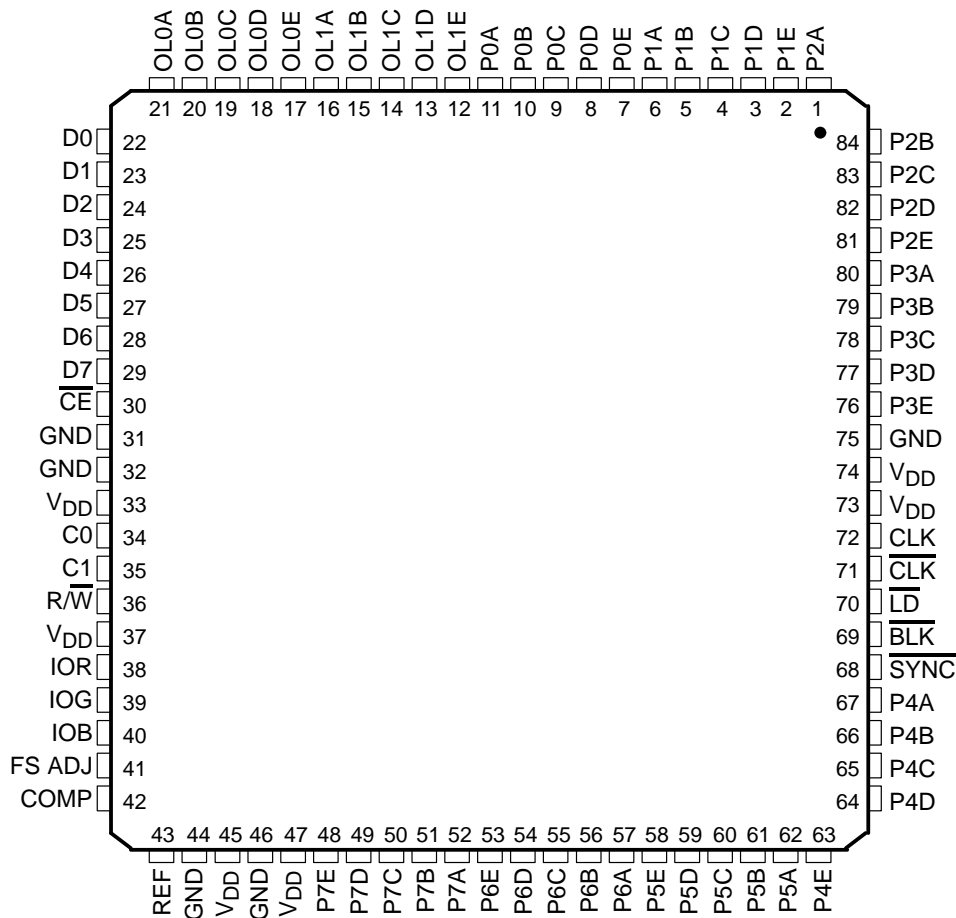
• (ESD symbol or alignment dot on top)

84-PIN GA PACKAGE (BOTTOM VIEW)

12	P4E	P5B	P5C	P5E	P6B	P6C	P6E	P7B	P7D	V _{DD}	GND	COMP
11	P4A	P4C	P5A	P5D	P6A	P6D	P7A	P7C	P7E	V _{DD}	GND	IOB
10	$\overline{\text{SYNC}}$	P4B	P4D							REF	FS ADJ	IOG
9	$\overline{\text{LD}}$	$\overline{\text{BLK}}$									IOR	V _{DD}
8	CLK	$\overline{\text{CLK}}$									R/ $\overline{\text{W}}$	C1
7	V _{DD}	V _{DD}									C0	V _{DD}
6	GND	P3E									GND	GND
5	P3D	P3C									D7	$\overline{\text{CE}}$
4	P3B	P3A	(ESD symbol or alignment dot on top)						●	D5	D6	
3	P2E	P2C	P2A							D0	D2	D4
2	P2D	P1E	P1D	P1A	P0D	P0B	OL1E	OL1B	OL0E	OL0B	D1	D3
1	P2B	P1C	P1B	P0E	P0C	P0A	OL1D	OL1C	OL1A	OL0D	OL0C	OL0A
	M	L	K	J	H	G	F	E	D	C	B	A

(ESD symbol or alignment dot on top)

HFG PACKAGE
(TOP VIEW)



84-pin GA package pin assignments

SIGNAL	PIN NO.
$\overline{\text{BLK}}$	L9
$\overline{\text{SYNC}}$	M10
$\overline{\text{LD}}$	M9
$\overline{\text{CLK}}$	L8
CLK	M8
Port 0	
P0A	G1
P0B	G2
P0C	H1
P0D	H2
P0E	J
Port 1	
P1A	J2
P1B	K1
P1C	L1
P1D	K2
P1E	L2
Port 2	
P2A	K3
P2B	M1
P2C	L3
P2D	M2
P2E	M3
Port 3	
P3A	L4
P3B	M4
P3C	L5
P3D	M5
P3E	L6
Port 4	
P4A	M11
P4B	L10
P4C	L11
P4D	K10
P4E	M12

SIGNAL	PIN NO.
Port 5	
P5A	K11
P5B	L12
P5C	K12
P5D	J11
P5E	J12
Port 6	
P6A	H11
P6B	H12
P6C	G12
P6D	G11
P6E	F12
Port 7	
P7A	F11
P7B	E12
P7C	E11
P7D	D12
P7E	D11
Overlay Select 0	
OL0A	A1
OL0B	C2
OL0C	B1
OL0D	C1
OL0E	D2
Overlay Select 1	
OL1A	D1
OL1B	E2
OL1C	E1
OL1D	F1
OL1E	F2
DAC Current Outputs	
I0G	A10
I0B	A11
I0R	B9

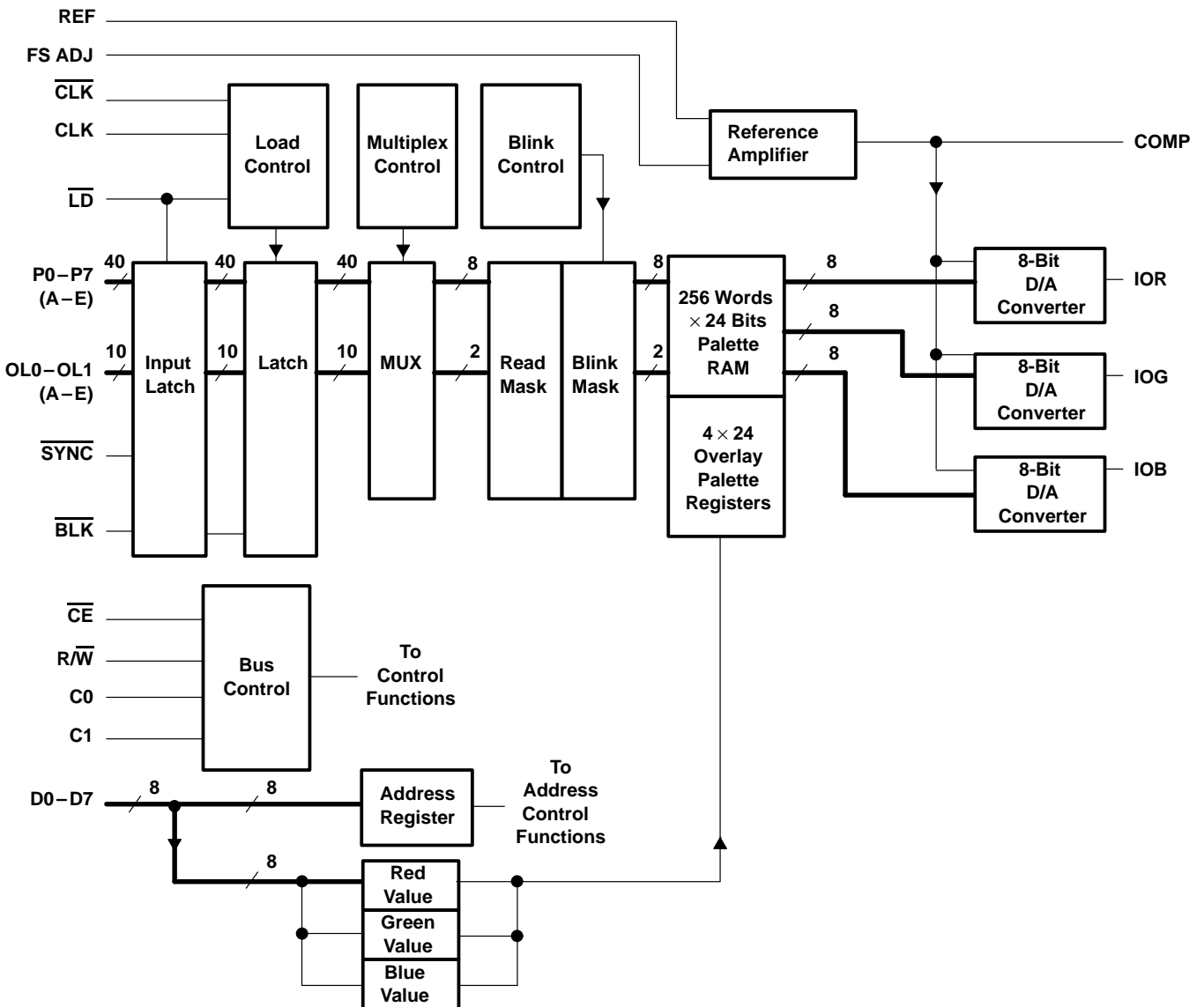
SIGNAL	PIN NO.
Power, Reference and MPU Interface	
V _{DD}	C12
V _{DD}	C11
V _{DD}	A9
V _{DD}	L7
V _{DD}	M7
V _{DD}	A7
GND	B12
GND	B11
GND	M6
GND	B6
GND	A6
COMP	A12
FS ADJ	B10
REF	C10
$\overline{\text{CE}}$	A5
R/ $\overline{\text{W}}$	B8
C1	A8
C0	B7
Data Bus	
D0	C3
D1	B2
D2	B3
D3	A2
D4	A3
D5	B4
D6	A4
D7	B5

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functional block diagram



Terminal Functions

TERMINAL NAME	NO.†	I/O	DESCRIPTION
BLK	69	I	Composite blank control input. This TTL-compatible blanking input is stored in the input latch on the rising edge of LD. When low, BLK drives the DAC outputs to the blanking level as shown in Table 6. This causes the P0–P7 (A–E) and OL0–OL1 (A–E) inputs to be ignored. When high, BLK allows the device to perform in the standard manner.
C0, C1	34, 35	I	Command control inputs. C0 and C1 specify the type of write or read operation (see Tables 1, 2, 3, and 4). These TTL-compatible inputs are latched on the falling edge of CE.
CE	30	I	Chip-enable input. This TTL-compatible input control allows data to be stored and enables data to be written or read (see Figure 1). When low, CE enables data to be written or read. When high, CE allows data to be internally latched on the rising edge during write operations. Care should be taken to avoid transients on this input.
CLK	72	I	Clock input. CLK provides the pixel clock rate. CLK and CLK inputs are designed to be driven by ECL logic using a 5-V single supply.
CLK	71	I	Clock input. CLK is the complement of CLK and also provides the pixel clock rate.
COMP	42	I	Compensation input. COMP is used to compensate the internal reference amplifier (see the video generation section). A 0.1-μF ceramic capacitor is connected between this terminal and VDD (see Figure 4). The highest possible supply voltage rejection ratio is attained by connecting the capacitor to VDD rather than to GND.
D0–D7	22–29	I	Data input bus. This TTL-compatible bus transfers data into or out of the device. The data bus is an 8-bit bidirectional bus where D0 is the least significant bit.
FS ADJ	41	I	Full-scale adjust control input. A resistor R _{set} (see Figure 4), which is connected between this terminal and GND, controls the magnitude of the full-scale video signal. The proportional current and voltage relationships in Figure 3 are maintained independently of the full-scale output current. The relationships between R _{set} and the IOR, IOG, and IOB full-scale output currents are: $R_{set}(\Omega) = 11294 \times V_{ref}(V) / IOG(mA)$ $IOR, IOB (mA) = 8067 \times V_{ref}(V) / R_{set}(\Omega)$
GND	31, 32, 44, 46, 75		Ground. All GND terminals must be connected together.
IOR, IOG IOB	38, 39, 40	O	Current outputs red, green, and blue. High-impedance red, green, and blue video analog current outputs can directly drive a 75-Ω cable coaxial terminated at each end (see Figure 4).
LD	70	I	Load-control input. This TTL-compatible load control (LD) input latches the P0–P7 (A–E), OL0–OL1 (A–E), BLK, and SYNC inputs on its rising edge. The LD strobe occurs at 1/4 or 1/5 the clock rate and may be phased independently of CLK and CLK. The LD duty cycle limits are specified in the timing requirements table.
OL0A–OL1A OL0B–OL1B OL0C–OL1C OL0D–OL1D OL0E–OL1E	12–21	I	Overlay selection inputs. These TTL-compatible inputs for the palette-overlay registers are stored in the input latch on the rising edge of LD. These inputs (up to 2 bits per pixel) along with bit CR6 of the command register (refer to the command register section and Table 5) specify whether the color information is selected from the palette RAM or the overlay registers. If the color information is selected from the overlay registers, the OL0–OL1 (A–E) inputs address a particular overlay register. The OL0–OL1 (A–D) or OL0–OL1 (A–E) inputs are simultaneously input to the device (see the description of bit CR7 in the command register section). The OL0–OL1 (A) inputs are processed first, then the OL0–OL1 (B) inputs, and so on. When obtaining the color information from the overlay registers, the P0–P7 (A–E) inputs are ignored. Unused inputs should be connected to GND.
P0A–P7A P0B–P7B P0C–P7C P0D–P7D P0E–P7E	1–11, 48–67, 76–84	I	Address inputs. These TTL-compatible inputs for the palette RAM are stored in the input latch on the rising edge of LD. These address inputs (up to 8 bits per pixel) select one of 256 24-bit words in the palette RAM, which is subsequently input to the red, green, and blue D/A converters as three 8-bit or 4-bit bytes. Four or five addresses are simultaneously input to the P0–P7 (A–D) or P0–P7 (A–E) ports, respectively (see the description of bit CR7 in the command register section). The word addressed by P0A–P7A is first sent to the DACs, then the word addressed by P0B–P7B, and so on. Unused inputs should be connected to GND.
REF	43	I	Reference voltage input. Voltage of 1.235 V is supplied at this input. An external voltage reference circuit, shown in Figure 4, is suggested. Generating the reference voltage with a resistor network is not recommended since low-frequency power supply noise directly couples into the DAC output signals. This input must be decoupled by connecting a 0.1-μF ceramic capacitor between V _{ref} and GND.

† Terminal numbers shown are for the HFG package only. For the GA package terminal assignments, see page 3.

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Terminal Functions (Continued)

TERMINAL NAME	NO.†	I/O	DESCRIPTION
R/W	36	I	Read/write input. This TTL-compatible control input is latched on the falling edge of \overline{CE} (see Figure 1). When low, R/W writes data to the device. Data is internally latched on the rising edge of \overline{CE} . When high, R/W reads data from the device.
\overline{SYNC}	68	I	Composite sync control input. This TTL-compatible \overline{SYNC} input is stored in the input latch on the rising edge of \overline{LD} . When low, \overline{SYNC} turns off a 40 IRE current source on the IOG output (see Figure 3). This input does not override any control data input (see Table 6). It should be brought low during the blanking interval only (see Figure 3). When high, \overline{SYNC} allows the device to perform in the standard manner.
V_{DD}	33, 37, 45, 47, 73, 74		Supply voltage. All V_{DD} terminals must be connected together.

† Terminal numbers shown are for the HFG package only. For the GA package terminal assignments, see page 3.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1)	7 V
Voltage range on any digital input (see Note 1)	–5 V to $V_{DD} + 0.5$ V
Analog output short-circuit current to any power supply or common, I_{OS}	unlimited
Operating free-air temperature range, T_A	–55°C to 125°C
Storage temperature range	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the recommended operating conditions section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V _{DD}		4.5	5	5.5	V
High-level Input voltage, V _{IH}	CLK, $\overline{\text{CLK}}$	V _{DD} – 1		V _{DD} + 0.5	V
	Other inputs	2		V _{DD} + 0.5	V
Low-level Input voltage, V _{IL}	CLK, $\overline{\text{CLK}}$	–0.5		V _{DD} – 1.6	V
	Other inputs	–0.5		0.8	V
Reference voltage, V _{ref}		1.2	1.235	1.26	V
Output load resistance, R _L			37.5		Ω
FS ADJ resistor, R _{Set}			523		Ω
Operating free-air temperature, T _A		–55		125	°C

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electrical characteristics over recommended ranges of supply voltage and operating free-air temperature, $R_{set} = 523 \Omega$, $V_{ref} = 1.235 \text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
I_{ref}	Input reference current			10		μA
k_{SVR}	Supply voltage rejection ratio	$f = 1 \text{ kHz}$, See Figure 4		0.5		$\frac{\%}{\Delta V_{DD}}$
I_{DD}	Supply current	$V_{DD} = 5 \text{ V}$, $T_A = 20^\circ\text{C}$		195		mA
		$V_{DD} = 5.5 \text{ V}$, $T_A = -55^\circ\text{C}$		550		
I_{IH}	High-level input current	CLK, $\overline{\text{CLK}}$			10	μA
		Other inputs			10	μA
I_{IL}	Low-level input current	CLK, $\overline{\text{CLK}}$			-10	μA
		Other inputs			-10	μA
C_i	Input capacitance, digital	$f = 1 \text{ MHz}$, $V_{I(PP)} = 1 \text{ V}$		4	20*	pF
$C_{i(CLK)}$	Input capacitance, CLK, $\overline{\text{CLK}}$	$f = 1 \text{ MHz}$, $V_{I(PP)} = 1 \text{ V}$		4	20*	pF
V_{OH}	High-level output voltage, D0–D7	$I_{OH} = -800 \mu\text{A}$	2.4			V
V_{OL}	Low-level output voltage, D0–D7	$I_{OL} = 6.4 \text{ mA}$		0.4		V
I_{OZ}	High-impedance-state output current				10	μA
z_o	Output impedance			50		$k\Omega$
C_o	Output capacitance ($f = 1 \text{ MHz}$, $I_O = 0$)			13	20*	pF

* On products compliant to MIL-STD-883, Class B, this parameter is not production tested.

† All typical values are at $T_A = 25^\circ\text{C}$.

timing requirements over recommended ranges of supply voltage and operating free-air temperature, $R_{set} = 523 \Omega$, $V_{ref} = 1.235 \text{ V}$ (see Note 2)

	MIN	MAX	UNIT
Clock frequency		110	MHz
$\overline{\text{LD}}$ frequency		27.5	MHz
t_{su1} Setup time, R/\overline{W} , C0, C1 high before $\overline{\text{CE}}\downarrow$	0		ns
t_{su2} Setup time, write data before $\overline{\text{CE}}\uparrow$	35		ns
t_{su3} Setup time, pixel and control	3		ns
t_{h1} Hold time, R/\overline{W} , C0, C1 high after $\overline{\text{CE}}\downarrow$	15		ns
t_{h2} Hold time, write data after $\overline{\text{CE}}\uparrow$	3		ns
t_{h3} Hold time, pixel and control	2		ns
t_{w1} Pulse duration, $\overline{\text{CE}}$ low	50		ns
t_{w2} Pulse duration, $\overline{\text{CE}}$ high	25		ns
t_{w3} Pulse duration, CLK high	4		ns
t_{w4} Pulse duration, CLK low	4		ns
t_{w5} Pulse duration, $\overline{\text{LD}}$ high	15		ns
t_{w6} Pulse duration, $\overline{\text{LD}}$ low	15		ns
t_{c1} Clock cycle time	9.09		ns
t_{c2} $\overline{\text{LD}}$ cycle time	36.36		ns

† See Figures 1 and 2.

NOTE 2: TTL input signals are 0 to 3 V with less than 3 ns rise/fall times between 10% and 90% levels. ECL input signals are $V_{DD} - 1.8 \text{ V}$ to $V_{DD} - 0.8 \text{ V}$ with less than 2 ns rise/fall times between 20% and 80% levels. For input and output signals, timing reference points are at the 50% signal level. Analog output loads are less than 10 pF. D0–D7 output loads are less than 40 pF.

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operating characteristics over recommended ranges of supply voltage and operating free-air temperature, $R_{set} = 523 \Omega$, $V_{ref} = 1.235 \text{ V}$ (unless otherwise noted)

analog outputs

PARAMETER		MIN	TYP†	MAX	UNIT
E_L	Integral linearity error (each DAC)			±1	LSB
E_D	Differential linearity error			±1	LSB
	Gray-scale error			±5%	
I_O	Output current				
	White level relative to blank	17.69	19.05	20.4	mA
	White level relative to black	16.74	17.62	18.5	
	Black level relative to blank	0.95	1.44	1.9	
	Blank level on IOR, IOB	−10	5	50	μA
	Blank level on IOG	6.29	7.6	8.96	mA
	Sync level on IOG	−10	5	50	μA
	LSB size		69.1		μA
	DAC to DAC matching		2%	5%	
	Output compliance voltage	−1		1.2	V

† All typical values are at $T_A = 25^\circ\text{C}$.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $R_{set} = 523 \Omega$, $V_{ref} = 1.235 \text{ V}$ (see Note 2)

PARAMETER		MIN	TYP	MAX	UNIT
t_{en1}	\overline{CE} low to data bus enabled	10			ns
t_{en2}	\overline{CE} low to data valid			75	ns
t_{dis}	\overline{CE} high to data bus disabled			15	ns
t_d	Analog output delay time (see Note 3)		10		ns
t_t	Analog output transition time (see Note 4)		2		ns
t_s	Analog output settling time (see Note 5)		9		ns
	Glitch impulse (see Note 6)		50		pV-s
	Analog output skew		0	2	ns
	Pipeline delay	6		10	clock cycles

- NOTES: 2. TTL input signals are 0 to 3 V with less than 3 ns rise/fall times between 10% and 90% levels. ECL input signals are $V_{DD} - 1.8 \text{ V}$ to $V_{DD} - 0.8 \text{ V}$ with less than 2 ns rise/fall times between 20% and 80% levels. For input and output signals, timing reference points are at the 50% signal level. Analog output loads are less than 10 pF. D0–D7 output loads are less than 40 pF.
3. Measured from 50% point of rising clock edge to 50% point of full-scale transition
4. Measured between 10% and 90% of full-scale transition
5. Measured from 50% point of full-scale transition to output settling within ±1 LSB. Settling time does not include clock and data feedthrough.
6. Glitch impulse includes clock and data feedthrough. The −3-dB test bandwidth is twice the clock rate.

PARAMETER MEASUREMENT INFORMATION

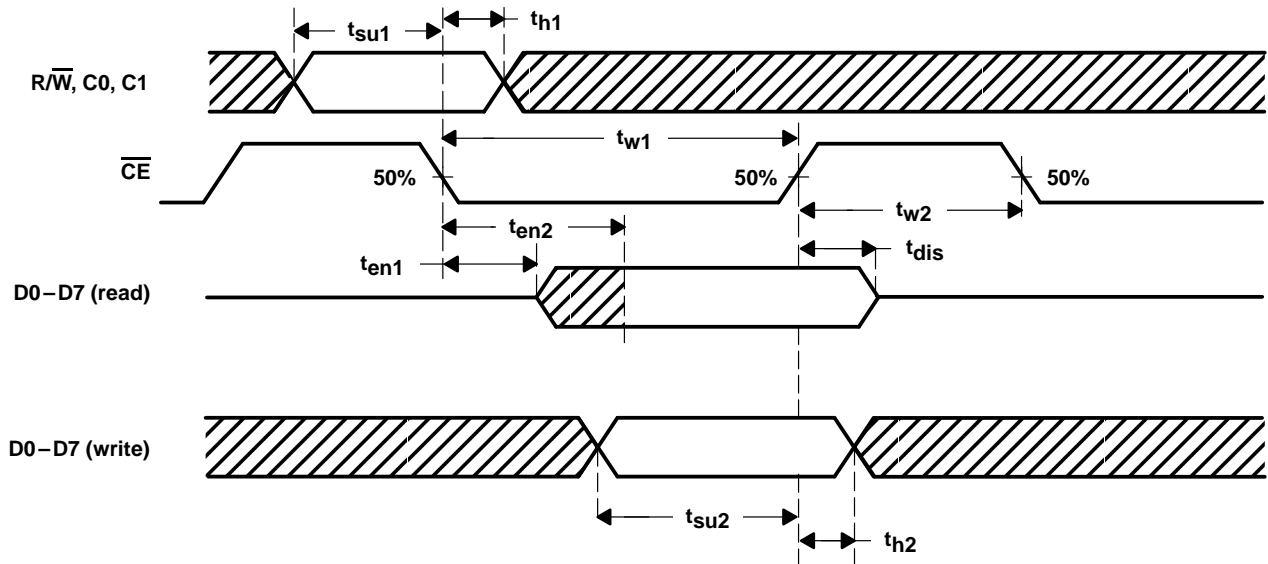


Figure 1. Read/Write Timing Waveform

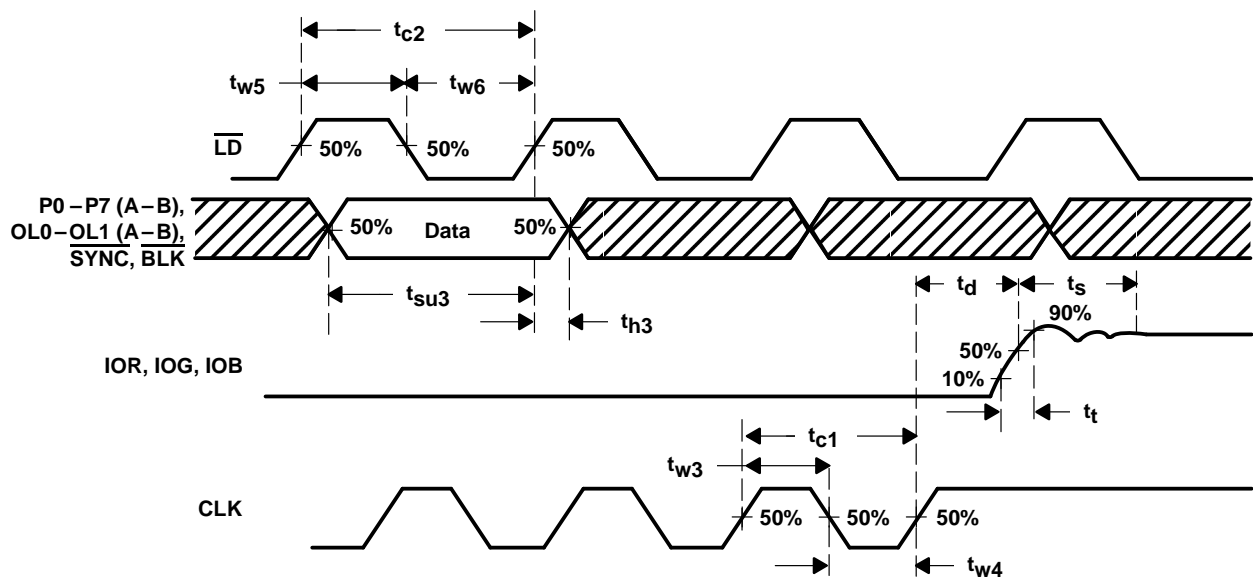


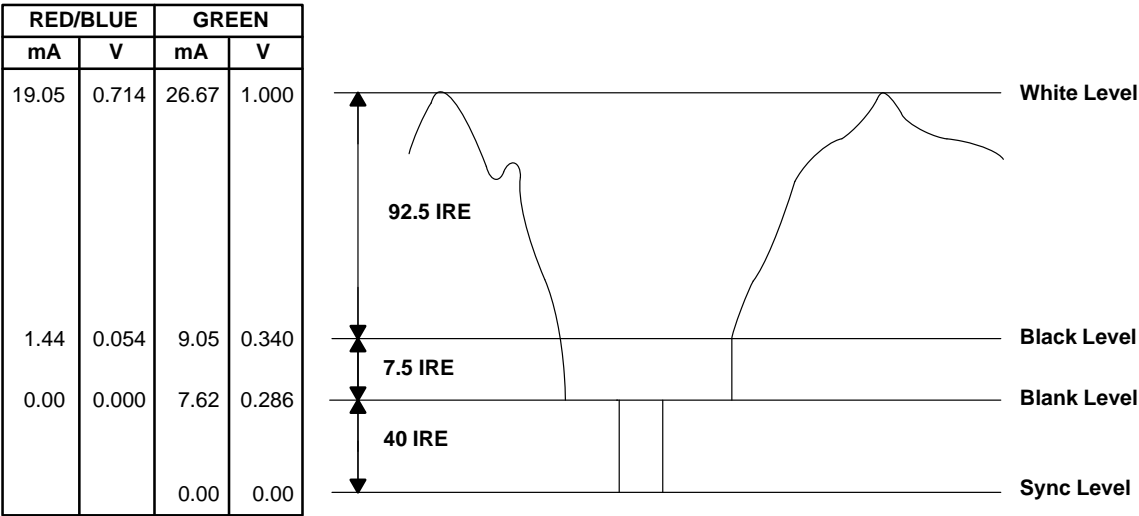
Figure 2. Video Input/Output Timing Waveform

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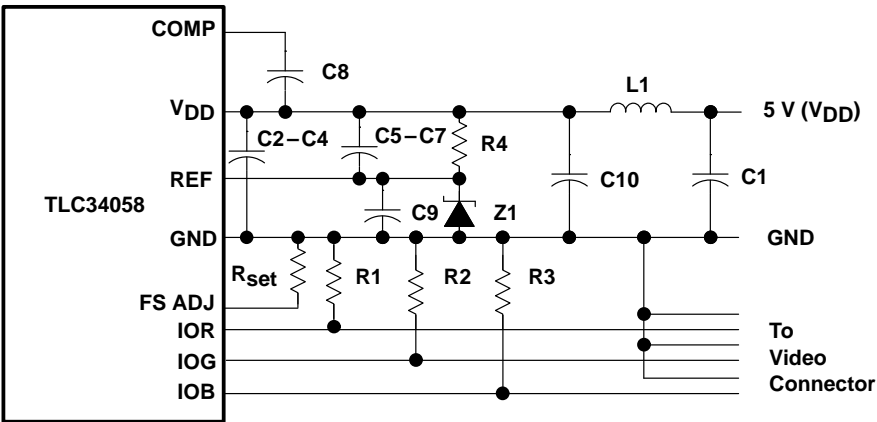
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PARAMETER MEASUREMENT INFORMATION



NOTE: The IRE (Institute of Radio Engineers – now IEEE) scale is used for defining the relative voltage levels of the sync, white, black, and blank levels in a monitor circuit. The reference white level is set at 100 IRE units. The blanking level is set at ϕ IRE units. One IRE unit is equivalent to 1/100 of the difference between the reference white level and the blanking level.

Figure 3. Composite Video Output Waveforms



LOCATION	DESCRIPTION	VENDOR PART NUMBER
C1–C4, C8, C9	0.1-μF ceramic capacitor	Erie RPE112Z5U104M50V
C5–C7	0.01-μF ceramic chip capacitor	AVX 12102T903QA1018
C10	33-μF tantalum capacitor	Mallory CSR13-K336KM
L1	ferrite bead	Fair-Rite 2743001111
R1, R2, R3	75-Ω 1% metal film resistor	Dale CMF-55C
R4	1000-Ω 1% metal film resistor	Dale CMF-55C
Rset	523-Ω 1% metal film resistor	Dale CMF-55C
Z1	1.2-V diode	National Semiconductor LM385Z-1.2

NOTE: The above listed vendor numbers are listed only as a guide. Substitution of devices with similar characteristics does not degrade the performance of the TLC34058.

Figure 4. Circuit Diagram

PARAMETER MEASUREMENT INFORMATION

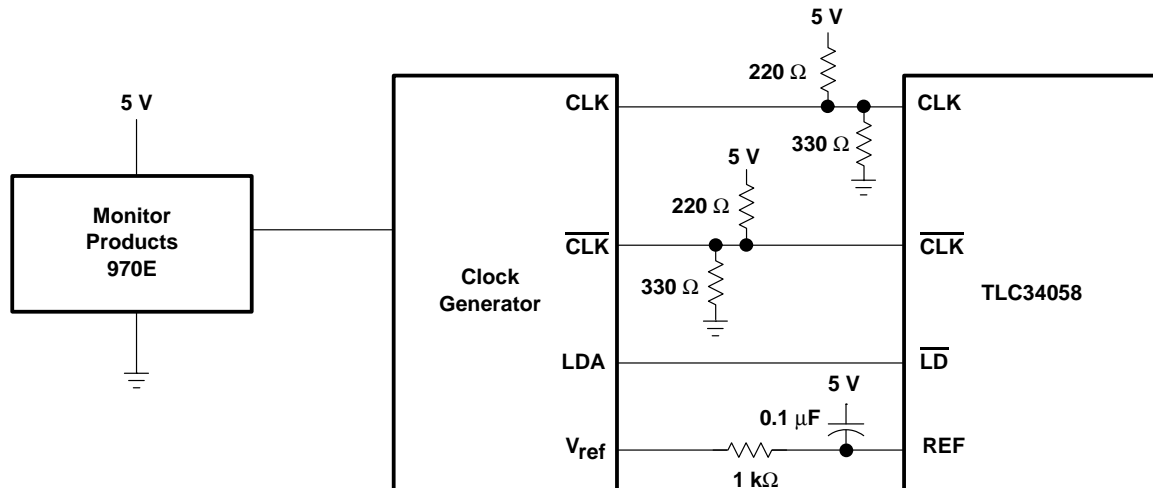


Figure 5. Generating the Clock, Load, and Voltage-Reference Signals

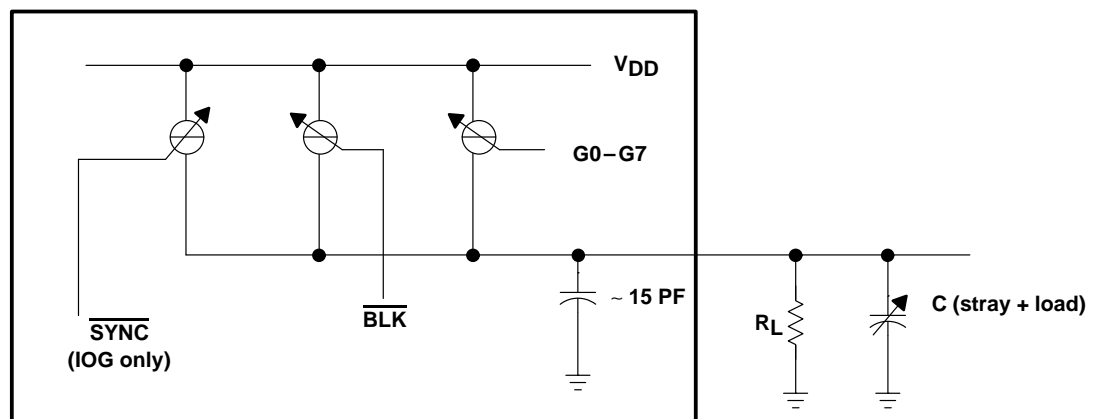


Figure 6. Equivalent Circuit of the Current Output (IOG)

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APPLICATION INFORMATION

device ground plane

Use of a four-layer PC board is recommended. All the ground pins, voltage reference circuitry, power supply bypass circuitry, analog output signals, and digital signals as well as any output amplifiers should have a common ground plane.

device analog power plane (APP)

The device plus associated analog circuitry should have a separate analog power plane (APP) for V_{DD} . The APP powers the device, voltage reference circuitry, and any output amplifiers. It is connected to the overall PCB power plane (V_{DD}) at a single point through a ferrite bead, which should be within three inches of the device. This connection is shown in Figure 4.

PCB power plane and PCB ground plane

The PCB power plane powers the digital circuitry. The PCB power plane and PCB ground planes should not overlay the APP unless the plane-to-plane noise is common mode.

supply decoupling

Bypass capacitors should have the shortest possible lead lengths to reduce lead inductance. For best results, connect a parallel combination of 0.1- μ F ceramic and 0.01- μ F chip capacitors from each V_{DD} to GND. If chip capacitors are not feasible, radial-lead ceramic capacitors may be substituted. These capacitors should be located as close to the device as possible.

The performance of the internal power supply noise-rejection circuitry decreases with noise frequency. If a switching power supply is used for V_{DD} , close attention must be paid to reducing power supply noise. To reduce such noise, power the APP with a three-terminal voltage regulator.

digital interconnect

Isolate the digital inputs from the analog outputs and other analog circuitry as much as possible. Shielding the digital inputs reduces noise on the power and ground lines. Minimize the lengths of clock and data lines to prevent high-frequency clock and data information from inducing noise into the analog part of the video system. Active termination resistors for the digital inputs should be connected to the PCB power plane, not the APP. Ensure that these digital inputs do not overlay the device ground plane.

analog signal interconnect

Minimizing the lead lengths between groups of V_{DD} and GND minimizes inductive ringing. To minimize noise pickup due to reflections and impedance mismatch, locate the device as close to the output connectors as possible. The external voltage reference should also be as close to the device as possible to minimize noise pickup. To maximize high-frequency supply voltage rejection, overlay the video output signals to the device ground plane and not the APP.

Each analog output has a 75- Ω load resistor connected to GND for maximum performance. To minimize reflections, the resistor connections between current output and ground should be as close to the device as possible.

APPLICATION INFORMATION

clock interfacing

To facilitate the generation of high-frequency clock signals, CLK and $\overline{\text{CLK}}$ are designed to accept differential signals that can be generated with 5-V (single-supply) ECL logic. Due to noise margins of the CMOS process, CLK and $\overline{\text{CLK}}$ must be differential signals. Connecting a single-ended clock signal to CLK and connecting $\overline{\text{CLK}}$ to GND does not work. CLK and $\overline{\text{CLK}}$ require termination resistors ($220\ \Omega$ to V_{DD} and $330\ \Omega$ to GND) that should be as close to the device as possible.

$\overline{\text{LD}}$ is typically generated by dividing the clock frequency by four (4:1 multiplexing) or five (5:1 multiplexing) and translating the resulting signal to TTL levels. Since no phase relationship between the $\overline{\text{LD}}$ and CLK signals is required, any propagation delay in $\overline{\text{LD}}$ caused by the divider circuitry does not affect device performance.

The pixel, overlay, sync, and blank data are latched on the rising edge of $\overline{\text{LD}}$. $\overline{\text{LD}}$ may also be used as the shift clock for the video DRAMs. In short, $\overline{\text{LD}}$ provides the fundamental timing for the video system.

The Bt438 clock generator (from Brooktree) is recommended for generating the CLK, $\overline{\text{CLK}}$, $\overline{\text{LD}}$, and REF signals. It supports both 4:1 and 5:1 multiplexing. Alternately, the Bt438 can interface the device to a TTL clock. Figure 5 illustrates the interconnection between the Bt438 and the device.

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microprocessor-unit (MPU) interface

As shown in the functional block diagram, the MPU has direct access to the internal control registers and color overlay palettes via a standard MPU interface. Since the palette-RAM and overlay registers have dual ports, they can be updated without affecting the display refresh process. One port is allocated for updating or reading data and the other for display.

palette-RAM write or read

The palette-RAM location is addressed by the internal 8-bit address register (ADDR0–ADDR7). The MPU can either write to or read from this register. The register eliminates the need for external address multiplexers. ADDR0–ADDR7 are updated via D0–D7. To address the red, green, and blue part of a particular RAM location, the internal address register is provided with two additional bits, ADDR_a and ADDR_b. These address bits count modulo 3 and are reset to 0 when the MPU accesses the internal-address register.

After writing to or reading from the internal-address register, the MPU executes three write or read cycles (red, green, and blue). The register ADDR_{ab} is incremented after each of these cycles so that the red, green, and blue information is addressed from the correct part of the particular RAM location. During the blue write cycle, the red, green, and blue color information is adjoined to form a 24-bit word, which is then written to the particular RAM location. After the blue write/read cycle, the internal address register bits ADDR0–ADDR7 are incremented to access the next RAM location. For an entire palette-RAM write or read, the bits ADDR0–ADDR7 are reset to 00 after accessing the FF (256) palette-RAM location.

Two additional control bits, C0 and C1, are used to differentiate the palette-RAM read/write function from other operations that utilize the internal-address register. C0 and C1 are respectively set high and low for writing to or reading from the palette RAM. Table 1 summarizes this differentiation, along with other internal-address-register operations. C0 and C1 are each set low for writing to or reading from the internal-address register.

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Table 1. Writing to or Reading From Palette RAM

R/W	C1	C0	ADDRb	ADDRa	FUNCTION
L	L	L	X	X	Write ADDR0–ADDR7: D0–D7 → ADDR0–ADDR7; 0 → ADDRa,b
L	L	H	L	L	Write red color: D0–D7 → RREG; increment ADDRa,b
L	L	H	L	H	Write green color: D0–D7 → GREG; increment ADDRa,b
L	L	H	H	L	Write blue color: D0–D7 → BREG; increment ADDRa,b; increment ADDR0–ADDR7; write palette RAM
H	L	L	X	X	Read ADDR0–ADDR7: ADDR0–ADDR7 → D0–D7; 0 → ADDRa,b
H	L	H	L	L	Read red color: R0–R7 → D0–D7; increment ADDRa,b
H	L	H	L	H	Read green color: G0–G7 → D0–D7; increment ADDRa,b
H	L	H	H	L	Read blue color: B0–B7 → D0–D7; increment ADDRa,b; increment ADDR0–ADDR7

X = irrelevant

overlay-register write/read

With a few exceptions, the overlay-register operation is identical to the palette-RAM write/read operation (refer to the palette-RAM write/read section). Upon writing to or reading from the internal-address register, the additional-address register ADDRab is automatically reset to 0. ADDRab counts modulo 3 as the red, green, and blue information is written to or read from a particular overlay register. The four overlay registers are addressed with internal-address-register values 00–03. After writing/reading blue information, the internal-address register bits ADDR0–ADDR7 are incremented to the next overlay location. After accessing overlay register value 03, the internal address register does not reset to 00 but is advanced to 04.

For writing to or reading from the internal-address register, C0 and C1 are set low. When accessing the overlay registers, C0 and C1 are set high. Refer to Table 2 for a quick reference.

Table 2. Writing to or Reading From Overlay Registers

R/W	C1	C0	ADDRb	ADDRa	FUNCTION
L	L	L	X	X	Write ADDR0–ADDR7: D0–D7 → ADDR0–7; 0 → ADDRa,b
L	H	H	L	L	Write red color: D0–D7 → RREG; increment ADDRa,b
L	H	H	L	H	Write green color: D0–D7 → GREG; increment ADDRa,b
L	H	H	H	L	Write blue color: D0–D7 → BREG; increment ADDRa,b; increment ADDR0–ADDR7; write overlay register
H	L	L	X	X	Read ADDR0–ADDR7: ADDR0–ADDR7 → D0–D7; 0 → ADDRa,b
H	H	H	L	L	Read red color: R0–R7 → D0–D7; increment ADDRa,b
H	H	H	L	H	Read green color: G0–G7 → D0–D7; increment ADDRa,b
H	H	H	H	L	Read blue color: B0–B7 → D0–D7; increment ADDRa,b; increment ADDR0–ADDR7

X = irrelevant

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control-register write/read

The four control registers are addressed with internal-address-register values 04–07. On writing to or reading from the internal-address register, the additional address bits ADDRab are automatically reset to 0. To facilitate read-modify-write operations, the internal-address register does not increment after writing to or reading from the control registers. All control registers may be accessed at any time. When accessing the control registers, C0 and C1 are respectively set low and high. Refer to Table 3 for a quick reference.

Table 3. Writing to or Reading From Control Registers

R/W	C1	C0	ADDRba	ADDRab	FUNCTION
L	L	L	X	X	Write ADDR0–ADDR7: D0–D7 → ADDR0–ADDR7; 0 → ADDRa,b
L	H	L	L	L	Write control register: D0–D7 → control register
H	L	L	X	X	Read ADDR0–ADDR7: ADDR0–ADDR7 → D0–D7; 0 → ADDRa,b
H	H	L	L	L	Read control register: control register → D0–D7

X = irrelevant

summary of internal-address-register operations

Table 4 provides a summary of operations that use the internal-address register. Figure 1 presents the read/write timing for the device. If an invalid address is loaded into the internal-address register, the device ignores subsequent data from the MPU during a write operation and sends incorrect data to the MPU during a read operation.

Table 4. Internal-Address-Register Operations

INTERNAL-ADDRESS-REGISTER VALUE (ADDR0–ADDR7) (HEX)	C1	C0	MPU ACCESS	ADDRab (COUNTS MODULO 3)	COLOR
00–FF	L	H	Color-palette RAM	00 01 11	Red value Green value Blue value
00–03	H	H	Over color 0 to 3	00 01 110	Red value Green value Blue value
04	H	L	Read-mask register		
05	H	L	Blink-mask register		
06	H	L	Command register		
07	H	L	Test register		

interruption of display-refresh pixel data (via simultaneous pixel-data retrieval and MPU write)

If the MPU is writing to a particular palette-RAM location or overlay register (during the blue cycle) and the display-refresh process is accessing pixel data from the same RAM location or overlay register, one or more pixels on the display screen may be disturbed. If the MPU write data is valid during the complete chip-enable period, a maximum of one pixel is disturbed.

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frame-buffer interface and timing

An internal latch and multiplexer enables the frame buffer to send the pixel data to the device at TTL rates. On the rising edges of $\overline{\text{LD}}$, information for four or five consecutive pixels is latched into the device. This information includes the palette-RAM address (up to 8 bits), the overlay-register address (up to 2 bits), and the sync and blank information for each of the four or five consecutive pixels. The timing diagram for this pixel-data input transfer is shown in Figure 2, along with the video output waveforms (IOR, IOG, and IOB). With this architecture, the sync and blank timing can only be recognized with four- or five-pixel resolution.

The display-refresh process follows the first-in first-out format. Color data is output from the device in the same order in which palette RAM and overlay addresses are input. This process continues until all four or five pixels have been output, at which point the cycle repeats.

The overlay timing can be controlled by the pixel timing; however, this approach requires that the frame buffer emit additional bit planes to control the overlay selection on a pixel basis. Alternately, the overlay timing can be controlled by external-character or cursor-generation timing (see the color selection section).

No phase relationship between the $\overline{\text{LD}}$ and CLK signals is required (see Figure 2). Therefore, the $\overline{\text{LD}}$ signal can be derived by externally dividing the CLK signal by four or five. Any propagation delay in $\overline{\text{LD}}$ caused by the divider circuitry does not render the device nonfunctional. Regardless of the phase relationship between $\overline{\text{LD}}$ and CLK, the pixel, overlay, sync, and blank data are latched on the rising edge of $\overline{\text{LD}}$.

The device has an internal load signal (not brought out to a pin) that is synchronous to CLK and follows $\overline{\text{LD}}$ by at least one and not more than four clock cycles. This internal load signal transfers the $\overline{\text{LD}}$ -latched data into a second set of latches, which are then internally multiplexed at the pixel clock or CLK signal frequency.

For 4:1 or 5:1 multiplexing, a rising edge of $\overline{\text{LD}}$ should occur every four or five clock cycles. Otherwise, the internal load signal generation circuitry cannot lock onto or synchronize with $\overline{\text{LD}}$.

color selection

The read mask, blink mask, and command registers process eight bits of color information (P0–P7) and two bits of overlay information (OL0–OL1) for each pixel every clock cycle. Control registers allow individual bit planes to be enabled/disabled for display and/or blinked at one of four blink rates and duty cycles (see the command register section, bits CR4–CR5).

By monitoring the $\overline{\text{BLK}}$ input to determine vertical retrace intervals, the device ensures that a color change due to blinking occurs only during the nonactive display time. A color change does not occur in the middle of the screen. A vertical retrace is sensed when $\overline{\text{BLK}}$ is low for at least 256 $\overline{\text{LD}}$ cycles. The color information is then selected from the palette RAM or overlay registers in accordance with the processed input pixel data. Table 5 presents the effect of the processed input pixel data upon color selection. P0 is the least significant bit (LSB) of the color-palette RAM. When CR6 is high and both OL1 and OL0 are low, color information resides in the color-palette RAM. When CR6 is low or either of the overlay inputs is high, the overlay registers provide the DAC inputs.

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Table 5. Input Pixel Data Versus Color Selection

COMMAND- REGISTER BIT	OVERLAY- SELECT INPUT		COLOR ADDRESS (HEX)	COLOR INFORMATION
CR6	OL1	OL0	P7–P0	
H	L	L	00	Color palette entry 00
H	L	L	01	Color palette entry 01
•	•	•	•	• • • •
•	•	•	•	• • • •
•	•	•	•	• • • •
H	L	L	FF	Color palette entry FF
L	L	L	XX	Overlay register 0
X	L	H	XX	Overlay register 1
X	H	L	XX	Overlay register 2
X	H	H	XX	Overlay register 3

X = irrelevant

video generation

The TLC34058 presents eight bits of red, green, and blue information from either the palette RAM or overlay registers to the three 8-bit DACs during every clock cycle. The DAC outputs produce currents that correlate to their respective color input data. These output currents are translated to voltage levels that drive the color CRT monitor. The $\overline{\text{SYNC}}$ and $\overline{\text{BLK}}$ signals adjust the DAC analog output currents to generate specific output levels that are required in video applications. Table 6 shows the effect of $\overline{\text{SYNC}}$ and $\overline{\text{BLK}}$ upon the DAC output currents. Figure 3 presents the overall composite video output waveforms. Only the green output (IOG) contains sync information.

The DAC architecture ensures monotonicity and reduced switching transients by using identical current sources and routing their outputs to the DAC current output or GND. Utilizing identical current sources eliminates the need for precision component ratios within the DAC ladder circuitry. An on-chip operational amplifier stabilizes the DAC full-scale output current over temperature and power supply variations.

Table 6. Effects of $\overline{\text{SYNC}}$ and $\overline{\text{BLK}}$ Upon DAC Output Currents (see Note 7)

DESCRIPTION	IOG (mA)	IOR, IOB (mA)	SYNC	BLK	DAC INPUTS
White	26.67	19.05	H	H	FF
Data	data + 9.05	data + 1.44	H	H	data
Data w/o $\overline{\text{SYNC}}$	data + 1.44	data + 1.44	L	H	data
Black	9.05	1.44	H	H	00
Black w/o $\overline{\text{SYNC}}$	1.44	1.44	L	H	00
Black	7.62	0	H	L	xx
$\overline{\text{SYNC}}$	0	0	L	L	xx

NOTE 7: The data in this table is measured with full-scale IOG current = 26.67 mA, $R_{\text{set}} = 523 \Omega$, $V_{\text{ref}} = 1.235 \text{ V}$.

command register

The MPU can write to or read from the command register at any time. The command register is not initialized. CR0 corresponds to the D0 data bus line. Refer to Table 7 for a quick reference.

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Table 7. Command Register

COMMAND-REGISTER BIT	COMMAND-REGISTER BIT FUNCTION	COMMAND-REGISTER BIT DESCRIPTION
CR7	Multiplex-select bit low: selects 4:1 multiplexing high: selects 5:1 multiplexing	This bit selects either 4:1 or 5:1 multiplexing for the palette RAM and overlay-register address, SYNC, and BLK inputs. If 4:1 multiplexing is selected, the device ignores the E palette RAM and overlay-register-address inputs. These inputs should be connected to GND, and the \overline{LD} signal frequency should be 1/4 of the clock frequency. If 5:1 is specified, all of the palette RAM and overlay-register-address inputs are used and the \overline{LD} signal should be 1/5 of the clock frequency.
CR6	RAM-enable bit low: use overlay register 0 high: use palette RAM	When the overlay select bits (OL0 and OL1) are both low, this bit causes the DACs color information to be selected from overlay register 0 or the palette RAM.
CR5, CR4	Blink-rate-select bits 00: 16 on, 48 off (25/75) 01: 16 on, 16 off (50/50) 10: 32 on, 32 off (50/50)	These two bits select the blink-rate cycle time and duty cycle. The on and off numbers specify the blink-rate cycle time as the number of vertical periods. The numbers in parentheses specify the duty cycle in (on/off) percent.
CR3	OL1 blink-enable bit low: disable blinking high: enable blinking	If this bit is a high, the OL1 (A–E) inputs toggle between a logic 0 and their input value at the selected blink rate before latching the incoming pixel data. Simultaneously, command-register CR1 must be set high. If the CR2 bit is low, the OL0 (A–E) inputs are unaffected.
CR2	OL0 blink-enable bit low: disable blinking high: enable blinking	If this bit is high, the OL0 (A–E) inputs toggle between a logic 0 and their input value at the selected blink rate before latching the incoming pixel data. Simultaneously, command-register CR0 must be set high. If the CR2 bit is low, the OL0 (A–E) inputs are unaffected.
CR1	OL1 display-enable bit low: disable high: enable	If this bit is low, the OL1 (A–E) inputs are forced to a logic 0 before latching the incoming pixel data. If the CR1 bit is high, the OL1 (A–E) inputs are affected.
CR0	OL0 display-enable bit low: disable high: enable	If this bit is low, the OL0 (A–E) inputs are forced to a logic 0 before latching the incoming pixel data. If the CR0 bit is high, the OL0 (A–E) inputs are affected.

read-mask register

The read-mask register is used to enable (high) or disable (low) the eight bit planes (P0–P7) within the palette-RAM addresses. The enabling or disabling is accomplished by logic ANDing the read-mask register with the palette-RAM address before addressing the palette RAM. Read-mask register bit 0 corresponds to data-bus line D0. The MPU can write to or read from this register at any time. This register is not initialized.

blink-mask register

The blink-mask register is used to enable (high) or disable (low) the blinking of bit planes within the palette-RAM addresses. For example, if blink-mask register bit n is set high, the true Pn value addresses the palette RAM during the on portion of the blink cycle. During the off part of the blink cycle, the Pn value is replaced with a 0 before the palette RAM is addressed. The blink-rate cycle time and duty cycle is specified by command-register bits CR4 and CR5. If blink-mask-register bit n is set low, the true Pn value always addresses the palette RAM. Blink-mask-register bit 0 corresponds to data-bus line D0. This register is not initialized.

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test register

The test register allows the MPU to read the inputs to the DAC for diagnostic purposes. The MPU can write to or read from this register at any time. This register is not initialized. Only the four least significant bits can be written to, while all eight bits can be read. Test-register bit 0 corresponds to data-bus line D0. A function description of this register is presented in Table 8.

Table 8. Functional Description of Test Register

TR3–TR0	D4–D7	FUNCTION
0100	4 MSBs of blue data input	MPU read or write D0–D3
0010	4 MSBs of green data input	
0001	4 MSBs of red data input	
1100	4 LSBs of blue data input	MPU read D0–D7
1010	4 LSBs of green data input	
1001	4 LSBs of red data input	

To read the DAC inputs, the MPU must first load the test register four least significant bits. One of the test register bits, b0 (red DAC), b1 (green DAC), or b2 (blue DAC), must be set high and the other two bits low. This process determines whether the inputs to the red, green, or blue DAC are read. The test register bit b3 must be set high for reading the four most significant DAC inputs or low for reading the four least significant inputs. The MPU then reads the test register while the test register's four least significant bits contain the previously written information. Either the device clock must be slowed down to the MPU cycle time or the same pixel and overlay data must be continuously presented to the device during the entire MPU read cycle.

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