LED DRIVER

FEATURES

- 16 Channels
- Drive Capability
  – 0 to 80 mA (Constant-Current Sink) x 16 ch
- Constant Current Accuracy
  – ±1% (typ)
- 1 Port of Serial Data Input/Output
- Fast Switching Output: T_r / T_f = 10ns (typ)
- CMOS Input/Output
- 30 MHz Data Transfer Rate
- Vcc = 3 V to 5.5 V
- Operating Temperature = -20°C to 85 °C
- LED Supply Voltage up to 17 V
- 32-pin HTSSOP (PowerPAD™) Package
- Dot Correction
  – 128-Step For Each Individual 16 ch
- Controlled In-Rush Current
- Error Information
  – LOD: LED Open Detection
  – TEF: Thermal Error Flag

APPLICATIONS

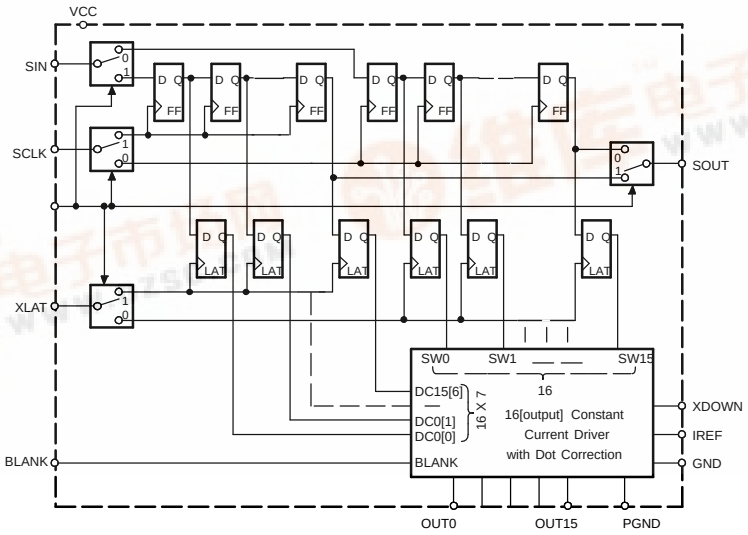
- LED Display
- LED Signboard

DESCRIPTION

The TLC5922 is a constant-current sink driver with 128 steps of adjustable current value (dot-correction). Each of the 16 channels has an individually controlled dot-correction and an ON/OFF state. Both the ON/OFF and dot-correction have their respective modes set via 1 port of serial I/F. The maximum current value of the constant-current output of all 16 channels is programmed by a single external resistor. An external processor programs each of the 16 channels of the TLC5922 with the desired ON/OFF state and dot-correction value through a single serial interface. After all data is loaded, the processor then latches the information into the TLC5922 and enables the outputs.

The TLC5922 includes two error flags. First is the LED open detection (LOD) which indicates a broken LED at an output terminal. The second is a thermal error flag (TEF) which indicates an over temperature condition. The TLC5922 has two methods to communicate these error flags to the external processor. One method is on a dedicated output pin, XDOWN. The other method is through the serial data output pin, SOUT.

FUNCTIONAL BLOCK DIAGRAM

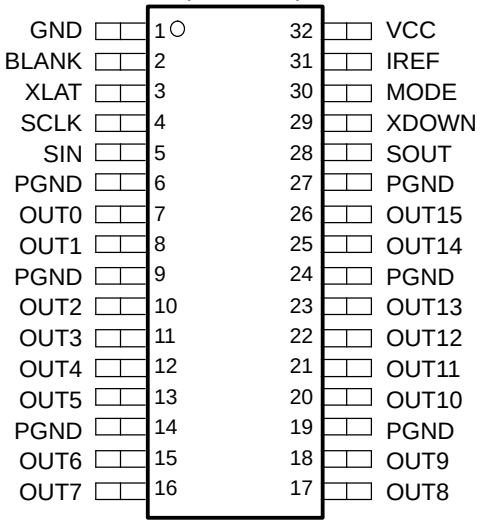


ORDERING INFORMATION (1)

T_A	PACKAGE	PART NUMBER (1)
-20 °C to 85 °C	4 mm x 4 mm, 32-pin HTSSOP	TLC5922DAP

(1) The DAP package is available in tape and reel. Add R suffix (TLC5922DAPR) to order quantities of 2000 parts per reel.

DAP PACKAGE
(TOP VIEW)



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
BLANK	2	2	Blank(Light OFF). When BLANK=H, All OUTx outputs are forced OFF. When BLANK=L, ON/OFF of OUTx outputs are controlled by input data.
GND	1		Ground
IREF	31	I/O	Reference current terminal
MODE	30	I	Mode select. When MODE=L, SIN, SOUT, SCLK, XLAT are connected to ON/OFF control logic. When MODE=H, SIN, SOUT, SCLK, XLAT are connected to dot-correction logic.
OUT0	7	O	Constant current output
OUT1	8	O	Constant current output
OUT2	10	O	Constant current output
OUT3	11	O	Constant current output
OUT4	12	O	Constant current output
OUT5	13	O	Constant current output
OUT6	15	O	Constant current output
OUT7	16	O	Constant current output
OUT8	17	O	Constant current output
OUT9	18	O	Constant current output
OUT10	20	O	Constant current output
OUT11	21	O	Constant current output
OUT12	22	O	Constant current output
OUT13	23	O	Constant current output
OUT14	25	O	Constant current output
OUT15	26	O	Constant current output
PGND	6, 9, 14, 19, 24, 27		Power ground

Terminal Functions (continued)

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
SCLK	4	I	Data shift clock. Note that the internal connections are switched by MODE (pin #30). At SCLK↑, the shift-registers selected by MODE shift the data.
SIN	5	I	Data input of serial I/F
SOUT	28	O	Data output of serial I/F
VCC	32		Power supply voltage
XDOWN	29	O	Error output. XDOWN is open drain terminal. XDOWN gets L when LOD or TEF detected.
XLAT	3	I	Data latch. Note that the internal connections are switched by MODE (pin #30). At XLAT↑, the latches selected by MODE get new data.

ABSOLUTE MAXIMUM RATINGS (1)

See (2)

		UNIT
Supply voltage (2)	V_{CC}	- 0.3 V to 6 V
Output current (dc)	$I_{L(LC)}$	90 mA
Input voltage range (2)	$V_{(BLANK)}$, $V_{(XLAT)}$, $V_{(SCLK)}$, $V_{(SIN)}$, $V_{(MODE)}$	- 0.3 V to V_{CC} + 0.3 V
Output voltage range (2)	$V_{(SOUT)}$, $V_{(XDOWN)}$	- 0.3 V to V_{CC} + 0.3 V
	$V_{(OUT0)}$ - $V_{(OUT15)}$	-0.3 V to 18.0 V
ESD rating	HBM (JEDEC JESD22-A114, Human Body Model)	2 kV
	CDM (JEDEC JESD22-C101, Charged Device Model)	500 V
Storage temperature range, T_{stg}		-40°C to 150°C
Continuous total power dissipation at (or below) T_A = 25°C		3.9 W
Power dissipation rating at (or above) T_A = 25°C		31.4 mW/°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to network ground terminal.

RECOMMENDED OPERATING CONDITIONS DC CHARACTERISTICS

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		3		5.5	V
Voltage applied to output, V_O (Out0 - Out15)				17	V
High-level input voltage, V_{IH}		0.8 VCC		VCC	V
Low-level input voltage, V_{IL}		GND		0.2 VCC	V
High-level output current, I_{OH}	V_{CC} = 5 V at SOUT			-1	mA
Low-level output current, I_{OL}	V_{CC} = 5 V at SOUT, XDOWN			1	mA
Constant output current, $I_{O(LC)}$	OUT0 to OUT15			80	mA
Operating free-air temperature range, T_A (1)		-20		85	°C

(1) Please contact TI sales for slightly extended temperature range.

AC CHARACTERISTICS

V_{CC} = 3 V to 5.5 V, T_A = -20°C to 85°C (unless otherwise noted)

			MIN	TYP	MAX	UNIT
f_{SCLK}	Clock frequency	SCLK			30	MHz
t_{wh0}/t_{wl0}	CLK pulse duration	SCLK=H/L	20			ns
t_{wh1}	XLAT pulse duration	XLAT=H	20			ns
t_{su0}	Setup time	SIN - SCLK↑	10			ns
t_{su1}		SCLK↑-XLAT↓	10			ns
t_{su2}		MODE↑↓-SCLK↑	10			ns
t_{su3}		MODE↑↓-XLAT↓	10			ns
t_{h0}	Hold time	SCLK↑-SIN	10			ns
t_{h1}		XLAT↓-SCLK↑	10			ns
t_{h2}		SCLK↑-MODE↑↓	10			ns
t_{h3}		XLAT↓-MODE↑↓	10			ns

ELECTRICAL CHARACTERISTICS

V_{CC} = 3 V to 5.5 V, T_A = - 20°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = - 1 mA, SOUT	V_{CC}0.5V			V
V_{OL}	Low-level output voltage	I_{OL} = 1 mA, SOUT			0.5	V
I_I	Input current	V_I = V_{CC} or GND, BLANK, XLAT,SCLK, SIN, MODE	-1		1	µA
I_{CC}	Supply current	No data transfer, All output OFF, V_O = 1 V, $R_{(IREF)}$ = 10 kΩ			6	mA
		No data transfer, All output OFF, V_O = 1 V, $R_{(IREF)}$ = 1.3 kΩ			12	
		Data transfer 30 MHz, All output ON, V_O = 1 V, $R_{(IREF)}$ = 1.3 kΩ			25	
		Data transfer 30 MHz, All output ON, V_O = 1 V, $R_{(IREF)}$ = 600 kΩ		36	65 (1)	
I_{OLC}	Constant output current	All output ON, V_O= 1 V, $R_{(IREF)}$ = 600Ω	70	80	90	mA
I_{OKL0}	Leakage output current	All output OFF, V_O= 15 V, $R_{(IREF)}$ = 600Ω , OUT0 to OUT15			0.1	µA
I_{OKL1}		VXDOWN = 5.5 V, No TEF and LOD			10	µA
ΔI_{OLC}	Constant current error	All output ON, V_O = 1 V, $R_{(IREF)}$ = 600 Ω, OUT0 to OUT15		±1	± 4	%
ΔI_{OLC1}	Power supply rejection ratio	All output ON, V_O = 1 V, $R_{(IREF)}$ = 600 Ω, OUT0 to OUT15		± 1	± 4	%/V
ΔI_{OLC2}	Load regulation	All output ON, V_O = 1 V to 3 V, $R_{(IREF)}$ = 600 Ω, OUT0 to OUT15		± 2	± 6	%/V
T_{TEF}	Thermal error flag threshold	Junction temperature, rising temperature (2)	150		180	°C
$V_{(LOD)}$	LED open detection threshold			0.3		V
V_{IREF}	Reference voltage output	$R_{(IREF)}$ = 600 Ω		1.22		V

(1) Measured at device start-up temperature. Once the IC is operatiing (self heating), lower I_{CC} values will be seen. See Figure 12.
(2) Not tested. Specified by design.

SWITCHING CHARACTERISTICS

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_r	Rise time	SOUT(see (1))			20	ns
		OUTx, V_{CC} = 5 V, T_A = 60°C, DCx = 7F (see (2))		10	30	
t_f	Fall time	SOUT(see (1))			20	ns
		OUTx, V_{CC} = 5 V, T_A = 60°C, DCx = 7F (see (2))		10	30	
t_{pd}	Propagation delay time	SCLK↑ - SOUT↑↓ (see (3))			300	ns
		MODE↑↓ - SOUT↑↓ (see (3))			300	
		BLANK↓ - OUT0↑↓ (see (4))			60	
		XLAT↑ - OUT0↑↓ (see (4))			60	
		OUTx↑↓-XDOWN↑↓ (see (5))			1000	
		XLAT↑-I_{OUT}(dot-correction) (see (6))			1000	
	Output delay time	OUTn↑↓-OUT(n+1)↑↓ (see (4))	14	22	30	ns

(1) See Figure 4. Defined as from 10% to 90%
(2) See Figure 5. Defined as from 10% to 90%
(3) See Figure 4, Figure 9and Figure 10
(4) See Figure 5 and Figure 9
(5) See Figure 5, Figure 6, and Figure 9
(6) See Figure 5 and Figure 10

PIN EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS

(Note: Resistor values are equivalent resistance and not tested).

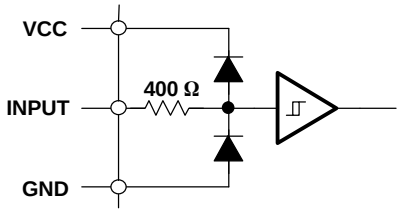


Figure 1. Input Equivalent Circuit (BLANK, XLAT, SCLK, SIN, MODE)

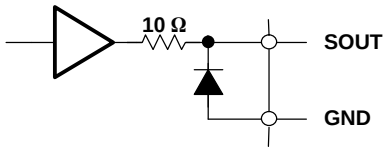


Figure 2. Output Equivalent Circuit

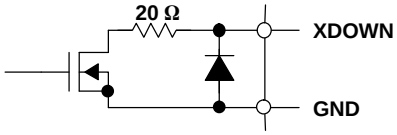


Figure 3. Output Equivalent Circuit (XDOWN)

PARAMETER MEASUREMENT INFORMATION

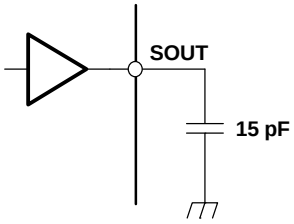


Figure 4. Test Circuit for Tr0, Tf1, Td0, Td1

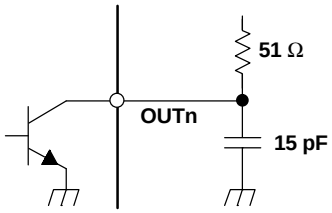


Figure 5. Test Circuit for Tr1, Tf1, Td2, Td3, Td5, Td6

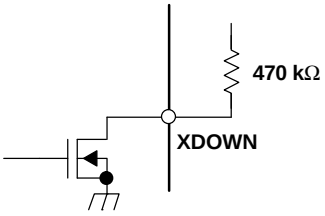


Figure 6. Test Circuit for Td4

PRINCIPLES OF OPERATION

Setting Constant-Current Value

The maximum programmable output current for all 16 outputs is set by a single resistor, $R_{(IREF)}$, which is placed between IREF and GND. The current flowing through $R_{(IREF)}$ is sampled by the TLC5922 and multiplied by a scaling factor of 40 to set the maximum output current for all outputs. The voltage on IREF is set by an internal band gap with a nominal value of 1.22V. The maximum programmable output current is set by Equation 1:

$$I_{MAX} = \frac{V_{IREF}}{R_{IREF}} \times 40 \quad (1)$$

where:

V_{IREF} = 1.22V

R_{IREF} = User selected external resistor (R_{IREF} should not be smaller than 600Ω)

Setting Dot-Correction

The TLC5922 has the capability to adjust the brightness of each channel, OUT0,...,OUT15. This capability is called dot-correction. The external processor programs each of the 16 channels of the TLC5922 with a 7 bit word that adjusts each respective output from 0% to 100% of the maximum output current, Imax. The 7 bits provides 2^7 (= 128) programmable current values. Equation 2 below determines the output current for each output:

$$I_{Outn} = \frac{I_{MAX} \times DC_n}{127} \quad (2)$$

PRINCIPLES OF OPERATION (continued)

where:

I_{Max} = the maximum programmable current of each output

DCn = the programmed dot-correction value for output n (DCn = 0, 1, 2 ...127)

n = 0, 1, 2 ... 15

Forcing OFF the Constant Current Outputs

The BLANK input pin is used to disable all OUTx constant-current output terminals. When BLANK is a logic 1, all OUTx are forced off, regardless of any other logic operations.

Internal Register Definitions

The TLC5922 has two separate serial data shift-registers and two separate data-latches. The first combination of registers and latches controls the ON/OFF function of the output. These are referred to as the EN_REG registers and EN_LATCHn latches, where n= 0,1...15 and specifies the output channel. There are 16 EN_REG registers and 16 EN_LATCHn latches. Both are one bit each. Figure 7 shows how these are connected.

The second combination of registers and latches controls the dot-correction value for each output. These are referred to as the DC_REG registers and DC_LATCHn latches, where n=0,1...15 and specifies the output channel. There are 112 DC_REG data shift-registers (1 bit each) and 16 DC_LATCHn latches (seven bits each). Figure 8 shows how these are connected.

All data to the TLC5922 comes from the SIN pin. The MODE pin determines whether the inputs and outputs of the TLC5922 are connected to the ON/OFF logic or the dot-correction logic. When MODE is a logic 0, all data is connected to the ON/OFF logic. When MODE is a logic 1, all data is connected to the dot-correction logic.

Each rising edge of the SCLK pin shifts the data in either the EN_REG or DC_REG registers. Each rising edge of the XLAT pin transfers the data from the selected registers (either EN_REG or DC_REG) and latches it into the selected latch (EN_LATCHn or DC_LATCHn).

Turning ON/OFF the Constant Current Outputs

The TLC5922 EN_LATCHn data-latches hold the ON/OFF information for each output. When the MODE input is low, the processor can access both the EN_LATCHn and EN_REG registers. The 16 cascaded EN_REG shift registers transfer ON/OFF data from SIN to SOUT output at each rising edge of the SCLK pin. XLAT is held low when the ON/OFF data is clocked into the TLC5922. When all data is clocked in, the rising edge of the XLAT pin transfers and latches the ON/OFF data into the EN_LATCHn latches. Each of the 16 EN_LATCHn data-latches holds a 1 bit digital code that turns each of the 16 outputs on or off. The processor must clock in 16 bits of data to fully program the ON/OFF setting for all 16 outputs. The ON/OFF data becomes valid on the OUTn outputs when BLANK goes low.

During the XLAT=H(MODE=L), shift-register loads the LOD status of each 16 outputs (and the controller can read the LOD status from SOUT). Note that incoming data from the controller is latched at XLAT↑(MODE=L), and afterwards, the shift-register loads LOD status during XLAT=H(MODE=L).

PRINCIPLES OF OPERATION (continued)

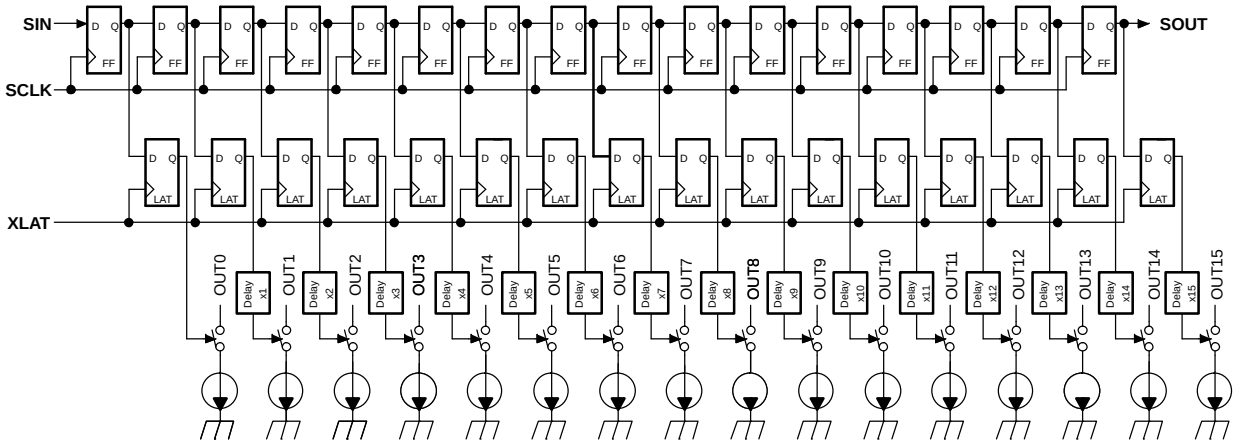


Figure 7. Shift Register and Data Latch for ON/OFF Setting

Delay Between Outputs

The TLC5922 has graduated delay circuits between outputs. In Figure 7, these delay circuits can be found between OUTn and constant current block. The fixed delay time is 20 ns (TYP), OUT0 has no delay, OUT1 has 20 ns delay, OUT2 has 40 ns delay. This delay prevents large inrush currents, which reduce power supply bypass capacitor requirements when the outputs turn on.

Setting Dot-Correction

The TLC5922 DC_LATCHn data latches hold the dot-correction information for each output. When the MODE input is high, the processor can access both the DC_LATCHn and DC_REG registers. The 112 cascaded DC_REG shift registers transfer dot-correction data from SIN to SOUT output at each rising edge of the SCLK pin. XLAT is held low when the dot-correction data is clocked into the TLC5922. When all data is clocked in, the rising edge of the XLAT pin transfers and latches the dot-correction data into the DC_LATCHn latches. Each of the 16 DC_LATCHn data-latches holds a 7 bit digital code to adjust the constant current value for each of the 16 outputs. The processor must clock in 112 bits of data to fully program the dot-correction for all 16 channnels.

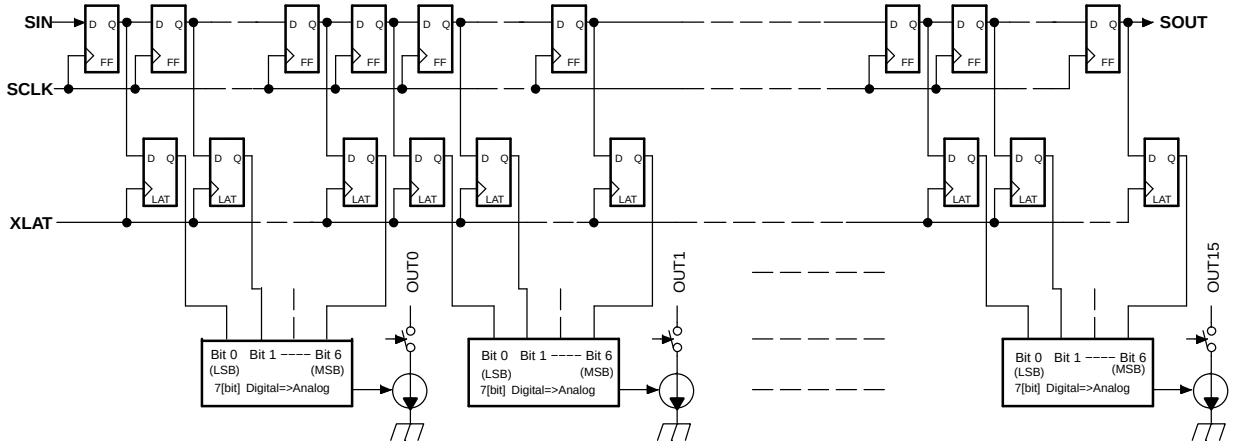


Figure 8. Shift Register and Data Latch for Dot-Correction

PRINCIPLES OF OPERATION (continued)

Error Information Output

The open-drain output, XDOWN, is used to report both of the TLC5922 error flags. (Note: the XDOWN output must be pulled to V_{CC} with a pullup resistor)

During normal operating conditions, an internal FET connected to the XDOWN pin is turned off. The voltage on XDOWN is pulled up to V_{CC} through the pullup resistor. If TEF or LOD is detected (see following sections), the internal FET is turned on, and XDOWN is pulled to GND.

Since XDOWN is an open-drain output, multiple ICs can be OR'ed together and pulled up to V_{CC} with a single pullup resistor. This reduces the number of signals needed to report a system error.

TEF: Thermal Error Flag

The TLC5922 provides a temperature error flag (TEF) circuit to indicate an over-temperature condition of the IC. If the junction temperature exceeds the threshold temperature (160^{o}C typ), the TEF circuit trips and pulls XDOWN to ground.

LOD: LED Open Detection

The TLC5922 provides an LED open detection circuit (LOD). This circuit reports an error if any one of the 16 LEDs is open, or is disconnected from the circuit. The LOD circuit trips when two conditions are met simultaneouly: When OUTn is programmed to be on, and when the voltage at OUTn is less than 0.3V (Note: the voltage at each OUTn is sampled 1µS after being turned on).

An LOD failure is reported in two ways. First, the LOD circuit only monitors OUTn when the OUTn is turned on. Each OUTn is individually monitored. The state of all 16 outputs are OR'ed together and reported at the XDOWN pin.

Second, the LOD circuit may also be monitored from the SOUT pin. When the MODE pin is low and the XLAT pin goes high, the 16 bits of ON/OFF data get transferred from the EN_REG registers to the EN_LATCHn latches. At the same time, the LOD status of each output is transferred to the EN_REG registers. These 16 bits of LOD data are then clocked out of the SOUT pin as the new ON/OFF data is clocked into the SIN pin. This reporting scheme allows the processor to determine the state of each LED.

PRINCIPLES OF OPERATION (continued)

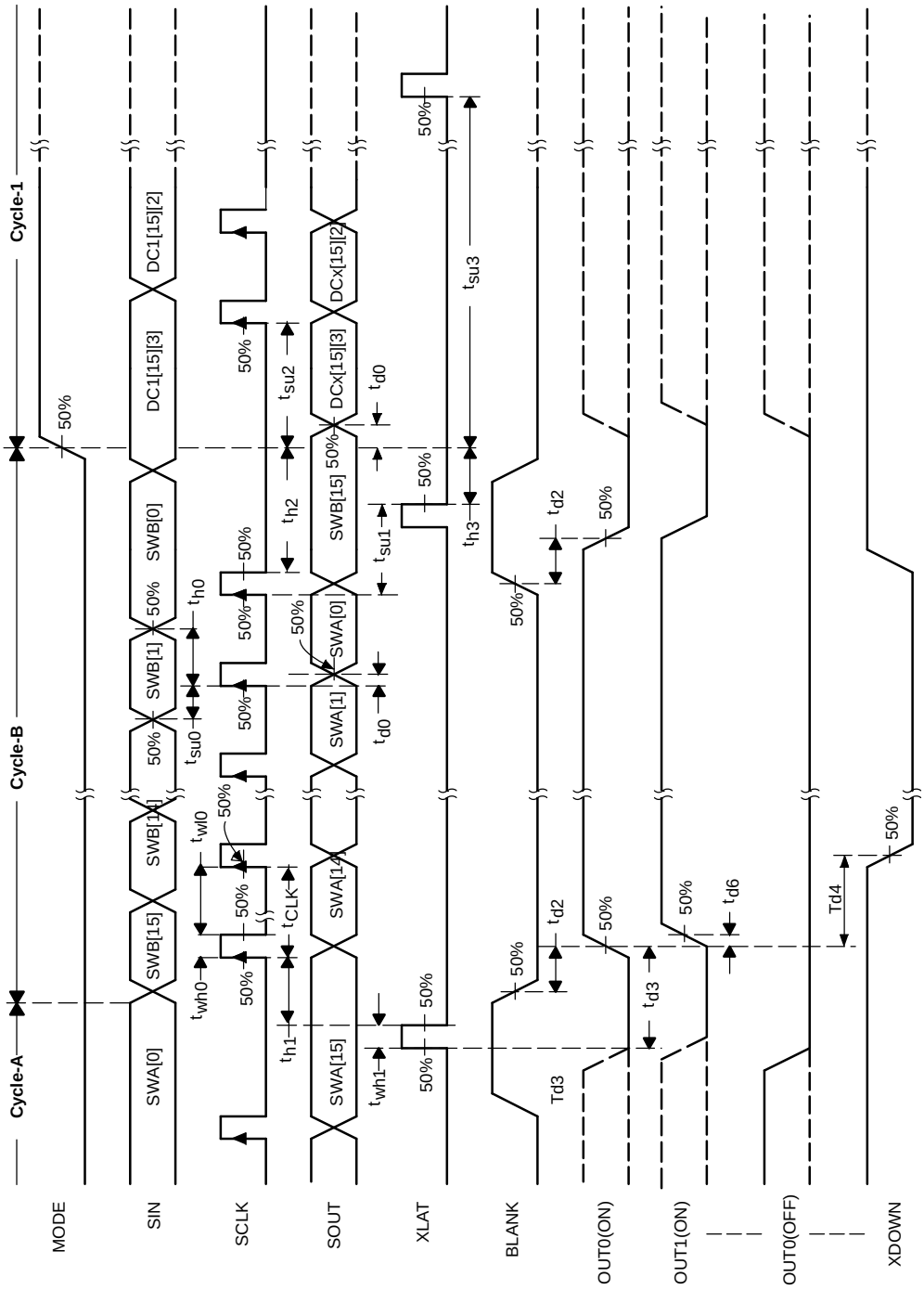


Figure 9. Timing Chart Example for ON/OFF Setting to Dot-Correction

PRINCIPLES OF OPERATION (continued)

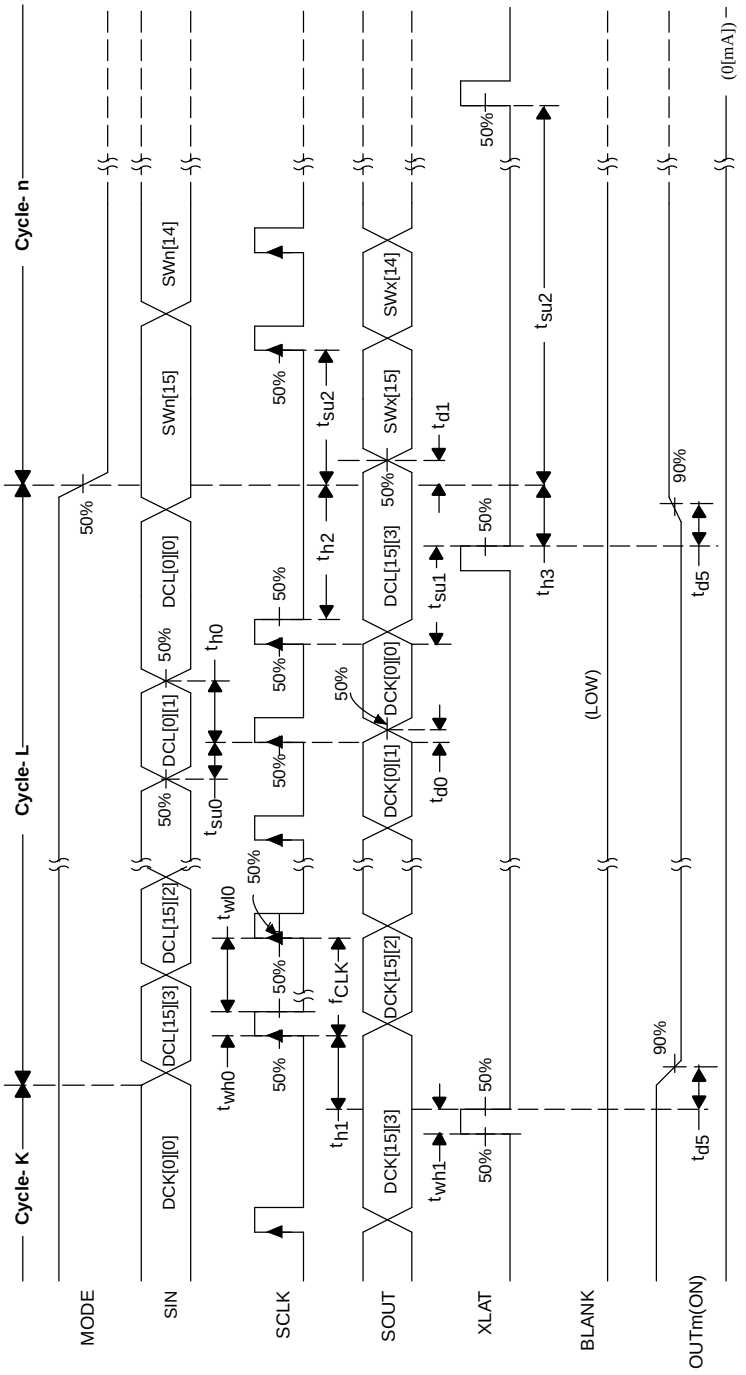


Figure 10. Timing Chart Example for Dot-Correction to ON/OFF Setting

PRINCIPLES OF OPERATION (continued)

Power Rating - Free-Air Temperature

Figure 11 shows total power dissipation. Figure 12 shows supply current versus free-air temperature.

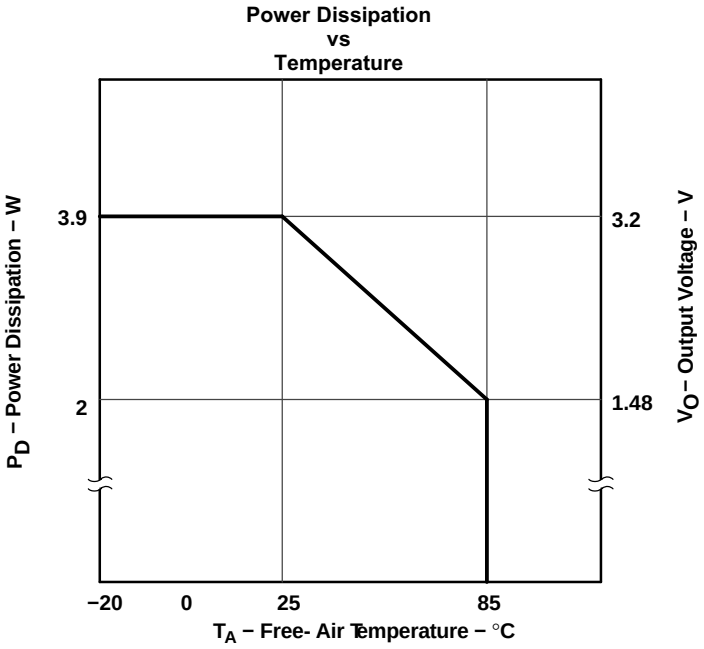
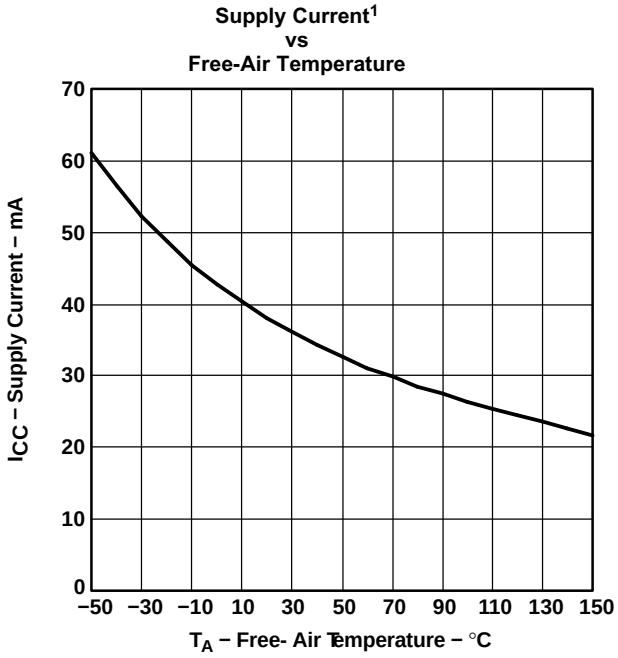


Figure 11



1. Data Transfer = 30 MHz / All Outputs, ON/V_O = 1 V / R_{IREF} = 600 Ω / AV_{DD} = 5 V

Figure 12

PRINCIPLES OF OPERATION (continued)

Constant Output Current - Reference Resistor

Figure 13 shows the maximum output current, I_{OLC}, versus $R_{(IREF)}$. In Figure 13, $R_{(IREF)}$ is the value of the resistor between IREF terminal to ground, and I_{OLC} is the constant output current of OUT0,.....OUT15.

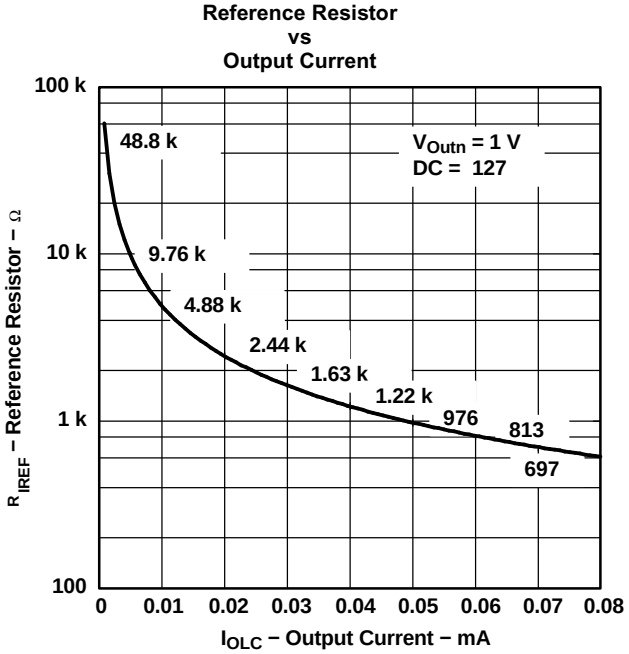
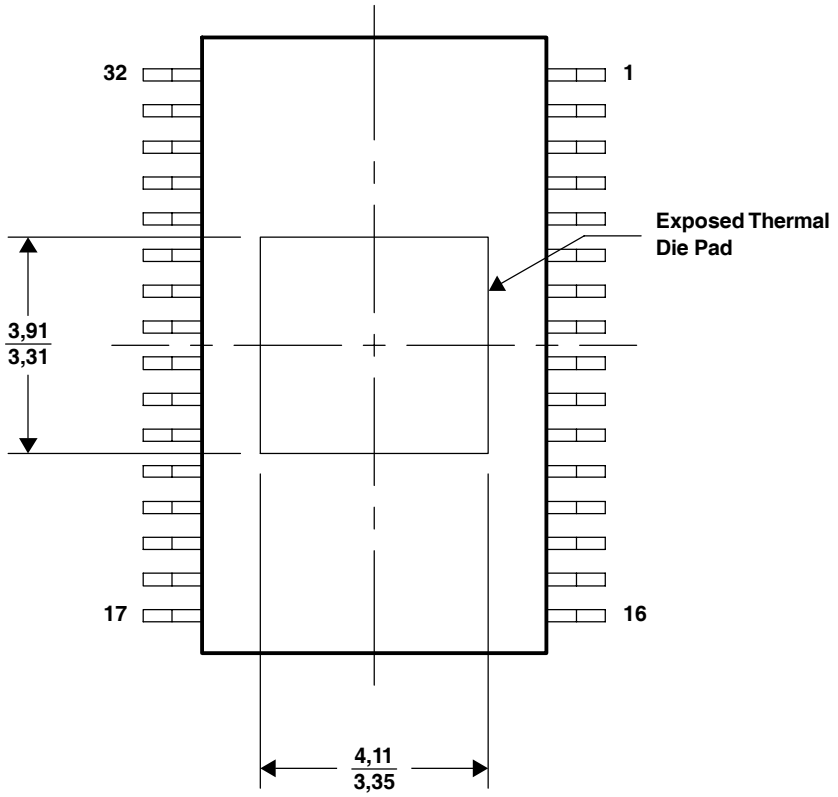


Figure 13

THERMAL INFORMATION

The DAP PowerPAD™ package incorporates an exposed thermal die pad that is designed to be attached directly to an external heat sink. When the thermal die pad is soldered directly to the printed circuit board (PCB), the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal die pad can be attached directly to a ground plane or special heat sink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, *PowerPAD Thermally Enhanced Package*, Texas Instruments Literature No. SLMA002 and Application Brief, *PowerPAD Made Easy*, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com. See Figure 1 for DAP package exposed thermal die pad dimensions.



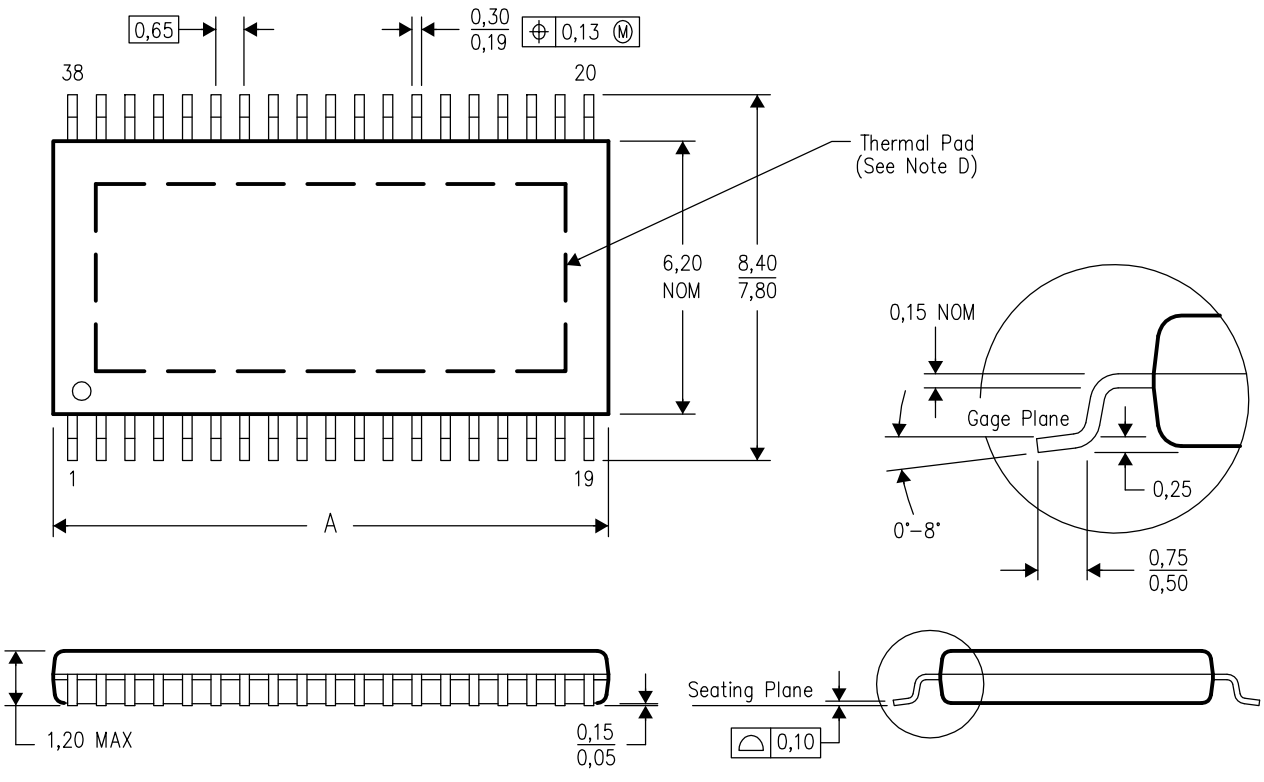
NOTE: All linear dimensions are in millimeters.

Figure 1. DAP Package Exposed Thermal Die Pad Dimensions

PowerPAD is a trademark of Texas Instruments.

DAP (R–PDSO–G**) PowerPAD™ PLASTIC SMALL–OUTLINE PACKAGE

38 PINS SHOWN



DIM \ PINS **	28	30	32	38
A MAX	9,80	11,10	11,10	12,60
A MIN	9,60	10,90	10,90	12,40

4073257/B 08/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. Falls within JEDEC MO–153

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Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265