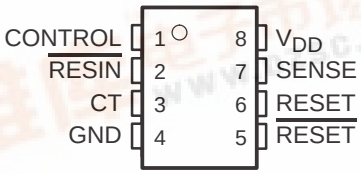
TLC7701-EP, TLC7705-EP, TLC7733-EP
MICROPOWER SUPPLY VOLTAGE SUPERVISORS

SGLS013A – MARCH 2003 – REVISED SEPTEMBER 2003

- **Controlled Baseline**
  - **One Assembly/Test Site, One Fabrication Site**
- **Extended Temperature Performance of −40°C to 125°C**
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product Change Notification**
- **Qualification Pedigree†**
- **Power-On Reset Generator**
- **Automatic Reset Generation After Voltage Drop**
- **Precision Voltage Sensor**
- **Temperature-Compensated Voltage Reference**
- **Programmable Delay Time by External Capacitor**
- **Supply Voltage Range . . . 2 V to 6 V**
- **Defined $\overline{\text{RESET}}$ Output from $V_{DD} \geq 1$ V**
- **Power-Down Control Support for Static RAM With Battery Backup**
- **Maximum Supply Current of 16 μA**
- **Power Saving Totem-Pole Outputs**

† Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

PW PACKAGE
(TOP VIEW)



description

The TLC77xx family of micropower supply voltage supervisors provide reset control, primarily in microcomputer and microprocessor systems.

During power-on, $\overline{\text{RESET}}$ is asserted when V_{DD} reaches 1 V. After minimum V_{DD} (≥ 2 V) is established, the circuit monitors SENSE voltage and keeps the reset outputs active as long as SENSE voltage ($V_{I(SENSE)}$) remains below the threshold voltage. An internal timer delays return of the output to the inactive state to ensure proper system reset. The delay time, t_d, is determined by an external capacitor:

$$t_d = 2.1 \times 10^4 \times C_T$$

Where

C_T is in farads

t_d is in seconds

Except for the TLC7701, which can be customized with two external resistors, each supervisor has a fixed SENSE threshold voltage set by an internal voltage divider. When SENSE voltage drops below the threshold voltage, the outputs become active and stay in that state until SENSE voltage returns above threshold voltage and the delay time, t_d, has expired.

In addition to the power-on-reset and undervoltage-supervisor function, the TLC77xx adds power-down control support for static RAM. When CONTROL is tied to GND, RESET will act as active high. The voltage monitor contains additional logic intended for control of static memories with battery backup during power failure. By driving the chip select ($\overline{\text{CS}}$) of the memory circuit with the RESET output of the TLC77xx and with the CONTROL driven by the memory bank select signal ($\overline{\text{CSH1}}$) of the microprocessor (see Figure 10), the memory circuit is automatically disabled during a power loss. (In this application the TLC77xx power has to be supplied by the battery.)

ORDERING INFORMATION†

T_A	PACKAGE‡		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 125°C	TSSOP − PW	Tape and reel	TLC7701QPWREP	7701QE
	TSSOP − PW	Tape and reel	TLC7705QPWREP	7705QE
	TSSOP − PW	Tape and reel	TLC7733QPWREP	7733QE

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

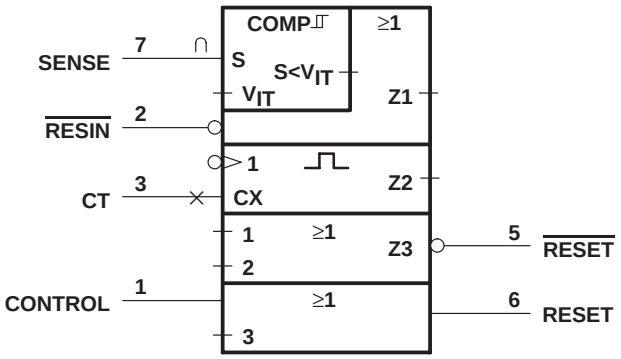
‡ The PW package is only available left-end taped and reeled (indicated by the R suffix on the device type; e.g., TLC7701QPWREP).

FUNCTION TABLE

CONTROL	$\overline{RESIN}$	$V_{I(SENSE)}>V_{IT+}$	RESET	$\overline{RESET}$
L	L	False	H	L
L	L	True	H	L
L	H	False	H	L
L	H	True	L§	H§
H	L	False	H	L
H	L	True	H	L
H	H	False	H	L
H	H	True	H	H§

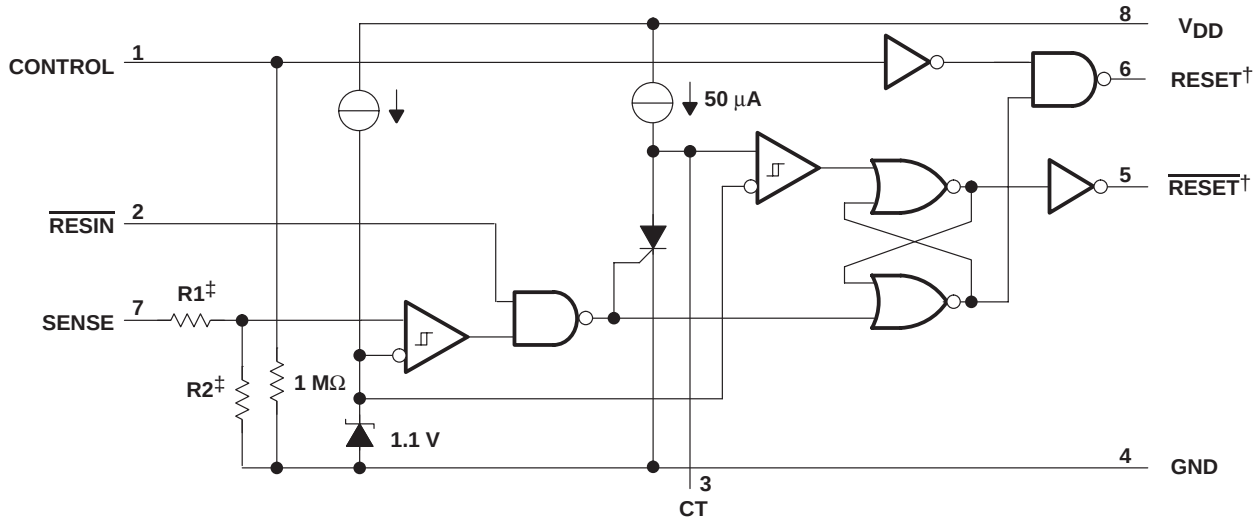
§ RESET and $\overline{RESET}$ states shown are valid for $t > t_d$.

logic symbol¶



¶ This symbol is in accordance with ANSI/IEEE Std 91−1984 and IEC Publication 617-12.

functional block diagram

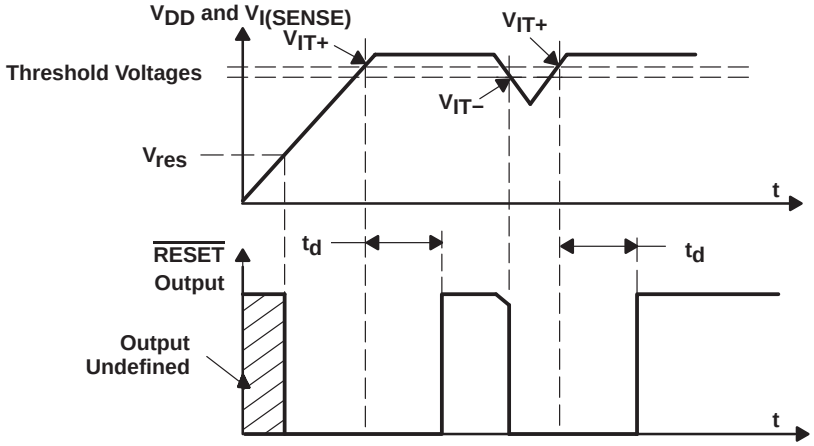


† Outputs are totem-pole configuration. External pullup or pulldown resistors are not required.

‡ Nominal values:

	R1 (Typ)	R2 (Typ)
TLC7701	0	∞
TLC7705	910 kΩ	290 kΩ
TLC7733	750 kΩ	450 kΩ

timing diagram



absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1) . . . . . 7 V
Input voltage range, CONTROL, $\overline{RESIN}$, SENSE (see Note 1) . . . . . −0.3 V to 7 V
Maximum low output current, I_{OL} . . . . . 10 mA
Maximum high output current, I_{OH} . . . . . −10 mA
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{DD}$) . . . . . ±10 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{DD}$) . . . . . ±10 mA
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A: TL77xxQ . . . . . −40°C to 125°C
Storage temperature range, T_{stg} . . . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
PW	525 mW	4.2 mW/°C	273 mW	105 mW

recommended operating conditions at specified temperature range

		MIN	MAX	UNIT
Supply voltage, V_{DD}		2	6	V
Input voltage, V_I		0	V_{DD}	V
High-level input voltage at $\overline{RESIN}$ and CONTROL‡, V_{IH}		$0.7 \times V_{DD}$		V
Low-level input voltage at $\overline{RESIN}$ and CONTROL‡, V_{IL}			$0.2 \times V_{DD}$	V
High-level output current, I_{OH}	$V_{DD} \ge 2.7$ V		−2	mA
Low-level output current, I_{OL}	$V_{DD} \ge 2.7$ V		2	mA
Input transition rise and fall rate at $\overline{RESIN}$ and CONTROL, $\Delta t/\Delta V$			100	ns/V
Operating free-air temperature range, T_A		−40	125	°C

‡ To ensure a low supply current, V_{IL} should be kept < 0.3 V and $V_{IH} > V_{DD} - 0.3$ V.

electrical characteristics over recommended operating conditions (see Note 2) (unless otherwise noted)

PARAMETER				TEST CONDITIONS	TLC77xx			UNIT
					MIN	TYP†	MAX	
V_{OH}	High-level output voltage	I_{OH} = −20 µA		V_{DD} = 2 V	1.8			V
				V_{DD} = 2.7 V	2.5			
				V_{DD} = 4.5 V	4.3			
		I_{OH} = −2 mA		V_{DD} = 4.5 V	3.7			
V_{OL}	Low-level output voltage	I_{OL} = 20 µA		V_{DD} = 2 V			0.2	V
				V_{DD} = 2.7 V			0.2	
				V_{DD} = 4.5 V			0.2	
		I_{OL} = 2 mA		V_{DD} = 4.5 V			0.5	
V_{IT-}	Negative-going input threshold voltage, SENSE (see Note 3)		TLC7701	V_{DD} = 2 V to 6 V	1.04	1.1	1.16	V
			TLC7705		4.43	4.5	4.63	
			TLC7733		2.855	2.93	3.03	
V_{hys}	Hysteresis voltage, SENSE		TLC7701	V_{DD} = 2 V to 6 V		30		mV
			TLC7705			70		
			TLC7733					
V_{res}	Power-up reset voltage‡			I_{OL} = 20 µA			1	V
I_I	Input current	$\overline{\text{RESIN}}$		V_I = 0 V to V_{DD}			2	µA
		CONTROL		V_I = V_{DD}		7	15	
		SENSE		V_I = 5 V		5	10	
		SENSE, TLC7701 only		V_I = 5 V			2	
I_{DD}	Supply current			$\overline{\text{RESIN}}$ = V_{DD}, SENSE = V_{DD} ≥ V_{IT}max + 0.2 V, CONTROL = 0 V, Outputs open		9	16	µA
$I_{DD(d)}$	Supply current during t_d			V_{DD} = 5 V, V_{CT} = 0 , $\overline{\text{RESIN}}$ = V_{DD}, SENSE = V_{DD}, CONTROL = 0 V, Outputs open		120	150	µA
C_I	Input capacitance, SENSE			V_I = 0 V to V_{DD}		50		pF

† Typical values apply at T_A = 25°C.

‡ The lowest supply voltage at which $\overline{\text{RESET}}$ becomes active. The symbol V_{res} is not currently listed within EIA or JEDEC standards for semiconductor symbology. Rise time of V_{DD} ≥ 15 µs/V.

NOTES: 2. All characteristics are measured with C_T = 0.1 µF.

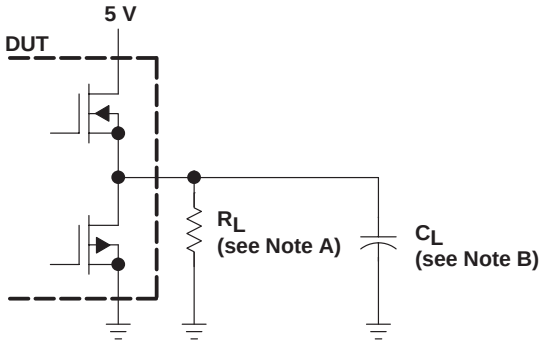
3. To ensure best stability of the threshold voltage, a bypass capacitor (ceramic, 0.1 µF) should be connected near the supply terminals.

switching characteristics at V_{DD} = 5 V, R_L = 2 kΩ, C_L = 50 pF, T_A = Full Range (unless otherwise noted)

PARAMETER		MEASURED		TEST CONDITIONS	TLC77xx			UNIT
		FROM (INPUT)	TO (OUTPUT)		MIN	TYP	MAX	
t_d	Delay time	$V_{I(SENSE)} \geq V_{IT+}$	RESET and $\overline{\text{RESET}}$	$\overline{\text{RESIN}} = 0.7 \times V_{DD}$, CONTROL = $0.2 \times V_{DD}$, C_T = 100 nF, T_A = Full range, See timing diagram	1.1	2.1	4.2	ms
t_{PLH}	Propagation delay time, low-to-high-level output	SENSE	$\overline{\text{RESET}}$	$V_{IH} = V_{IT+}$max + 0.2 V, $V_{IL} = V_{IT-}$min − 0.2 V, $\overline{\text{RESIN}} = 0.7 \times V_{DD}$, CONTROL = $0.2 \times V_{DD}$, CT = NC†			20	µs
t_{PHL}	Propagation delay time, high-to-low-level output						5	
t_{PLH}	Propagation delay time, low-to-high-level output		RESET				5	
t_{PHL}	Propagation delay time, high-to-low-level output						20	
t_{PLH}	Propagation delay time, low-to-high-level output	$\overline{\text{RESIN}}$	$\overline{\text{RESET}}$	$V_{IH} = 0.7 \times V_{DD}$, $V_{IL} = 0.2 \times V_{DD}$, SENSE = V_{IT+}max + 0.2 V, CONTROL = $0.2 \times V_{DD}$, CT = NC†			20	µs
t_{PHL}	Propagation delay time, high-to-low-level output						60	ns
t_{PLH}	Propagation delay time, low-to-high-level output		RESET				65	ns
t_{PHL}	Propagation delay time, high-to-low-level output						20	µs
t_{PLH}	Propagation delay time, low-to-high-level output	CONTROL	RESET	$V_{IH} = 0.7 \times V_{DD}$, $V_{IL} = 0.2 \times V_{DD}$, SENSE = V_{IT+}max + 0.2 V, $\overline{\text{RESIN}} = 0.7 \times V_{DD}$, CT = NC†			58	ns
t_{PHL}	Propagation delay time, high-to-low-level output						58	ns
	Low-level minimum pulse duration to switch RESET and $\overline{\text{RESET}}$	SENSE		$V_{IH} = V_{IT+}$max + 0.2 V, $V_{IL} = V_{IT-}$min − 0.2 V,	3			µs
		$\overline{\text{RESIN}}$		$V_{IL} = 0.2 \times V_{DD}$, $V_{IH} = 0.7 \times V_{DD}$	1			
t_r	Rise time		RESET and $\overline{\text{RESET}}$	10% to 90%		8		ns/V
t_f	Fall time			90% to 10%		4		

† NC = No capacitor, and includes up to 100-pF probe and jig capacitance.

PARAMETER MEASUREMENT INFORMATION



NOTES: A. For switching characteristics, R_L = 2 kΩ.
B. C_L = 50 pF includes jig and probe capacitance.

Figure 1. RESET AND $\overline{\text{RESET}}$ Output Configurations

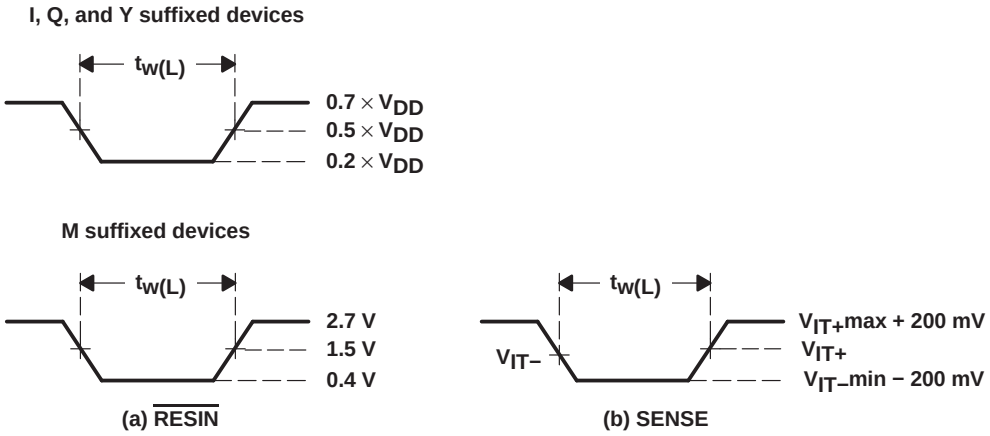


Figure 2. Input Pulse Definition Waveforms

TYPICAL CHARACTERISTICS

NORMALIZED INPUT THRESHOLD VOLTAGE vs TEMPERATURE

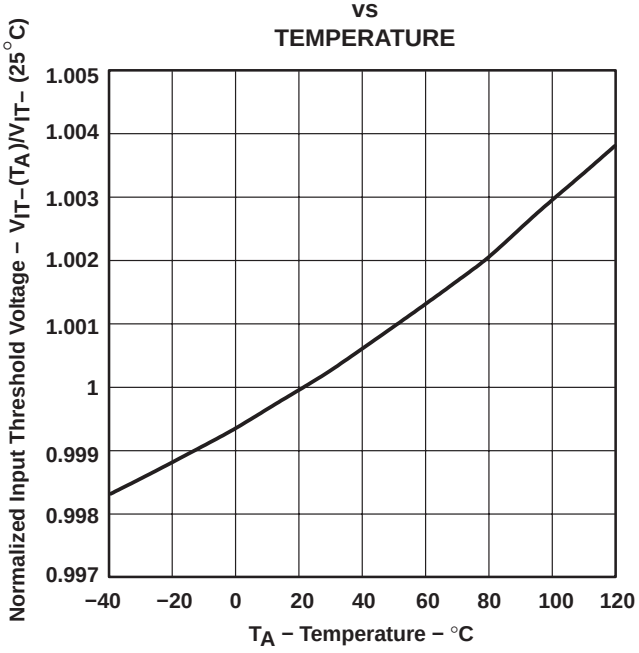


Figure 3

SUPPLY CURRENT vs SUPPLY VOLTAGE

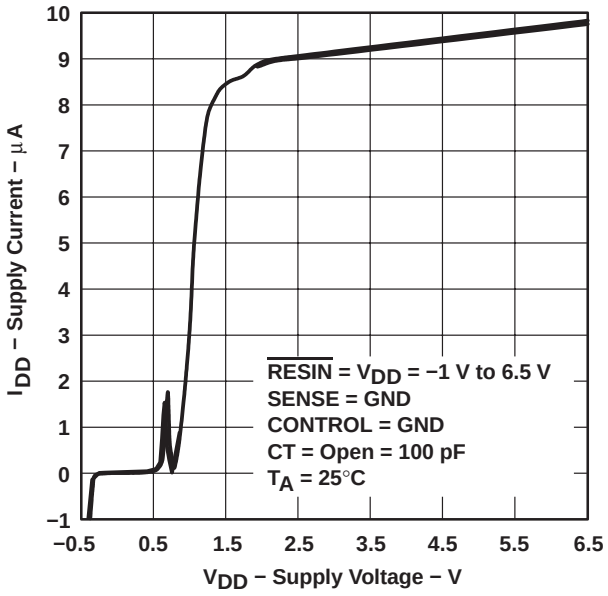


Figure 4

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

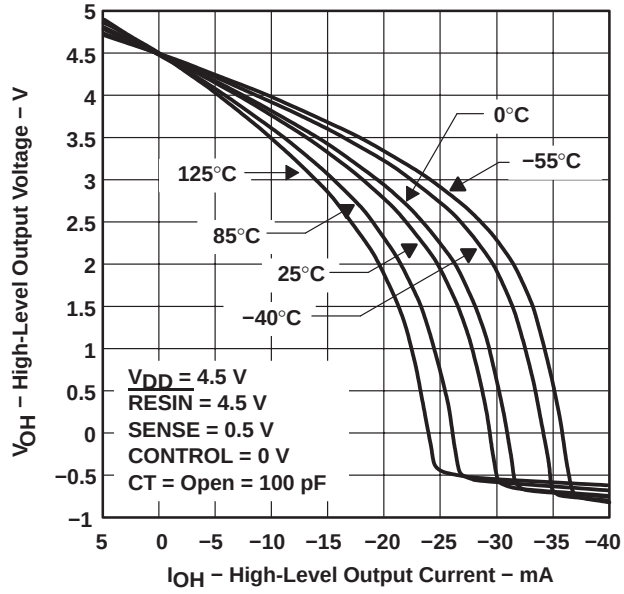


Figure 5

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

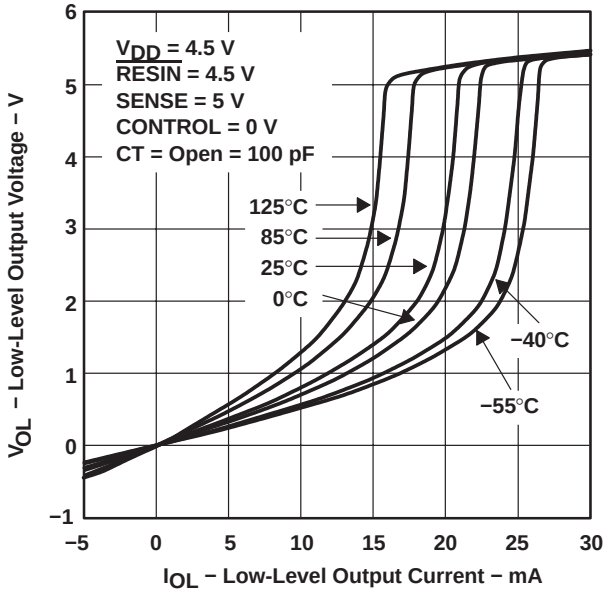


Figure 6

TYPICAL CHARACTERISTICS

INPUT CURRENT vs INPUT VOLTAGE AT SENSE

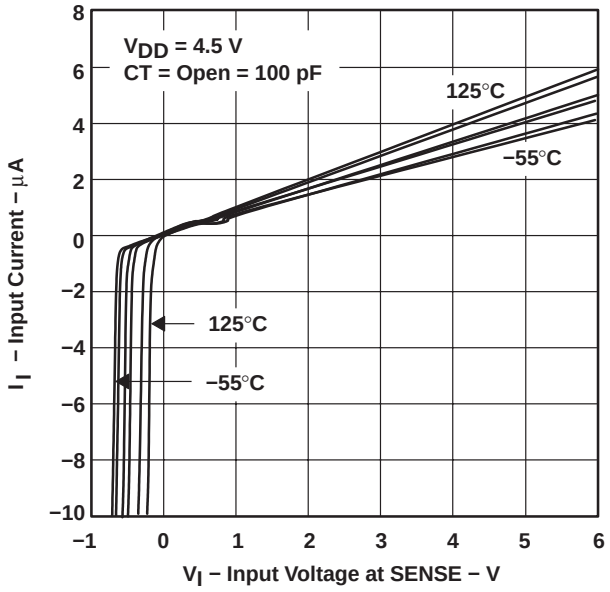


Figure 7

MINIMUM PULSE DURATION AT SENSE vs SENSE THRESHOLD OVERDRIVE

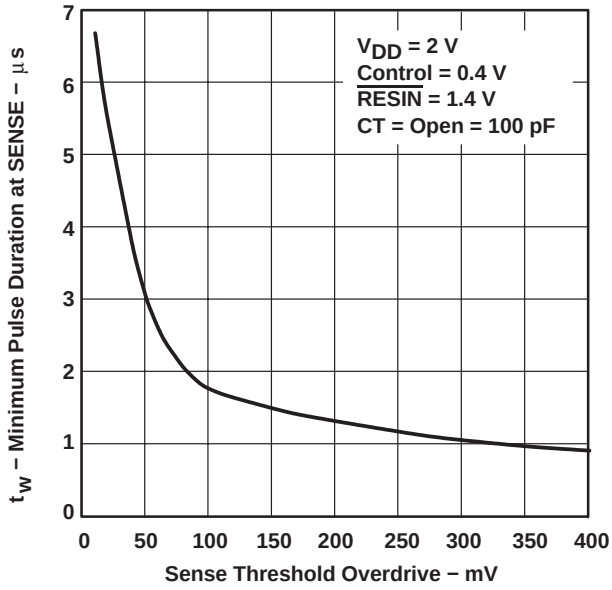


Figure 8

APPLICATION INFORMATION

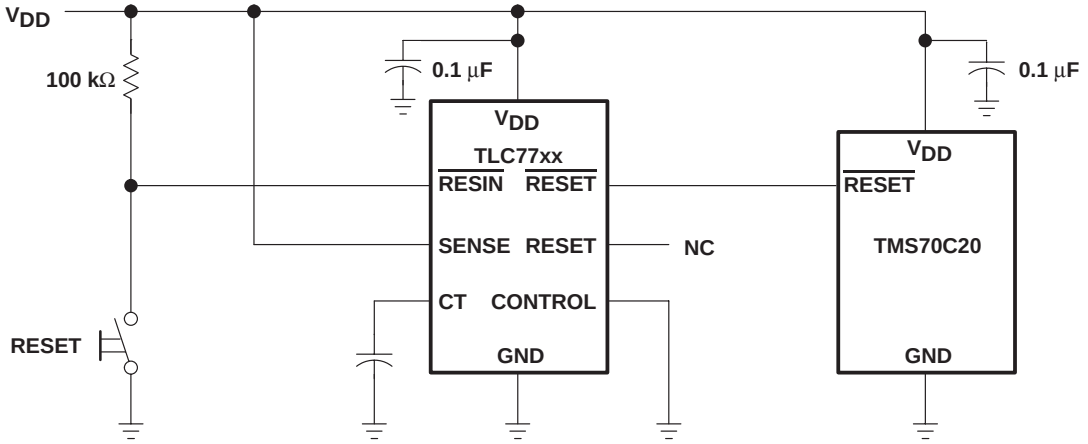


Figure 9. Reset Controller in a Microcomputer System

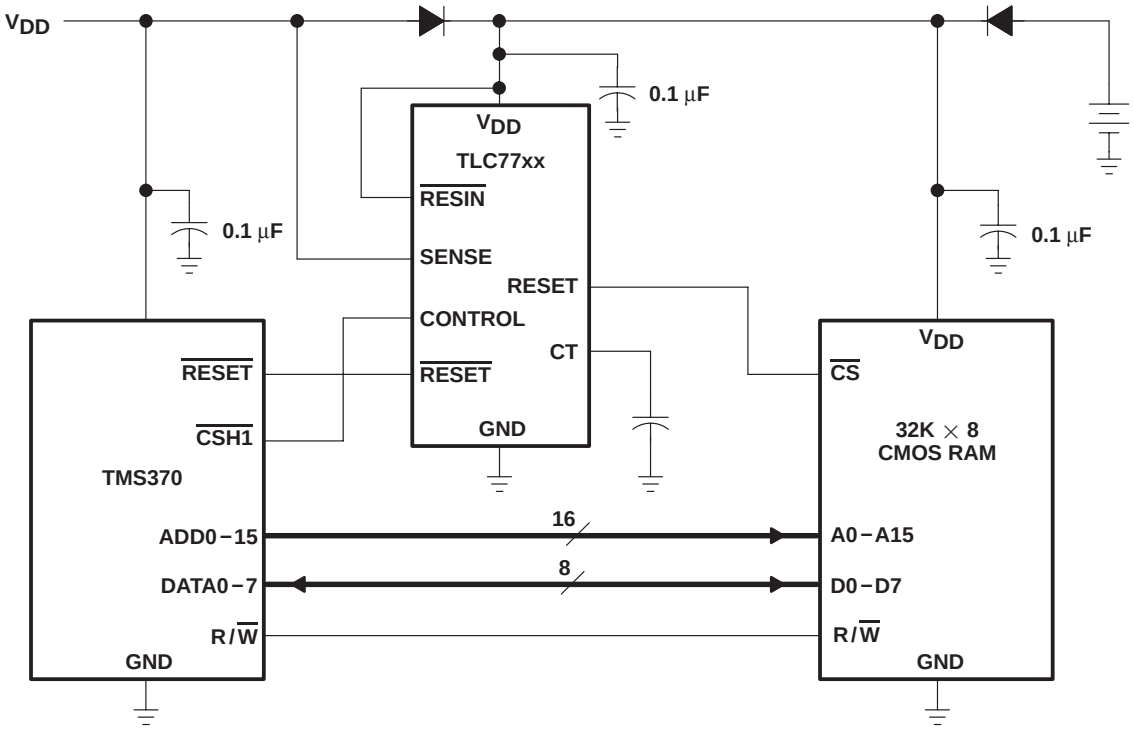
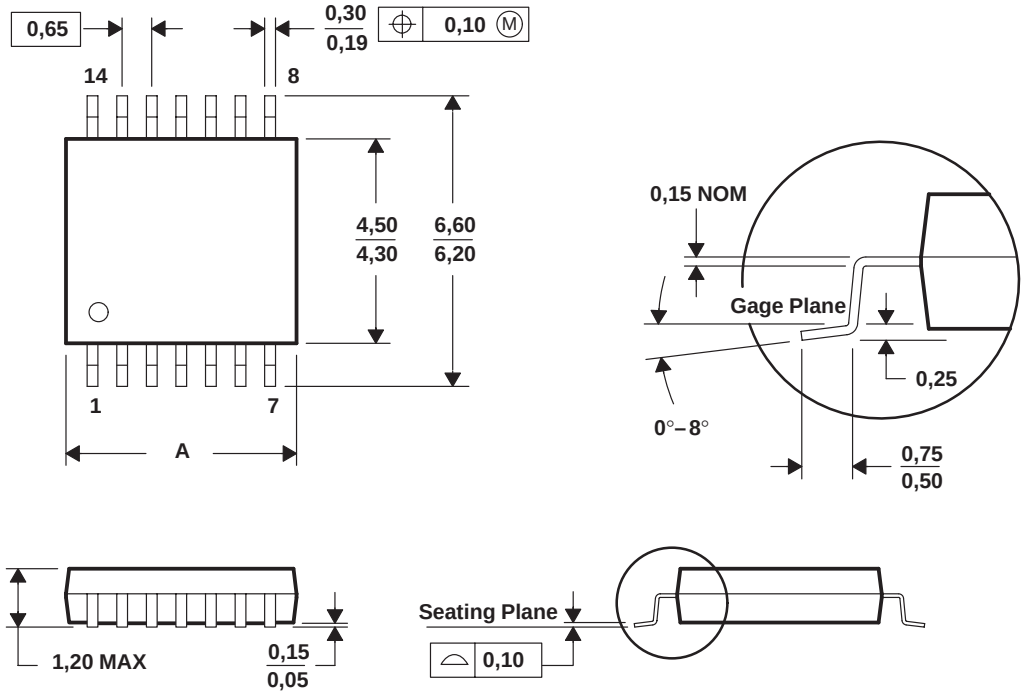


Figure 10. Data Retention During Power Down Using Static CMOS RAMs

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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