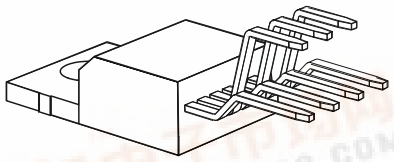
SIEMENS

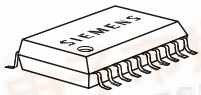
5-V Low-Drop Voltage Regulator TLE 4261-2

Features

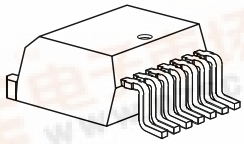
- High accuracy 5 V ± 2%
- Very low-drop voltage
- Very low quiescent current
- Low starting-current consumption
- Proof against reverse polarity
- Input voltage up to 42 V
- Overvoltage protection up to 65 V (≤ 400 ms)
- Short-circuit-proof
- External setting of reset delay
- Integrated watchdog circuit
- Wide temperature range
- Overtemperature protection
- Suitable for automotive use
- EMC proofed (100 V/m)



P-TO220-7-1



P-DSO-20-6



P-TO220-7-8

	Type	Ordering Code	Package
▼	TLE 4261-2	Q67000-A9110	P-TO220-7-1
▼	TLE 4261-2 G	Q67000-A9140	P-DSO-20-6 (SMD)
▼	TLE 4261-2 GL	Q67006-A9193	P-TO220-7-8 (SMD)

▼ Please also refer to the new pin compatible device TLE 4271

Functional Description

TLE 4261-2 is a high accuracy 5-V low-drop voltage regulator in a P-TO220-7 or in a P-DSO package. The maximum input voltage is 42 V (65 V/≤ 400 ms). The device can produce an output current of more than 500 mA. It is short-circuit-proof and incorporates temperature protection that disables the circuit at impermissibly high temperatures.

Application Description

The IC regulates an input voltage V_I in the range 6 V < V_I < 40 V to V_{Qrated} = 5.0 V. A reset signal is generated for an output voltage V_O of < 4.75 V. The reset delay can be set with an external capacitor. A connected microprocessor is monitored by the integrated watchdog circuit; if pulses are missing, the reset output is set low. The pulse repetition rate can be set within wide limits with the capacitor for reset delay. If this input is connected to a voltage of > 6 V, the watchdog function is deactivated. The device also features an inhibit input, which is activated by a voltage of > 6 V and then works on this input through internal hysteresis up to approx. 3 V. A voltage of < 2 V on the inhibit input turns off the regulator, current drain then dropping to max. 50 µA.

Design Notes for External Components

The input capacitor C_I causes a low-resistant powerline and limits the rise times of the input voltage. The IC is protected against rise times up to 100 V/µs. It is possible to damp the tuned circuit consisting of supply inductance and input capacitance with a resistor of approx. 1 Ω in series to C_I.

The output capacitor maintains the stability of the regulating loop. Stability is guaranteed with a rating of 22 µF min. at an ESR of 3 Ω max. in the operating temperature range.

Circuit Description

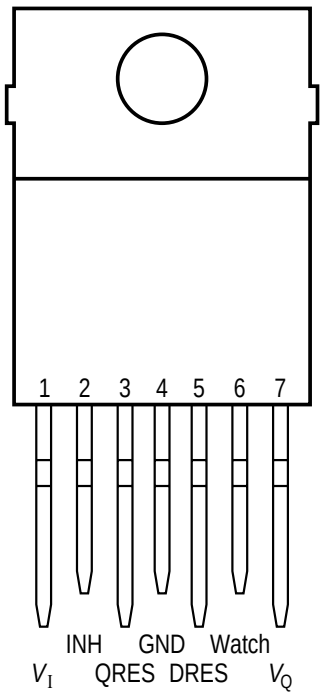
The control amplifier compares a reference voltage, which is kept highly accurate by resistance adjustment, to a voltage that is proportional to the output voltage and controls the base of the series PNP transistor via a buffer. Saturation control as a function of the load current prevents any over-saturation of the power element. If the output voltage drops below 95.5% of its typical value for more than 2 µs, a reset signal is triggered on pin 3 and an external capacitor discharged on pin 5. The reset signal is not cancelled until the voltage on the capacitor has exceeded the upper switching threshold V_{DT}. A positive-edge-triggered watchdog circuit monitors the connected microprocessor and will likewise trigger a reset if pulses are missing. The IC can be disabled by a low level on the inhibit input and the current consumption drops to < 50 µA.

The IC also incorporates a number of circuits for protection against:

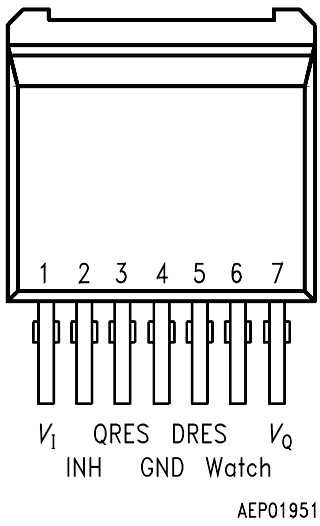
- Overload
- Overvoltage
- Overtemperature
- Reverse polarity

Pin Configuration
(top view)

TLE 4261-2



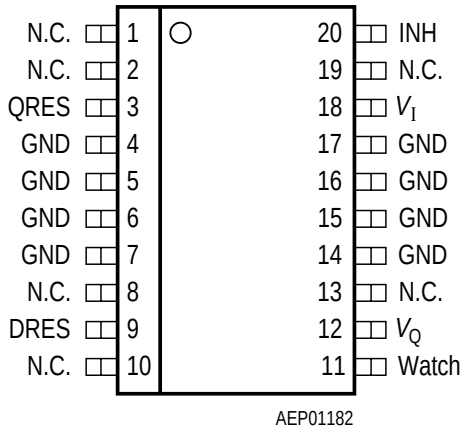
TLE 4261-2 GL



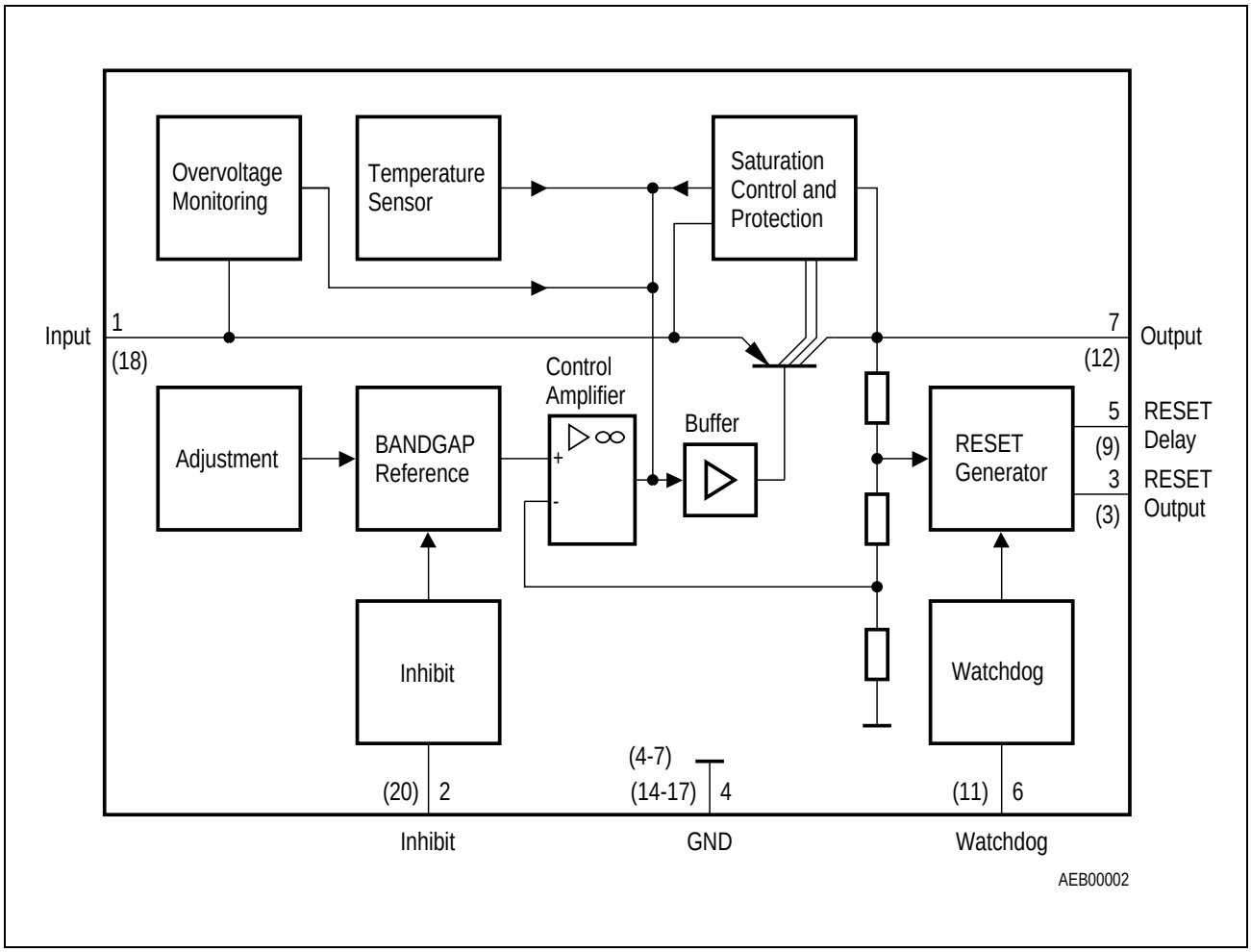
Pin Definitions and Functions

Pin No.	Symbol	Function
1	V_I	**Input voltage**; block a capacitor directly to ground on the IC. The capacitor rating will depend on the vihicle electric system. Oscillation of the output voltage can be damped by a resistor of approx. 1 Ω in series with the input capacitor.
2	INH	**Inhibit**; switches off the IC when low.
3	QRES	**Reset output**; open collector output controlled by the reset delay.
4	GND	**Ground**
5	DRES	**Reset delay**; wired to ground using a capacitor.
6	Watch	**Watchdog**; monitors the microprocessor when active.
7	V_Q	**5-V output**; block to ground using a capacitor of ≥ 22-µF. ESR is ≤ 3 Ω in the operating temperature range.

TLE 4261-2 G



Pin No.	Symbol	Function
18	V_I	**Input voltage**; block a capacitor directly to ground on the IC. The capacitor rating will depend on the vihicle electric system. Oscillation of the output voltage can be damped by a resistor of approx. 1 Ω in series with the input capacitor.
20	INH	**Inhibit**; switches off the IC when low.
3	QRES	**Reset output**; open collector output controlled by the reset delay.
4 -7, 14 - 17	GND	**Ground**
9	DRES	**Reset delay**; wired to ground using a capacitor.
11	Watch	**Watchdog**; monitors the microprocessor when active.
12	V_Q	**5-V output**; block to ground using a capacitor of ≥ 22-µF. ESR is ≤ 3 Ω in the operating temperature range.
1, 2, 8, 10, 13, 19	N.C.	**Not connected**



Block Diagram

Absolute Maximum Ratings
T_J = – 40 to 150 °C

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Input					
Input voltage	V_I	– 42	42	V	–
	V_I	–	65	V	$t \leq 400$ ms
Input current	I_I	–	1.6	A	–
Inhibit					
Voltage	V_2	– 0.3	42	V	–
Current	I_2	–	5	mA	–
Reset Output					
Voltage	V_R	– 0.3	42	V	–
Current	I_R	–	–	–	internally limited
Ground					
Current	I_{GND}	–	0.5	A	–
Reset Delay					
Voltage	V_D	– 0.3	42	V	–
Current	I_D	–	–	–	internally limited
Output					
Differential voltage	$V_I - V_Q$	– 5.25	V_I	V	–
Current	I_Q	–	1.4	A	–

Absolute Maximum Ratings (cont'd)
T_J = – 40 to 150 °C

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Temperature					
Junction temperature	T_j	–	150	°C	–
Storage temperature	T_{stg}	– 50	150	°C	–
Operating Range					
Input voltage	V_I [1)]	–	32	V	–
Junction temperature	T_j	– 40	150	°C	–
Thermal Resistance					
System-air	R_{thSA}	–	65 (70)[2)]	K/W	–
System-case	R_{thSC}	–	3 (15)[2)]	K/W	–

1) see diagram

2) Figures in parenthesis refer to TLE 4261-2 G.

Characteristics

V_I = 13.5 V; T_j = 25 °C; $V_5 \geq$ 6 V (unless otherwise specified)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Normal Operation						
Output voltage	V_Q	4.9	5.0	5.1	V	I_Q = 100 mA – 40 °C ≤ T_j ≤ 125 °C
Output current	I_Q	–	–	50	µA	0 V ≤ V_I ≤ 2 V; V_2 = V_I; – 40 °C ≤ T_j ≤ 125 °C
Output current	I_Q	500	1000	–	mA	V_I = 17 V to 28 V
Current consumption $I_q = I_I - I_Q$	I_q	–	–	3.5	mA	I_Q = 0 mA, V_W >6 V
Current consumption $I_q = I_I - I_Q$	I_q	–	–	10	mA	6 V ≤ V_I ≤ 28 V I_Q = 150 mA
Current consumption $I_q = I_I - I_Q$	I_q	–	5.0	65	mA	6 V ≤ V_I ≤ 28 V I_Q = 500 mA
Current consumption $I_q = I_I - I_Q$	I_q	–	40	80	mA	V_I ≤ 6 V I_Q = 500 mA
Drop voltage	V_{DR}	–	0.35	0.5	V	V_I = 4.5 V; I_Q = 0.5 A
Drop voltage	V_{DR}	–	0.2	0.3	V	V_I = 4.5 V; I_Q = 0.15 A
Load regulation	ΔV_Q	–	15	35	mV	25 mA ≤ I_Q ≤ 500 mA
Supply-voltage regulation	ΔV_Q	–	15	50	mV	V_I ≤ 6 V to 28 V; I_Q = 100 mA
Supply-voltage regulation	ΔV_Q	–	5	25	mV	V_I ≤ 6 V to 16 V; I_Q = 100 mA
Ripple rejection	SVR	–	54	–	dB	f = 100 Hz; V_r = 0.5 V_{SS}
Temperature drift of output voltage	α_{VQ}	–	2×10^{-4}	–	1/°C	–

Characteristics (cont'd)

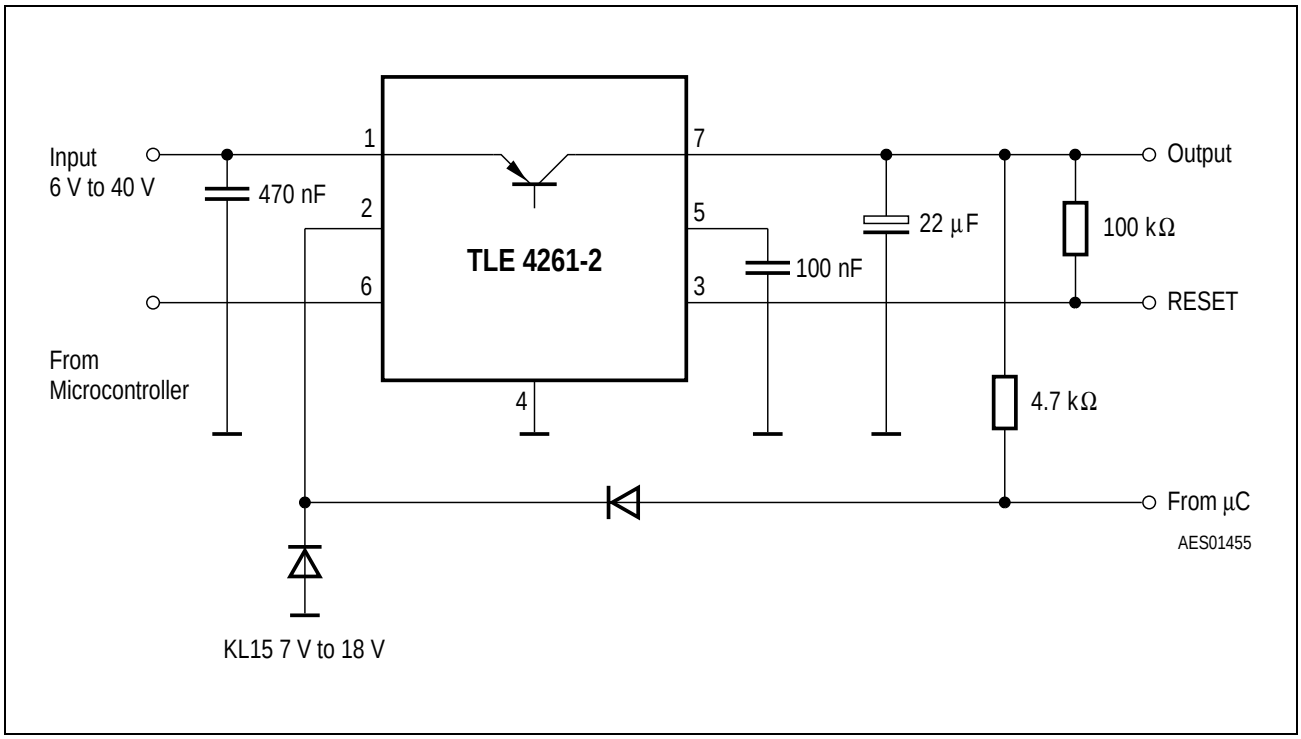
V_I = 13.5 V; T_j = 25 °C; $V_5 \geq$ 6 V (unless otherwise specified)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Inhibit Operation						
Current consumption	I_1	–	–	50	µA	V_2 = 2 V; I_Q = 0
Current consumption	I_2	–	–	100	µA	V_2 = 6 V
Switching threshold for inhibit	V_2	5.0	5.5	6.0	V	IC turned ON
Switching threshold for inhibit	V_2	2.0	2.7	3.7	V	IC turned OFF
Reset Generator						
Switching threshold	V_{RT}	94	95.5	97	%	in % of V_Q; I_Q > 500 mA; V_I = 6 V
Saturation voltage, reset output	V_R	–	0.25	0.40	V	I_R = 1 mA
Reverse current	I_R	–	–	1	µA	V_R = 5 V
Charge current	I_D	18.75	25	31.25	µA	V_C = 1.5 V
Switching threshold	V_{ST}	0.9	1	1.1	V	–
Delay switching threshold	V_{DT}	2.25	2.50	2.75	V	–
Saturation voltage, delay output	V_C	–	–	100	mV	V_I = 4.5 V and I_d
Delay time	t_D	–	10	–	ms	C_D = 100 nF
Delay time	t_t	–	2	–	µs	–

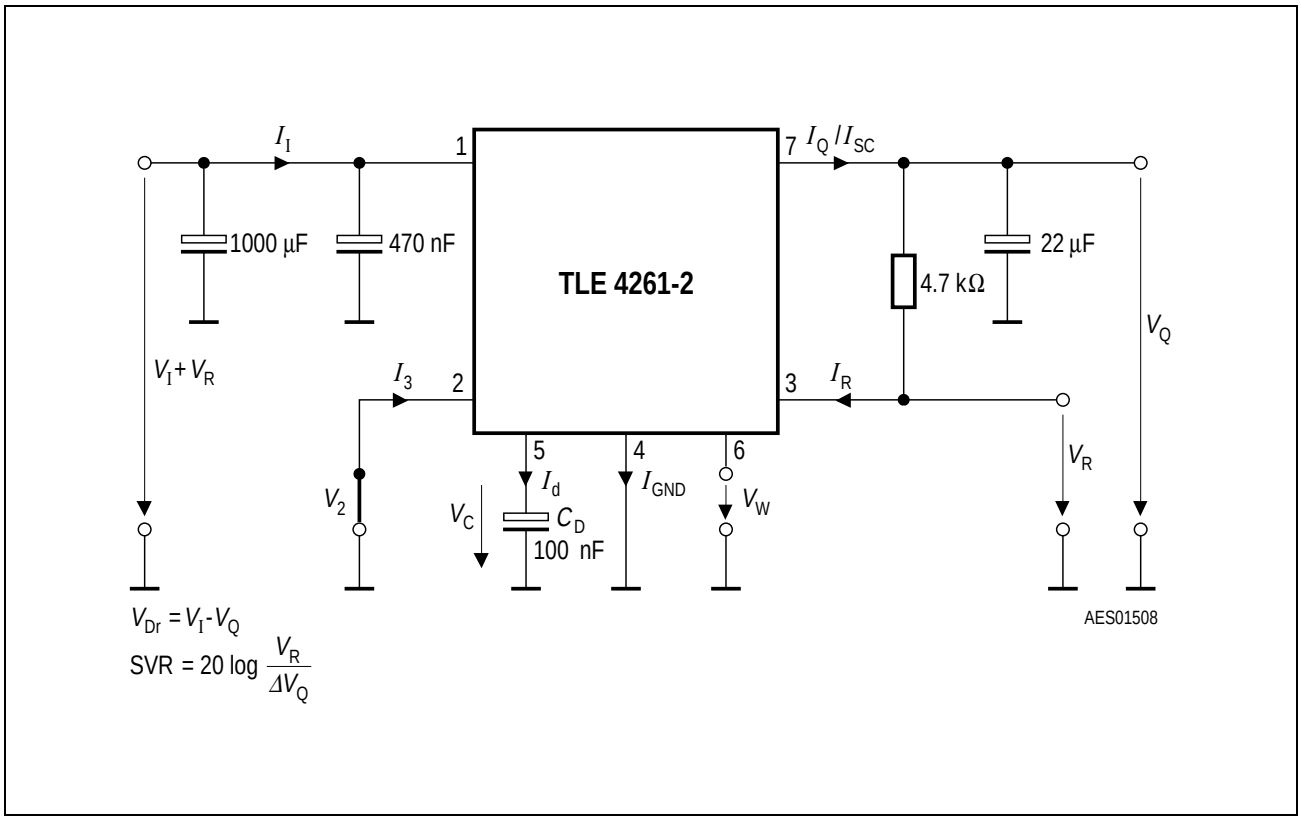
Characteristics (cont'd)

V_I = 13.5 V; T_j = 25 °C; $V_5 \geq$ 6 V (unless otherwise specified)

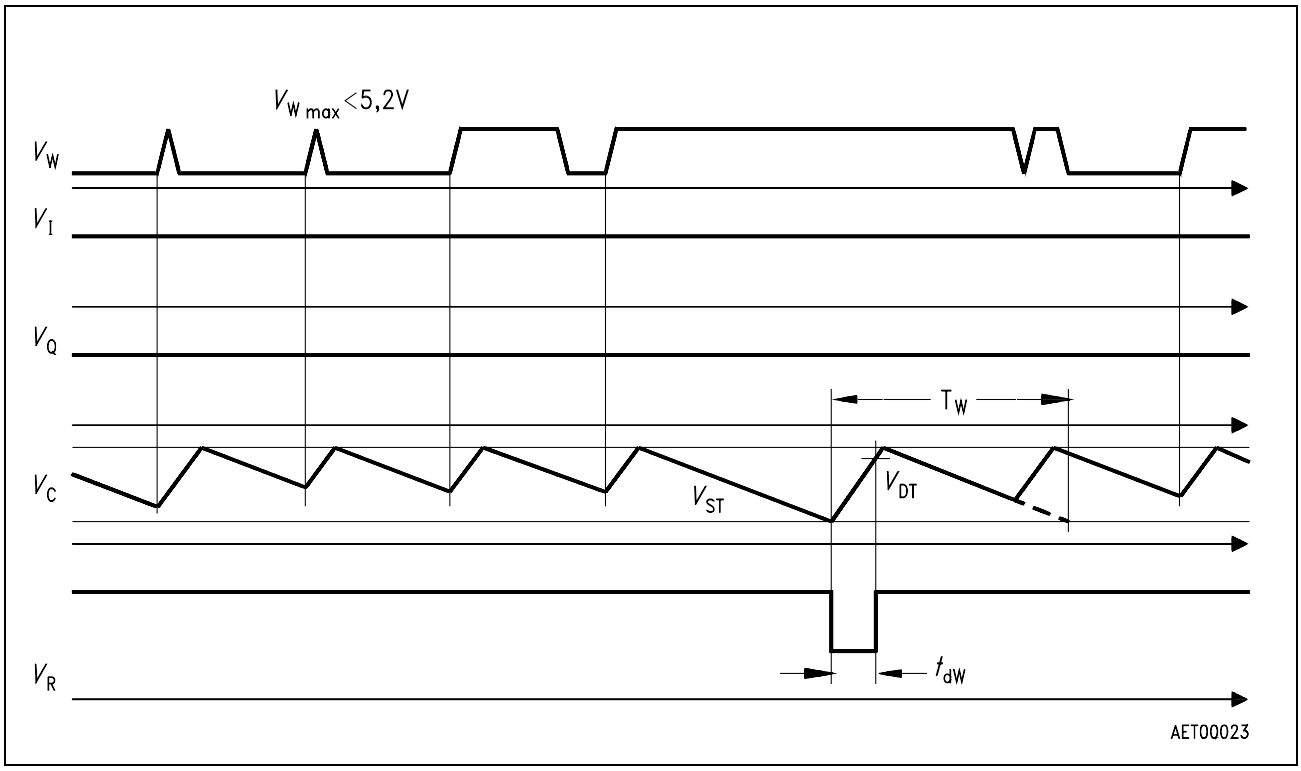
Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Watchdog						
Turn-OFF voltage	V_W	5.2	5.6	6.0	V	–
Discharge current	I_{CD}	5.6	7.5	9.4	µA	V_C = 1.5 V
Switching voltage	V_{CD}	2.95	3.05	3.15	V	–
Pulse intervall	T_W	–	35	–	ms	C_D = 100 nF
General Data						
Turn-Off voltage	V_{IOFF}	41	43	45	V	I_Q < 1 mA
Turn-Off hysteresis	ΔV_I	–	6.5	–	V	–
Leakage current	I_{QS}	–	–	50	µA	V_Q = 0 V; V_I = 45 V
Reverse output current	I_{QR}	–	–	1.5	mA	V_Q = 5 V; V_I and V_2 open



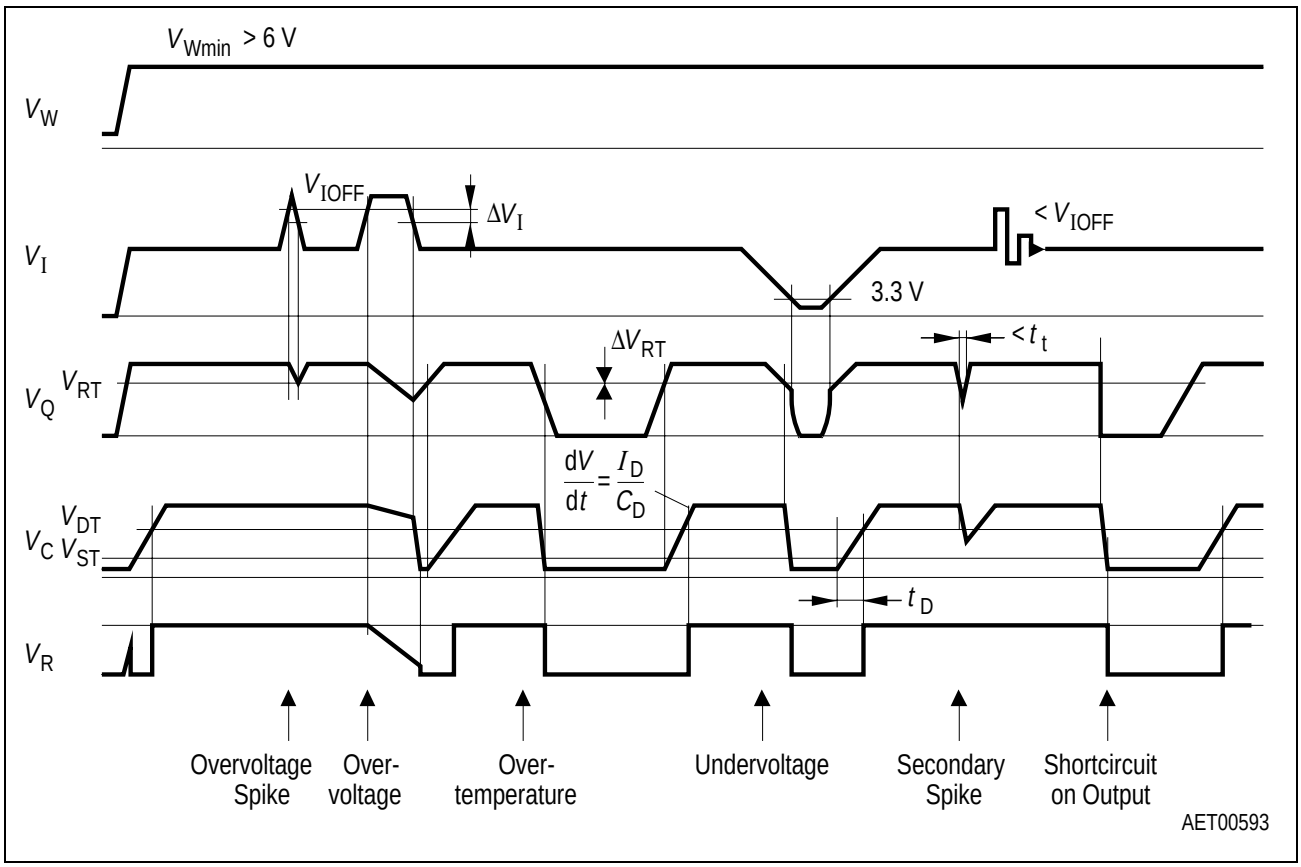
Application Circuit



Test Circuit

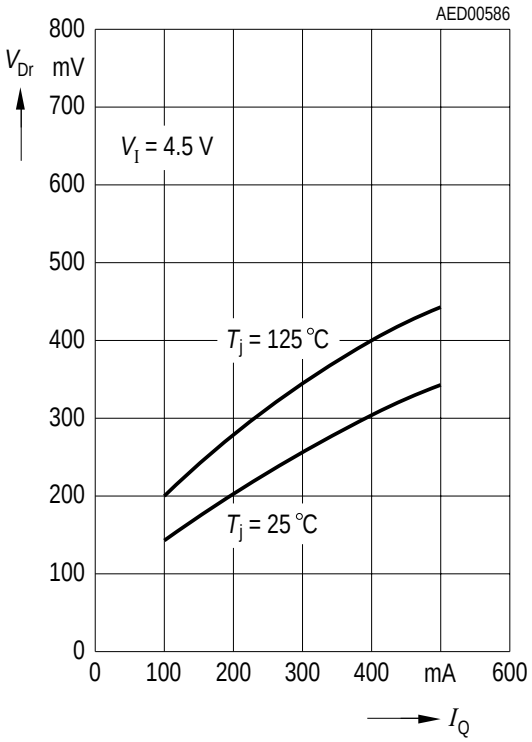


Time Responce in Watchdog Condition

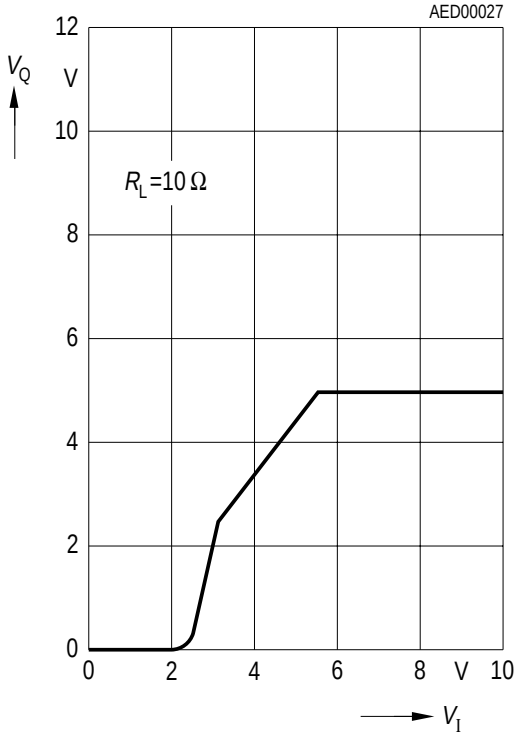


Timing with Watchdog OFF

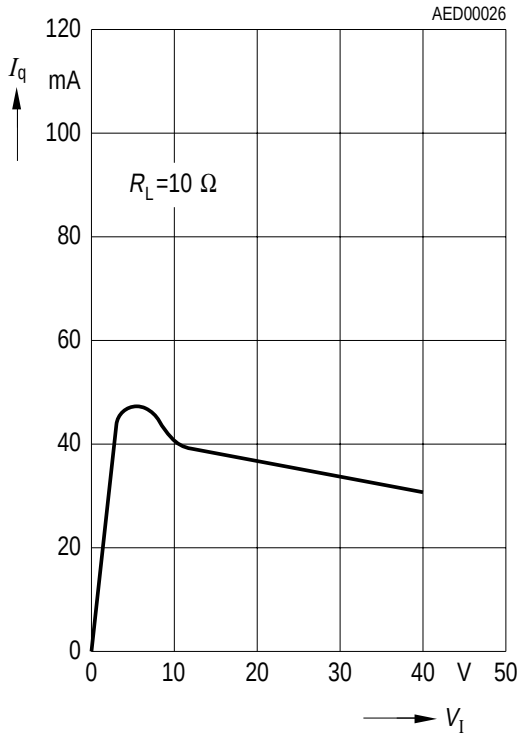
Drop Voltage versus Output Current



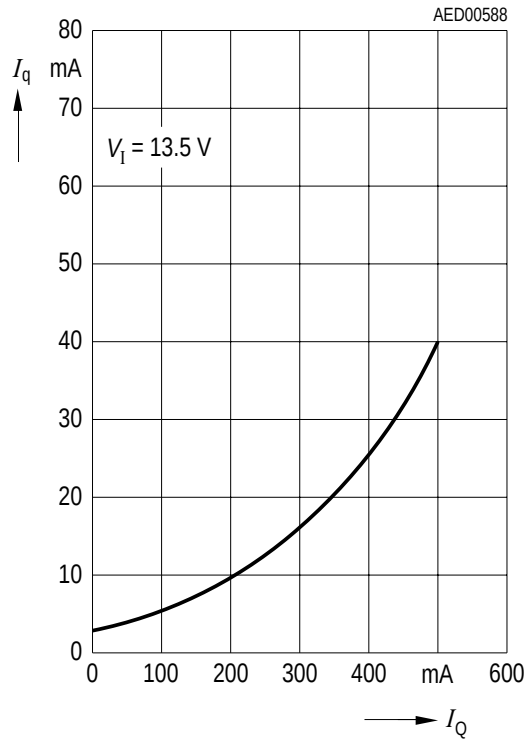
Output Voltage versus Input Voltage



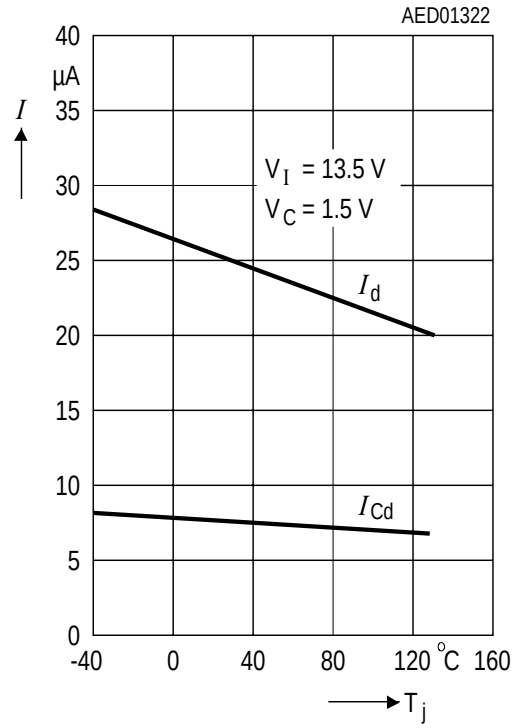
Current Consumption versus Input Voltage



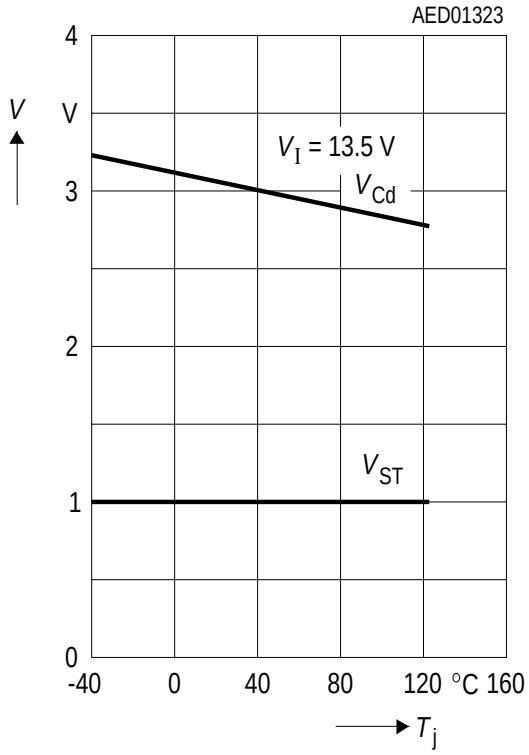
Current Consumption versus Output Current



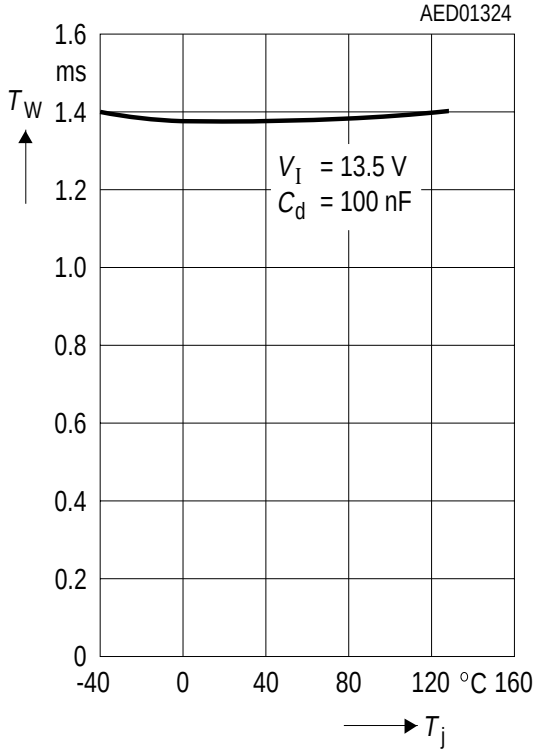
Charge Current I_D and Discharge Current I_{CD} versus Temperature



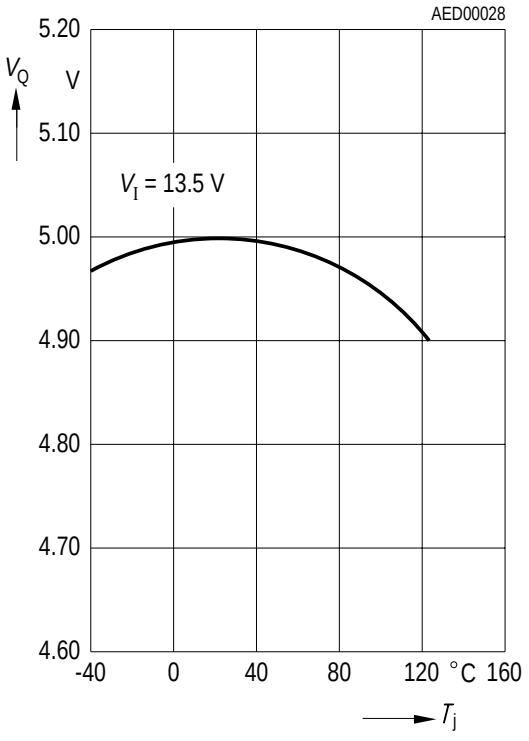
Switching Voltage V_{CD} and V_{ST} versus Temperature



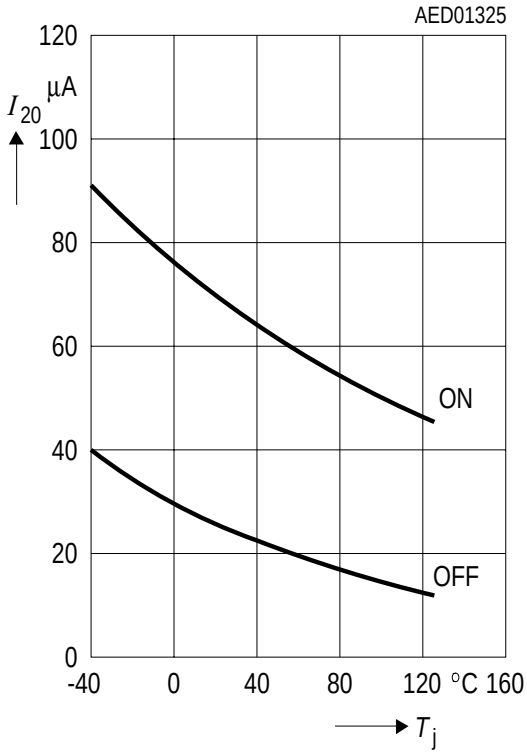
Pulse Interval T_W versus Temperature



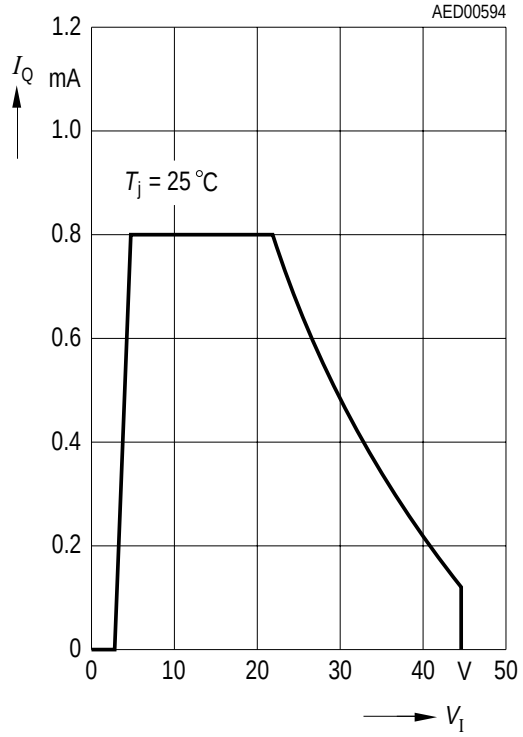
Output Voltage versus Temperature



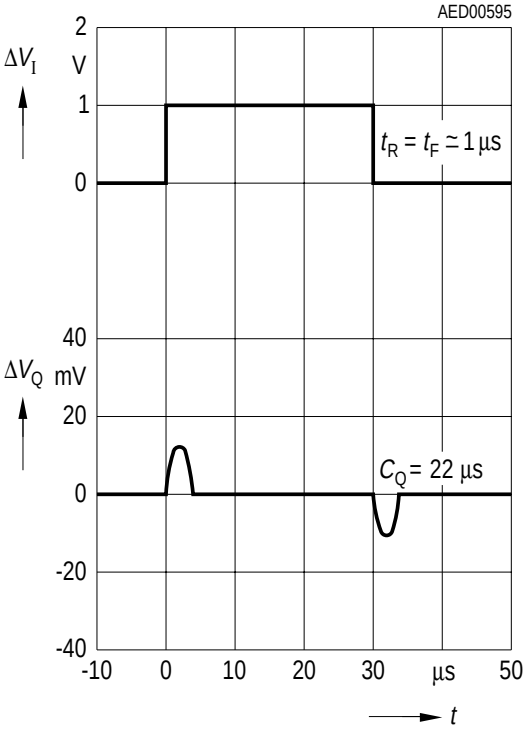
Current Consumption of Inhibit at the Switching Point versus Temperature



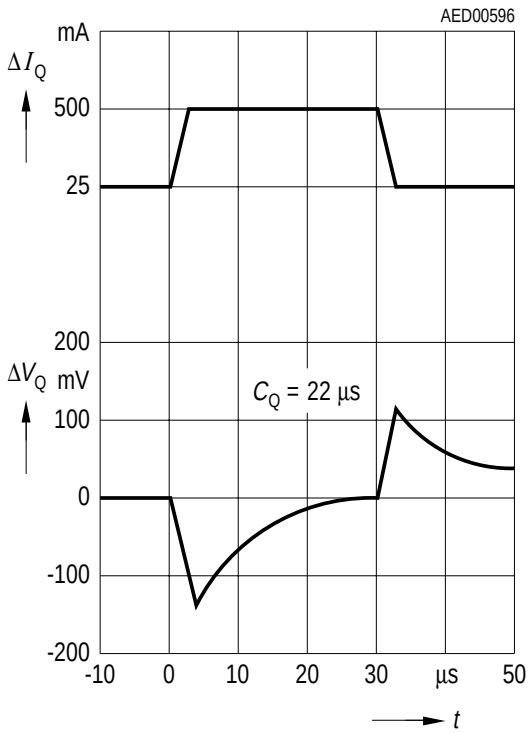
Output Current versus Input Voltage



Input Step Responce



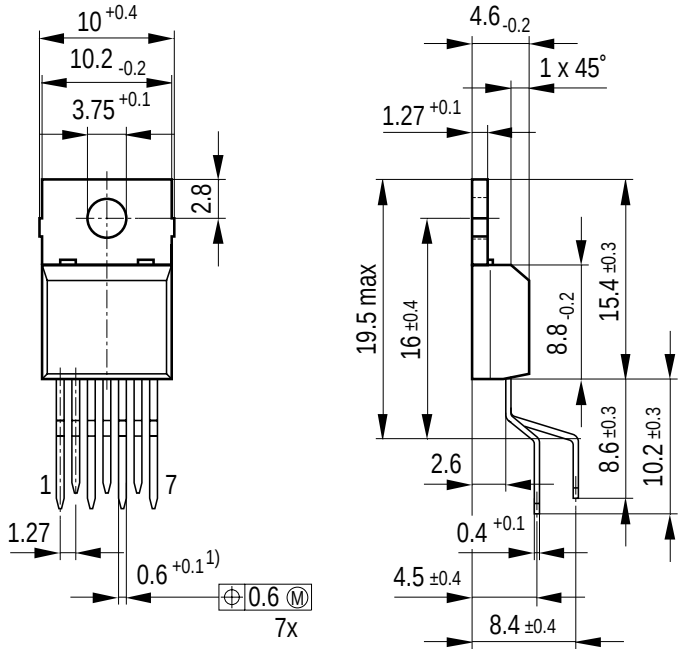
Load Step Responce



Package Outlines

P-TO220-7-1

(Plastic Transistor Single Outline)



1) 0.75 $_{-0.15}$ at dam bar (max 1.8 from body)

1) 0.75 $_{-0.15}$ im Dichtstegbereich (max 1.8 vom Körper)

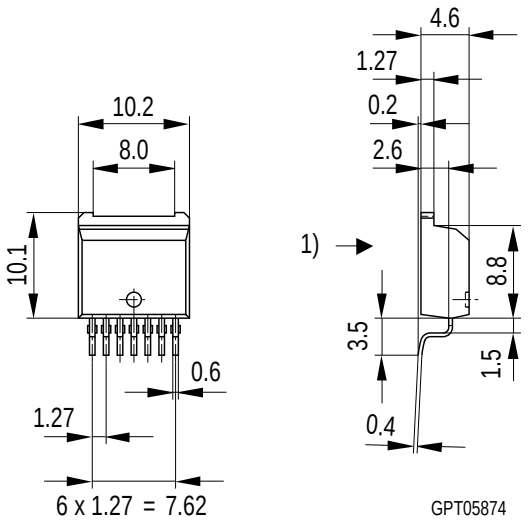
GPT05108

Sorts of Packing

Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”.

Dimensions in mm

P-TO220-7-8
(Plastic Transistor Single Outline)

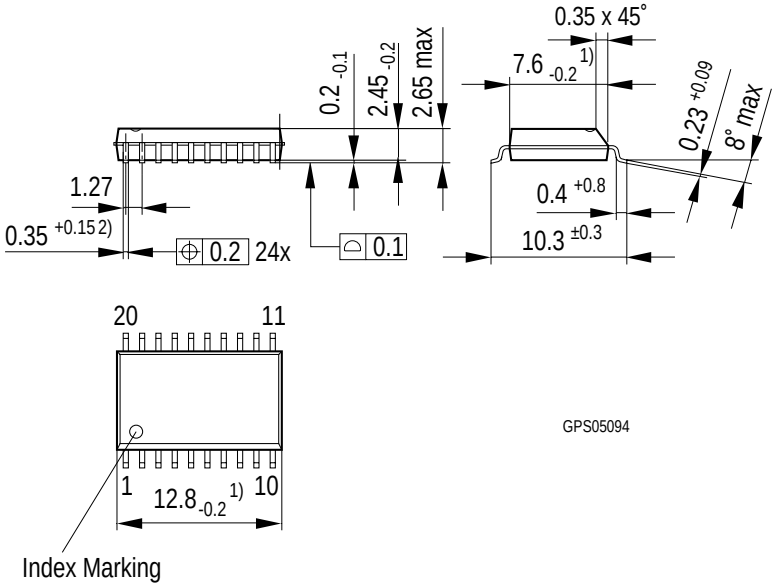


1) shear and punch direction burr free surface

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”.
SMD = Surface Mounted Device

Dimensions in mm

P-DSO-20-6
(Plastic Dual Small Outline)



1) Does not include plastic or metal protrusions of 0.15 max per side
2) Does not include dambar protrusion of 0.05 max per side

Sorts of Packing
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SMD = Surface Mounted Device

Dimensions in mm