Final Datasheet, Version 2.08, 2004-06-07

System Basis Chip TLE 6263

Integrated LS CAN, LDO and HS Switch

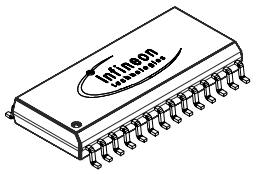
Automotive and Industrial

Infineon technologies

CAN-LDO-ASIC TLE 6263

Final Datasheet

1 Features



P-DSO-28-18
Enhanced Power

- Standard fault tolerant differential CAN-transceiver
- Bus failure management
- Low power mode management
- Receive only mode for CAN
- CAN data transmission rate up to 125 kBaud
- Low-dropout voltage 5V regulator
- High side switch
- 2 wake-up inputs
- Power on and under-voltage reset generator
- Window watchdog
- Fail-safe output
- Early warning feature (V_{CC} warning)
- Sense comparator input (V_{INT} warning)
- Standard 8 bit SPI-interface
- Flash program mode
- Wide input voltage range
- Wide temperature range
- Enhanced power P-DSO-Package

Type	Ordering Code	Package
TLE 6263 G	Q67007-A9465	P-DSO-28-18

2 Description

The TLE 6263 is a monolithic integrated circuit in an enhanced power P-DSO-28-18 package. The IC is optimized for use in advanced automotive electronic control units for body and convenience applications.

To support this applications the TLE 6263 covers the main smart power functions such as failure tolerant low speed CAN-transceiver for differential mode data transmission, low dropout voltage regulator (LDO) for internal and external 5V supply as well as a SPI (serial peripheral interface) to control and monitor the IC. Further there are integrated additional features like a high side switch that can be used e.g. for cyclic supply of an external wake-up circuitry, two wake-up inputs, a window watchdog circuit with fail safe output as well as a reset and early warning feature.

The IC is designed to withstand the severe conditions of automotive applications.

3 Pin Configuration

(top view)

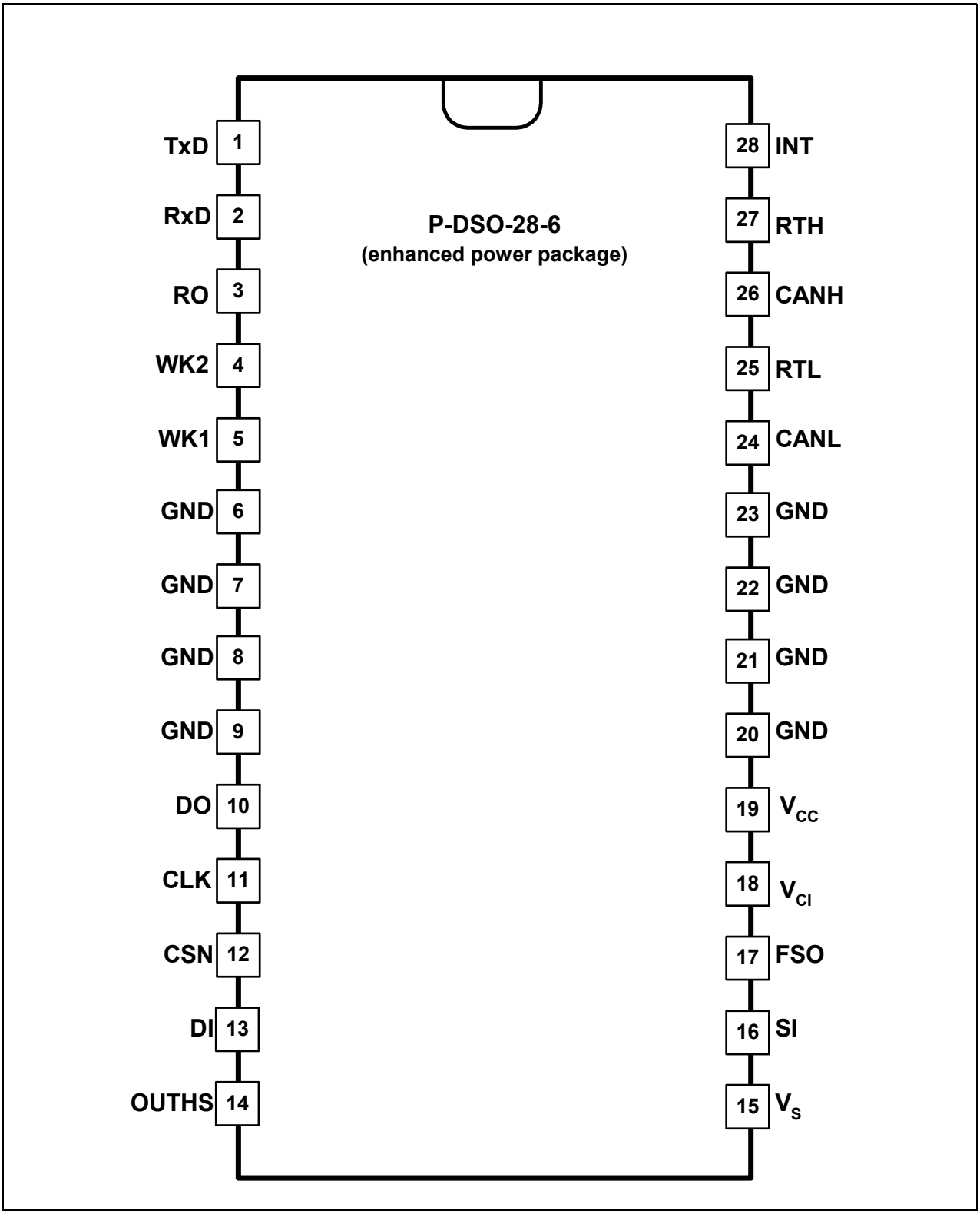


Figure 1: Pin Configuration TLE 6263 G (top view)

4 Pin Definitions and Functions

Pin No.	Symbol	Function
1	TxD	**Transmit data input;** integrated pull up; LOW: bus becomes dominant, HIGH: bus becomes recessive
2	RxD	**Receive data output;** push-pull output; LOW: bus becomes dominant, HIGH: bus becomes recessive
3	RO	**Reset output**; open drain output, integrated pull up, active low
4	WK2	**Wake-Up input 2;** for detection of external wake-up events, edge sensitive, in sleep mode monitored by cyclic sense feature when selected; weak pull up (2µA) to avoid unwanted wake ups
5	WK1	**Wake-Up input 1;** for detection of external wake-up events, edge sensitive, in sleep mode monitored by cyclic sense feature when selected; weak pull up (2µA) to avoid unwanted weak ups
6, 7, 8, 9, 20, 21, 22, 23	GND	**Ground;** to reduce thermal resistance place cooling areas on PCB close to this pins.
10	DO	**SPI data output**; this tri-state output transfers diagnosis data to the control device. Serial data transfered from DO is a 8 bit diagnosis word with the Least Significant Bit (LSB) transmitted first. The output will remain 3-stated unless the device is selected by a LOW on Chip-Select-Not (CSN). DO will accept data on the rising edge of CLK-signal; see **table 4, 5, 6** for Diagnosis protocol
11	CLK	**SPI clock input**; clocks the shiftregister; CLK has a pull down input, active HIGH, and requires CMOS logic level inputs
12	CSN	**SPI chip select not input**; CSN is a pull up input, active LOW, serial communication is enabled by pulling the CSN terminal low; CSN input should only be transitioned when CLK is low; CSN has an internal active pull up and requires CMOS logic level inputs
13	DI	**SPI data input**; receives serial data from the control device; serial data transmitted to DI is a 8 bit control word with the Least Significant Bit (LSB) being transferred first: the input has a pull down input, active HIGH, and requires CMOS logic level inputs; DI will accept data on the falling edge of CLK-signal; see **table 3** for input data protocol
14	OUTHS	**High side switch output;** controlled via SPI, in sleep mode controlled by internal cyclic sense function when selected

4 Pin Definitions and Functions (cont'd)

Pin No.	Symbol	Function
15	V_S	**Power supply input**; block to GND directly at the IC with ceramic capacitor
16	SI	**Sense comparator input;** for monitoring of external voltages, to program the detection level connect external voltage divider
17	FSO	**Fail safe output;** to supervise and control critical applications, high when watchdog is correctly served, LOW at any reset condition, open drain output, internal pull up, active LOW
18	V_{CI}	**Internal voltage supply**; for stabilization of internal power supply, block to GND with an external capacitor $C_{VI} \geq 100$ nF
19	V_{CC}	**Voltage regulator output;** for 5V supply, to stabilize block to GND with an external capacitor $C_Q \geq 100$ nF
24	CANL	**CAN-L bus line;** LOW in dominant state
25	RTL	**CANL-Termination output;** connect to CANL bus line via termination resistor
26	CANH	**CAN-H bus line;** HIGH in dominant state
27	RTH	**CANH-Termination input;** connect to CANH bus line via termination resistor
28	INT	**Interrupt output;** to monitor wake-up events or valid sense input condition; integrated pull up resistor; active LOW

5 Functional Block Diagram

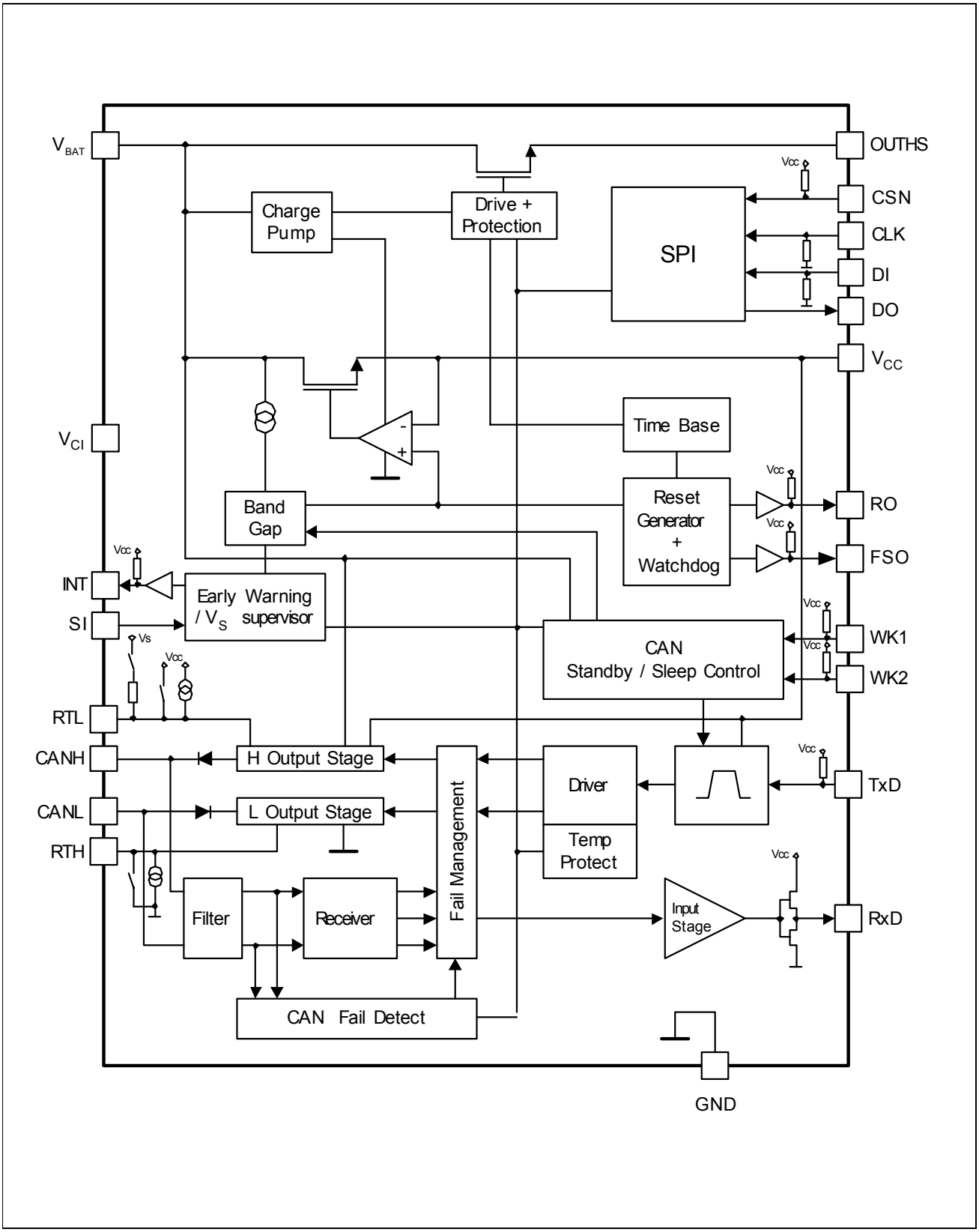


Figure 2: TLE 6263 G Functional Bloc Diagram

6 Circuit Description

The TLE 6263 is a monolithic IC, which incorporates a failure tolerant low speed CAN-transceiver for differential mode data transmission, a low dropout voltage regulator for internal and external 5V supply as well as a SPI (serial peripheral interface) to control and monitor the IC. Further there are integrated a high side switch, two wake-up inputs, a window watchdog circuit with fail safe output as well as a reset circuit and early warning function. **Figure 2** shows a schematic block diagram of the TLE 6263. **Table 1** shows the status of the different chip features during the four main operation modes.

Table 1: Truth table of the TLE 6263

Feature	normal mode	receive-only mode	V_{bat} stand-by mode	sleep mode
V_{CC}	ON	ON	ON	OFF
Reset	ON	ON	ON	OFF
Watchdog	ON	ON	ON[1)]	OFF
Fail safe output	ON	ON	ON[5)]	OFF
V_{INT}-Fail[2)]	ON	ON	ON	ON
Sense input	ON	ON	ON	OFF
Wake-up 1 / 2	ON[3)]	ON[3)]	ON	ON
HS-switch[4)]	ON	ON	ON	OFF
HS-cyclic-sense[4)]	OFF	OFF	ON	ON
SPI	ON	ON	ON	OFF
CAN transmit	ON	OFF	OFF	OFF
CAN receive	ON	ON	OFF	OFF
RTL output	switched to Vcc	switched to Vcc	switched to Vs	switched to Vs
RxD output	L = bus dominant; H = bus recessive	L = bus dominant; H = bus recessive	active low wake-up interrupt	low
INT output	active low early warning	active low early warning for V_{INT} and V_{CC}	active low early warning	low

[1)] at low V_{CC} output current only active when watchdog undercurrent function is not activated

[2)] can only be monitored in V_{bat}-stand-by mode via SPI

[3)] no wake-up interrupt generated, logic level status monitored via SPI

[4)] only active when selected via SPI

[5)] if watchdog under-current function active, than FSO = low

6.1 Operation Modes

The TLE 6263 offers four different operation modes that are controlled via the SPI interface (NSTB= SPI Input Bit3, ENT=SPI Input Bit2): the *normal operation mode*, the *receive-only mode*, the V_{bat} *stand-by mode* and the *sleep operation mode*. Please see the state diagram (**figure 3**).

Normal and Receive only Mode

In the normal operation mode both is possible, receiving and transmitting of messages, in the receive-only mode (RxD-only mode) the output stages are disabled which doesn't allow the CAN controller to send a message to the bus. In the state diagram (**figure 3**), V_{CC} is the status of the voltage regulator.

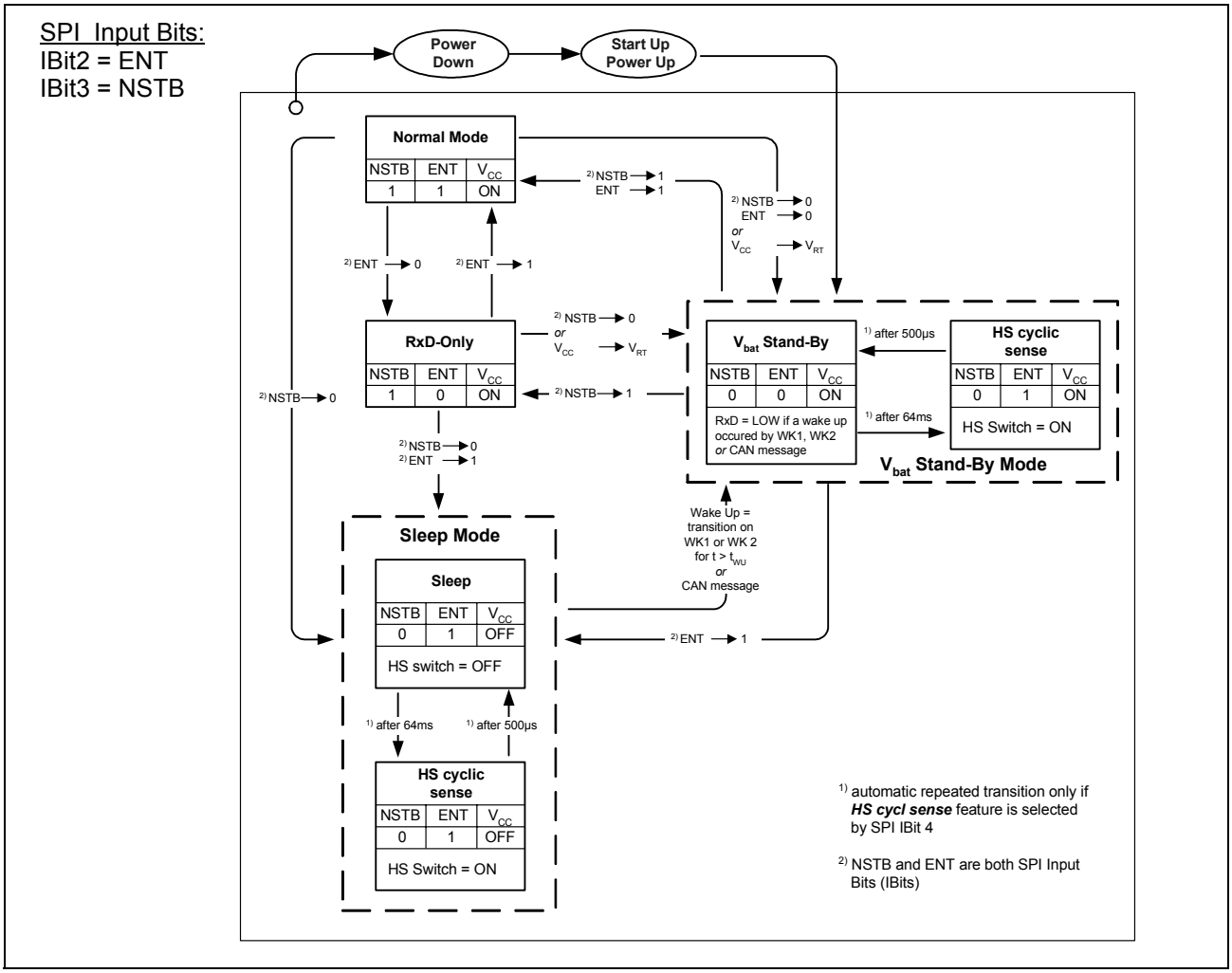


Figure 3: State Diagram

V_{bat} stand-by mode and sleep mode

In the V_{bat} stand-by mode and sleep mode the RTL output voltage is switched to V_S. Both modes are low power modes. In the sleep mode the whole application is switched

off by disabling the voltage regulator. That allows the total current consumption to drop down to less than 100 µA.

When a reset occurs, due to false watchdog triggering, the TLE6263 automatically switches from normal mode or receive-only mode respectively, to the V_{bat} stand-by mode. If a watchdog reset occurs in the V_{bat} stand-by mode the IC remains in this mode.

In sleep mode a wake-up at any of the wake-up inputs as well as via the bus lines (CANH or CANL) automatically sets the TLE 6263 in V_{bat} stand-by mode. In the V_{bat} stand-by mode a wake-up is monitored by setting the output RxD low. This feature works as a flag, to indicate a wake event to the microcontroller. To send and to receive messages, the CAN-transceiver has to be set to normal operation mode by the microcontroller.

In case the IC shall directly be set back to sleep mode after a wake-up, an internal wake-flip-flop has to be reseted via the SPI. Therefore IBIT1 has to be set high and then low again by a second SPI transmission. A transition from the V_{bat} stand-by mode to the normal mode or receive-only mode respectively, automatically resets the wake-flip-flop.

6.2 Low Dropout Voltage Regulator

The integrated low dropout voltage regulator is able to drive the internal loads (e.g. CAN-circuit) as well as external 5V loads. Its output voltage tolerance is better than ± 2%. The maximum output current is limited to 110 mA.

An external reverse current protection is recommended at the pin Vs to prevent the output capacitor from being discharged by negative transients or low input voltage.

Stability of the output voltage is guaranteed for output capacitors $C_Q \geq 100$ nF, nevertheless it is recommended to use capacitors $C_Q \geq 10$ µF to buffer the output voltage and therefore improve the reset behavior at input voltage transients.

To stabilize the internal supply a capacitor $C_{VI} \geq 100$ nF directly connected to the pin V_{CI} is required.

6.3 CAN Transceiver

The TLE 6263 is optimized for low speed data transmission up to 125 kBaud in automotive applications. **Figure 4** shows the principle configuration of a CAN network.Normally a differential signal is transmitted and received respectively. When a bus wiring failure (see **table 2**) is detected the device automatically switches to a dedicated CANH or CANL single-wire mode to maintain the communication if necessary. Further a receive-only mode is implemented that allows a separate CAN node diagnosis. During normal and RxD-only mode, RTL is switched to V_{CC} and RTH to GND. During V_{bat} stand-by and the cyclic wake mode, RTL is switched to V_S and RTH to GND.

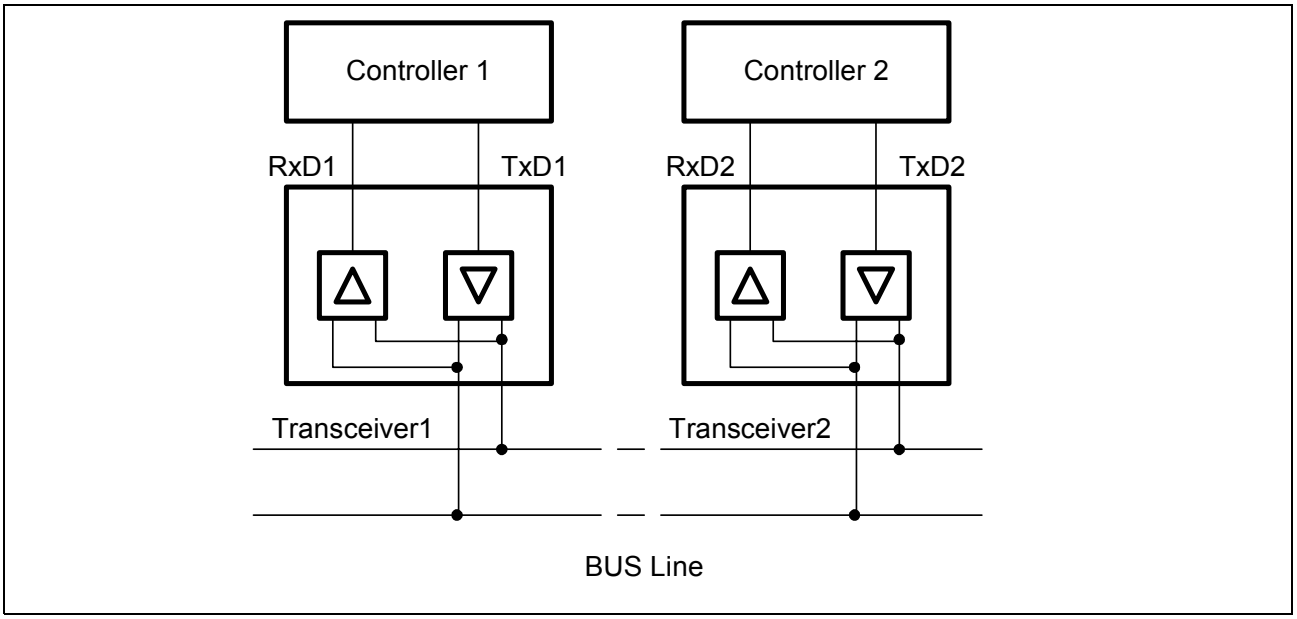


Figure 4: CAN Network Example

Receive-only Mode

The receive only mode is designed for a special test procedure to check the bus connections. **Figure 5** shows a network consisting of 5 nodes. If the connection between node 1 and node 3 shall be tested, the nodes 2,4 and 5 are switched into receive only mode. Node 1 and node 3 are in normal mode. If node 1 sends a message, node 3 is the only node which can acknowledge the message, the other nodes can only listen but cannot send an acknowledge bit. If node 1 receives the acknowledge bit from node 3, the connection is OK.

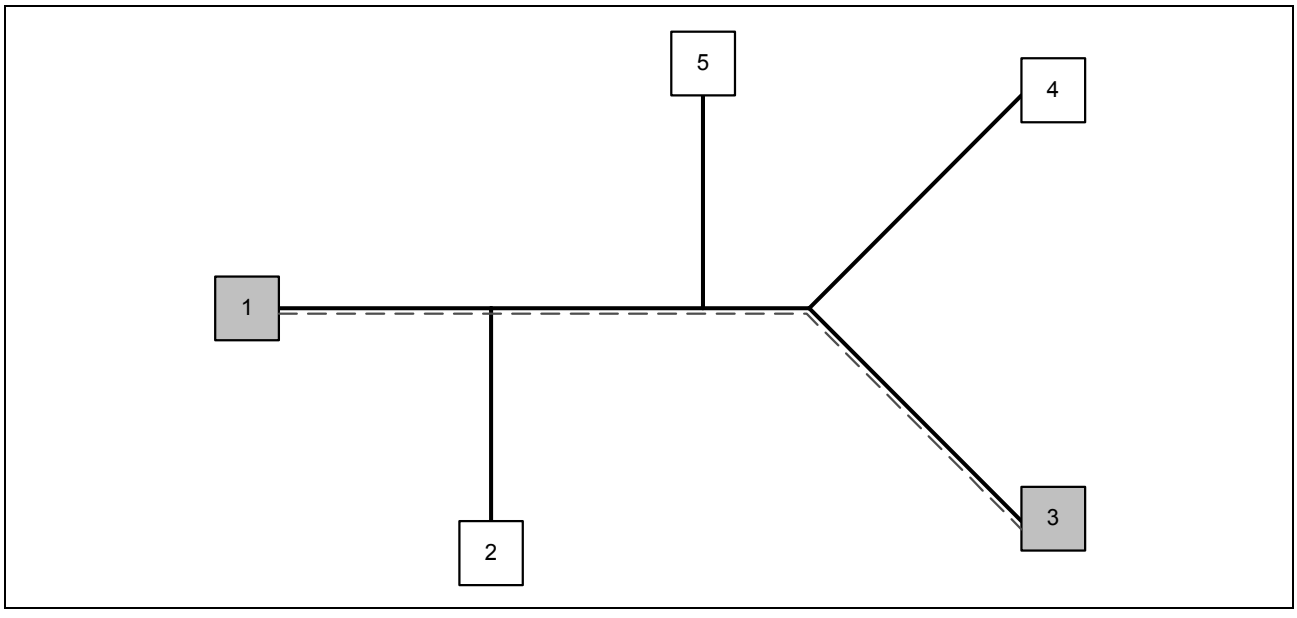


Figure 5: Testing the Bus Connection in Receive-only Mode

Electromagnetic Emmision (EME)

To reduce radiated electromagnetic emission (EME), the dynamic slopes of the CANL and CANH signals are both limited and symmetric. This allows the use of an unshielded twisted or parallel pair of wires for the bus. During single-wire transmission (one of the bus lines is affected by a bus line failure) the EME performance of the system is degraded from the differential mode.

6.4 Bus Failure Management

There are 9 different CAN bus wiring failures defined by the ISO 11519-2/ISO 11898-3 standard. These failures are devided into 7 failure groups (see **Table 2**). The difference between ISO11898-3 and ISO 11519-2 is also shown in **Table 2**. When a bus wiring failure is detected the device automatically switches to a dedicated CANH or CANL single-wire mode to maintain the communication if necessary. Therefore it is equipped with one differential receiver and four single ended comparators (two for each bus line).

To avoid false triggering by external RF influences, the single wire modes are activated after a certain delay time. As soon as the bus failure disappears the transceiver switches back to differential mode after another time delay.

The differential receiver threshold is set to typ. -2.5V. This ensures correct reception in the normal operation mode as well as in the failure cases 1, 2, 3a(6a) and 4(5) with a noise margin as high as possible. When one of the bus failures 3(6), 5(4), 6(3), 6a(3a), and 7 is detected, the defective bus wire is disabled by switching off the affected bus termination and output stage. The failure cases in brackets() are the failure cases according to ISO 11898-3. Simultaneously the multiplexing output of the receiver circuit is switched to the unaffected single ended comparator

The bus failures are monitored via the diagnosis protocoll of the SPI. A general indication of a CAN failure during normal mode at CANH or CANL is reported by OBIT 4 and 5. It is also possible to distinguish 6 CAN bus failures or failure groups on the SPI output bits 3 to 7 in the RxOnly mode(see **Table 2** and **5**). The failures are reported until transmission of the next CAN word begins.

In case the transmission data input TxD is permanently dominant, both, the CANH and CANL transmitting stage are disabled after a certain delay time t_{TxD}. This is necessary to prevent the bus from being blocked by a defective protocol unit or short to GND at the TxD input.

In order to protect the transceiver output stages from being damaged by shorts on the bus lines, current limiting circuits are integrated. The CANL and CANH output stage respectively are protected by an additional temperature sensor, that disables them as soon as the junction temperature exceeds the maximum value. In the temperature shut-down condition of the CAN output stages receiving messages from the bus lines is still possible.

Table 2: CAN bus line failure cases

failure #	failure description according to ISO 11898-3	failure description according to 11519-2
1	CANH line interrupted	CANL line interrupted
2	CANL line interrupted	CANH line interrupted
3	CANH shorted to Vbat	CANL shorted to Vbat
3a	CANH shorted to Vcc	CANL shorted to Vcc
4	CANL shorted to GND	CANH shorted to GND
5	CANH shorted to GND	CANL shorted to GND
6	CANL shorted to Vbat	CANH shorted to Vbat
6a	CANL shorted to Vcc	CANH shorted to Vcc
7	CANL shorted to CANH	CANL shorted to CANH

6.5 SPI (serial peripheral interface)

The 8-bit wide programming word (input word, see **table 3**) is read in via the data input DI, and this is synchronized with the clock input CLK supplied by the µC. The diagnostic information depends on the operation mode. The internal latches for the V_{bat}-stand-by diagnosis are reseted when leaving this mode.

Table 3, Input Data Protocol all modes

IBIT	
7	Watchdog Undercurrent Control
6	Set V_{INT}-Fail + V_{CC} Fail Flag
5	OUTHS ON
4	OUTHS Cyclic Sense
3	Not Standby
2	Enable Transmit
1	Reset Internal WK-FF
0	Watchdog Trigger

H = ON
L = OFF

Table 4, Diagnosis Data Protocol normal mode

OBIT	
7	HS UV / Temp-Shut Down
6	HS Overcurrent
5	CANL bus fail
4	CANH bus fail
3	WK2 logic level
2	WK1 logic level
1	Window Watchdog Reset
0	Temperature Prewarning

H = ON
L = OFF

The transmission cycle begins when the TLE6263 is selected by the chip select not input CSN (H to L). After the CSN input returns from L to H, the word that has been read in becomes the new control word. The DO output switches to tri-state status at this point, thereby releasing the DO bus circuit for other uses. For details of the SPI timing please refer to **figure 6 to 9**.

Table 5, Diagnosis Data Protocol RxD-only mode

OBIT	
7	CAN Failure 5(4) and 7
6	CAN Failure 6 (3)
5	CAN Failure 6a (3a)
4	CAN Failure 2(1) and 4(5)
3	CAN Failure 3(6)
2	CAN Failure 1(2) and 3a(6a)
1	Window Watchdog Reset
0	Temperature Prewarning

H = ON
L = OFF
()... values in brackets according to ISO11898-3 see table 2

Table 6, Diagnosis Data Protocol V_{bat}-Stand-by mode

OBIT	
7	V_{CC} Not-Fail
6	V_{INT} Not-Fail
5	WK1/2 Initialization Fail
4	Wake via CAN bus lines
3	WK2 voltage level
2	WK1 voltage level
1	Window Watchdog Reset
0	Temperature Prewarning

H = ON
L = OFF

6.6 Window Watchdog, Reset

When the input voltage exceeds the reset threshold voltage the reset output RO is switched HIGH after a delay time of typ. 8ms. This is necessary for a defined start of the microcontroller when the application is switched on. As soon as an under-voltage condition of the output voltage ($V_{CC} < V_{RT}$) appears, the reset output RO is switched LOW again (power on and under-voltage reset). The LOW signal is guaranteed down to an output voltage $V_Q \geq 1V$. Please refer to **figure 13**, *Reset Timing Diagram*.

In sleep operation mode, the watchdog circuit is automatically disabled.

Long Open Window

After the above described delayed reset (LOW to HIGH transition of RO) the window watchdog circuit is started by opening a long open window of typ. 65ms. The long open window allows the microcontroller to run his set-up and then to trigger the watchdog via the SPI, refer to **figure 11**,*Watchdog Timeout Definitions*. Within the long open window

period a watchdog trigger is detected as a “rising edge” by sampling a HIGH on the IBIT 0. The trigger is accepted when the CSN input becomes HIGH after the transmission of the SPI word. After each reset as well as after a power on condition the default value of IBIT 0 is LOW.

Closed and Open Window

A correct watchdog trigger results in starting the window watchdog by opening a closed window of typ. 6 ms followed by a open window of typ. 10 ms. From now on the microcontroller has to service the watchdog trigger by inverting the IBIT 0 alternating. The “negative” or “positive” edge has to meet the open window time. A correct watchdog service immediately results in starting the next closed window. Please refer to **figure 12**, *Watchdog Timing Diagram.*

Watchdog Reset

Should the trigger signal not meet the open window a watchdog reset is created by setting the reset output RO low for a period of typ. 2 ms. Then the watchdog starts again by opening a long open window. In addition, the SPI OBIT 1 (diagnosis bit 1) is set HIGH until the next successful watchdog trigger to monitor a watchdog reset. OBIT1 is also HIGH until the watchdog is correctly triggered after power-up / start-up. For fail safe reasons the TLE6263 is automatically switched in Vbat-stand-by mode if a watchdog trigger failure occurs. So the power consumption can be minimized in case of a permanent faulty microcontroller.

In case of either an undervoltage reset or a watchdog reset all SPI input registers (IBIT 0 to IBIT 7) are set low.

Undercurrent Disabling Function

To avoid cyclic wake-up’s of the microcontroller due to missing watchdog pulses when the microcontroller is in a low power mode, an automatic undercurrent disabling function of the watchdog circuit can be selected for the TLE 6263 V_{bat}-stand-by mode. For activation of this feature, the V_{CC} output current in the V_{bat}-stand-by mode has to be less than the undercurrent threshold ($I_{CC} < I_{CCWD}$) and in addition the SPI IBIT 7 has to be set HIGH. When the microcontroller returns back to normal mode or the output current becomes higher than $I_{CC} > I_{CCWD}$ the watchdog circuit is enabled again. A long open window is started then, to ensure a simple synchronization of the watchdog timing to the watchdog services of the microcontroller.

6.7 Flash program mode

To disable the watchdog feature a flash program mode is available. This mode is selected by applying a voltage of $6.8V < V_{INT} < 7.2V$ at pin INT. This is useful e.g. if the flash-memory of the micro has to be programmed and therefore a regular watchdog triggering is not possible. If the SPI is required in the flash program mode to change e.g. the mode of the TLE6263 the first input telegram has to be “00000000”.

6.8 Fail Safe feature

The output FSO becomes HIGH when the watchdog is correctly serviced by the microcontroller for the fourth time. As soon as either an under-voltage reset or watchdog reset occurs, it is set LOW again. This feature is very useful to control critical applications independent of the due function of the microcontroller e.g. to disable the power supply in case of a microcontroller failure.

6.9 Sense Comparator (pin SI) and V_{INT}-fail

The sense comparator (early warning function) compares a voltage defined by the user to an internal reference voltage. Therefore the voltage to be supervised has to be scaled down by an external voltage divider in order to compare it to the internal sense threshold V_{SIth}. This feature can be used e.g. to supervise the battery voltage in front of the reverse protection diode. The microcontroller is given a pre-warning before an under-voltage reset due to low input voltage occurs. The pre-warning is flagged by setting the interrupt output INT low in normal mode, receive only mode and V_{bat}-stand-by mode. In sleep operation mode the sense function is inactive. Calculation of the voltage divider can be easily done since the sense input current can be neglected. An internal blanking time prevents from false triggering due to line transients. Further improvement is possible by the use of an external ceramic capacitor switched between SI and GND (see *Application Diagram* **Figure 15**).

6.10 V_{INT}- and V_{CC}-fail flag

To activate the V_{INT} supervisor feature the SPI IBIT 6 has to be set HIGH to set an internal flip-flop. This automatically sets the V_{bat}-stand-by OBIT 6 HIGH, too. Should the internal supply voltage become lower than the internal threshold $V_{VINT,th}$ (typ. 2.5V) the NOT V_{INT}-Fail bit becomes LOW to indicate the low voltage condition. All SPI input registers are set LOW due to a low voltage condition of the internal supply voltage.

Like the wake-up diagnosis the V_{INT}-Fail diagnosis can only be monitored in the V_{bat}-stand-by mode. The V_{INT}-Fail feature can also be used to give an indication when the ECU has been changed and therefore a pre-setting routine of the microcontroller has to be started.

Further to the reset threshold there is another supervisor threshold implemented, to monitor the output voltage V_{CC}. This threshold is called $V_{VCC,th}$ (typ. 2.5V). The NOT V_{CC}-Fail feature is monitored via OBIT 7 in the V_{bat}-stand-by mode and set, like the NOT V_{INT}-Fail flag, via IBIT 6 (so both fail features are activated with the IBIT 6 but monitored via OBIT 6 and OBIT 7 during V_{bat}-stand-by).

In the receive-only mode both fail bits cause the interrupt output INT to go low.

6.11 Wake-Up Inputs WK1, WK2

In addition to a wake-up from sleep mode via the bus lines CANH or CANL it is also possible to wake-up the TLE6263 from low power mode via the wake-up inputs WK1 and WK2. The wake-up inputs are sensitive to a transition of the voltage level, either from high to low or the other way round. They are active in all operation modes. In the normal mode the current logic level at WK1/2 is monitored via the SPI (see **table 4 and 6**).

A positive or negative voltage edge at WK1/2 in V_{bat}-stand-by mode or sleep mode immediately results in setting the output RxD low to signal a wake-up. After a wake-up via WK1/2 the transmission of the SPI diagnosis word in the V_{bat}-stand-by mode shows the logic level that has caused the wake-up. To get the current voltage levels at WK1/2 in the V_{bat}-stand-by mode the internal wake flip-flop has to be reseted by the IBIT1 for each transmission. As long as IBIT1 is set high or the internal wake flip-flop is reseted respectively, in the V_{bat}-stand-by mode the RxD output is blocked to signal a new wake-up event via the CAN-bus or the wake-up inputs.

Further to the continues sensing at the wake-up inputs a cyclic sense feature is possible. When the OUTHS cyclic sense feature is selected via the SPI IBIT 4 the high side switch as well as the WK1/2 inputs are periodically activated by the TLE6263 in the sleep and V_{bat}-stand-by mode.

When switching the TLE6263 into sleep mode (cyclic sense feature activated) the voltage level at the wake-inputs is sensed 2 times to initialize the reference voltage. Should this initialisation fail (2 samples are unequal) the device is automatically set in V_{bat}-stand-by mode and the initialisation error is shown on the OBIT 5. To enter the sleep mode now directly from the V_{bat}-stand-by mode, the internal wake flip-flop has to be reseted by the IBIT 1.

6.12 Interrupt output INT

Like the reset output, the interrupt output is a low active output. It is used to monitor low voltage conditions at the sense input in normal mode and stand-by mode (see **table 8**). In the receive-only mode the V_{INT}-fail flag and V_{CC} supervisor are monitored.

6.13 High Side Switch

The high side output OUTHS is able to switch loads up to 150 mA. Its on-resistance is 1.0 Ω typ. @ 25°C. This switch is controlled via the SPI input bits 4 and 5. In normal mode, receive-only mode and V_{bat}-stand-by mode the high side output is switched on and off, respectively via the SPI input bit 5.

To supply external wake-up circuits in sleep mode and V_{bat}-stand-by mode the output OUTHS can be periodically switched on by the TLE6263 itself. In order to activate this cyclic sense feature the SPI IBIT 4 has to be set high. The auto-timing period then is typ. 65 ms, the on-time is typ. 1 ms. Should there be any over-current condition at the switch in the sleep mode (cyclic sense activated) or V_{bat}-stand-by mode a wake-up is flagged

via the RxD output. The over-current condition is monitored on the SPI OBIT 6 in normal operation mode.

The SPI OBIT 0 flags a thermal pre-warning of the high side switch. By this the microcontroller is able to reduce the power dissipation of the TLE6263 by switching off functions of minor priority until the temperature threshold of the thermal shutdown is reached. Further OUTHS is protected against short circuit and overload. As soon as the under-voltage condition of the supply voltage is met ($V_S < V_{UVOFF}$), the switch is automatically disabled by the under-voltage lockout circuit. Moreover the switch is automatically disabled when a reset or watchdog reset occurs.

6.14 Hints for unused pins

SI: connect to V_S

OUTHS: leave open

WK1/2: connect to V_S or leave open

INT: leave open

RO: leave open

FSO: leave open

SI: switch to Vs

7 Electrical Characteristics

7.1 Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Voltages					
Supply voltage	V_S	-0.3	28	V	
Supply voltage	V_S	-0.3	40	V	t_p< 0.5s; t_p/T < 0.1
Regulator output voltage	V_{CC}	-0.3	5.5	V	
CAN bus voltage (CANH, CANL)	$V_{CANH/L}$	-20	28	V	
CAN bus voltage (CANH, CANL)	$V_{CANH/L}$	-40	40	V	V_S >0 V t_p< 0.5s; t_p/T < 0.1
Logic input voltages (DI, CLK, CSN, OSC, TxD)	V_I	-0.3	V_{CC} +0.3	V	0 V < V_S < 24 V 0 V < V_{CC} < 5.5 V
Logic output voltage (DO, RO, INT, RxD, FSO)	$V_{DRI,RD}$	-0.3	V_{CC} +0.3	V	0 V < V_S < 24 V 0 V < V_{CC} < 5.5 V
Termination input voltage (RTH, RTL)	$V_{TL/TH}$	-0.3	V_S +0.3	V	0 V < V_S < 24 V 0 V < V_{CC} < 5.5 V
Input voltages at WK1/2 and SI	$V_{WK/SI}$	-40	40	V	
Electrostatic discharge voltage at pin CANH, CANL, GND, V_S	V_{esd}	-3	3	kV	human body model, C = 100 pF, R = 1.5 kΩ
Electrostatic discharge voltage at any other pin	V_{esd}	-1	1	kV	human body model, C = 100 pF, R = 1.5 kΩ
Currents					
Output current; Vcc	I_{CC}	–	–	A	1) internally limited
Output current; OUTHS	I_{OUTH1}	1)	0.2	A	1) internally limited

Note 1): Not subject to production test - specified by design

7.1 Absolute Maximum Ratings (cont'd)

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Temperatures					
Junction temperature	T_j	– 40	150	°C	–
Storage temperature	T_{stg}	– 50	150	°C	–

Note: Maximum ratings are absolute ratings; exceeding any one of these values may cause irreversible damage to the integrated circuit.

7.2 Operating Range

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Supply voltage	V_S	$V_{UV\ OFF}$	20	V	After V_S rising above $V_{UV\ ON}$
Supply voltage	V_S	$V_{UV\ OFF}$	40	V	thermally limited
Supply voltage slew rate	dV_S/dt	–0.5	5	V/µs	
Logic input voltage (DI, CLK, CSN, TxD)	V_I	– 0.3	V_{CC}	V	
Output capacitor	C_{CC}	100		nF	
Output capacitor	C_{VI}	100	460	nF	
SPI clock frequency	f_{clk}		1.5	MHz	
Junction temperature	T_j	– 40	150	°C	

Thermal Resistances

Junction pin	$R_{thj\text{-}pin}$	–	25	K/W	
Junction ambient	$R_{thj\text{-}a}$	–	65	K/W	

Note: Calculation of the junction temperature $T_j = T_{amb} + P \times R_{thj\text{-}a}$

7.3 Electrical Characteristics

V_S = 13.5 V; I_{CC} = 1 mA; normal mode; all outputs open; – 40 °C < T_j < 150 °C (max. 125°C for CAN circuit characteristics); all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Quiescent current Pin V_S						
Current consumption $I_Q = I_S - I_{CC}$	I_Q	–	5.5	10	mA	normal mode; I_{CC} = 30 mA; TxD recessive
Current consumption $I_Q = I_S - I_{CC}$	I_Q	–	8	10	mA	normal mode; I_{CC} = 30 mA; TxD dominant
Current consumption $I_Q = I_S - I_{CC}$	I_Q	–	300	400	µA	stand-by mode; T_j=25°C; I_{CC} = 1 mA; Ibit 7 = H
Current consumption	I_Q	–	50	80	µA	sleep mode; T_j=25°C; SPI Ibit 4 = L; V_{CC} = V_{CCI} = 0 V
Current consumption	I_Q			3	mA	OUTHS active; SPI Ibit 4 = H; sleep mode; V_{CC} = V_{CCI} = 0 V
Voltage Regulator; Pin V_{CC}						
Output voltage	V_{CC}	4.9	5.0	5.1	V	0.1 mA< I_{CC}< 100 mA 6 V< V_I< 20 V
Output voltage	V_{CC}	4.8	5.0	5.2	V	0A < I_{CC} < 100 µA
Line regulation	ΔV_{CC}			50	mV	6 V < V_S < 16 V; I_{CC} = 1mA
Load regulation	ΔV_{CC}			50	mV	5mA< I_{CC}< 100mA; V_S = 6V
Power supply ripple rejection	$PSRR$		40		dB	V_S < 1 Vss; $C_Q \geq$ 10µF 100Hz< f <100kHz
Output current limit	I_{CCmax}	110	120		mA	note 1)
Output current limit	I_{CCmax}		120		mA	V_{CC} = 0 V
Drop voltage $V_{DR} = V_S - V_{CC}$	V_{DR}			0.5	V	I_{CC} = 80 mA; note 1)

note 1) measured when the output voltage V_{CC} has dropped 100 mV from the nominal value obtained at 13.5 V input voltage V_S

7.3 Electrical Characteristics (cont'd)

V_S = 13.5 V; I_{CC} = 1 mA; normal mode; all outputs open; – 40 °C < T_j < 150 °C (max. 125°C for CAN circuit characteristics); all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Oscillator						
internal oscillating frequency	f_{OSC}		125		kHz	
Internal cycling time (1/64 * f_{OSC})$^{-1}$	t_{CYL}	0.43	0.51	0.64	ms	
Internal cycling time (1/64 * f_{OSC})$^{-1}$	t_{CYL}	0.30	0.51	0.72	ms	sleep mode
Reset Generator; Pin RO						
Reset threshold voltage	V_{RT}	4.5	4.65	4.8	V	V_{CC} decreasing
Reset low output voltage	V_{RO}		0.2	0.4	V	I_{RO} = 1mA for $V_{CC} = V_{RT}$ or I_{RO} = 200 µA for $V_{CC} \geq$ 1V
Reset high output voltage	V_{RO}	4.0		V_{CC}+ 0.1	V	
Reset pull up current	I_{RO}	20	200	500	µA	V_{RO} = 0V
Reset reaction time	t_{RR}	1	2	10	µs	$V_{CC} < V_{RT}$ to RO = L
Reset delay time (16 cyl.)	t_{RD}	6.9	8.5	12	ms	
Watchdog Generator						
Watchdog trigger	t_{WD}	7.2	10	13.6	ms	
Long open window (128 cyl.)	t_{LW}	55	65	81	ms	
Closed window (12 cyl.)	t_{CW}	5.1	6.1	7.7	ms	
Open window (20 cyl.)	t_{OW}	8.6	10.2	13	ms	
Watchdog reset-puls time (4 cyl.)	t_{WDR}	1.7	2	3	ms	
Watchdog undercurrent disable threshold	I_{CCWD}	0.5	4	7	mA	T_j < 85 °C; Watchdog OFF when $I_{CC} < I_{CCWD}$ and SPI-Ibit 7= H

7.3 Electrical Characteristics (cont'd)

V_S = 13.5 V; I_{CC} = 1 mA; normal mode; all outputs open; – 40 °C < T_j < 150 °C (max. 125°C for CAN circuit characteristics); all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Watchdog Undercurrent disable hysteresis	$I_{CCWDhys}$		0.5		mA	
Watchdog Undercurrent reaction time	t_{LHR}		8		µs	T_j=25°C
Fail Safe Output; Pin FSO						
Watchdog edge count difference to set HIGH	n_{FS}		4		V	
Fail Safe low output voltage	V_{FS}		0.2	0.4	V	I_{FSO}= 1mA for $V_{CC} = V_{RT}$ or I_{FSO} = 200 µA for $V_{CC} \geq$ 1V
Fail Safe high output voltage	V_{FS}	4.0		V_{CC}+ 0.1	V	I_{FSO}= -1mA for $V_{CC} \geq V_{RT}$
Sense Input (Early Warning) SI, V_{INT}-Fail, Interrupt Output INT						
Sense In threshold voltage	$V_{SI,th}$	2.1	2.3	2.5	V	V_{SI} decreasing until INT transition to LOW
Sense In threshold hysteresis	$V_{SI,hys}$		200		mV	
Sense Input Current	I_{SI}		0.1		µA	$V_{SI} \geq$ 0 V
Sense reaction time	$t_{S,r}$	5	10	20	µs	$V_S < V_{S,th}$ to INT = low
Interrupt Out high voltage	$V_{INThigh}$	0.7 x V_{CC}	–	V_{CC}	V	I_0 = – 20 µA
Interrupt Out low voltage	V_{INTlow}	0	–	0.9	V	I_0 = 1.25 mA
Interrupt pull up current	I_{INT}	20	150	500	µA	V_{INT} = 0V
V_{CC}-Fail threshold voltage	$V_{VCC,th}$	2.3	2.8	3.1	V	
V_{CC}-Fail reaction time	$t_{VCC,r}$		5		µs	$V_{CC} < V_{VCC,th}$ to Obit 6 = low; V_{bat}-stand-by mode
V_{INT}-Fail threshold voltage	$V_{VINT,th}$	1.5	3.2	4.3	V	proportional to V_S

7.3 Electrical Characteristics (cont'd)

V_S = 13.5 V; I_{CC} = 1 mA; normal mode; all outputs open; – 40 °C < T_j < 150 °C (max. 125°C for CAN circuit characteristics); all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Wake-Up Inputs WK1 / WK2						
Wake-up threshold voltage	V_{WUth}	2	3	4	V	sleep mode; Vbat-stand-by mode
Minimum time for wake-up	t_{WU}	10	15	32	µs	sleep mode; Vbat-stand-by mode
Input current	I_{WK}		-2		µA	V_{WK} = 0 V
High Side Output OUTHS; (controlled by bit 4 and bit 5 of SPI input word)						
Static Drain-Source ON-Resistance; I_{OUTH3} = – 0.15 A	$R_{DSON\ HS}$	–	1.0	1.5	Ω	T_j = 25 °C
			–	3.0	Ω	
			2.5	3.0	Ω	5.2 V ≤ V_S ≤ 9 V T_j = 25 °C
			–	5.0	Ω	5.2 V ≤ V_S ≤ 9 V
Active zener voltage	V_{OUTHS}		–2		V	I_{OUTHS} = – 0.15 A
Clamp diode forward voltage	V_{OUTHS}			1	V	I_{OUTHS} = 0.15 A
Leakage current	I_{QLHS}		–4		µA	V_{OUTHS} = 0 V
Switch ON delay time	t_{dONHS}			20	µs	CSN high to OUTHS
Switch OFF delay time	t_{dOFFHS}			20	µs	CSN high to OUTHS
Overcurrent shutdown threshold	I_{SDHS}	– 0.8	– 0.3	– 0.2	A	–
Shutdown delay time	t_{dSDHS}	10	35	50	µs	
Current limit	I_{OCLHS}	– 1.2	– 0.6	– 0.3	A	
UV-Switch-ON voltage	$V_{UV\ ON}$	–	5.2	6.0	V	V_S increasing
UV-Switch-OFF voltage	$V_{UV\ OFF}$	4.5	4.7	5.2	V	V_S decreasing
UV-ON/OFF-Hysteresis	$V_{UV\ HY}$	–	0.5	–	V	$V_{UV\ ON} - V_{UV\ OFF}$
Cyclic sense period (128 cyl.)	$t_{P\ CS}$	38	65	92	ms	sleep mode SPI-bit 4 = H,

7.3 Electrical Characteristics (cont'd)

V_S = 13.5 V; I_{CC} = 1 mA; normal mode; all outputs open; – 40 °C < T_j < 150 °C (max. 125°C for CAN circuit characteristics); all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Cyclic sense period (128 cyl.)	$t_{P\,CS}$	55	65	80	ms	Vbat-stand-by mode; SPI-bit 4 = H; watchdog under-current feature active
Cyclic sense ON time (1 cyl.)	$t_{CS\,on}$		0.5		ms	
CAN-Transceiver						
Receiver Output R×D						
HIGH level output voltage	V_{OH}	V_{CC} -0.9		V_{CC}	V	I_0 = -250 µA
LOW level output voltage	V_{OL}	0		0.9	V	I_0 = 1.25 mA
Transmission Input T×D						
HIGH level input voltage threshold	V_{IH}		0.52× V_{CC}	0.7 × V_{CC}	V	
LOW level input voltage threshold	V_{IL}	0.3 × V_{CC}	0.48× V_{CC}		V	
HIGH level input current	I_{IH}	-150	-30	-10	µA	V_i = 4 V
LOW level input current	I_{IL}	-600	-300	-40	µA	V_i = 1 V
Bus Lines CANL, CANH						
Differential receiver recessive-to-dominant threshold voltage	V_{dRxDrd}	-2.8	-2.5	-2.2	V	
Differential receiver dominant-to-recessive threshold voltage	V_{dRxDdr}	-3.1	-2.9	-2.5	V	
CANH recessive output voltage	V_{CANHr}	0.1	0.2	0.3	V	TxD = V_{CC}; R_{RTH} < 4 kΩ

7.3 Electrical Characteristics (cont'd)

V_S = 13.5 V; I_{CC} = 1 mA; normal mode; all outputs open; – 40 °C < T_j < 150 °C (max. 125°C for CAN circuit characteristics); all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
CANL recessive output voltage	V_{CANLr}	V_{CC} -0.2			V	TxD = V_{CC}; R_{RTL} < 4 kΩ
CANH dominant output voltage	V_{CANHd}	V_{CC} -1.4	V_{CC} -1.0	V_{CC}	V	TxD = 0 V; I_{CANH} = – 40 mA
CANL dominant output voltage	V_{CANLd}		1.0	1.4	V	TxD = 0 V; I_{CANL} = 40 mA
CANH output current	I_{CANH}	-110	-80	-50	mA	V_{CANH} = 0 V; TxD = 0 V
		-5		5	µA	sleep mode; V_{CANH} = 12 V
CANL output current	I_{CANL}	50	80	110	mA	V_{CANL} = 5 V; TxD = 0 V
		-5		5	µA	sleep mode; V_{CANL} = 0 V
Voltage detection threshold for short-circuit to battery voltage on CANH and CANL	$V_{det(th)}$	6.5	7.3	8.0	V	
CANH wake-up voltage threshold	$V_{H,wk}$	1.2	1.9	2.7	V	low power modes
CANL wake-up voltage threshold	$V_{L,wk}$	2.2	3.1	3.9	V	low power modes
CANH single-ended receiver threshold	V_{CANH}	1.6	2.1	2.6	V	failure cases 3, 5, 7 recessive to dominant
CANL single-ended receiver threshold	V_{CANL}	2.4	2.9	3.4	V	failure case 6 and 6a recessive to dominant
CANL leakage current	I_{CANLl}	-5		5	µA	V_{CC} = 0 V, V_S = 0 V, V_{CANL} = 13.5 V
CANH leakage current	I_{CANHl}	-5		5	µA	V_{CC} = 0 V, V_S = 0 V, V_{CANH} = 5 V

7.3 Electrical Characteristics (cont'd)

V_S = 13.5 V; I_{CC} = 1 mA; normal mode; all outputs open; – 40 °C < T_j < 150 °C (max. 125°C for CAN circuit characteristics); all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Termination Outputs RTL, RTH						
RTL to V_{CC} switch-on resistance	R_{RTL}		40	95	Ω	I_o = – 10 mA;
RTL to BAT switch series resistance	R_{oRTL}	5	15	30	kΩ	V_{BAT}-stand-by *or* sleep mode
RTH to ground switch-on resistance	R_{RTH}		40	95	Ω	I_o = 10 mA;
RTH output voltage	V_{oRTH}		0.7	1.0	V	I_o = 1 mA; sleep mode *or* V_{BAT}-stand-by
RTH pull-down current	I_{RTHpd}	40	75	120	µA	failure cases 6 and 6a
RTL pull-up current	I_{RTLpu}	-120	-75	-40	µA	failure cases 3, 3a, 5 and 7
RTH leakage current	I_{RTHl}	-5		5	µA	V_{CC} = 0 V, V_S = 0 V, V_{RTH} = 5 V, T_j < 85 °C
RTL leakage current	I_{RTLl}	-5		5	µA	V_{CC} = 0 V, V_S = 0 V V_{RTL} = 13.5 V, T_j < 85 °C
CAN-Transceiver						
Dynamic Characteristics						
CANH and CANL bus output transition time recessive-to-dominant	t_{rd}	0.6	1.2	2.1	µs	10% to 90%; C_1 = 10 nF; C_2 = 0; R_1 = 100 Ω
CANH and CANL bus output transition time dominant-to-recessive	t_{dr}	0.3	0.6	1.3	µs	10% to 90%; C_1 = 1 nF; C_2 = 0; R_1 = 100 Ω
Minimum dominant time for wake-up on CANL or CANH	$t_{wu(min)}$	12	20	32	µs	Stand-by modes

7.3 Electrical Characteristics (cont'd)

V_S = 13.5 V; I_{CC} = 1 mA; normal mode; all outputs open; – 40 °C < T_j < 150 °C (max. 125°C for CAN circuit characteristics); all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Failure cases 3 and 6 detection time	t_{fail}	25	45	80	µs	
Failure case 6a detection time		2.0	4.8	8.0	ms	
Failure cases 5 and 7 detection time		1.0	2.0	4.0	ms	
Failure cases 5, 6, 6a and 7 recovery time		25	45	80	ms	
Failure cases 3 recovery time		250	500	750	µs	
Failure cases 5 and 7 detection time	t_{fail}	0.4	1.0	2.4	ms	Stand-by modes
Failure cases 6 and 6a detection time		0.8	4.0	8.0	ms	Stand-by modes
Failure cases 5, 6, 6a and 7 recovery time		0.4	1.0	2.4	ms	Stand-by modes
Propagation delay TxD-to-RxD LOW (recessive to dominant)	$t_{PD(L)}$	–	1.5	2.1	µs	C_1 = 100 pF; C_2 = 0; R_1 = 100 Ω; no failures and bus failure cases 1, 2, 3a and 4
		–	1.7	2.4	µs	C_1 = C_2 = 3.3 nF; R_1 = 100 Ω; no bus failure and failure cases 1, 2, 3a and 4
		–	1.8	2.5	µs	C_1 100 pF; C_2 = 0; R_1 = 100 Ω; bus failure cases 3, 5, 6, 6a and 7
		–	2.0	2.6	µs	C_1 = C_2 = 3.3 nF; R_1 =100 Ω; bus failure cases 3, 5, 6, 6a and 7

7.3 Electrical Characteristics (cont'd)

V_S = 13.5 V; I_{CC} = 1 mA; normal mode; all outputs open; – 40 °C < T_j < 150 °C (max. 125°C for CAN circuit characteristics); all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Propagation delay TxD-to-RxD HIGH (dominant to recessive)	$t_{PD(H)}$	–	1.3	2.0	µs	C_1 = 100 pF; C_2 = 0; R_1 =100 Ω; no failures and bus failure cases 1, 2, 3a and 4
		–	2.5	3.5	µs	C_1 = C_2 = 3.3 nF; R_1 = 100 Ω; no bus failure and failure cases 1, 2, 3a and 4
		–	1.3	2.1	µs	C_1 100 pF; C_2 = 0; R_1 = 100 Ω; bus failure cases 3, 5, 6, 6a and 7
		–	1.7	2.6	µs	C_1 = C_2 = 3.3 nF; R_1 = 100 Ω; bus failure cases 3, 5, 6, 6a and 7
Edge-count difference (falling edge) between CANH and CANL for failure cases 1, 2, 3a and 4 detection	n_e	–	4	–	–	
Edge-count difference (rising edge) between CANH and CANL for failure cases 1, 2, 3a and 4 recovery		–	2	–	–	
TxD permanent dominant disable time	t_{TxD}	1.3	2.0	3.5	ms	

SPI-Interface

Logic Inputs DI, CLK and CSN

H-input voltage threshold	V_{IH}	–	–	0.7 x V_{CC}	V	–
L-input voltage threshold	V_{IL}	0.3 x V_{CC}	–	–	V	–
Hysteresis of input voltage	V_{IHY}	50	200	500	mV	–
Pull up current at pin CSN	I_{ICSN}	– 100	– 25	– 5	µA	$V_{CSN} = 0.7 \times V_{CC}$

7.3 Electrical Characteristics (cont'd)

V_S = 13.5 V; I_{CC} = 1 mA; normal mode; all outputs open; – 40 °C < T_j < 150 °C (max. 125°C for CAN circuit characteristics); all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Pull down current at pin DI and CLK	$I_{ICLK/DI}$	5	25	100	µA	$V_{DI} = 0.2 \times V_{CC}$
Input capacitance at pin CSN, DI or CLK	C_I	–	10	15	pF	Not subject to production test - specified by design
Logic Output DO						
H-output voltage level	V_{DOH}	V_{CC} – 1.0	V_{CC} – 0.7	–	V	I_{DOH} = 1 mA
L-output voltage level	V_{DOL}	–	0.2	0.4	V	I_{DOL} = – 1.6 mA
Tri-state leakage current	I_{DOLK}	– 10	–	10	µA	$V_{CSN} = V_{CC}$ 0 V < V_{DO} < V_{CC}
Tri-state input capacitance	C_{DO}	–	10	15	pF	Not subject to production test - specified by design
Data Input Timing Not subject to production test - specified by design						
Clock period	t_{pCLK}	1000	–	–	ns	–
Clock high time	t_{CLKH}	500	–	–	ns	–
Clock low time	t_{CLKL}	500	–	–	ns	–
Clock low before CSN low	t_{bef}	500	–	–	ns	–
CSN setup time	t_{lead}	500	–	–	ns	–
CLK setup time	t_{lag}	500	–	–	ns	–
Clock low after CSN high	t_{beh}	500	–	–	ns	–
DI setup time	t_{DISU}	250	–	–	ns	–
DI hold time	t_{DIHO}	250	–	–	ns	–
Input signal rise time at pin DI, CLK and CSN	t_{rIN}	–	–	200	ns	–
Input signal fall time at pin DI, CLK and CSN	t_{fIN}	–	–	200	ns	–

7.3 Electrical Characteristics (cont'd)

V_S = 13.5 V; I_{CC} = 1 mA; normal mode; all outputs open; – 40 °C < T_j < 150 °C (max. 125°C for CAN circuit characteristics); all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Data Output Timing						
Not subject to production test - specified by design						
DO rise time	t_{rDO}	–	50	100	ns	C_L = 100 pF
DO fall time	t_{fDO}	–	50	100	ns	C_L = 100 pF
DO enable time	t_{ENDO}	–	–	250	ns	low impedance
DO disable time	t_{DISDO}	–	–	250	ns	high impedance
DO valid time	t_{VADO}	–	100	250	ns	V_{DO} < 0.1 V_{CC}; V_{DO} > 0.9 V_{CC}; C_L = 100 pF
Thermal Prewarning and Shutdown (junction temperatures)						
Not subject to production test - specified by design						
OUTHS thermal prewarning ON temperature	T_{jPW}	120	145	170	°C	bit 0 of SPI diagnosis word
OUTHS thermal prewarning hyst.	ΔT	–	30	–	K	–
OUTHS thermal shutdown temp.	T_{jSD}	150	175	200	°C	–
OUTHS thermal switch-on temp.	T_{jSO}	120	–	170	°C	–
OUTHS thermal shutdown hyst.	ΔT	–	30	–	K	–
OUTHS ratio of SD to PW temp.	T_{jSD} / T_{jPW}		1.20	–	–	–
Vcc thermal shutdown temp.	T_{jSD}	155	185	200	°C	hysteresis 15°K (typ.)
OUTHS thermal shutdown temp.	T_{jSD}		150		°C	hysteresis 15°K (typ.)

8 Timing Diagrams

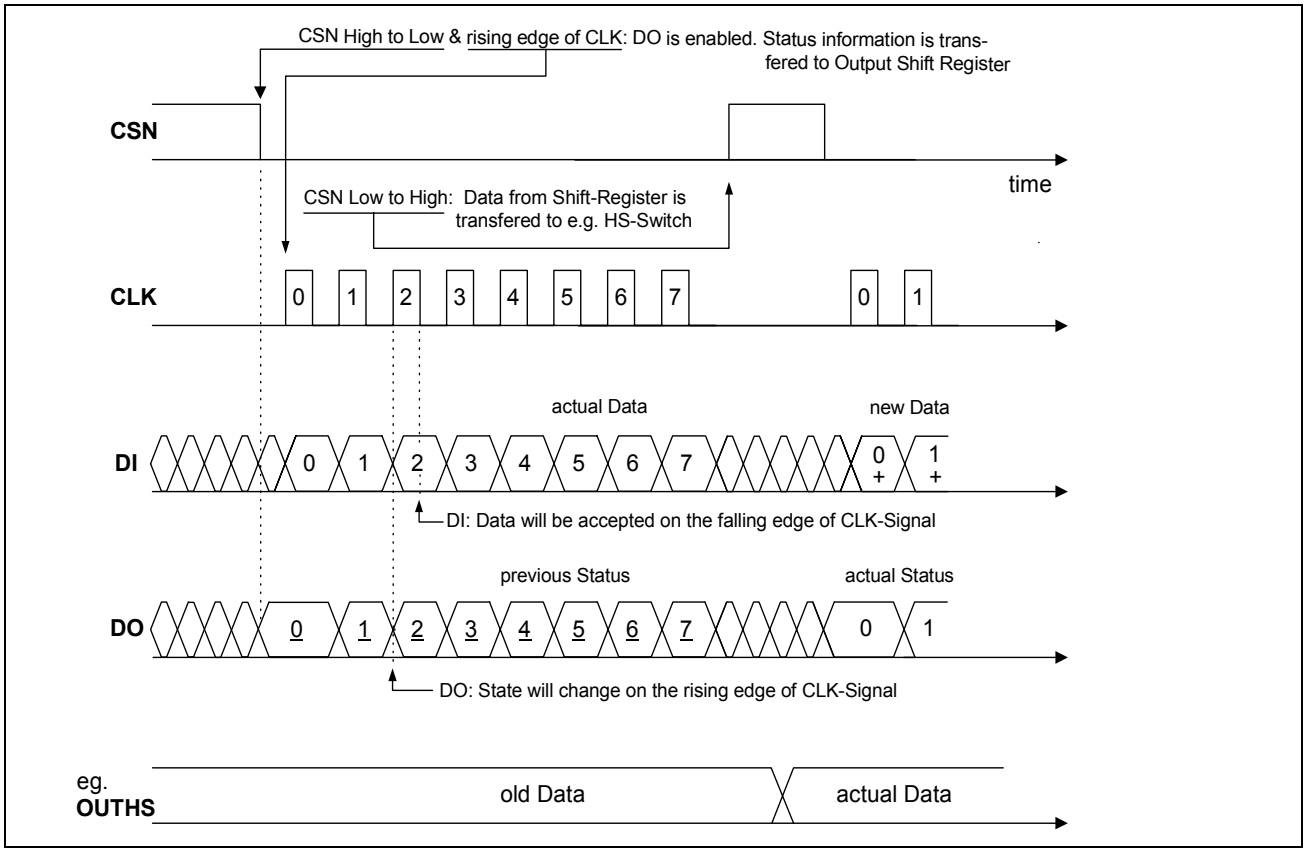


Figure 6: SPI-Data Transfer Timing

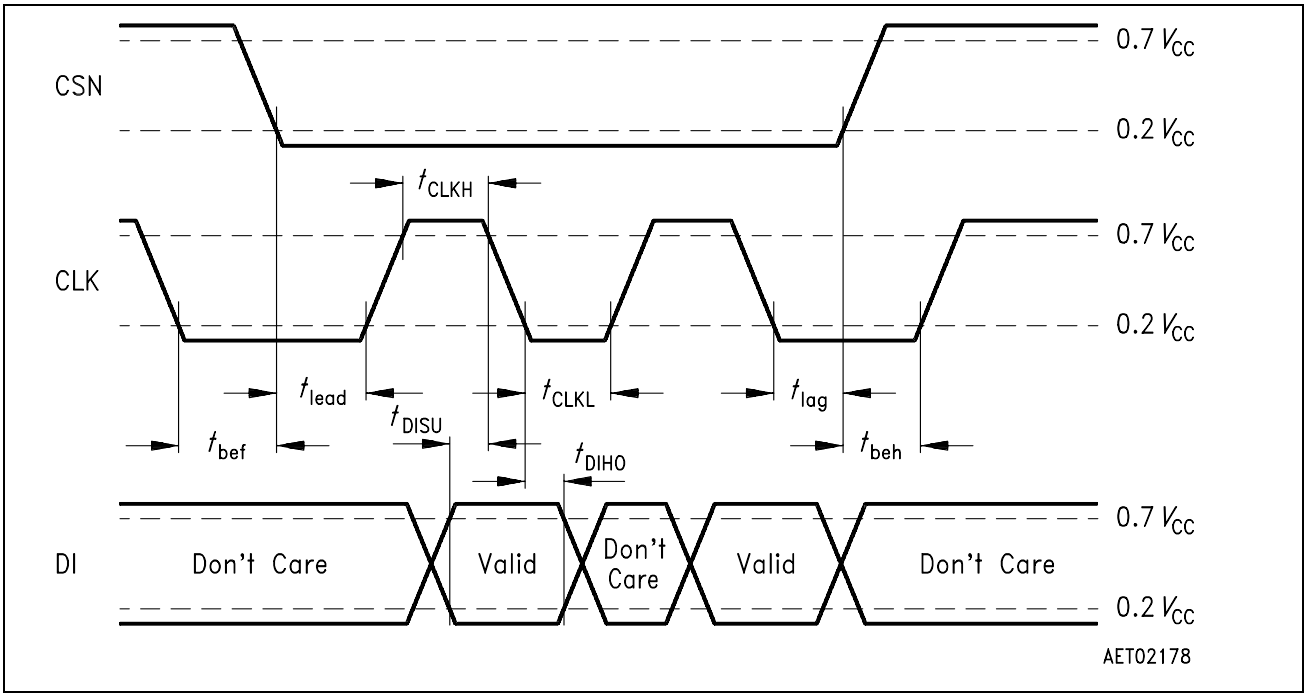


Figure 7: SPI-Input Timing

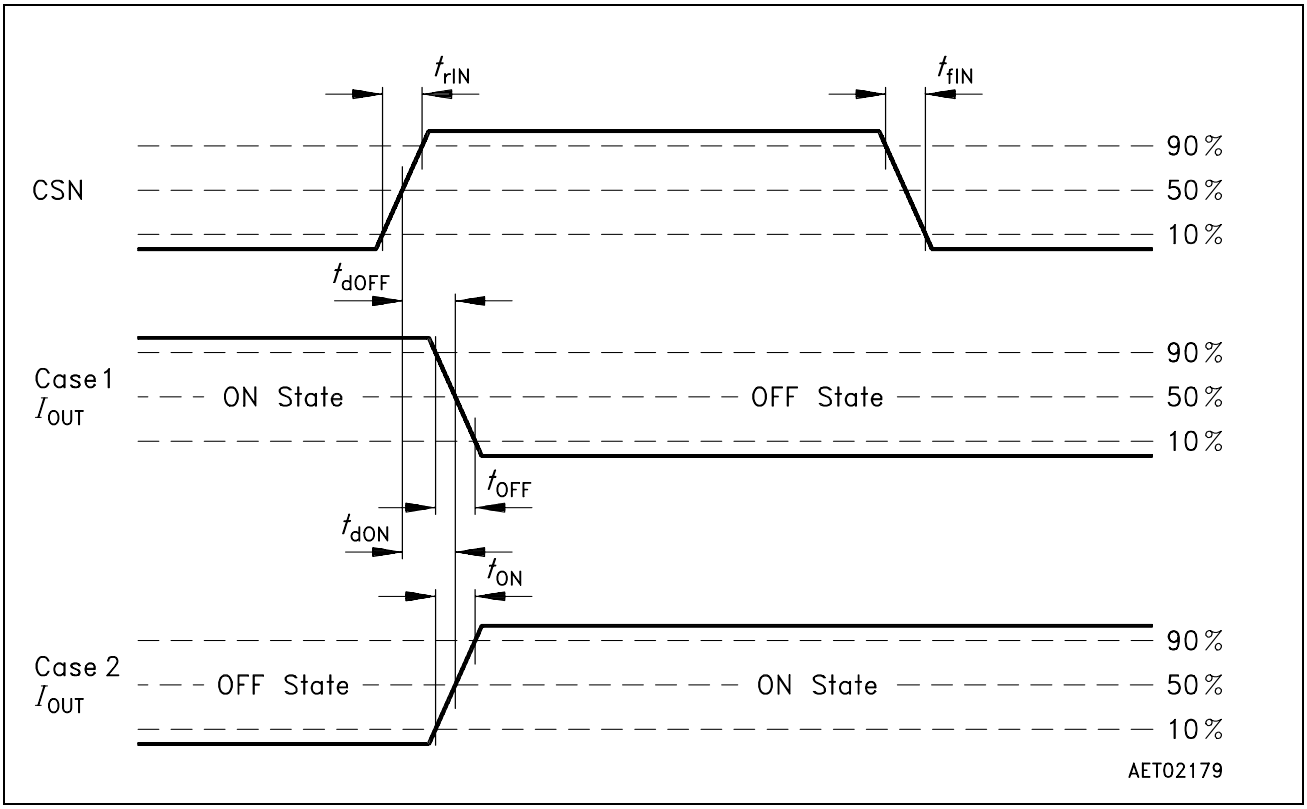


Figure 8: Turn OFF/ON Time

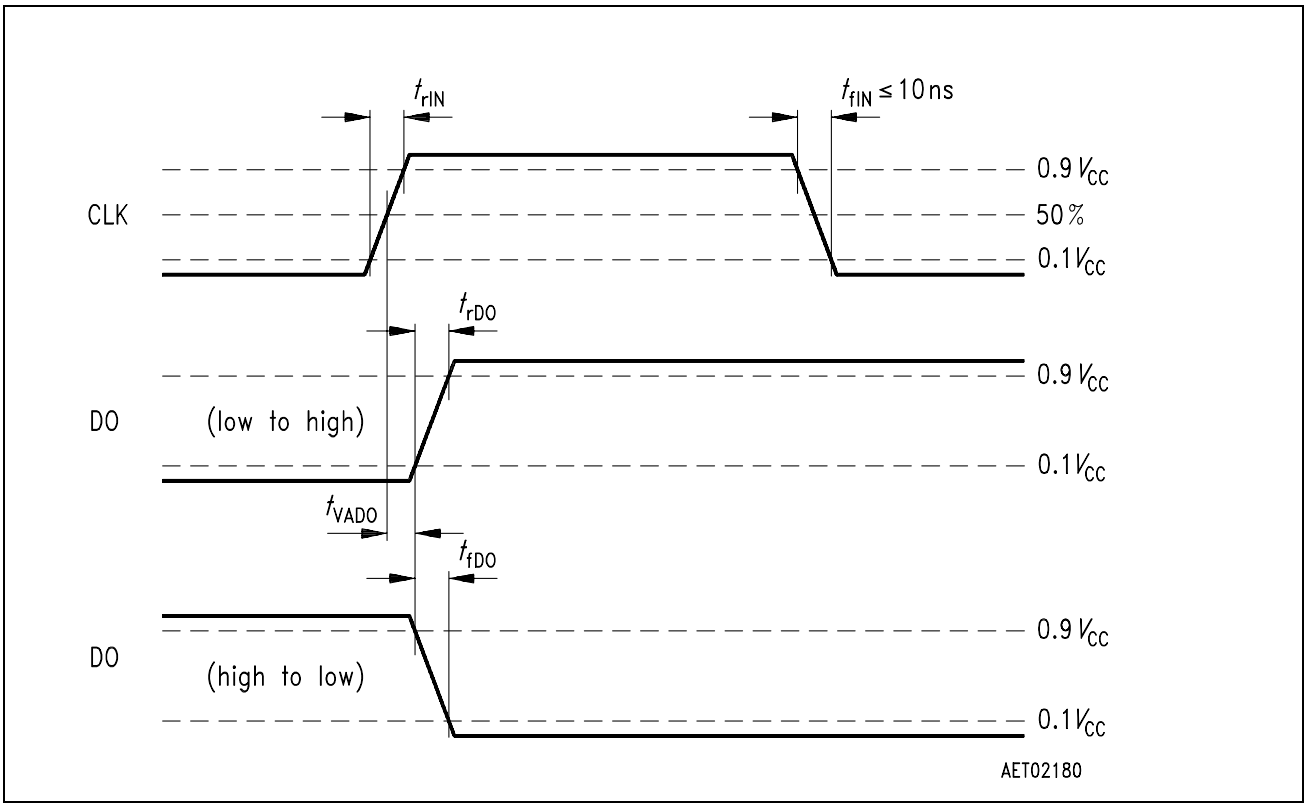


Figure 9: DO Valid Data Delay Time and Valid Time

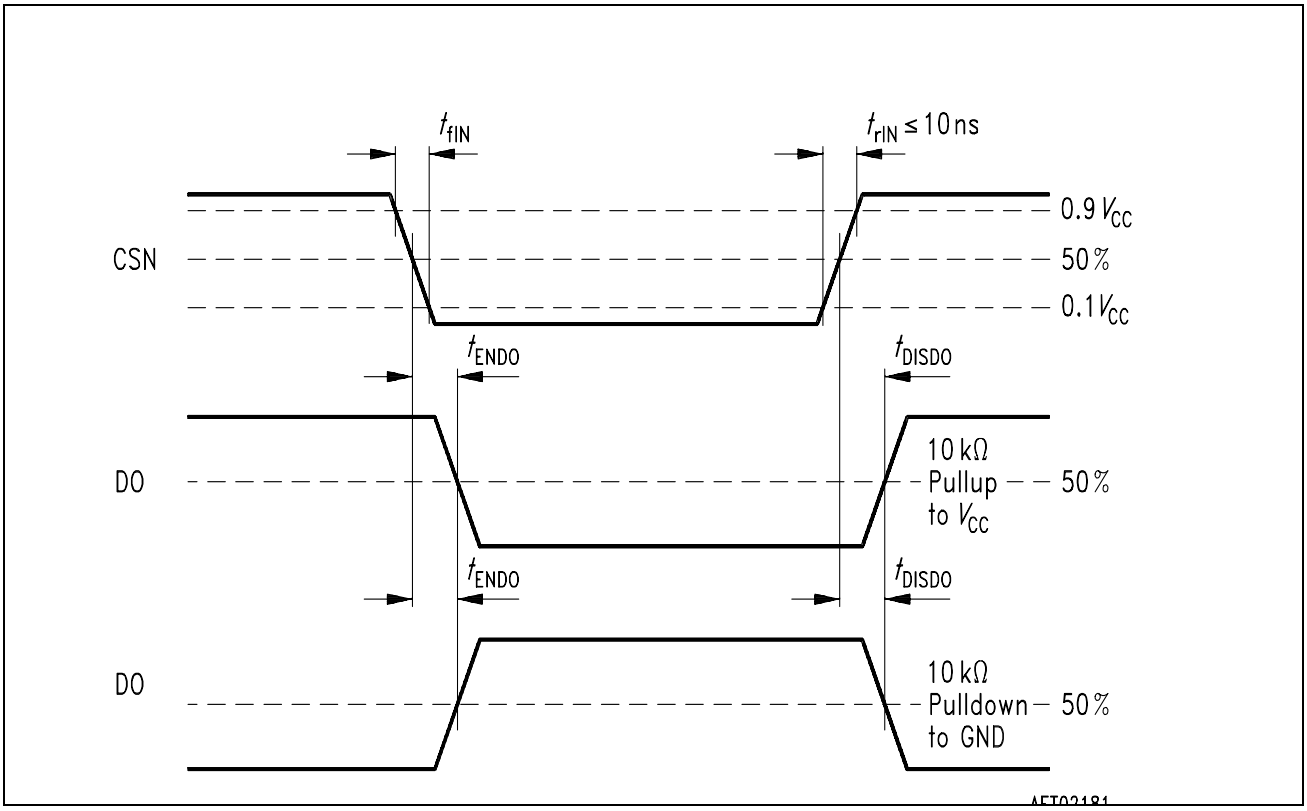


Figure 10: DO Enable and Disable Time

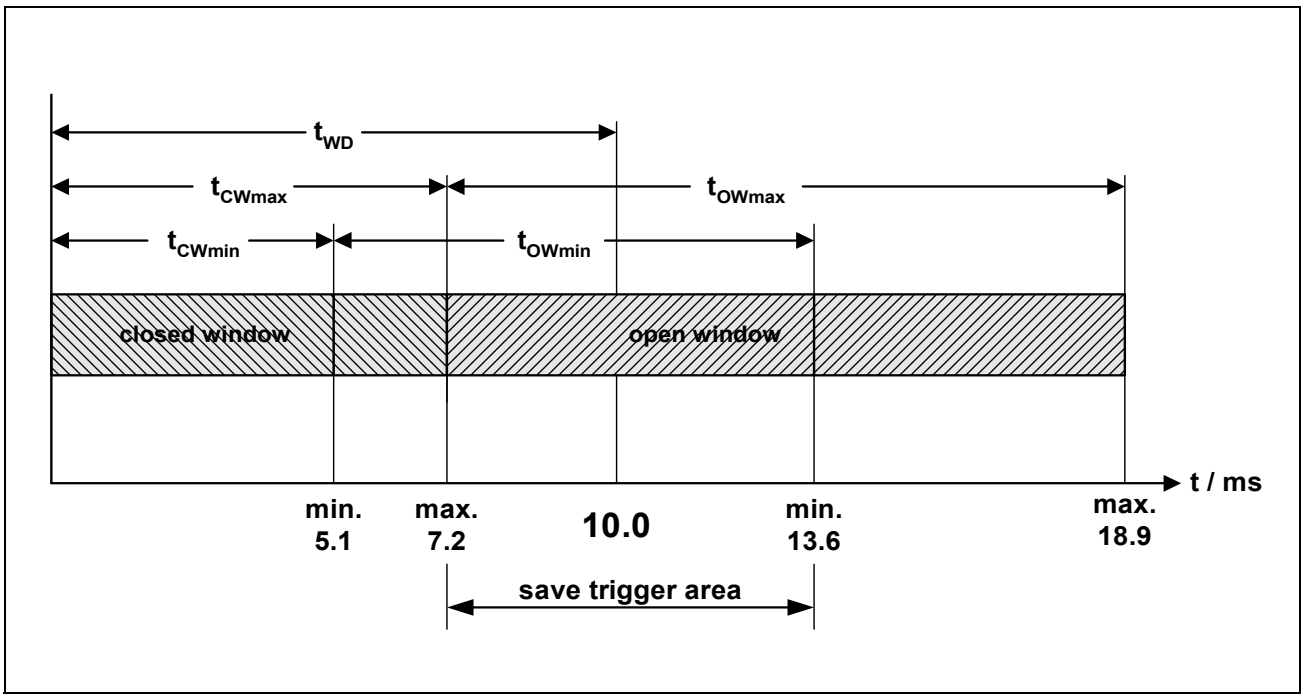


Figure 11: Watchdog Time-Out Definitions

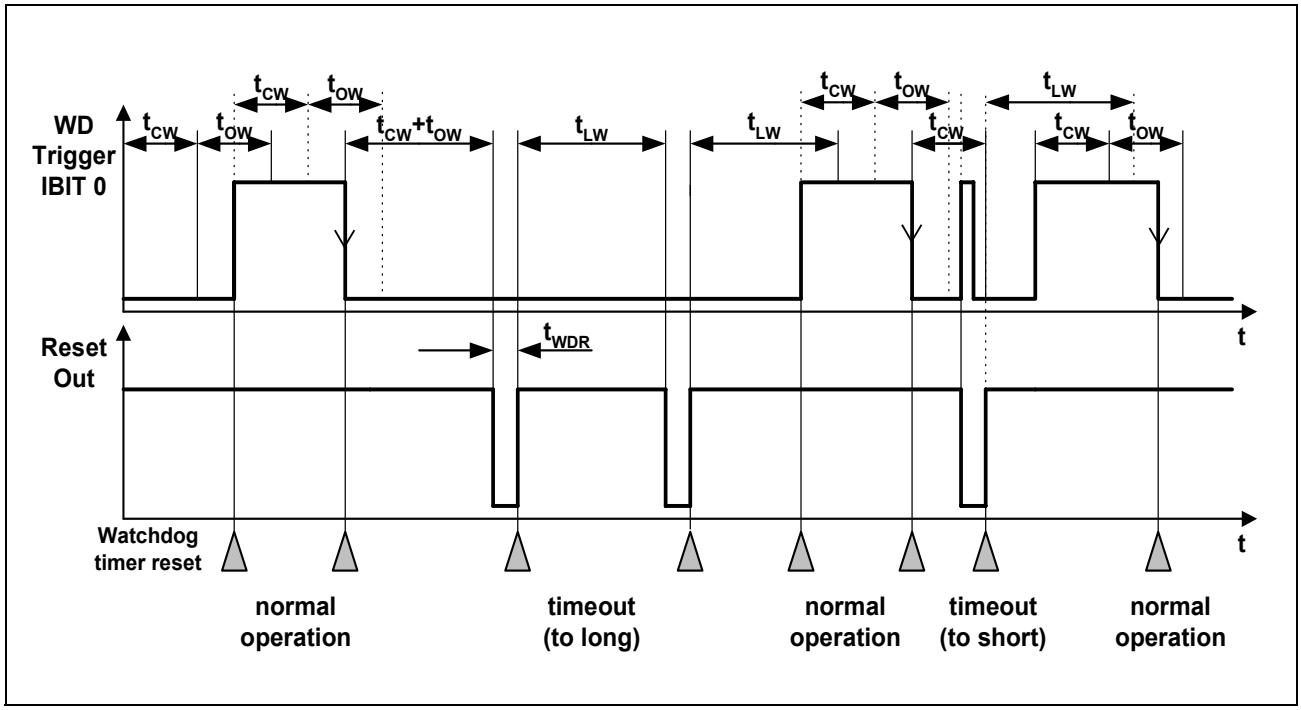


Figure 12: Watchdog Timing Diagram

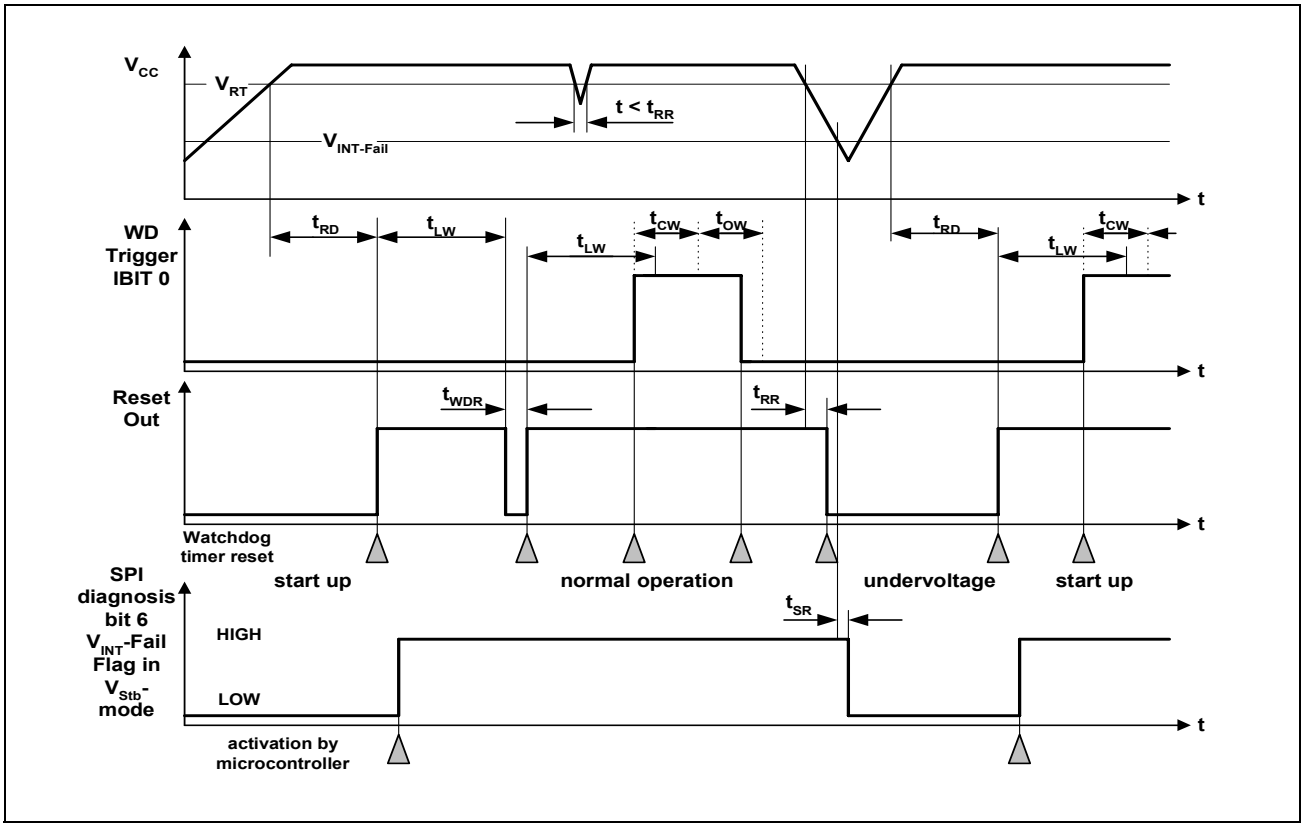


Figure 13: Reset Timing Diagram

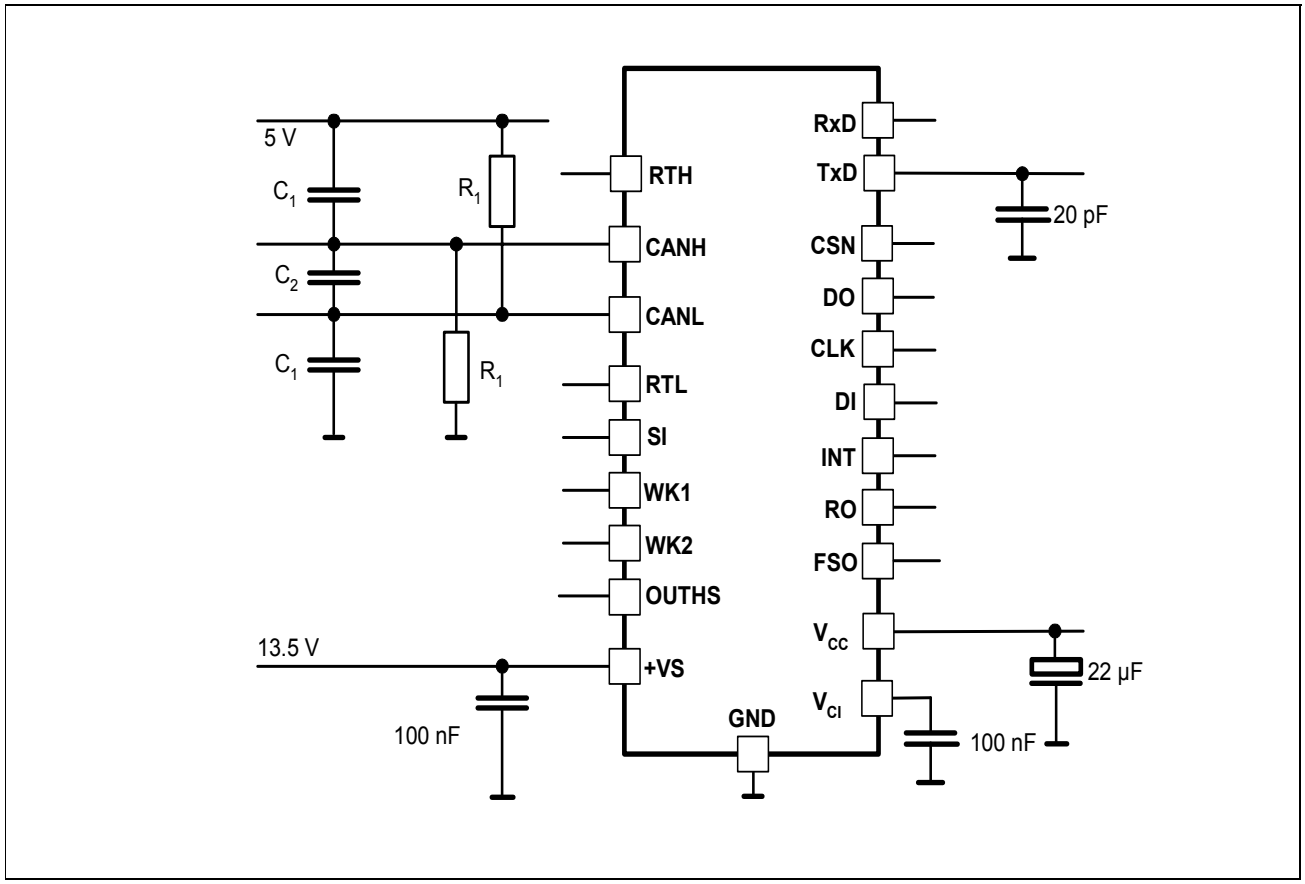


Figure 14: Test Circuit

9 Application

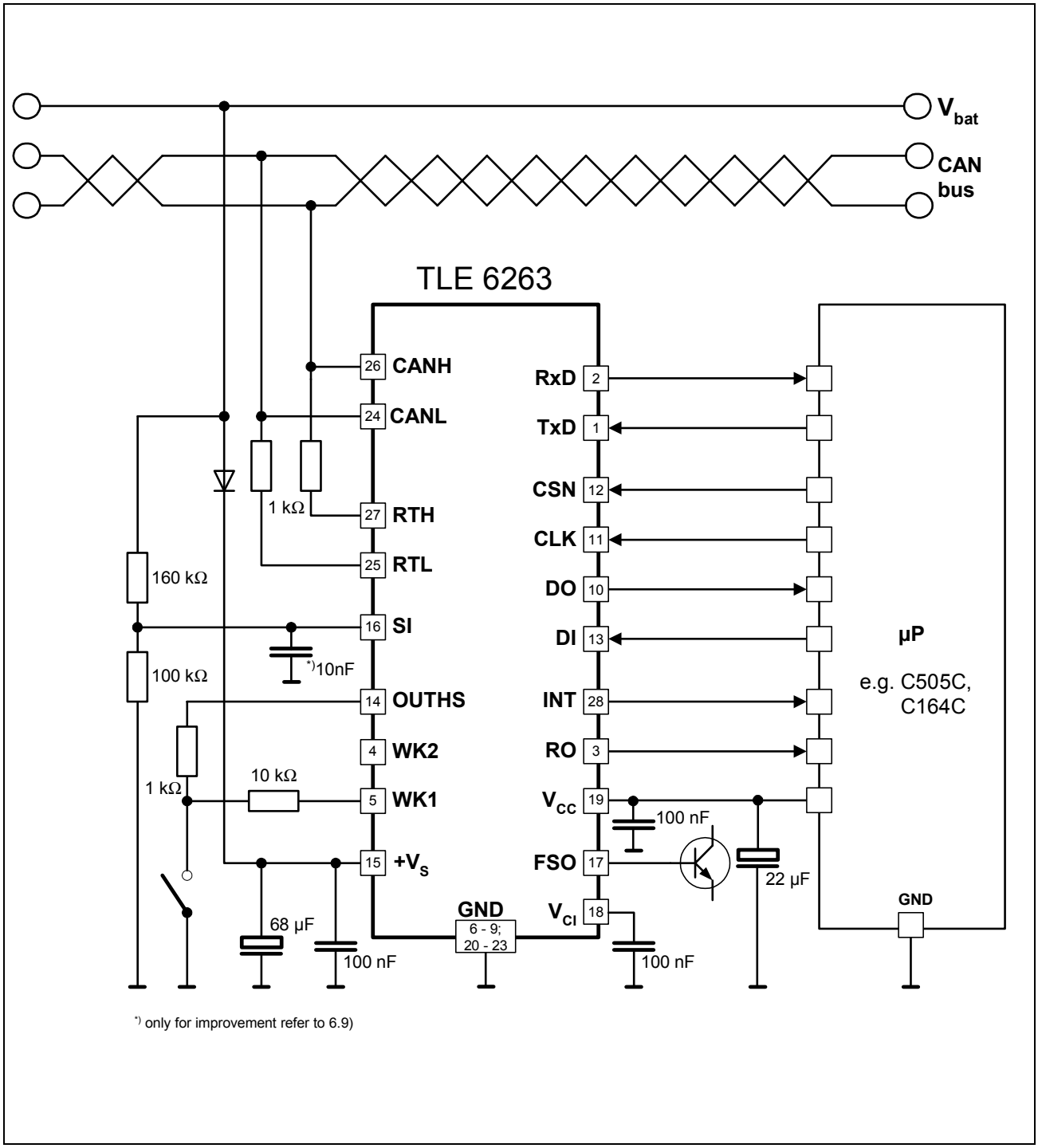
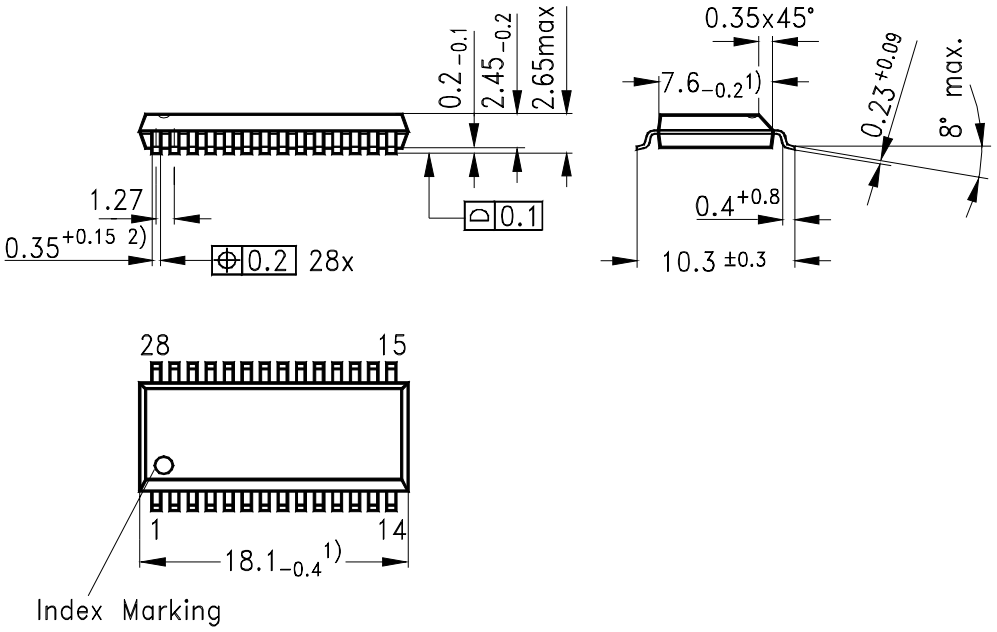


Figure 15: Application Circuit

10 Package Outlines

P-DSO-28-18
(Plastic Dual Small Outline Package)



1) Does not include plastic or metal protrusion of 0.15 max. per side
2) Does not include dambar protrusion of 0.05 max. per side

GPS05123

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”.
SMD = Surface Mounted Device

Dimensions in mm

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