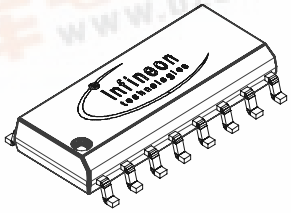
LIN-Transceiver LDO TLE 6285

Target Data Sheet



P-DSO-16-4

1 Overview

1.1 Features

- Single-wire transceiver, suitable for **LIN** protocol
- Transmission rate up to 20 kBaud
- Compatible to LIN specification
- Compatible to ISO 9141 functions
- Very low current consumption in sleep mode
- Control output for voltage regulator
- Short circuit proof to ground and battery
- Overtemperature protection
- Output voltage 5V, tolerance ≤ ± 2 %
- 150 mA output current capability
- Low-drop voltage
- Overtemperature protection
- Reverse polarity protection
- Short-circuit proof
- Adjustable reset threshold
- Wide temperature range
- Suitable for use in automotive electronics

Type	Ordering Code	Package
TLE 6285 G	on request	P-DSO-16-4

1.2 Description

The TLE 6285 is a single-wire transceiver with a LDO. It is chip by chip integrated circuit in a P-DSO-16-4 package. It works as an interface between the protocol controller and the physical bus. The TLE 6285 is especially suitable to drive the bus line in LIN systems in automotive and industrial applications. Further it can be used in standard ISO9141 systems.

In order to reduce the current consumption the TLE 6285 offers a sleep operation mode. In this mode a voltage regulator can be controlled in order to minimize the current consumption of the whole application (VR in sleep mode <1µA!). The on-chip voltage regulator (VR) is designed for this application but it is also possible to use an external

voltage regulator. A wake-up caused by a message on the bus enables the voltage regulator and sets the RxD output low until the device is switched to normal operation mode. To achieve proper operation of the µC, the device supplies a reset signal. The reset delay time is selected application specific by an external capacitor. The reset threshold is adjustable.

The IC is based on the Smart Power Technology SPT® which allows bipolar and CMOS control circuitry in accordance with DMOS power devices existing on the same monolithic circuit.

The TLE 6285 is designed to withstand the severe conditions of automotive applications.

1.3 Pin Configuration (top view)

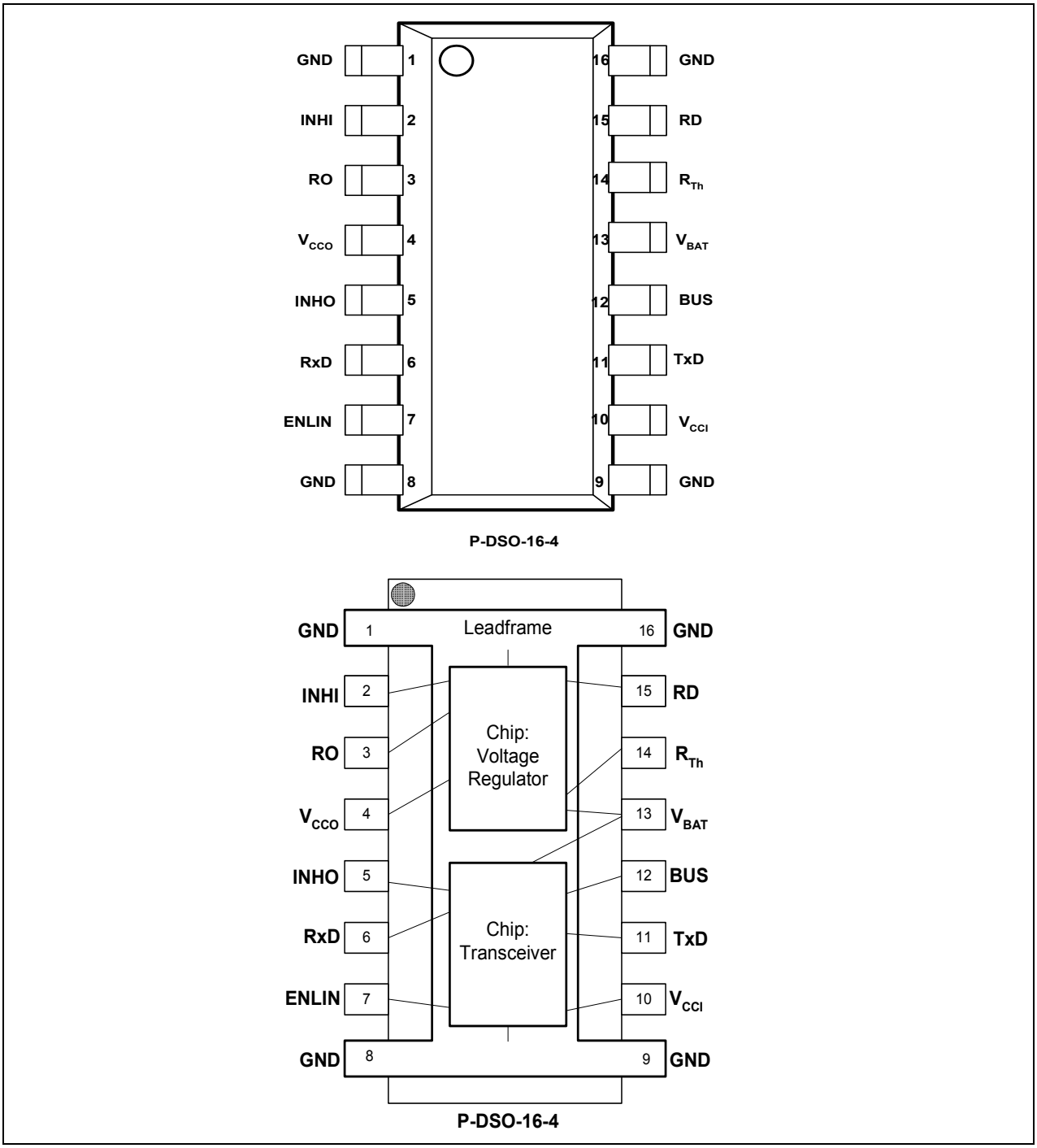


Figure 1 Pinout

1.4 Pin Definitions and Functions:

Pin No.	Symbol	Function
1,8,9,16	GND	**Ground;** place to cooling tabs to improve thermal behavior
2	INHI	**Inhibit Voltage Regulator Input;** TTL compatible, HIGH active (HIGH switches the VR on); connect to V_{BAT} if not needed
3	RO	**Reset Output;** open collector output connected to the output via a resistor of 20kΩ
4	V_{CCO}	**5V Output;** connected to GND with 22µF capacitor, ESC<3Ω
5	INHO	**Inhibit LIN Output;** to control a voltage regulator
6	RxD	**Receive Data Output;** internal 30kΩ pull up to Vs, LOW in dominat state
7	ENLIN	**Enable LIN Input;** integrated 30kΩ pull down, transceiver in normal operation mode when HIGH
10	V_{CCI}	**5V Supply Input;** V_{cc} input to supply the LIN transceiver
11	TxD	**Transmit Data Input;** internal 30kΩ pull up to Vs, LOW in dominant state
12	BUS	**LIN BUS Output/Input;** internal 30kΩ pull up to Vs, LOW in dominant state
13	V_{BAT}	**Battery Supply Input;** a reverse current protection diode is required, block GND with 100nF ceramic capacitor and 22µF capacitor
14	R_{Th}	**Reset Threshold;** internal defined typical 4.6V, adjustable down to 3.5V according to the voltage level on this pin; connect to GND if not needed
15	RD	**Reset delay;** connected to ground via external delay capacitor

1.5 Functional Block Diagram

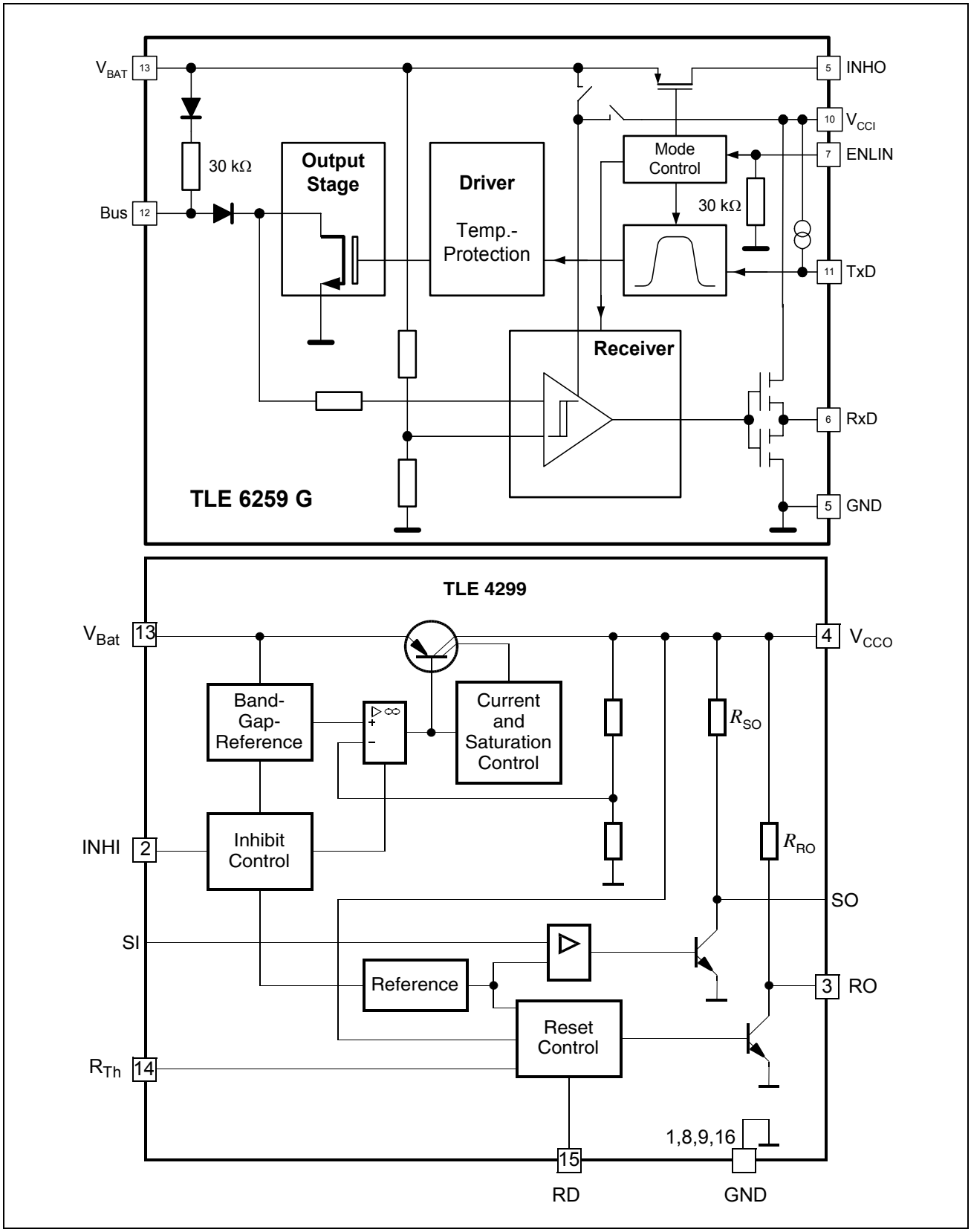


Figure 2 Block Diagram

2 Circuit Description

The TLE 6285 is a single-wire transceiver combined with a LDO. It is a chip by chip integrated circuit in a P-DSO-16-4 package. It works as an interface between the protocol controller and the physical bus. The TLE 6285 is especially suitable to drive the bus line in LIN systems in automotive and industrial applications. Further it can be used in standard ISO9141 systems. The on-chip voltage regulator with watchdog is designed for sleep mode applications but it is also possible to use an external voltage regulator.

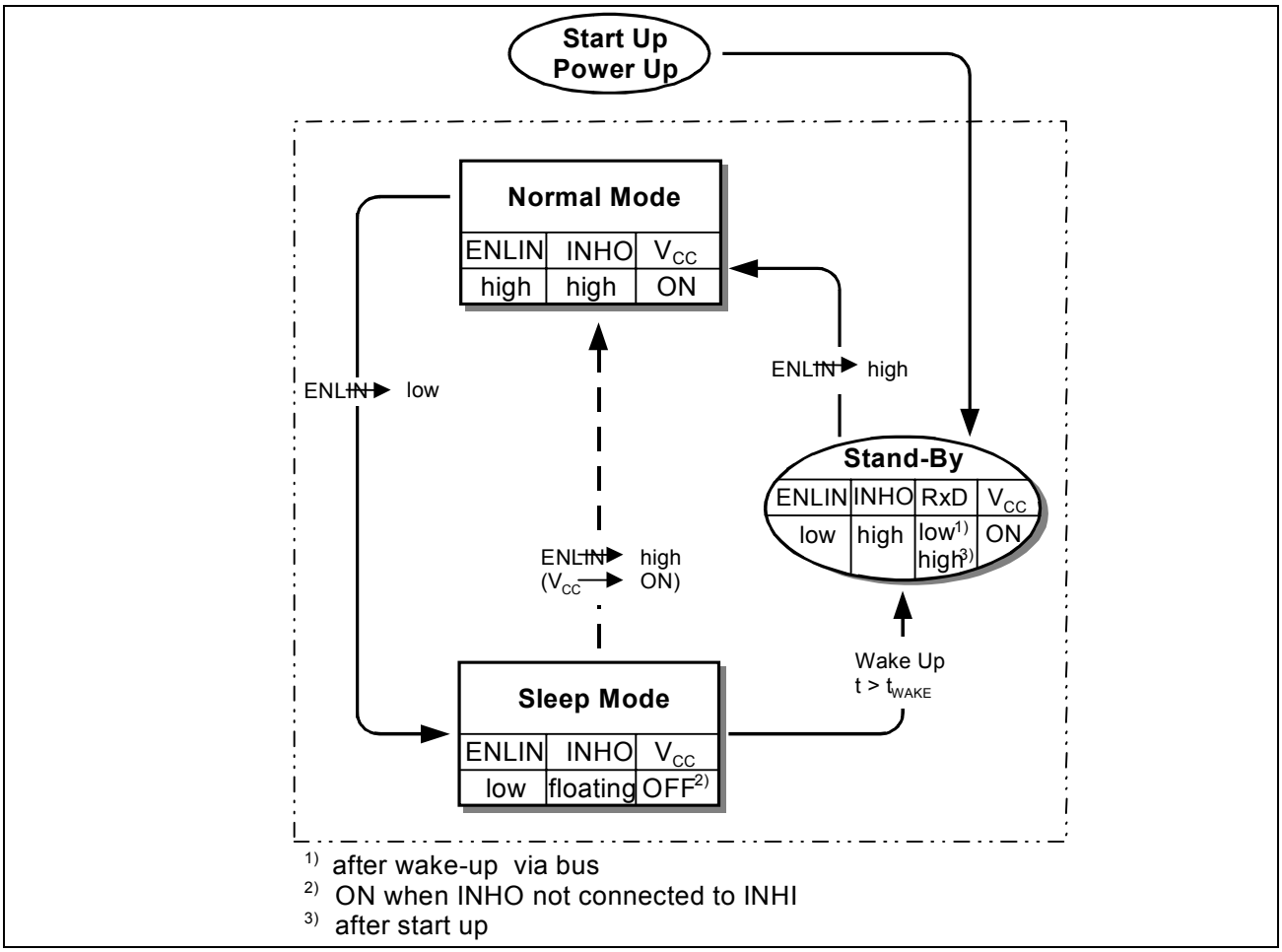


Figure 3 Operation Mode State Diagram

2.1 Operation Modes

In order to reduce the current consumption the TLE 6285 offers a sleep operation mode. This mode is selected by switching the enable input EN low (see **figure 3**, state diagram). In the sleep mode a voltage regulator can be controlled via the INHO output in order to minimize the current consumption of the whole application. A wake-up caused by a message on the communication bus automatically enables the voltage regulator by switching the INHO output high. In parallel the wake-up is indicated by setting the RxD output low. When entering the normal mode this wake-up flag is reset and the RxD output is released to transmit the bus data.

In case the voltage regulator control input is not connected to INH output or the microcontroller is active respectively, the TLE6285 can be set in normal operation mode without a wake-up via the communication bus.

2.2 LIN Transceiver

The LIN Transceiver has already a pull up resistor of 30kΩ as termination implemented. There is also a diode in this path, to protect the circuit from feedback of voltages from the bus line to the power supply. To configure the TLE 6285 as a master node, an additional external termination resistor of 1kΩ is required. To avoid reverse currents from the bus line into the battery supply line in case of an unpowered node, it is also recommended to place a diode in series to the external pull up. For small systems (low bus capacitance) the EMC performance of the system is supported by an additional capacitor of at least 1nF in the master node (see figure 6, application circuit).

An capacitor of 10µF at the supply voltage input V_S buffers the input voltage. In combination with the required reverse polarity diode this prevents the device from detecting power down conditions in case of negative transients on the supply line.

2.3 Input Capacitor

The input capacitor C_I is necessary for compensation of line influences. Using a resistor of approx. 1 Ω in series with C_I, the oscillating circuit consisting of input inductivity and input capacitance can be damped. The output capacitor is necessary for the stability of the regulating circuit. Stability is guaranteed at values ≥ 22 µF and an ESR of ≤ 5 Ω within the operating temperature range. For small tolerances of the reset delay the spread of the capacitance of the delay capacitor and its temperature coefficient should be noted.

2.4 Voltage regulator

The 6285 incorporates a PNP based very low drop linear voltage regular. It regulates the output voltage to V_{CC} = 5 V for an input voltage range of 5.5 V ≤ V_I ≤ 45 V. The control circuit protects the device against potential caused by damages overcurrent and overtemperature.

The internal control circuit achieves a 5 V output voltage with a tolerance of ± 2% in the temperature range of T_j = – 40 to 150 °C.

The device includes a power on reset and an under voltage reset function with adjustable reset delay time and adjustable reset switching threshold as well as a sense control/early warning function. The device includes an inhibit function to disable it when the ECU is not used for example while the motor is off.

The reset logic compares the output voltage V_{CC} to an internal threshold. If the output voltage drops below this level, the external reset delay capacitor C_D is discharged. When V_D is lower than V_{LD}, the reset output RO is switched Low. If the output voltage drop is

very short, the V_{LD} level is not reached and no reset-signal is asserted. This feature avoids resets at short negative spikes at the output voltage e.g. caused by load changes.

As soon as the output voltage is more positive than the reset threshold, the delay capacitor is charged with constant current. When the voltage reaches V_{UD} the reset output RO is set High again.

The reset threshold is either the internal defined V_{RT} voltage (typical 4.6 V) or can be lowered by a voltage level at the R_{Th} input down to 3.5 V. The reset delay time and the reset reaction time are defined by the external capacitor C_D. The reset function is active down to V_I = 1 V.

The device is capable to supply 150 mA. For protection at high input voltage above 25 V, the output current is reduced (SOA protection).

2.5 Reset

The power on reset feature is necessary for a defined start of the microprocessor when switching on the application. For the reset delay time after the output voltage of the regulator is above the reset threshold, the reset signal is set High again. The reset delay time is defined by the reset delay capacitor C_D at pin RD (refer to **figure 4 and 5**).

The under-voltage reset circuitry supervises the output voltage. In case V_Q decreases below the reset threshold the reset output is set LOW after the reset reaction time. The reset LOW signal is generated down to an output voltage V_{CC} to 1 V. Both the reset reaction time and the reset delay time is defined by the capacitor value.

The power on reset delay time is defined by the charging time of an external delay capacitor C_D.

$$C_D = (t_d \times I_D) / \Delta V \quad [1]$$

With C_D reset delay capacitor
t_d reset delay time
ΔV = V_{UD}, typical 1.8 V for power up reset
ΔV = $V_{UD} - V_{LD}$ typical 1.35 V for undervoltage reset
I_D charge current typical 6.5 µA

For a delay capacitor C_D =100 nF the typical power on reset delay time is 28 ms.

The reset reaction time t_{RR} is the time it takes the voltage regulator to set reset output LOW after the output voltage has dropped below the reset threshold. It is typically 1 µs for delay capacitor of 100 nF. For other values for C_D the reaction time can be estimated using the following equation:

$$t_{RR} = 10 \text{ ns / nF} \times C_D \quad [2]$$

The reset output is an open collector output with a pull-up resistor of typical 20 kΩ to Q. An external pull-up can be added with a resistor value of at least 5.6 kΩ.

In addition the reset switching threshold can be adjusted by an external voltage divider. The feature is useful for microprocessors which guarantee safe operation down to voltages below the internally set reset threshold of 4.65 V typical.

If the internal used reset threshold of typical 4.65 V is used, the pin RADJ has to be connected to GND.

If a lower reset threshold is required by the system, a voltage divider defines the reset threshold V_{Rth} between 3.5 V and 4.60 V:

$$V_{Rth} = V_{RADJ\ TH} \times (R_1 + R_2) / R_2 \quad [3]$$

$V_{RADJ\ TH}$ is typical 1.36 V.

3 Electrical Characteristics

3.1 Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Voltages					
Supply voltage	V_{CC}	-0.3	6	V	
Battery supply voltage	V_S	-0.3	40	V	
Bus input voltage	V_{bus}	-20	32	V	
Bus input voltage	V_{bus}	-20	40	V	t < 1 s
Logic voltages at EN, TxD, RxD	V_I	-0.3	V_{CC} + 0.3	V	0 V < V_{CC} < 5.5 V
Input voltages at INH	V_{INH}	-0.3	V_S + 0.3	V	
Output current at INH	I_{INH}		1	mA	
Reset output voltage	V_R	– 0.3	7	V	
Reset delay voltage	V_D	– 0.3	7	V	
Output voltage Vcc	V_Q	– 0.3	7	V	
INHIBIT voltage	V_{INH}	– 40	45	V	
Reset Threshold voltage	V_{Th}	– 0.3	7	V	
Reset Threshold current	I_{Th}	– 10	10	mA	
Electrostatic discharge voltage at Vs, Bus	V_{ESD}	-4	4	kV	human body model (100 pF via 1.5 kΩ)
Electrostatic discharge voltage	V_{ESD}	-2	2	kV	human body model (100 pF via 1.5 kΩ)
Temperatures					
Junction temperature	T_j	-40	150	°C	

Note: Maximum ratings are absolute ratings; exceeding any one of these values may cause irreversible damage to the integrated circuit.

3.2 Operating Range

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Supply voltage	V_{CC}	4.5	5.5	V	
Battery Supply Voltage	V_S	6	20	V	
Junction temperature	T_j	– 40	150	°C	–

Thermal Shutdown (junction temperature)

Thermal shutdown temp.	T_{jSD}	150	170	190	°C
Thermal shutdown hyst.	ΔT	–	10	–	K

Thermal Resistances

Junction ambient LIN	$R_{thj\text{-}a}$	–	185	K/W	–
Junction ambient Vreg	$R_{thj\text{-}a}$	–	70	K/W	–

3.3 Electrical Characteristics

4.5 V < V_{CC} < 5.5 V; 6.0 V < V_S < 20 V; R_L = 1 kΩ; V_{EN} > $V_{EN,ON}$; -40 °C < T_j < 125 °C; all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Remarks
		min.	typ.	max.		
Current Consumption LIN						
Current consumption	I_{CC}		0.5	1.5	mA	recessive state; $V_{TxD} = V_{CC}$
Current consumption	I_S		0.5	1.0	mA	recessive state; $V_{TxD} = V_{CC}$
Current consumption	I_{CC}		0.7	2.0	mA	dominant state; V_{TxD} = 0 V
Current consumption	I_S		0.7	1.5	mA	dominant state; V_{TxD} = 0 V
Current consumption	I_S		20	30	µA	sleep mode; T_j = 25 °C
Current consumption	I_S		20	40	µA	sleep mode
Current Consumption Vreg						
Current consumption; $I_q = I_I - I_Q$	I_q	–	65	105	µA	Inhibit ON; $I_Q \leq 1$ mA, T_j < 85 °C
Current consumption; $I_q = I_I - I_Q$	I_q	–	65	100	µA	Inhibit ON; $I_Q \leq 1$ mA, T_j = 25 °C
Current consumption; $I_q = I_I - I_Q$	I_q	–	170	500	µA	Inhibit ON; I_Q = 10 mA
Current consumption; $I_q = I_I - I_Q$	I_q	–	0.7	2	mA	Inhibit ON; I_Q = 50 mA
Current consumption; $I_q = I_I - I_Q$	I_q	–	–	1	µA	V_{INHI} = 0 V; T_j = 25 °C
Receiver Output R×D						
HIGH level output current	$I_{RD,H}$		-0.7	-0.4	mA	V_{RD} = 0.8 x V_{CC},
LOW level output current	$I_{RD,L}$	0.4	0.7		mA	V_{RD} = 0.2 x V_{CC},

3.3 Electrical Characteristics (cont'd)

4.5 V < V_{CC} < 5.5 V; 6.0 V < V_S < 20 V; R_L = 1 kΩ; V_{EN} > $V_{EN,ON}$; -40 °C < T_j < 125 °C; all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Remarks
		min.	typ.	max.		
Bus receiver						
Receiver threshold voltage, recessive to dominant edge	$V_{bus,rd}$	0.44 x V_S	0.48 x V_S		V	-8 V < V_{bus} < $V_{bus,dom}$
Receiver threshold voltage, dominant to recessive edge	$V_{bus,dr}$		0.52 x V_S	0.56 x V_S	V	$V_{bus,rec}$ < V_{bus} < 20 V
Receiver hysteresis	$V_{bus,hys}$	0.02 x V_S	0.04 x V_S	0.06 x V_S	mV	$V_{bus,hys}$ = $V_{bus,rec}$ - $V_{bus,dom}$
wake-up threshold voltage	V_{wake}	0.40 x V_S	0.55 x V_S	0.70 x V_S	V	
Transmission Input T×D						
HIGH level input voltage threshold	$V_{TD,H}$		2.9	0.7 x V_{CC}	V	recessive state
TxD input hysteresis	$V_{TD,hys}$	300	600		mV	
LOW level input voltage threshold	$V_{TD,L}$	0.3 x V_{CC}	2.1		V	dominant state
TxD pull up current	I_{TD}	-150	-110	-80	µA	V_{TxD} < 0.3 Vcc
Bus transmitter						
Bus recessive output voltage	$V_{bus,rec}$	0.9 x V_S		V_S	V	V_{TxD} = V_{CC}
Bus dominant output voltage	$V_{bus,dom}$	0		1.5	V	V_{TxD} = 0 V;
Bus short circuit current	$I_{bus,sc}$	40	85	125	mA	$V_{bus,short}$ = 13.5 V
Leakage current	$I_{bus,lk}$	-350	-100		µA	V_{CC} = 0 V, V_S = 0 V, V_{bus} = -8 V, T_j < 85 °C
			5	20	µA	V_{CC} = 0 V, V_S = 0 V, V_{bus} = 20 V, T_j < 85 °C
Bus pull up resistance	R_{bus}	20	30	47	kΩ	

3.3 Electrical Characteristics (cont'd)

4.5 V < V_{CC} < 5.5 V; 6.0 V < V_S < 20 V; R_L = 1 kΩ; V_{EN} > $V_{EN,ON}$; -40 °C < T_j < 125 °C; all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Remarks
		min.	typ.	max.		
Enable input (pin ENLIN)						
HIGH level input voltage threshold	$V_{EN,on}$		2.8	0.7 x V_{CC}	V	normal mode
LOW level input voltage threshold	$V_{EN,off}$	0.3 x V_{CC}	2.2		V	low power mode
EN input hysteresis	$V_{EN,hys}$	300	600		mV	
EN pull down resistance	R_{EN}	15	30	60	kΩ	
Inhibit output (pin INHO)						
HIGH level drop voltage $\Delta V_{INH} = V_S - V_{INH}$	ΔV_{INH}		0.5	1.0	V	I_{INHO} = - 0.15 mA
Leakage current	$I_{INH,lk}$	- 5.0		5.0	µA	sleep mode; V_{INHO} = 0 V
Vcc Output (pin Vcco)						
Output voltage	V_Q	4.90	5.00	5.10	V	1 mA ≤ I_Q ≤ 100 mA; 6 V ≤ V_I ≤ 16 V
Output voltage	V_Q	4.85	5.00	5.15	V	I_Q ≤ 150 mA; 6 V ≤ V_I ≤ 16 V
Current limit	I_Q	250	400	500	mA	–
Drop voltage	V_{dr}	–	0.22	0.5	V	I_Q = 100 mA[1)]
Load regulation	ΔV_Q	–	5	30	mV	I_Q = 1 mA to 100 mA
Line regulation	ΔV_Q	–	10	25	mV	V_I = 6 V to 28 V; I_Q = 1 mA
Power Supply Ripple rejection	PSRR	–	66	–	dB	f_r = 100 Hz; V_r = 1 V_{SS}; I_Q = 100 mA
Output voltage	V_Q	4.90	5.00	5.10	V	5 mA ≤ I_Q ≤ 150 mA; 6 V ≤ V_I ≤ 28 V
Output voltage	V_Q	4.90	5.00	5.10	V	6 V ≤ V_I ≤ 32 V; I_Q = 100 mA; T_j = 100 °C

3.3 Electrical Characteristics (cont'd)

4.5 V < V_{CC} < 5.5 V; 6.0 V < V_S < 20 V; R_L = 1 kΩ; V_{EN} > $V_{EN,ON}$; -40 °C < T_j < 125 °C; all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Remarks
		min.	typ.	max.		
Reset Generator (pins RO,RD)						
Switching threshold	V_{rt}	4.50	4.60	4.80	V	–
Reset pull up	R_{RO}	10	20	40	kΩ	–
Reset low voltage	V_R	–	0.17	0.40	V	V_Q < 4.5 V; internal R_{RO}; I_R = 1 mA
External reset pull up	$V_{R\ ext}$	5.6	–	–	kΩ	Pull up resistor to Q
Delay switching threshold	V_{DT}	1.5	1.85	2.2	V	–
Switching threshold	V_{ST}	0.40	0.50	0.60	V	–
Reset delay low voltage	V_D	–	–	0.1	V	V_Q < V_{RT}
Charge current	I_{ch}	4.0	8.0	12.0	µA	V_D = 1 V
Reset delay time	t_d	17	28	35	ms	C_D = 100 nF
Reset reaction time	t_{rr}	0.5	1.2	3.0	µs	C_D = 100 nF
Reset adjust switching threshold	$V_{RADJ\ TH}$	1.26	1.36	1.44	V	V_Q > 3.5 V
Inhibit Input (pin INHI)						
Inhibit OFF voltage range	$V_{\overline{INH}\ OFF}$	–	–	0.8	V	V_Q off
Inhibit ON voltage range	$V_{\overline{INH}\ ON}$	3.5	–	–	V	V_Q on
High input current	$I_{\overline{INH}\ ON}$	–	3	5	µA	V_{INHI} = 5 V
Low input current	$I_{\overline{INH}\ OFF}$	–	0.5	2	µA	V_{INHI} = 0 V

Note: The reset output is low within the range V_Q = 1 V to $V_{Q,rt}$

[1)] Drop voltage = V_i – V_Q (measured when the output voltage has dropped 100 mV from the nominal value obtained at 6 V input)

3.3 Electrical Characteristics (cont'd)

4.5 V < V_{CC} < 5.5 V; 6.0 V < V_S < 20 V; R_L = 1 kΩ; V_{EN} > $V_{EN,ON}$; -40 °C < T_j < 125 °C; all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Remarks
		min.	typ.	max.		
Dynamic Transceiver Characteristics						
falling edge slew rate	$S_{bus(L)}$	-3	-2.0	-1	V/µs	80% > V_{bus} > 20% C_{bus}= 3.3 nF; $T_{ambient}$ < 85 °C; V_{CC} = 5 V; V_S = 13.5 V
rising edge slew rate	$S_{bus(H)}$	1	1.5	3	V/µs	20% < V_{bus} < 80% C_{bus}= 3.3 nF; V_{CC} = 5 V; V_S = 13.5 V
Propagation delay TxD-to-RxD LOW (recessive to dominant)	$t_{d(L),TR}$	2	5	10	µs	C_{bus} = 3.3nF; V_{CC} = 5 V; V_S = 13.5 V C_{RxD} = 20 pF
Propagation delay TxD-to-RxD HIGH (dominant to recessive)	$t_{d(H),TR}$	2	5	10	µs	C_{bus} = 3.3 nF; V_{CC} = 5 V; V_S = 13.5 V C_{RxD} = 20 nF
Propagation delay TxD LOW to bus	$t_{d(L),T}$		1	4	µs	V_{CC} = 5 V
Propagation delay TxD HIGH to bus	$t_{d(H),T}$		1	4	µs	V_{CC} = 5 V
Propagation delay bus dominant to RxD LOW	$t_{d(L),R}$		1	4	µs	V_{CC} = 5V; C_{RxD} = 20pF
Propagation delay bus recessive to RxD HIGH	$t_{d(H),R}$		1	4	µs	V_{CC} = 5 V; C_{RxD} = 20 pF
Receiver delay symmetry	$t_{sym,R}$	-2		2	µs	$t_{sym,R}$ = $t_{d(L),R}$ - $t_{d(H),R}$
Transmitter delay symmetry	$t_{sym,T}$	-2		2	µs	$t_{sym,T}$ = $t_{d(L),T}$ - $t_{d(H),T}$
Wake-up delay time	t_{wake}	30	100	200	µs	

4 Diagrams

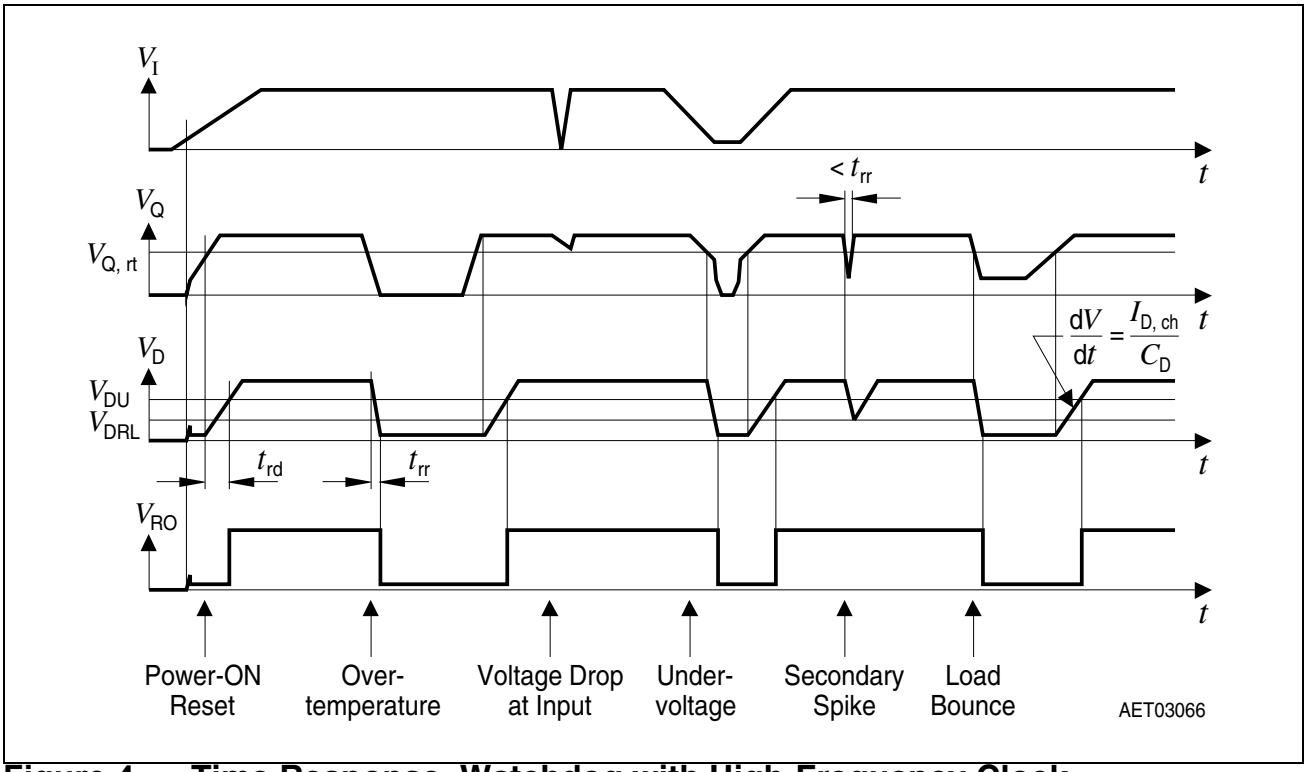
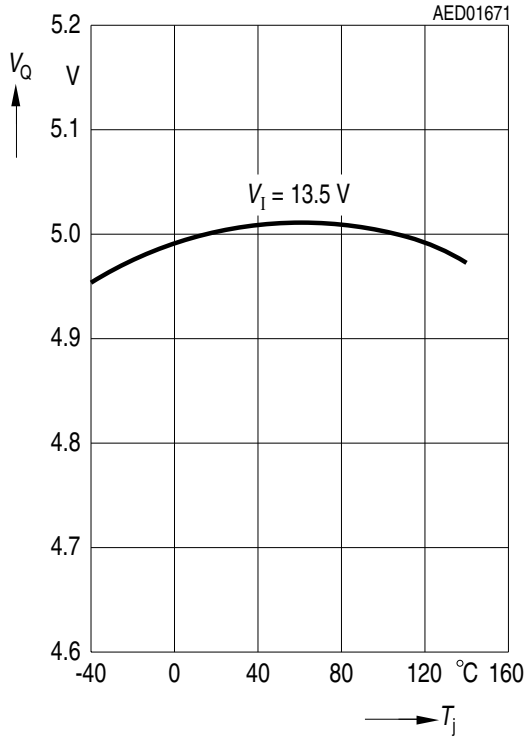


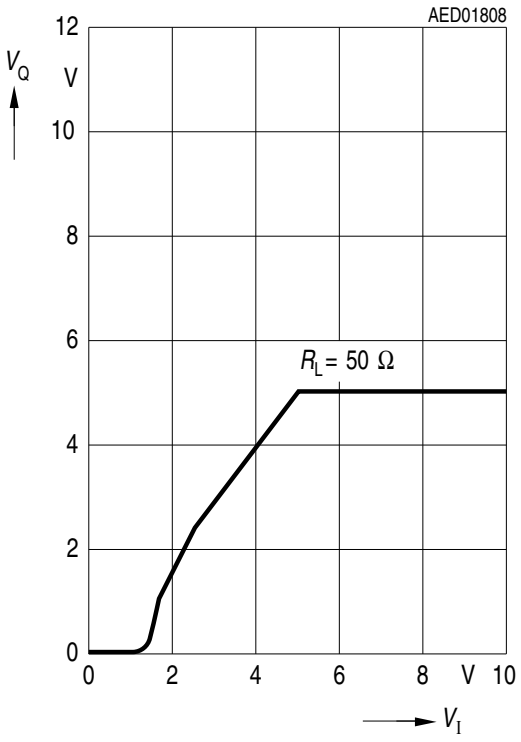
Figure 4 Time Response, Watchdog with High-Frequency Clock

Typical Performance Characteristics

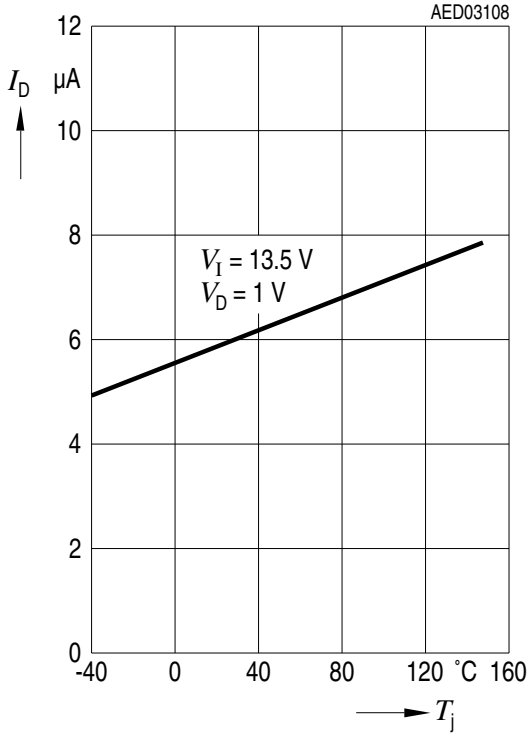
Output Voltage V_Q versus Temperature T_j



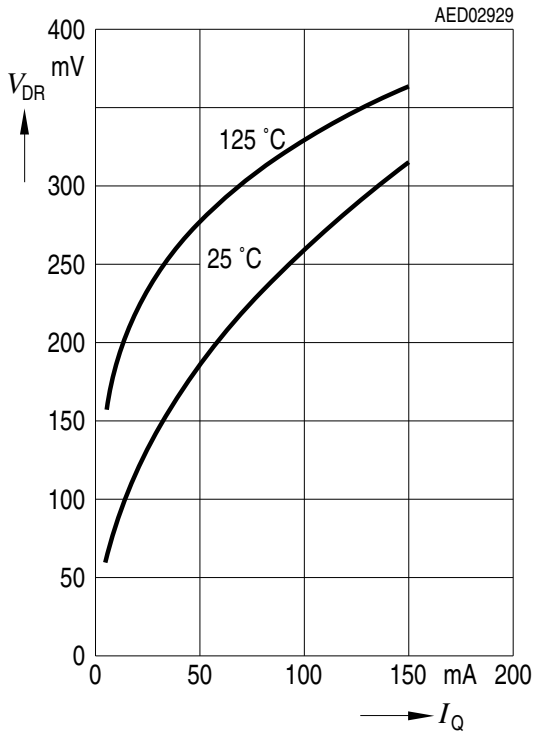
Output Voltage V_Q versus Input Voltage V_I



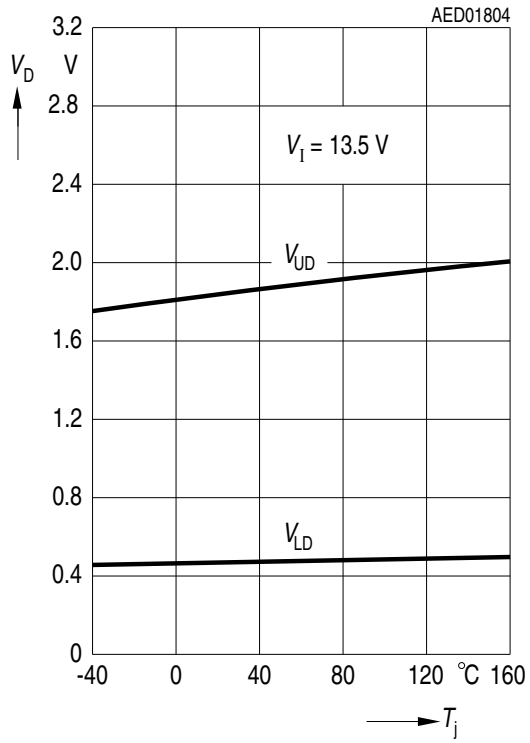
Charge Current I_{ch} versus Temperature T_j



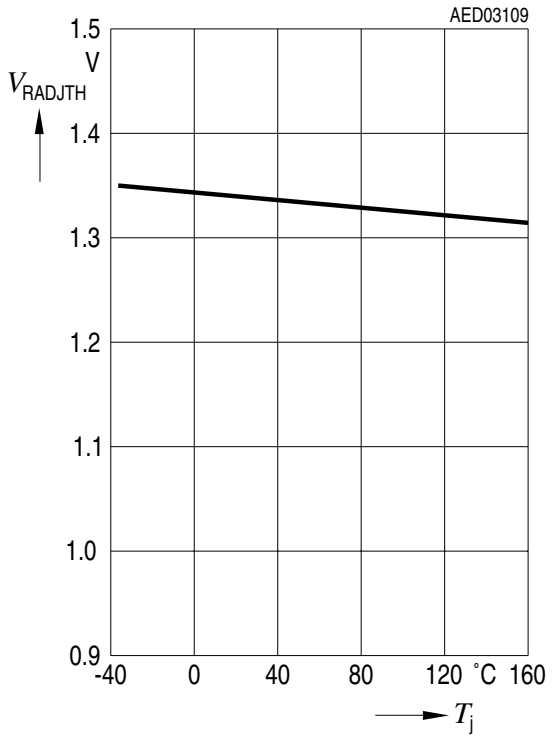
Drop Voltage V_{dr} versus Output Current I_Q



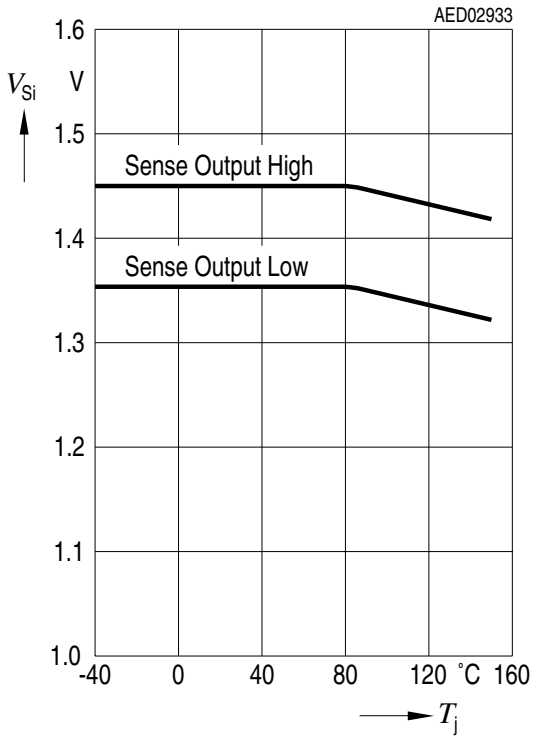
Switching Voltage V_{dt} and V_{st} versus Temperature T_j



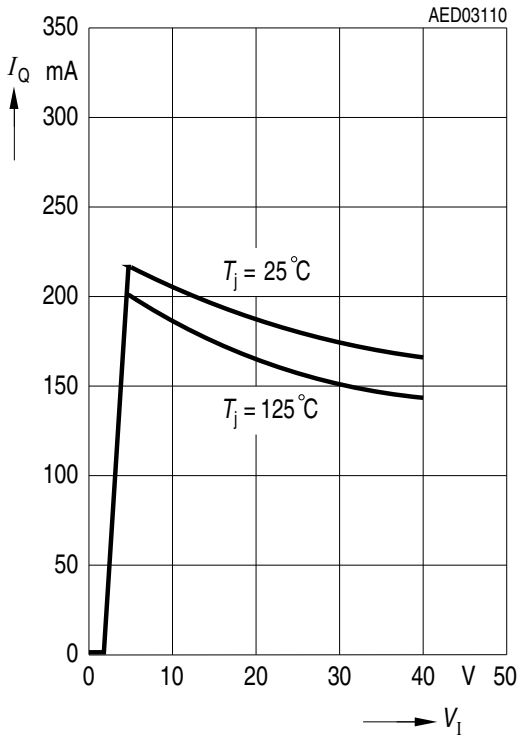
Reset Adjust Switching Threshold V_{RADJTH} versus Temperature T_j



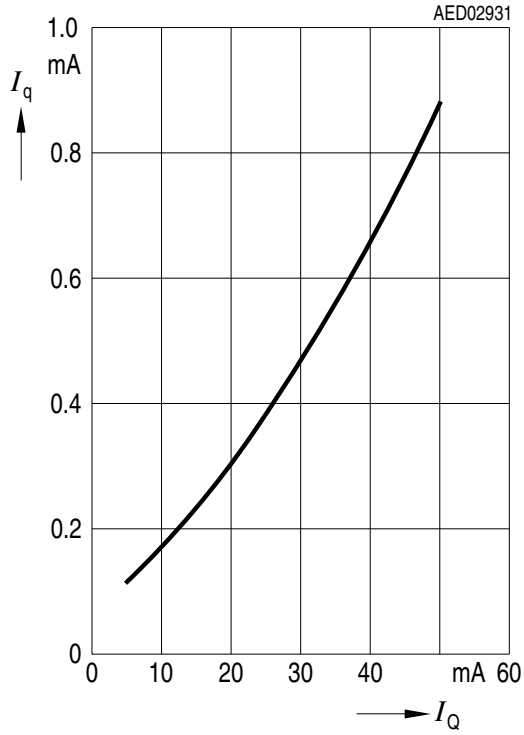
Sense Threshold V_{si} versus Temperature T_j



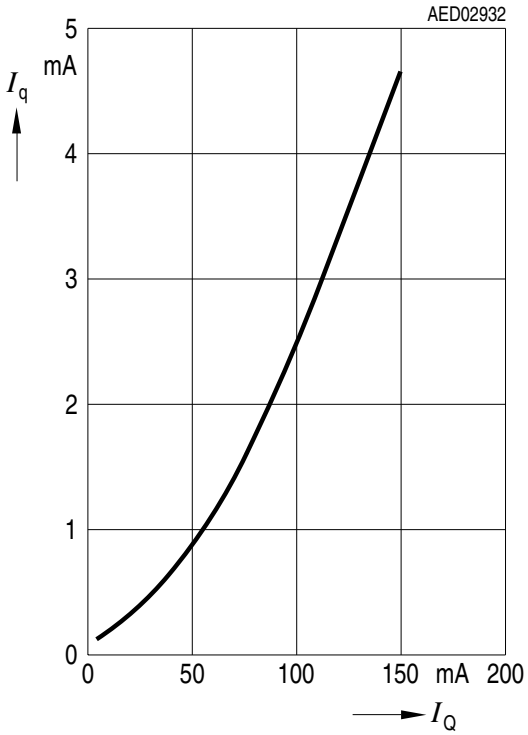
Output Current Limit I_Q versus Input Voltage V_I



Current Consumption I_q versus Output Current I_Q



Current Consumption I_q versus Output Current I_Q



5 Application

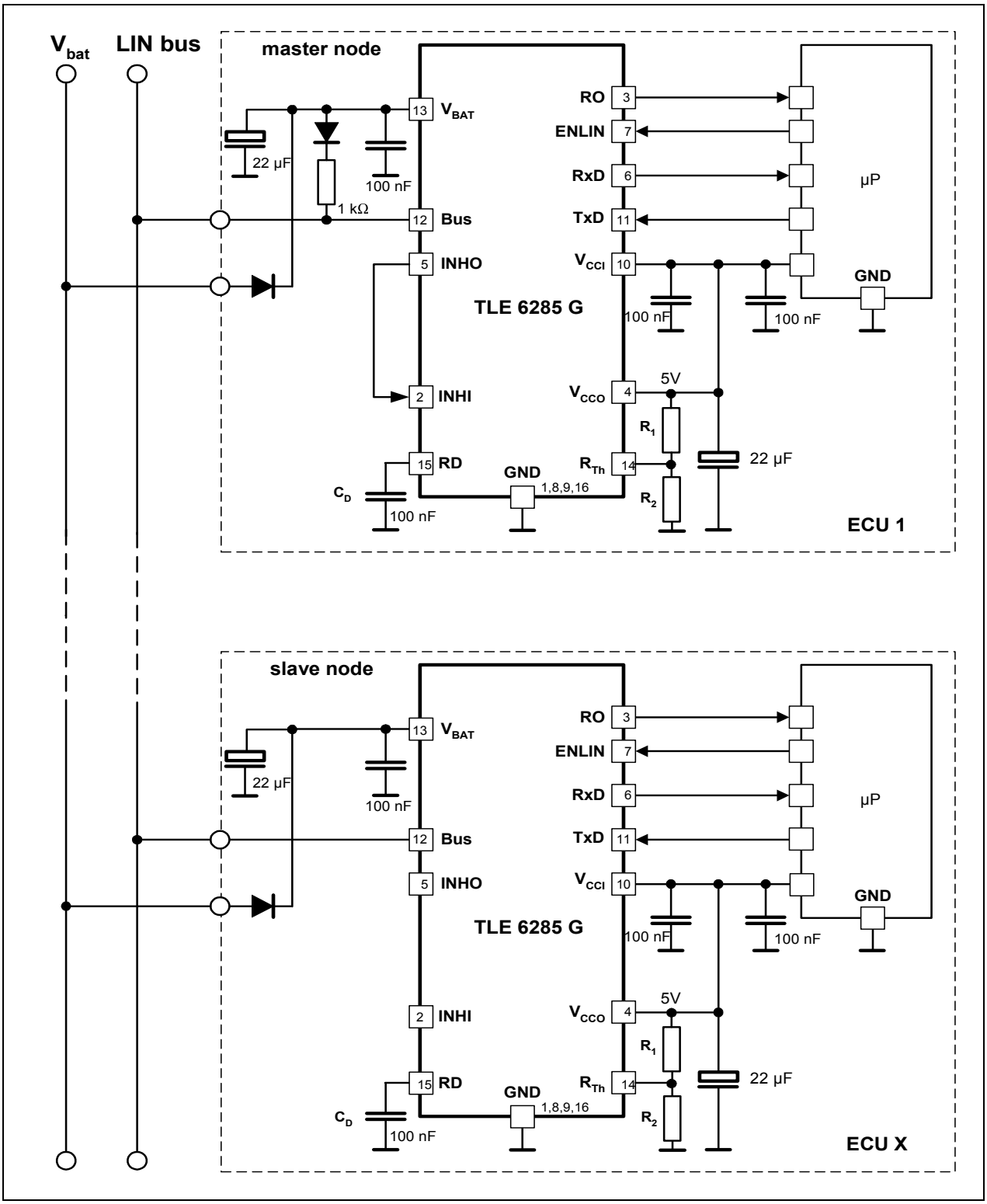
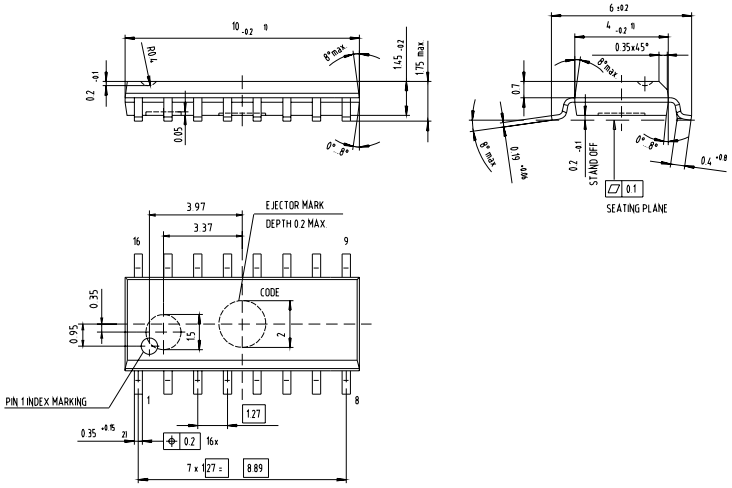


Figure 5 Application Circuit

6 Package Outlines

P-DSO-16-4
(Plastic Dual Small Outline Package)



Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”.

SMD = Surface Mounted Device

Dimensions in mm

Edition 1999-10-12

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