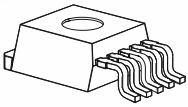
# 5-V Low Drop Voltage Regulator

# TLE 7276

## Features

- Output voltage 5 V ±2%
- Ultra low current consumption: typ. 20 µA
- 300 mA current capability
- Inhibit input
- Very low-drop voltage
- Short-circuit-proof
- Suitable for use in automotive electronics

P-TO252-5-1



P-TO263-5-1

## Functional Description

The TLE 7276 is a monolithic integrated low-drop voltage regulator for load currents up to 300 mA. An input voltage up to 42 V is regulated to $V_{Q,nom}$ = 5.0 V with a precision of ±2%. The sophisticated design allows to achieve stable operation even with ceramic output capacitors down to 470 nF. The device is designed for the harsh environment of automotive applications. Therefore it is protected against overload, short circuit and overtemperature conditions. Of course the TLE 7276 can be used also in all other applications, where a stabilized 5 V voltage is required. Due to its ultra low stand-by current consumption of typ. 20 µA the TLE 7276 is dedicated for use in applications permanently connected to $V_{BAT}$. The regulator can be shut down via an Inhibit input. An integrated output sink current circuitry keeps the voltage at the Output pin Q below 5.5 V even when reverse currents are applied. Thus connected devices are protected from overvoltage damage.

For applications requiring extremely low noise levels the Infineon voltage regulator family TLE 42XY and TLE 44XY is more suited than the TLE 7276. A mV-range output noise on the TLE 7276 caused by the charge pump operation is unavoidable due to the ultra low quiescent current concept.

| Type | Ordering Code | Package |
|---|---|---|
| TLE 7276 D | Q67006-A9733 | P-TO252-5-1, P-TO252-5-11 |
| TLE 7276 G | Q67006-A9732 | P-TO263-5-1 |

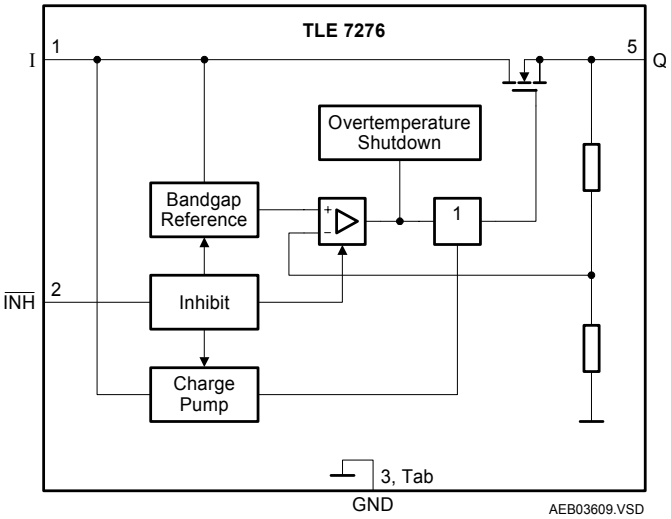



**Figure 1 Block Diagram**

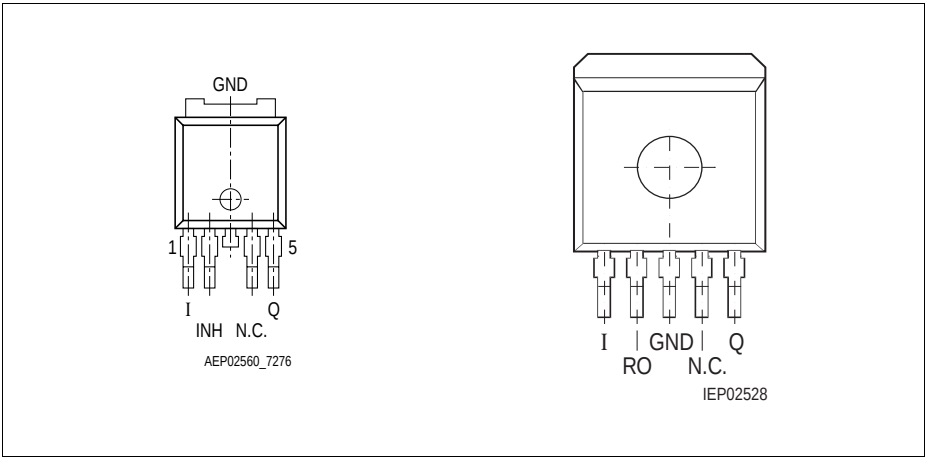



**Figure 2 Pin Configuration P-TO252-5 (D-PAK), P-TO263-5 (D²-PAK)**(top view)

**Table 1 Pin Definitions and Functions**

| Pin No. | Symbol | Function |
|---|---|---|
| 1 | I | **Input;** block to ground directly at the IC with a ceramic capacitor |
| 2 | $\overline{\text{INH}}$ | **Inhibit Input;** low level disables the IC. Integrated pull-down resistor |
| 3 | GND | **Ground;** internally connected to heat sink |
| 4 | N.C. | Not connected |
| 5 | Q | **Output;** block to ground with a ceramic capacitor, $C \geq 470$ nF |

**Table 2 Absolute Maximum Ratings**

| Parameter | Symbol | Limit Values | | Unit | Test Condition |
|---|---|---|---|---|---|
| | | Min. | Max. | | |
| **Input I** | | | | | |
| Voltage | $V_I$ | -0.3 | 45 | V | – |
| Current | $I_I$ | -1 | – | mA | – |
| **Inhibit $\overline{\text{INH}}$** | | | | | |
| Voltage | $V_{\overline{\text{INH}}}$ | -0.3 | 45 | V | Observe current limit $I_{\overline{\text{INH}},max}$ [1] |
| Current | $I_{\overline{\text{INH}}}$ | -1 | 1 | mA | – |
| **Output Q** | | | | | |
| Voltage | $V_Q$ | -0.3 | 5.5 | V | – |
| Voltage | $V_Q$ | -0.3 | 6.2 | V | $t$ < 10 s [2] |
| Current | $I_Q$ | -1 | – | mA | – |
| **Temperature** | | | | | |
| Junction temperature | $T_j$ | -40 | 150 | °C | – |
| Storage temperature | $T_{stg}$ | -50 | 150 | °C | – |

1) External resistor required to keep current below absolute maximum rating when voltages ≥ 5.5 V are applied.

2) Exposure to these absolute maximum ratings for extended periods ($t$ > 10 s) may affect device reliability.

*Note: Stresses above those listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

**Table 3 Operating Range**

| Parameter | Symbol | Limit Values | | Unit | Remarks |
|---|---|---|---|---|---|
| | | Min. | Max. | | |
| Input voltage | $V_I$ | 5.5 | 42 | V | – |
| Junction temperature | $T_j$ | -40 | 150 | °C | – |

**Table 4 Thermal Resistance**

| Parameter | Symbol | Limit Values | | Unit | Remarks |
|---|---|---|---|---|---|
| | | Min. | Max. | | |
| Junction case | $R_{thj\text{-}c}$ | – | 8 | K/W | – |
| Junction ambient | $R_{thj\text{-}a}$ | – | 80 | K/W | TO252[1)] |
| Junction ambient | $R_{thj\text{-}a}$ | – | 55 | K/W | TO263[2)] |

1) Worst case, regarding peak temperature; zero airflow; mounted on a PCB FR4, 80 × 80 × 1.5 mm³, heat sink area 300 mm²

2) Worst case, regarding peak temperature; zero airflow; mounted on a PCB FR4, 80 × 80 × 1.5 mm³, heat sink area 300 mm²

*Note: In the operating range, the functions given in the circuit description are fulfilled.*

**Table 5 Electrical Characteristics**

$V_I$ = 13.5 V; $V_{\overline{INH}}$ = 5 V; -40 °C < $T_j$ < 150 °C (unless otherwise specified)

| Parameter | Symbol | Limit Values | | | Unit | Measuring Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| **Output Q** | | | | | | |
| Output voltage | $V_Q$ | 4.9 | 5.0 | 5.1 | V | 0.1 mA < $I_Q$ < 300 mA; 6 V < $V_I$ < 16 V |
| Output voltage | $V_Q$ | 4.9 | 5.0 | 5.1 | V | 0.1 mA < $I_Q$ < 100 mA; 6 V < $V_I$ < 40 V |
| Output current limitation | $I_Q$ | 320 | – | – | mA | 1) |
| Output current limitation | $I_Q$ | – | – | 800 | mA | $V_Q$ = 0V |
| Current consumption; $I_q = I_I - I_Q$ | $I_q$ | – | 20 | 30 | µA | $I_Q$ = 0.1 mA; $T_j$ = 25 °C |
| Current consumption; $I_q = I_I - I_Q$ | $I_q$ | – | – | 40 | µA | $I_Q$ = 0.1 mA; $T_j \leq$ 80 °C |
| Quiescent current; inhibited | $I_q$ | – | 5 | 9 | µA | $V_{\overline{INH}}$ = 0 V; $T_j$ < 80 °C |
| Drop voltage | $V_{dr}$ | – | 250 | 500 | mV | $I_Q$ = 200 mA; $V_{dr} = V_I - V_Q$ 1) |
| Load regulation | $\Delta V_{Q, lo}$ | -40 | 15 | 40 | mV | $I_Q$ = 5 mA to 250 mA |
| Line regulation | $\Delta V_{Q, li}$ | -20 | 5 | 20 | mV | $V_I$ = 10V to 32 V; $I_Q$ = 5 mA |
| Power supply ripple rejection | $PSRR$ | – | 60 | – | dB | $f_r$ = 100 Hz; $V_r$ = 0.5 Vpp |
| Temperature output voltage drift | $dV_Q/dT$ | – | 0.5 | – | mV/K | – |
| Output Capacitor | $C_Q$ | 470 | – | – | nF | ESR < 3 Ohm |
| **Inhibit Input $\overline{INH}$** | | | | | | |
| Turn-on Voltage | $V_{\overline{INH}\ ON}$ | 3.1 | – | – | V | $V_Q \geq$4.9 V |
| Turn-off Voltage | $V_{\overline{INH}\ OFF}$ | – | – | 0.8 | V | $V_Q \leq$0.3 V |
| H-input current | $I_{\overline{INH}\ ON}$ | – | 3 | 4 | µA | $V_{\overline{INH}}$ = 5 V |
| L-input current | $I_{\overline{INH}\ OFF}$ | – | 0.5 | 1 | µA | $V_{\overline{INH}}$ = 0 V; $T_j$ < 80 °C |

1) Measured when the output voltage $V_Q$ has dropped 100 mV from the nominal value obtained at $V_I$ = 13.5 V.

## Application Information

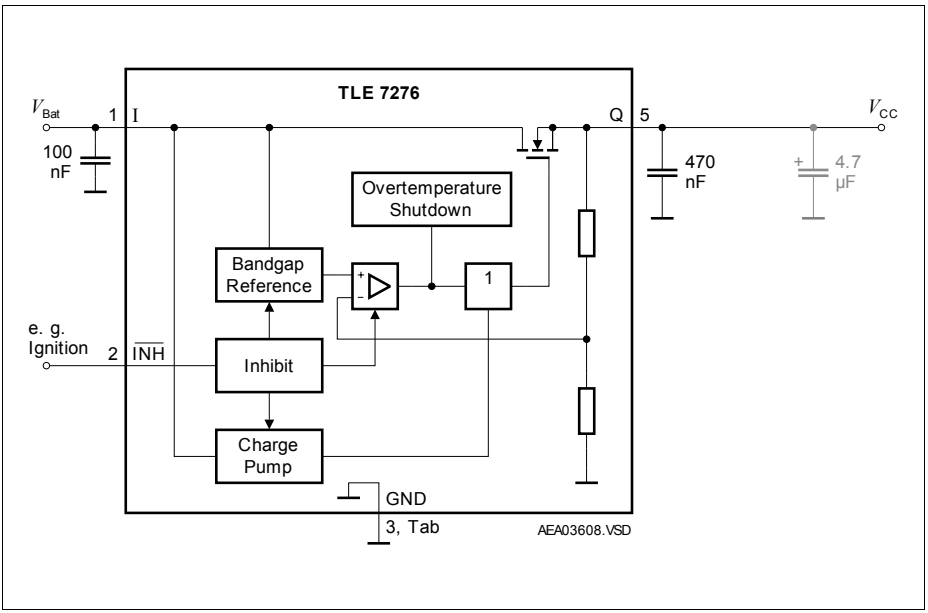



**Figure 3 Application Diagram**

### Input, Output

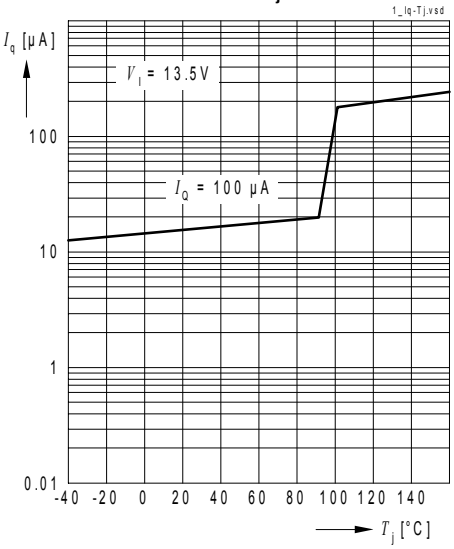
An input capacitor is necessary for damping line influences. A resistor of approx. 1 Ω in series with $C_I$, can damp the LC of the input inductivity and the input capacitor.

In contrast to most low drop voltage regulators the TLE 7276 only needs moderate capacitance at the output to assure stability of the regulation loop. This offers more design flexibility to the circuit designer providing for cost efficient solutions.

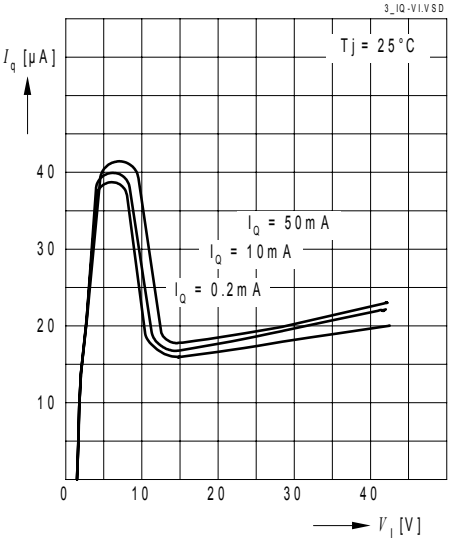
The TLE 7276 requires a ceramic output capacitor of at least 470 nF. In order to damp influences resulting from load current surges it is recommended to add an additional electrolytic capacitor of 4.7 µF to 47 µF at the output as shown in **Figure 3**.

## Typical Performance Characteristics

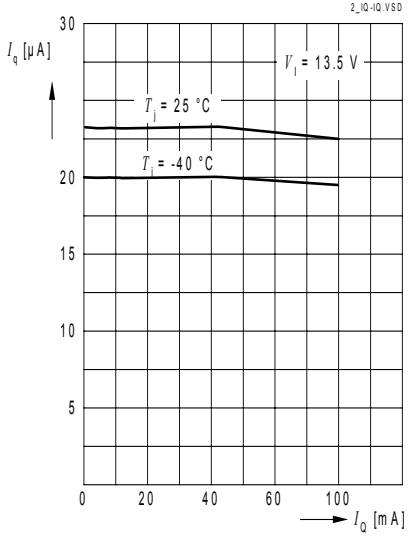
### Current Consumption $I_q$ versus Junction Temperature $T_j$



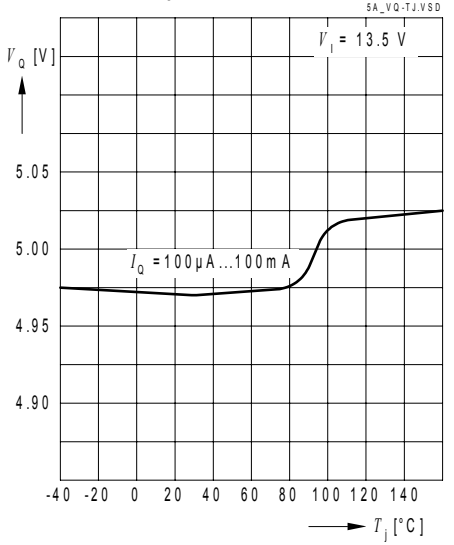

### Current Consumption $I_q$ versus Input Voltage $V_I$



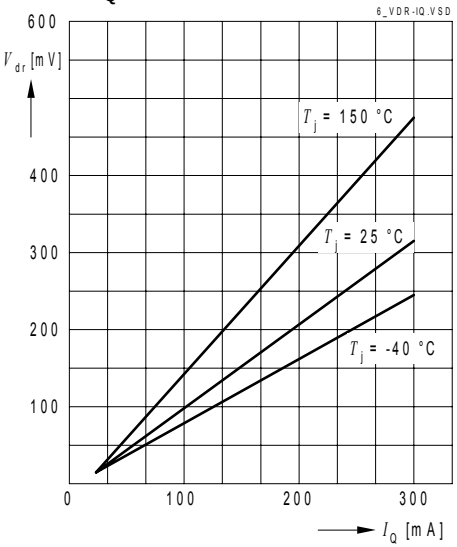

### Current Consumption $I_q$ versus Output Current $I_Q$



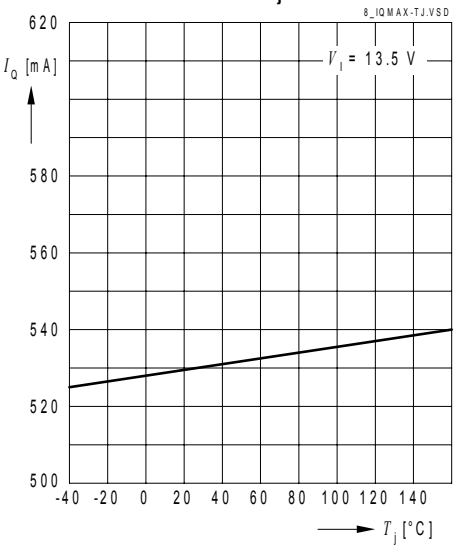

### Output Voltage $V_Q$ versus Junction Temperature $T_j$



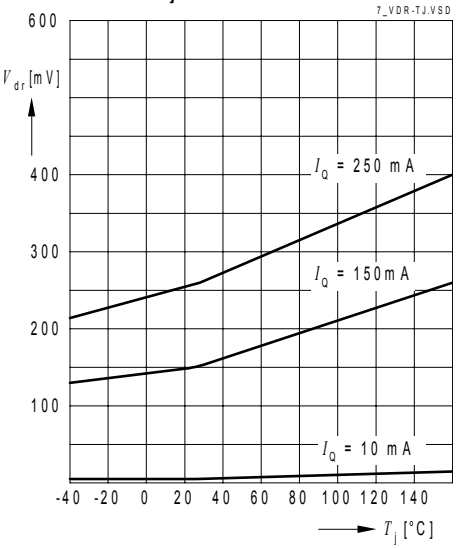
### Dropout Voltage $V_{dr}$ versus Output Current $I_Q$



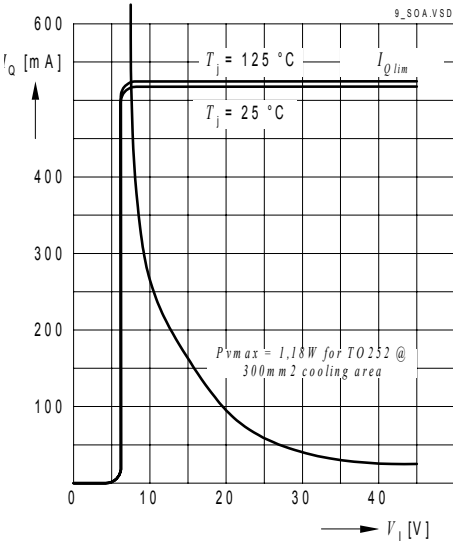

### Maximum Output Current $I_Q$ versus Junction Temperature $T_j$



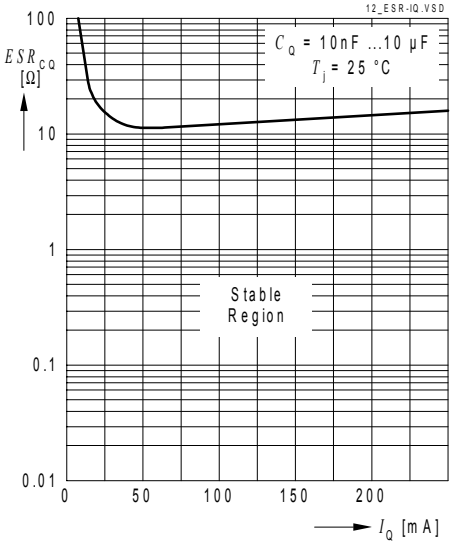

### Dropout Voltage $V_{dr}$ versus Junction Temperature $T_j$



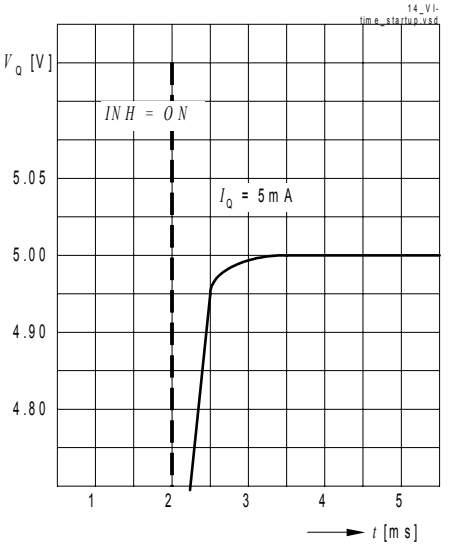

### Maximum Output Current $I_Q$ versus Input Voltage $V_I$



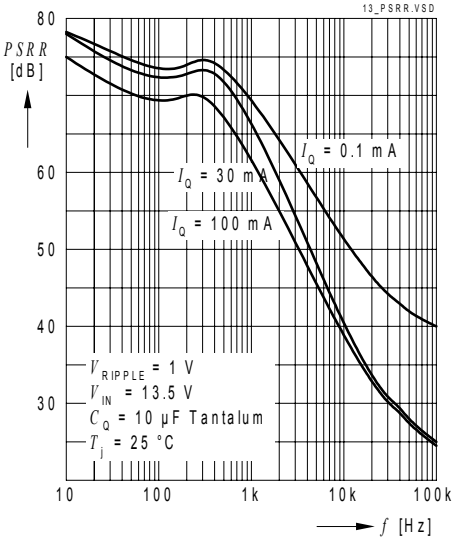
## Region of Stability



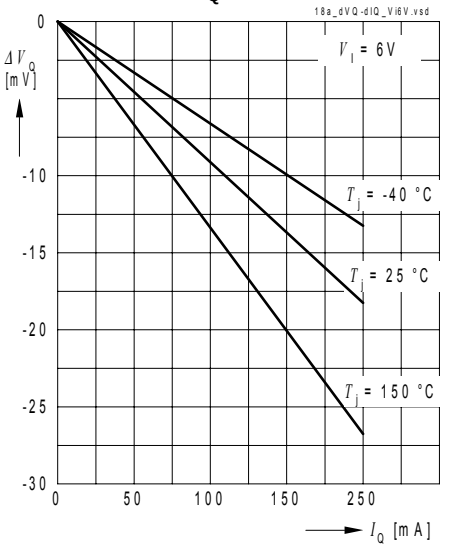

## Output Voltage $V_Q$ Start-up behaviour



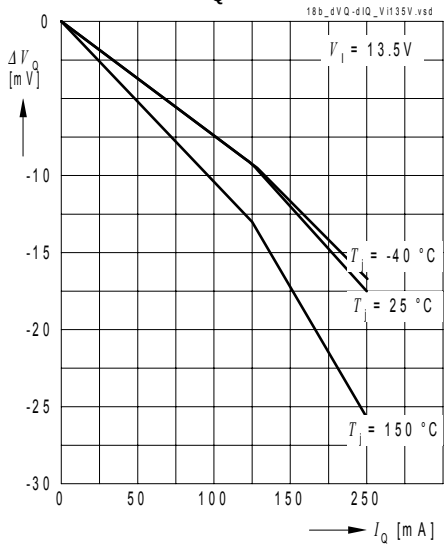

## Power Supply Ripple Rejection PSRR versus Frequency f



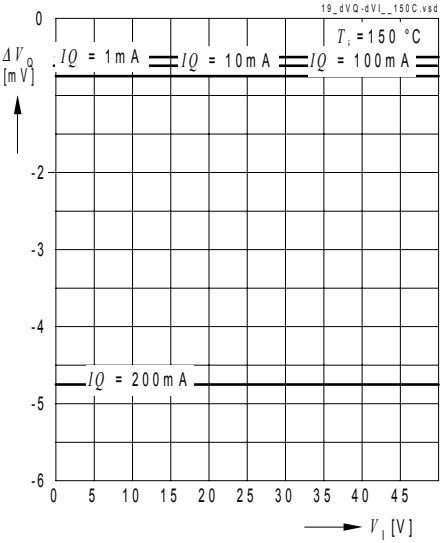

## Load Regulation $dV_Q$ versus Output Current Change $dI_Q$



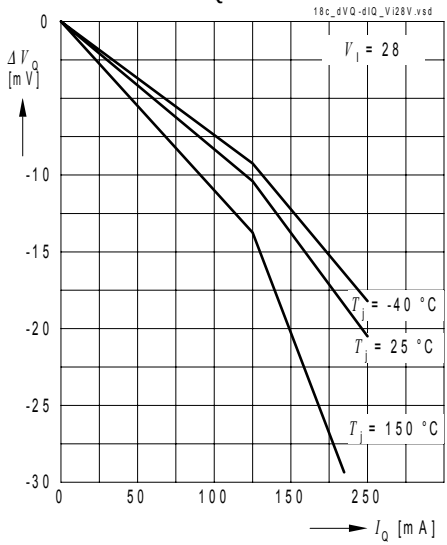
### Load Regulation $dV_Q$ versus Output Current Change $dI_Q$



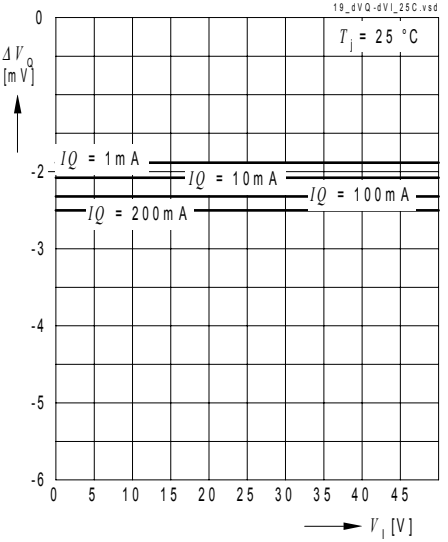

### Line Regulation $dV_Q$ versus Input Voltage Changed$V_I$



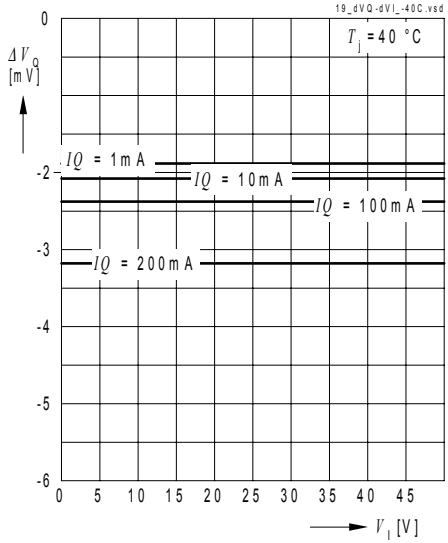

### Load Regulation $dV_Q$ versus Output Current Change $dI_Q$



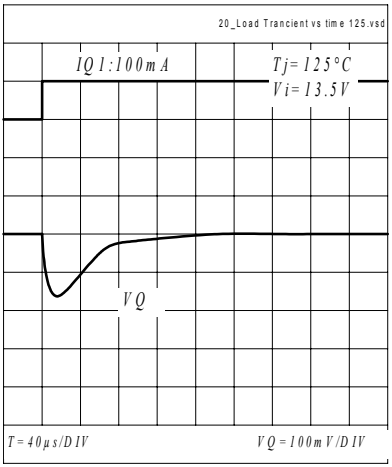

### Line Regulation $dV_Q$ versus Input Voltage Changed$V_I$



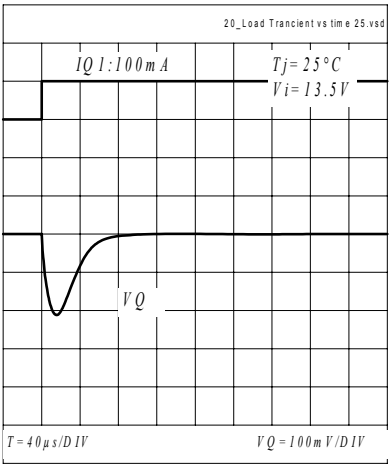
## Line Regulation $dV_Q$ versus Input Voltage Changed$V_I$



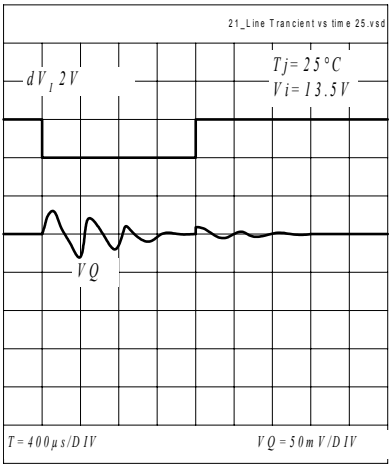

## Load Transient Response Peak Voltage $dV_Q$



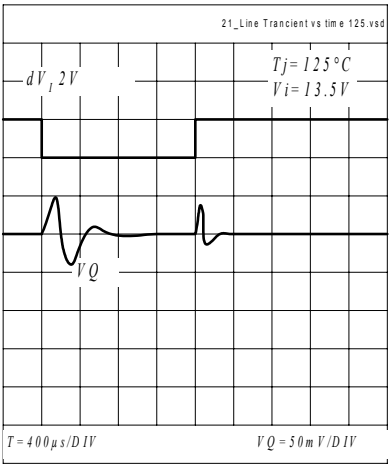

## Load Transient Response Peak Voltage $dV_Q$



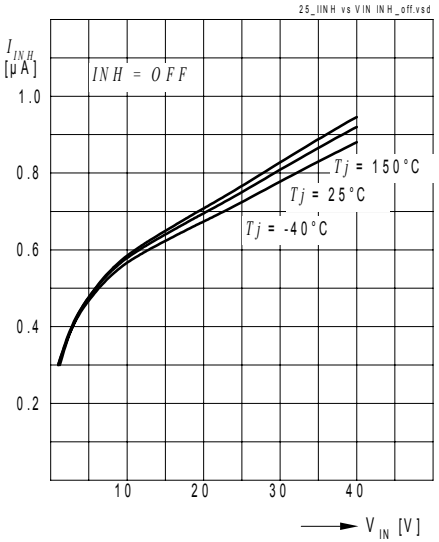

## Line Transient Response Peak Voltage $dV_Q$



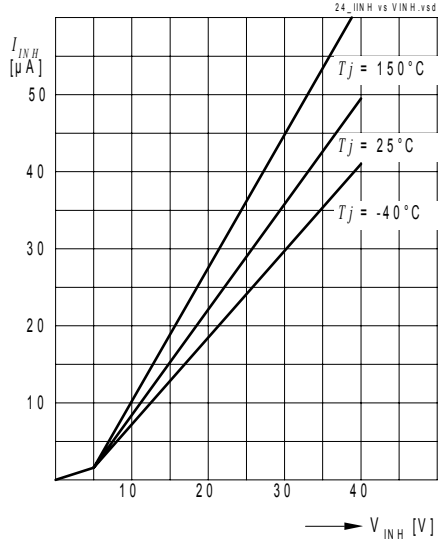
### Line Transient Response Peak Voltage $dV_Q$



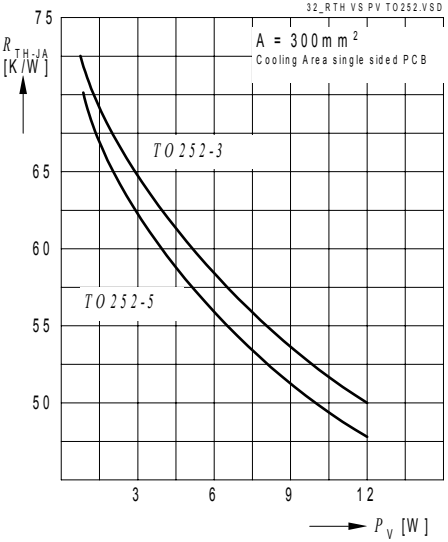

### Inhibit Input Current $I_{INH}$ versus Input Voltage $V_I$, INH=Off



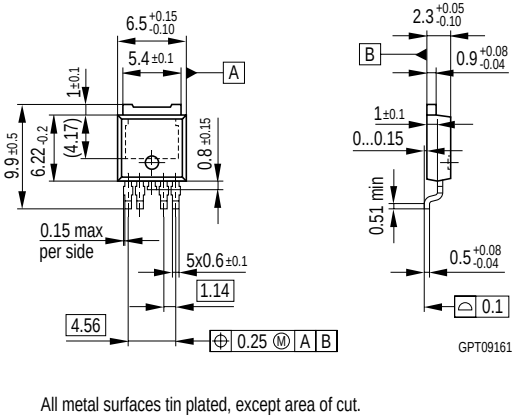

### nhibit Input Current $I_{INH}$ versus Inhibit Input Voltage $V_{INH}$




### Thermal Resistance Junction-Ambient $R_{THJA}$ versus Power Dissipation $P_V$



## Package Outlines




All metal surfaces tin plated, except area of cut.

**Figure 4** **P-TO252-5-1** (Plastic Transistor Single Outline)

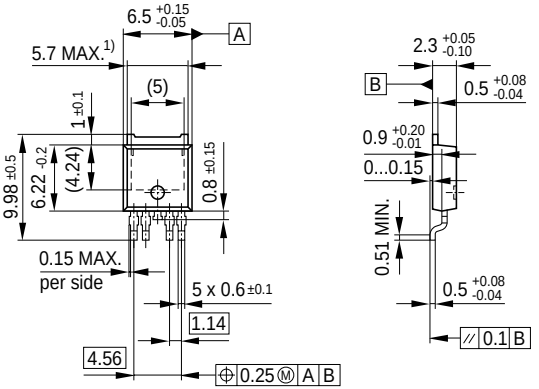
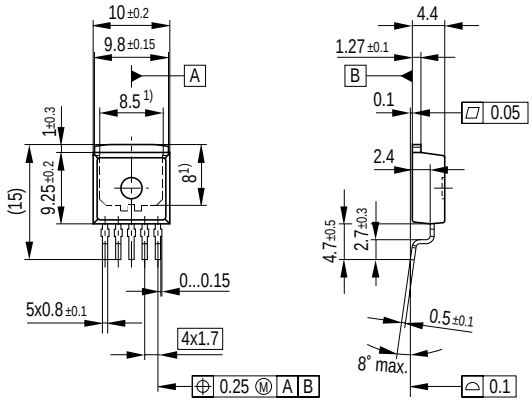



**Figure 5** **P-TO252-5-11** (Plastic Transistor Single Outline)




1) Typical
All metal surfaces tin plated, except area of cut.

GPT09113

**Figure 6** **P-TO263-5-1** (Plastic Transistor Single Outline)

**Edition 2005-02-05**

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**TLE 7276**
**5-V Low Drop Voltage Regulator**
**Revision History: 2005-02-05** Rev. 1.0

Previous Version: 0.21

| Page | Subjects (major changes since last revision) |
|---|---|
| | release of final version |
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