6.25-Gbps Cable and PC Board Equalizer

FEATURES

- **Multirate Operation up to 6.25 Gbps**
- **Compensates for up to 13-dB Loss on the Receive Side and up to 12-dB Loss on the Transmit Side at 3.125 GHz**
- **Suitable to Receive and Transmit 6.25-Gbps Data Over up to 60 Inches (1.5 Meters) of FR4 PC Boards**
- **Suitable to Receive and Transmit 6.25-Gbps Data Over up to 63 Feet (19.2 Meters) of 24-AWG Cable**
- **Ultralow Power Consumption**
- **Input Offset Cancellation**
- **High Input Dynamic Range**
- **Output Disable/Squelch Function**
- **Loss of Signal Detection**
- **Output Swing Select**
- **Output De-Emphasis Select**
- **Output Polarity Select**
- **CML Data Outputs**
- **Single 3.3-V Supply**
- **Surface-Mount, Small-Footprint, 3-mm × 3-mm, 16-Pin QFN Package**

APPLICATIONS

- **High-Speed Links in Communication and Data Systems**
- **Backplane, Daughtercard, and Cable Interconnects for PCI Express, InfiniBand, SAS, CEI, XAUI, Fibre Channel, and Ethernet**

DESCRIPTION

The TLK6201EA is a versatile, high-speed, limiting equalizer for applications in digital high-speed links with data rates up to 6.25 Gbps.

This device provides a high-frequency boost of 13 dB on the received data at 3.125 GHz, as well as sufficient gain to ensure a fully differential output swing for input signals as low as 100 mVp-p (at the input of a lossy interconnect line).

Four de-emphasis levels can be selected on the transmit side to provide up to 12 dB of additional high-frequency loss compensation.

The high input-signal dynamic range ensures low-jitter output signals even when overdriven with input signal swings as high as 2000 mVp-p.

The TLK6201EA implements fixed loss-of-signal detection, which can be used to implement a squelch function by connecting the LOS output to the adjacent DIS input.

The TLK6201EA is available in a small-footprint, 3-mm × 3-mm, 16-pin QFN package. It requires a single 3.3-V supply.

This power-efficient equalizer is characterized for operation from –40°C to 85°C.

BLOCK DIAGRAM

A simplified block diagram of the TLK6201EA is shown in Figure 1. This compact, low-power, 6.25-Gbps equalizer consists of a high-speed data path with offset cancellation circuitry, a loss-of-signal detection block, and a band-gap voltage reference and bias current generation block. The equalizer requires a single 3.3-V ±10% supply voltage. All circuit parts are described in detail as follows.

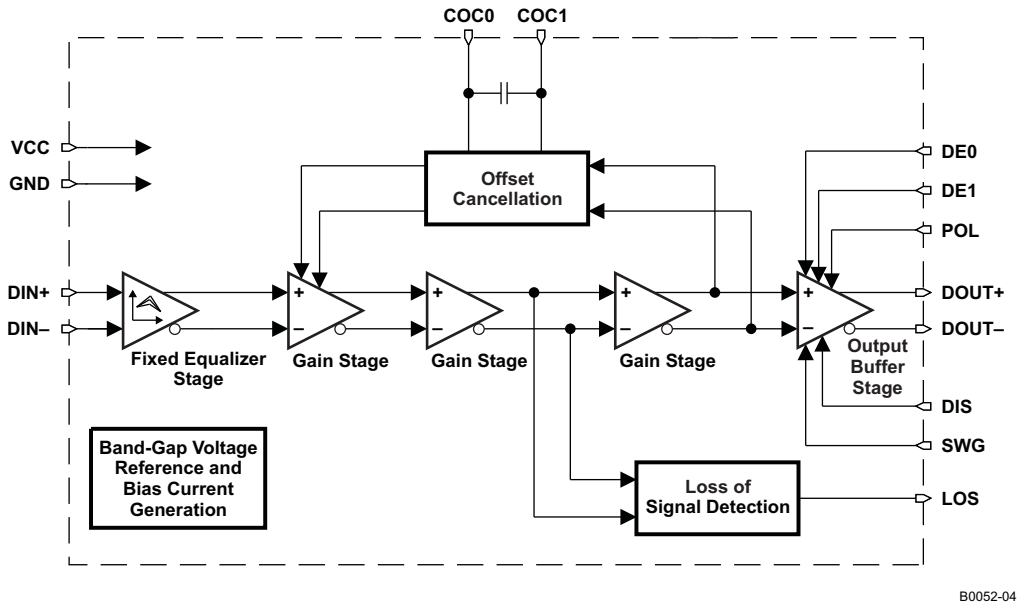


Figure 1. Simplified Block Diagram of the TLK6201EA

HIGH-SPEED DATA PATH

The high-speed data signal with frequency-dependent loss is applied to the data path by means of the input signal pins DIN+/DIN–. The data path consists of the fixed equalizer input stage, three gain stages which provide the required gain to ensure a limited-output signal, and an output buffer stage. The equalized and amplified data output signal is available at the output pins DOUT+/DOUT–, which provide 2 × 50-Ω back-termination to VCC. The output stage also includes a data polarity-switching function, which is controlled by the POL input, and a disable function, controlled by the signal applied to the DIS input pin.

The output swing can be increased 50% by applying a high-level signal to the SWG pin.

Up to 12 dB of output signal de-emphasis can be selected using the pins DE0 and DE1.

An offset cancellation compensates the inevitable internal offset voltages and thus ensures proper operation even for very small input data signals.

The low-frequency cutoff is as low as 3.5 kHz with the built-in filter capacitor. For applications which require even lower cutoff frequencies, an additional external filter capacitor can be connected to the COC0/COC1 pins.

LOSS-OF-SIGNAL DETECTION

The output signal of the second gain stage is monitored by the loss-of-signal detection circuitry. In this block, the input signal is compared to a fixed threshold. If the low frequency components of the input signal fall below this threshold, a loss of signal is indicated at the LOS pin.

A squelch function can be easily implemented by connecting the LOS output to the adjacent DIS input. This measure avoids chattering of the output when no input signal is present.

BAND-GAP VOLTAGE AND BIAS GENERATION

The TLK6201EA equalizer is supplied by a single 3.3-V ±10% supply voltage connected to the VCC pins. This voltage is referred to ground (GND).

An on-chip band-gap voltage circuit generates a supply-voltage-independent reference from which all internally required voltages and bias currents are derived.

DEVICE INFORMATION

The TLK6201EA is available in a small-footprint, 3-mm × 3-mm, 16-pin QFN package, with a lead pitch of 0.5 mm. The pinout is shown in Figure 2.

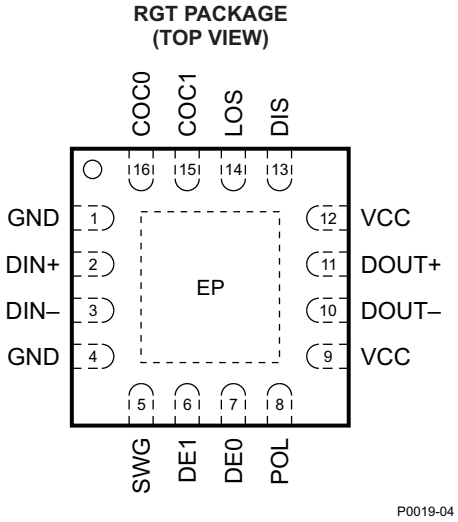


Figure 2. Pinout of TLK6201EA

TERMINAL FUNCTIONS

TERMINAL		TYPE	DESCRIPTION
NAME	NO.		
COC0	16	Analog	Offset cancellation filter capacitor terminal 2. Connect an additional filter capacitor between this pin and COC1 (pin 15). To disable the offset cancellation loop, connect COC1 and COC0 (pins 15 and 16).
COC1	15	Analog	Offset cancellation filter capacitor terminal 1. Connect an additional filter capacitor between this pin and COC0 (pin 16). To disable the offset cancellation loop, connect COC1 and COC0 (pins 15 and 16).
DE0	7	CMOS in	Selects 4 dB of output signal de-emphasis when set to high level. Internally pulled up.
DE1	6	CMOS in	Selects 8 dB of output signal de-emphasis when set to high level. Internally pulled up.
DIN+	2	Analog in	Noninverted data input. On-chip load terminated to ground. Connect a 100-Ω differential transmission line to terminals DIN+ and DIN–.
DIN–	3	Analog in	Inverted data input. On-chip load terminated to ground. Connect a 100-Ω differential transmission line to terminals DIN+ and DIN–.
DIS	13	CMOS in	Disables CML output stage when set to high level. Internally pulled down.
DOUT+	11	CML out	Noninverted data output. On-chip 50-Ω back-terminated to VCC.
DOUT–	10	CML out	Inverted data output. On-chip 50-Ω back-terminated to VCC.
GND	1, 4, EP	Supply	Circuit ground. Exposed die pad (EP) must be grounded.
LOS	14	CMOS out	High level indicates that the input signal amplitude is below the fixed threshold level.
POL	8	CMOS in	Output data signal polarity select (internally pulled up): Setting to high level or leaving pin open selects normal polarity. Low level selects inverted polarity.
SWG	5	CMOS in	Output swing control. The output swing is increased by 50% when set to high level. Internally pulled down.
VCC	9, 12	Supply	3.3-V, ±10% supply voltage

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)

		VALUE(1)	UNIT
V_{CC}	Supply voltage (2)	–0.3 to 4	V
V_{DIN+}, $V_{DIN–}$	Voltage at DIN+, DIN– (2)	0.5 to 4	V
V_{DIS}, V_{POL}, V_{DE1}, V_{DE0}, V_{SWG}, V_{COC1}, V_{COC0}	Voltage at DIS, POL, DE1, DE0, SWG, COC1, COC0 (2)	–0.3 to 4	V
$V_{COC,DIFF}$	Differential input voltage between COC1 and COC0	±1	V
$V_{DIN,DIFF}$	Differential input voltage between DIN+ and DIN–	±2.5	V
I_{DIN+}, $I_{DIN–}$, I_{DOUT+}, $I_{DOUT–}$	Continuous current at inputs and outputs	±25	mA
ESD	ESD ratings at all pins, human body model (HBM)	3	kV
$T_{J,max}$	Maximum junction temperature	125	°C
T_{stg}	Storage temperature range	–65 to 85	°C
T_A	Characterized free-air operating temperature range	–40 to 85	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	3	3.3	3.6	V
T_A	Free-air operating temperature	–40		85	°C
V_{IH}	High-level input voltage, CMOS	2			V
V_{IL}	Low-level input voltage, CMOS			0.8	V

DC ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage		3	3.3	3.6	V
I_{CC}	Supply current	DIS = SWG = low (includes CML output current)		45	54	mA
		DIS = low, SWG = high (includes CML output current)		55	67	
R_{OUT}	Output resistance, data	Single-ended to V_{CC}		50		Ω
	LOS high voltage	I_{source} = 1 mA	2.5			V
	LOS low voltage	I_{sink} = 1 mA			0.5	V

AC ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)
Typical operating condition is at V_{CC} = 3.3 V and T_A = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Low frequency –3-dB bandwidth	C_{OC} = open		3.5	10	kHz
		C_{OC} = 100 nF		0.8		
	Maximum data rate		6.25			Gbps
$V_{IN,MIN}$	Data input sensitivity(1)	BER < 10^{-12}, K28.5 pattern at 6.25 Gbps over a 36-inch, 7-mil-wide stripline on standard FR4, including two through-hole SMA connectors. Voltage measured at the input of the interconnect line.		40	50	mV_{P-P}
$V_{IN,MAX}$	Data input overload	Voltage at the input of an interconnect line	2000			mV_{P-P}
	High-frequency boost	f = 3.125 GHz (fixed input equalizer)	12	14	17	dB
V_{OD}	Differential data output voltage swing	DIS = low, SWG = low	600	800	1000	mV_{P-P}
		DIS = low, SWG = high	900	1200	1500	
V_{RIP}	Differential output ripple	DIS = high, 50% transitions of K28.5 pattern at 6.25 Gbps, no interconnect line, V_{IN} = 2000 mVp-p		0.25	10	mV_{RMS}
$V_{CM,OUT}$	Data output, common-mode voltage	DIS = low, SWG = low, dc-coupled 50 Ω to V_{CC}, single-ended terminations	V_{CC} – 0.25	V_{CC} – 0.2	V_{CC} – 0.15	V
		DIS = low, SWG = high, dc-coupled 50 Ω to V_{CC}, single-ended terminations	V_{CC} – 0.375	V_{CC} – 0.3	V_{CC} – 0.225	
DE	Output de-emphasis (see Figure 3)	DE0 = low, DE1 = low		0		dB
		DE0 = high, DE1 = low		–4		
		DE0 = low, DE1 = high		–8		
		DE0 = high, DE1 = high		–12		
DJ	Deterministic jitter	K28.5 pattern at 6.25 Gbps, no interconnect line, V_{IN} = 400 mVp-p, DE0 = low, DE1 = low, SWG = low		8		ps_{P-P}
		K28.5 pattern at 6.25 Gbps over a 36-inch, 7-mil-wide stripline on standard FR4 including two through-hole SMA connectors, V_{IN} = 400 mVp-p (voltage at the input of the interconnect line), DE0 = low, DE1 = low, SWG = low		12		
RJ	Random jitter	K28.5 pattern at 6.25 Gbps over a 36-inch, 7-mil-wide stripline on standard FR4 including two through-hole SMA connectors, V_{IN} = 400 mVp-p (voltage at the input of the interconnect line), DE0 = low, DE1 = low, SWG = low		1		ps_{RMS}
t_r	Output rise time	20% to 80%, no interconnect line, DE0 = low, DE1 = low		35	55	ps
t_f	Output fall time	20% to 80%, no interconnect line, DE0 = low, DE1 = low		35	55	ps
S11	Input return loss	10 Hz < f < 3.1 GHz		–15		dB
S22	Output return loss	10 Hz < f < 3.1 GHz		–12		dB

(1) The given differential input signal swing is valid for the low-frequency components of the input signal. The high-frequency components may be attenuated by up to 13 dB at 3.125 GHz.

AC ELECTRICAL CHARACTERISTICS (continued)

over operating free-air temperature range (unless otherwise noted)
Typical operating condition is at V_{CC} = 3.3 V and T_A = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{AS}	LOS assert threshold voltage	K28.5 pattern at 6.25 Gbps over a 36-inch, 7-mil-wide stripline on standard FR4 including two through-hole SMA connectors. Voltage measured at the input of the interconnect line. (2)	40	75		mV_{P-P}
V_{DAS}	LOS de-assert threshold voltage	K28.5 pattern at 6.25 Gbps over a 36-inch, 7-mil-wide stripline on standard FR4 including two through-hole SMA connectors. Voltage measured at the input of the interconnect line. (2)		130	250	mV_{P-P}
	LOS hysteresis	20 log(V_{DAS}/V_{AS}) (2)	2.5	4.5		dB
$t_{AS/DAS}$	LOS assert/de-assert time		2		100	µs
t_{DIS}	Disable response time			20		ns
	Latency	From DIN+/DIN– to DOUT+/DOUT–		150		ps

(2) This specification is for 0°C to 85°C. Depending on the interconnect line length and performance, the bit pattern, and the data rate, the assert and de-assert threshold voltage levels vary. For more information, see the *Typical Characteristics* section.

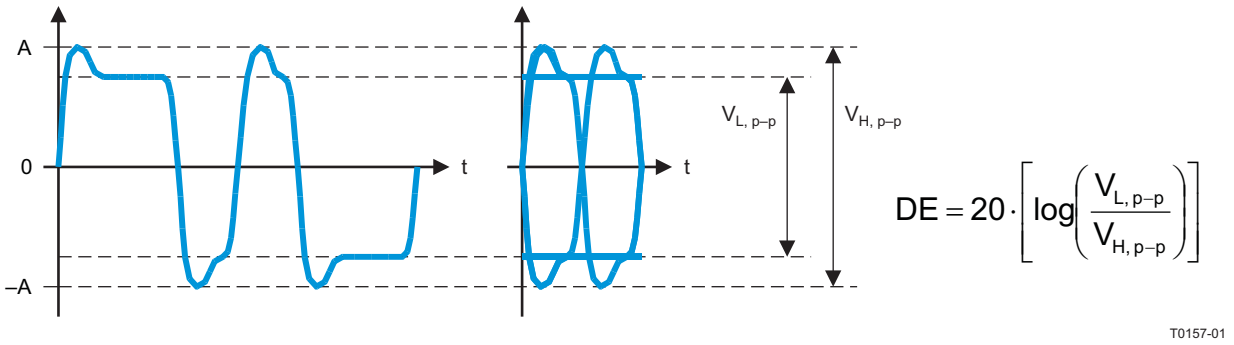


Figure 3. Output Signal De-Emphasis

APPLICATION INFORMATION

Figure 4 shows the TLK6201EA connected with an ac-coupled interface to the data signal source via a stripline transmission line on FR4 material. The output load is ac-coupled as well.

The ac-coupling capacitors C_1 through C_4 in the input and output data signal lines are the only required external components. In addition, if a very low cutoff frequency is required, as an option, an external filter capacitor C_{OC} may be used.

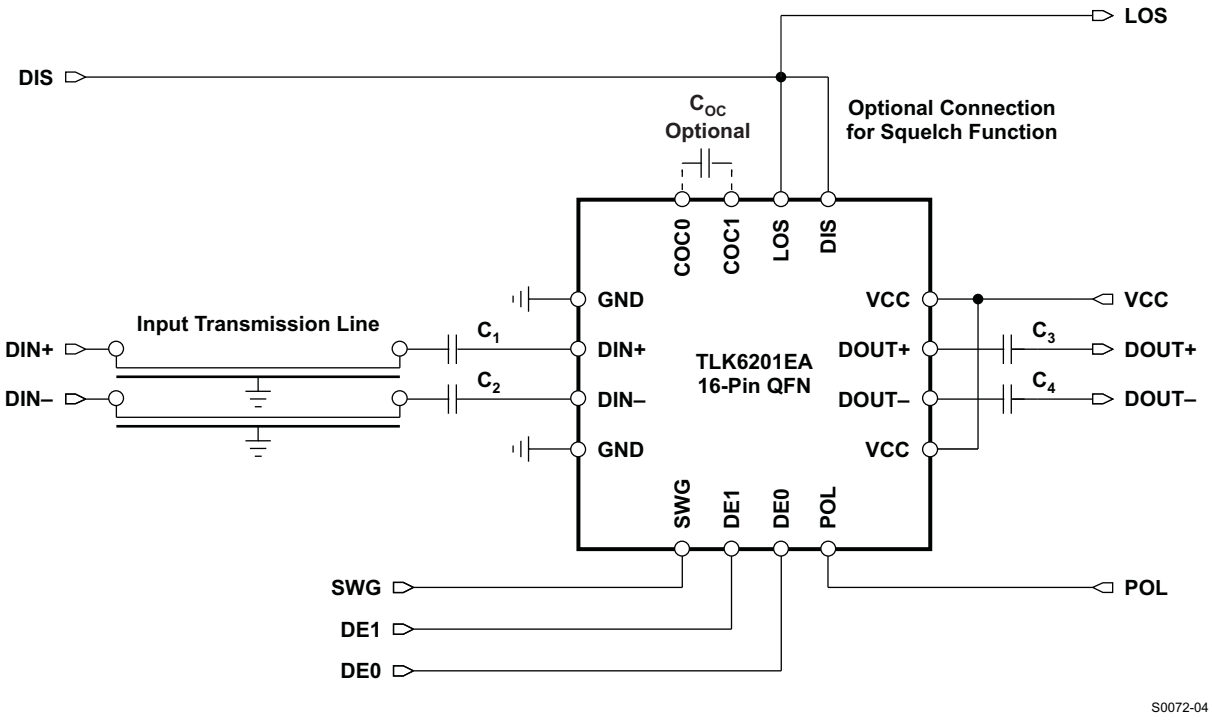


Figure 4. Basic Application Circuit with AC-Coupled I/Os

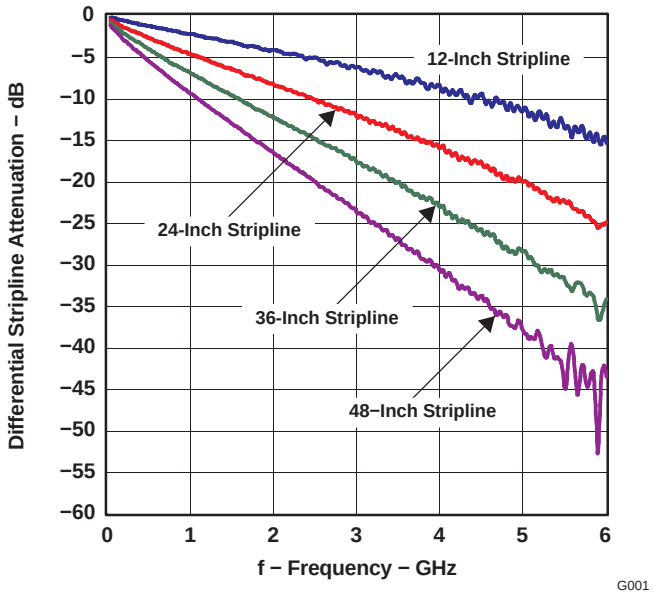


Figure 5. Attenuation Characteristics of Stripline Interconnect Lines

TYPICAL CHARACTERISTICS

Typical operating condition is at V_{CC} = 3.3 V, T_A = 25°C, V_{ID} = 400 mVp-p, DE0 = low, DE1 = low, SWG = low, and no interconnect line at the output (unless otherwise noted).

DIFFERENTIAL EQUALIZER INPUT SIGNAL (TOP) AND OUTPUT SIGNAL (BOTTOM) AT 6.25 GBPS USING A K28.5 PATTERN

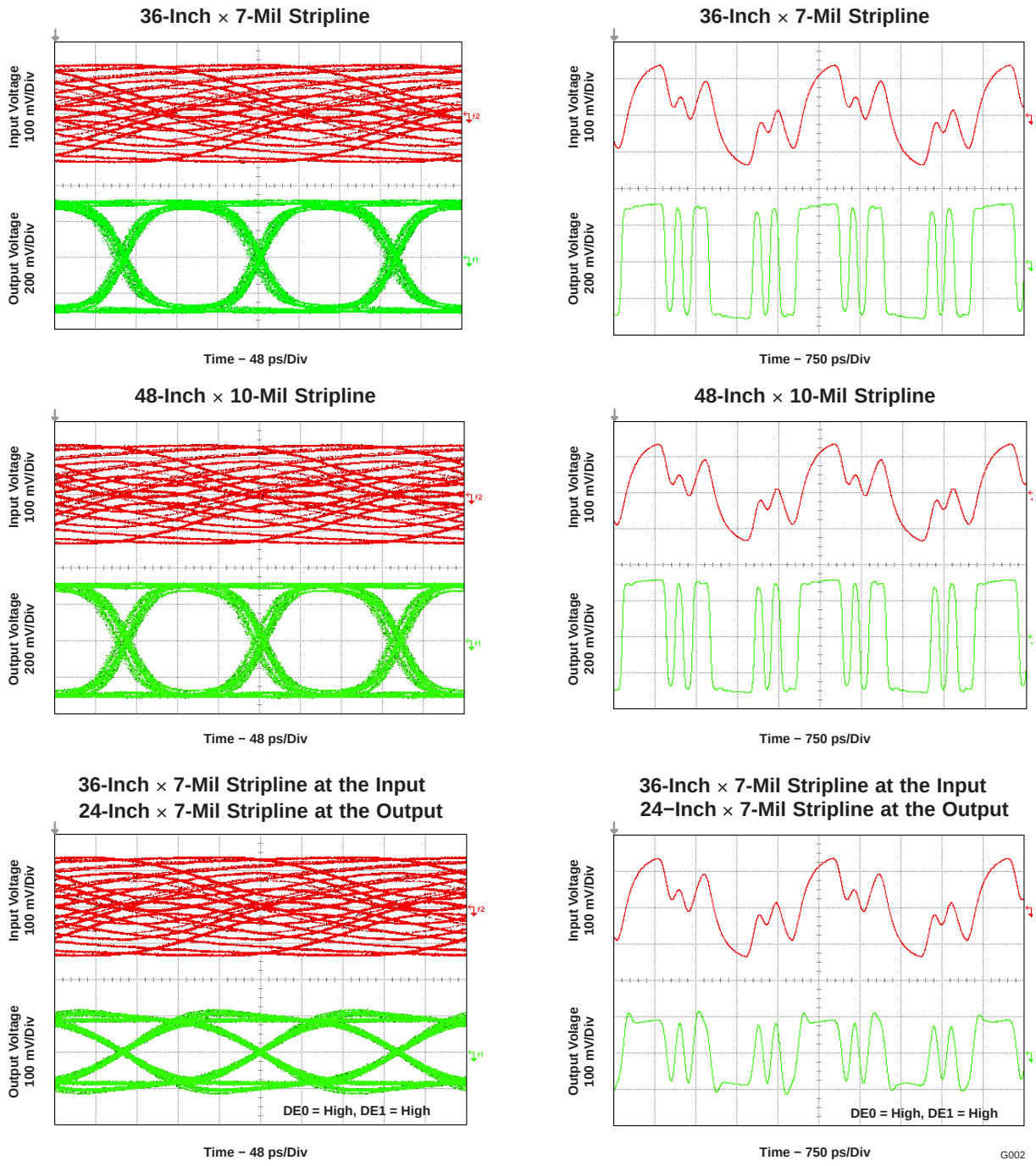


Figure 6. Equalizer Input and Output Signals With Different Interconnect Lines at 6.25 Gbps

TYPICAL CHARACTERISTICS (continued)

Typical operating condition is at V_{CC} = 3.3 V, T_A = 25°C, V_{IN} = 400 mVp-p, DE0 = low, DE1 = low, SWG = low, and no interconnect line at the output (unless otherwise noted).

DIFFERENTIAL EQUALIZER INPUT SIGNAL (TOP) AND OUTPUT SIGNAL (BOTTOM) AT 4.25 GBPS USING A K28.5 PATTERN

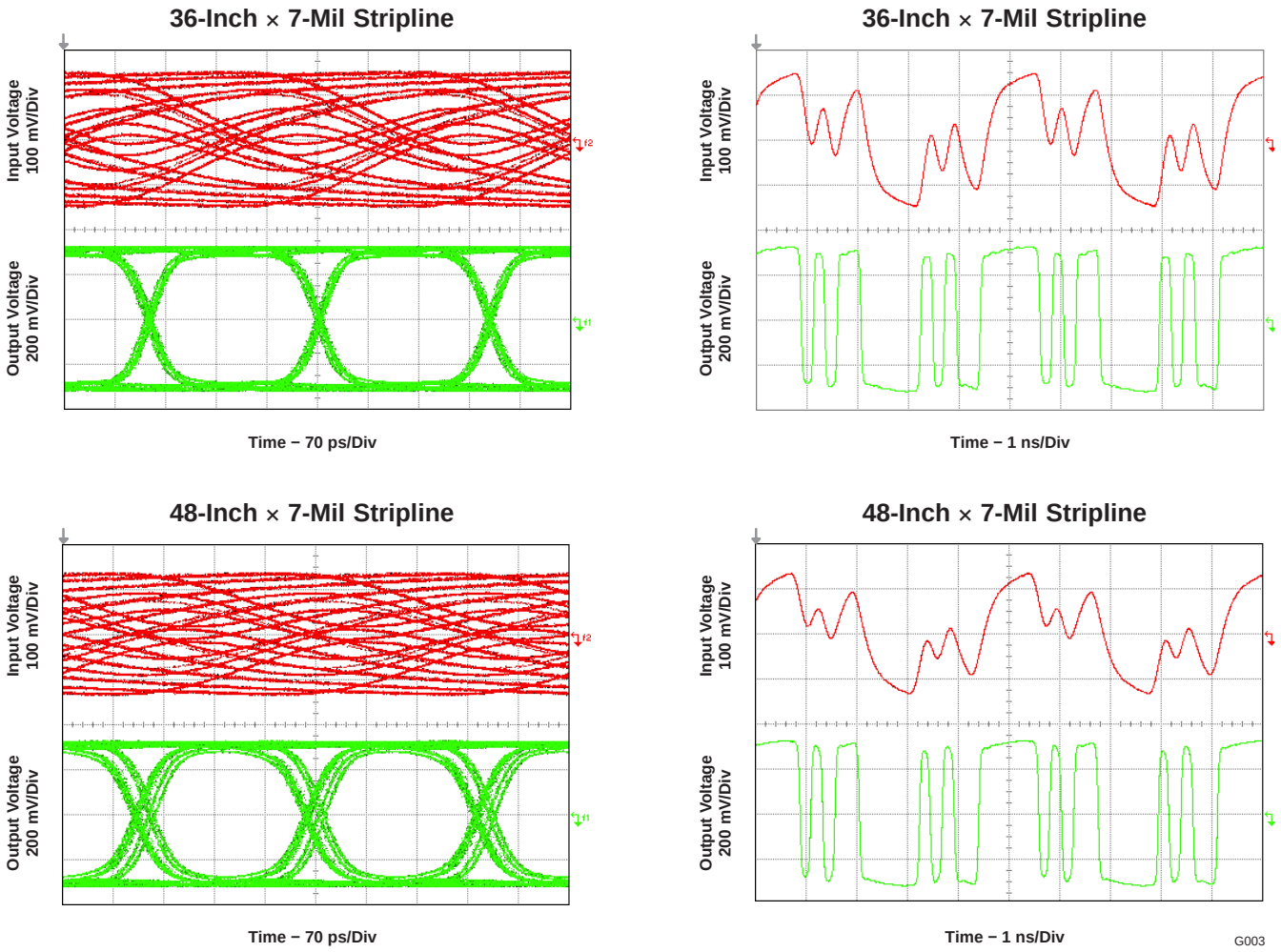


Figure 7. Equalizer Input and Output Signals With Different Interconnect Lines at 4.25 Gbps

TYPICAL CHARACTERISTICS (continued)

Typical operating condition is at V_{CC} = 3.3 V, T_A = 25°C, V_{IN} = 400 mVp-p, DE0 = low, DE1 = low, SWG = low, and no interconnect line at the output (unless otherwise noted).

DIFFERENTIAL EQUALIZER INPUT SIGNAL (TOP) AND OUTPUT SIGNAL (BOTTOM) AT 2.125 GBPS USING A K28.5 PATTERN

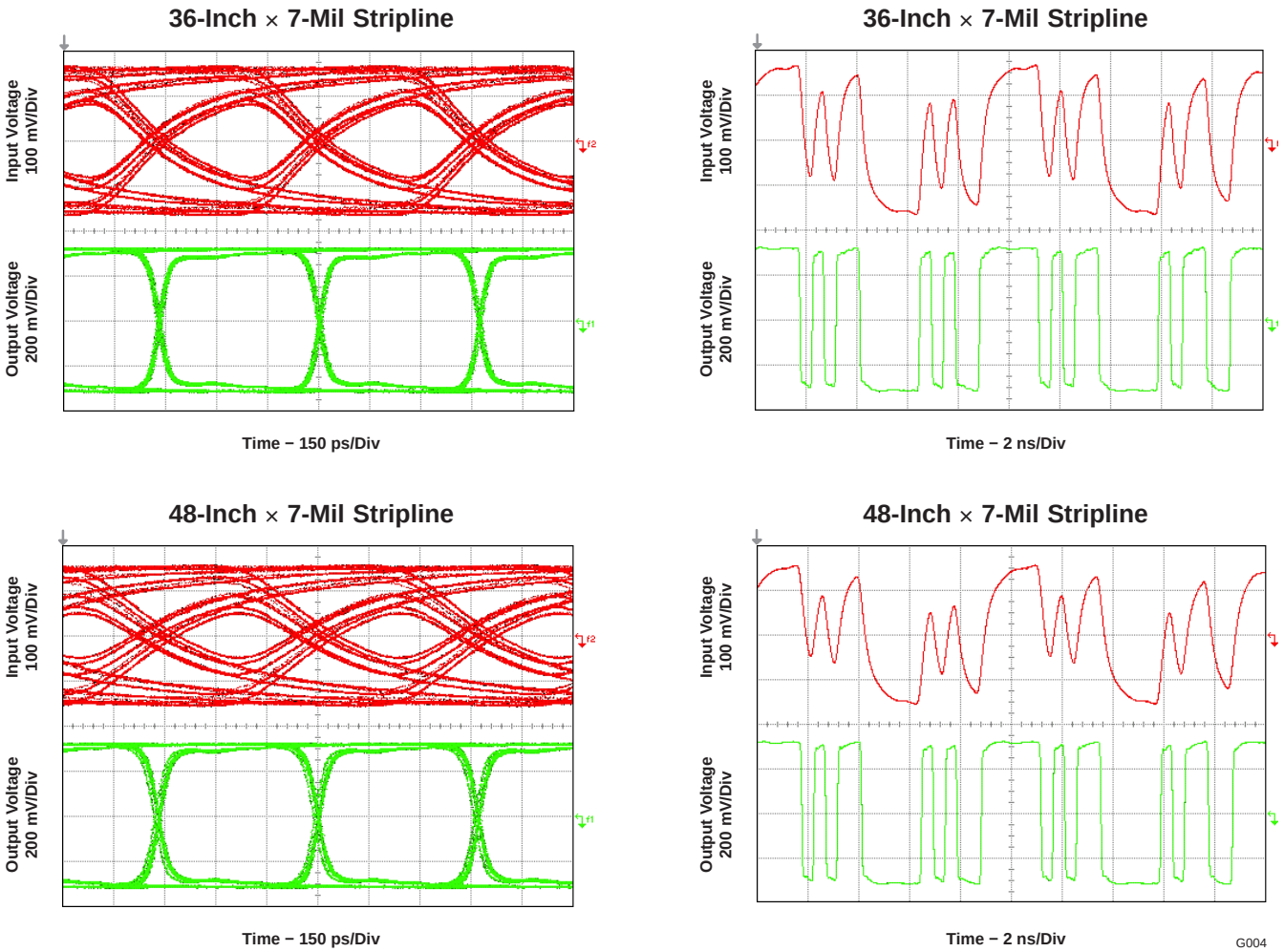


Figure 8. Equalizer Input and Output Signals With Different Interconnect Lines at 2.125 Gbps

TYPICAL CHARACTERISTICS (continued)

Typical operating condition is at V_{CC} = 3.3 V, T_A = 25°C, DE0 = low, DE1 = low, SWG = low, and no interconnect line at the output (unless otherwise noted).

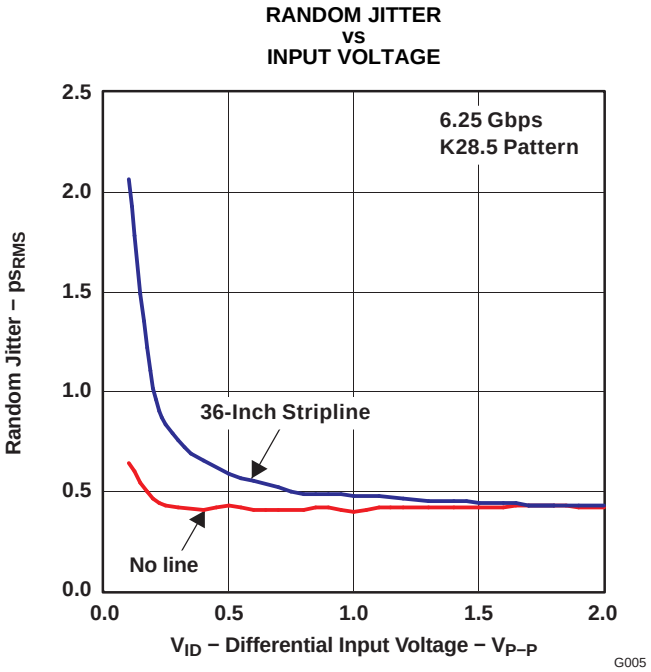


Figure 9.

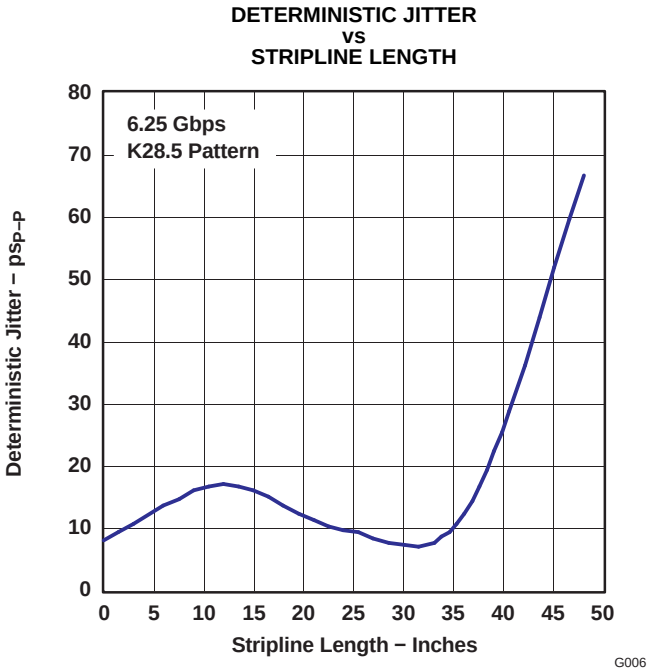


Figure 10.

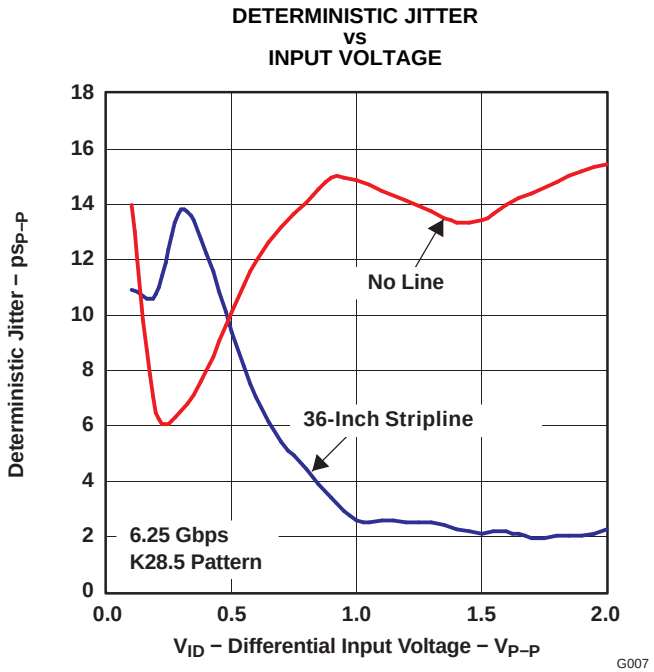


Figure 11.

TYPICAL CHARACTERISTICS (continued)

Typical operating condition is at V_{CC} = 3.3 V, T_A = 25°C, DE0 = low, DE1 = low, SWG = low, and no interconnect line at the output (unless otherwise noted).

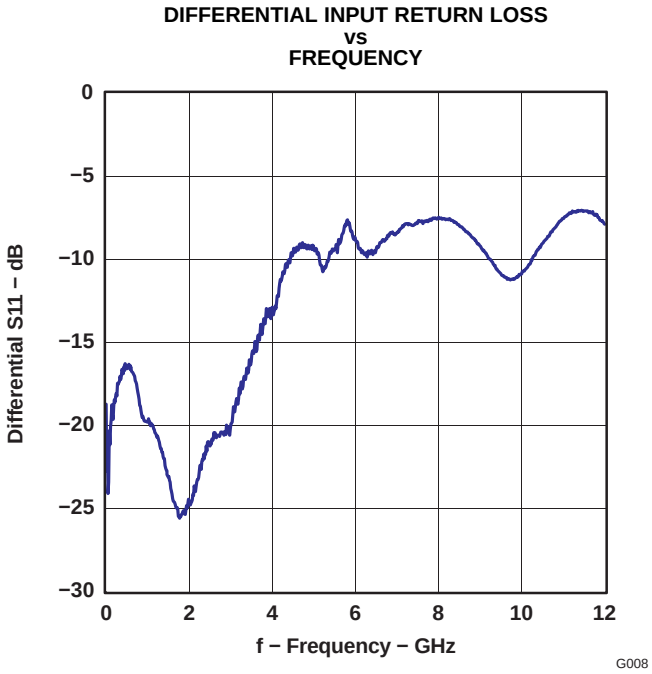


Figure 12.

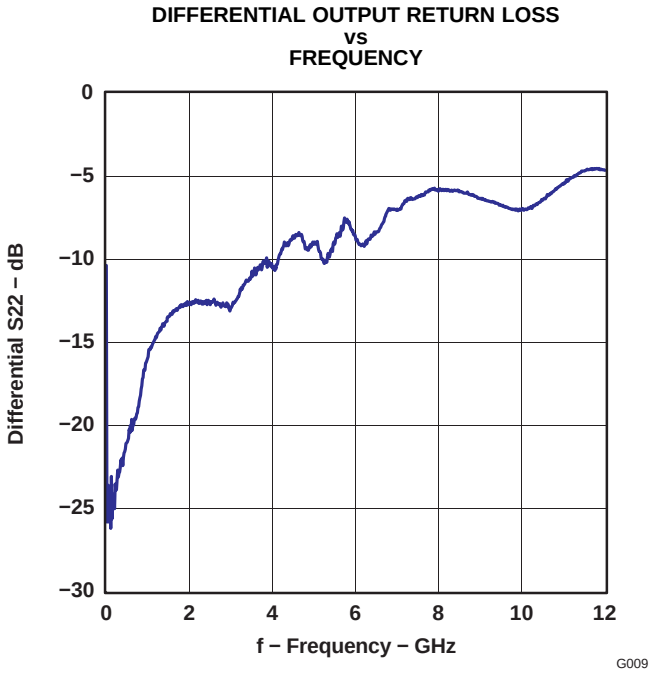


Figure 13.

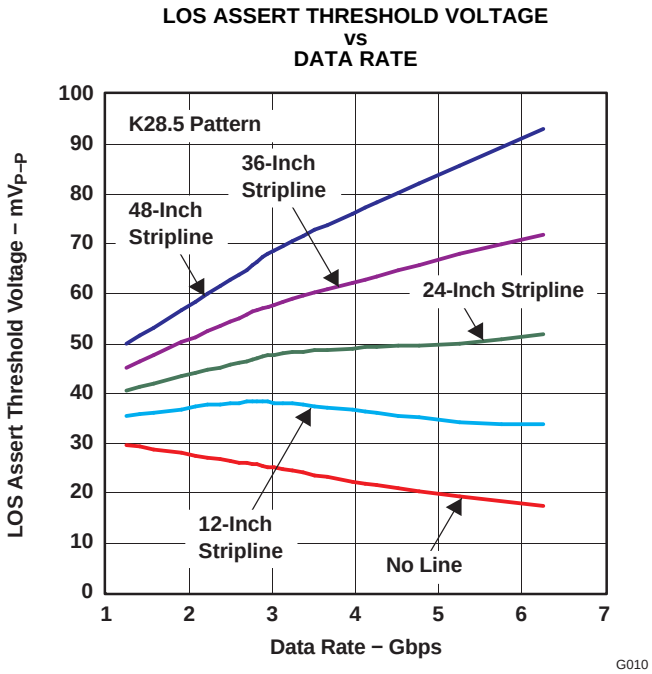


Figure 14.

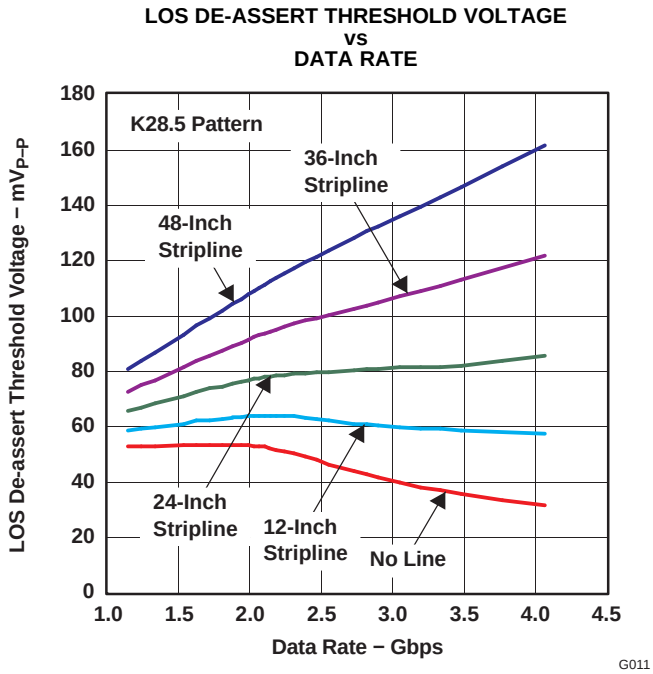


Figure 15.

THERMAL PAD MECHANICAL DATA

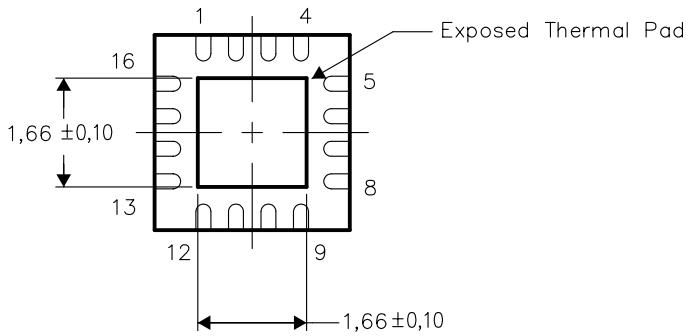
RGT (S–PQFP–N16)

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to a ground or power plane (whichever is applicable), or alternatively, a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No–Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

PACKAGE OPTION ADDENDUM

12-Sep-2006

PACKAGING INFORMATION

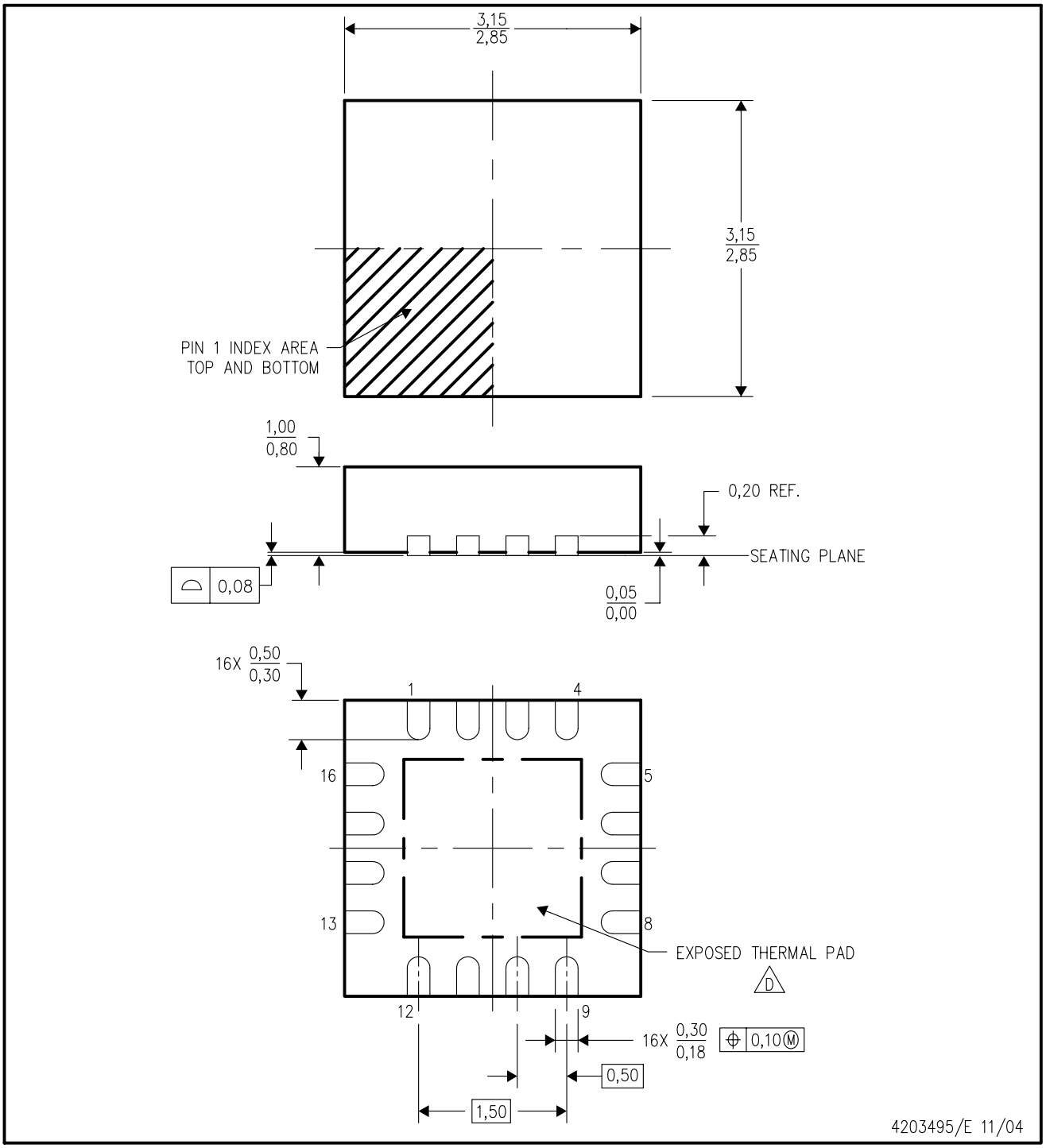
Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TLK6201EARGTR	ACTIVE	QFN	RGT	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TLK6201EARGTRG4	ACTIVE	QFN	RGT	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TLK6201EARGTT	ACTIVE	QFN	RGT	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TLK6201EARGTTG4	ACTIVE	QFN	RGT	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

RGT (S–PQFP–N16) PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–220.

THERMAL PAD MECHANICAL DATA

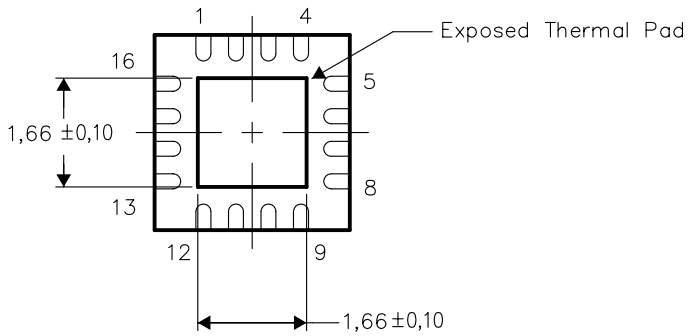
RGT (S–PQFP–N16)

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to a ground or power plane (whichever is applicable), or alternatively, a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No–Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

THERMAL PAD MECHANICAL DATA

RGT (S–PQFP–N16)

THERMAL INFORMATION

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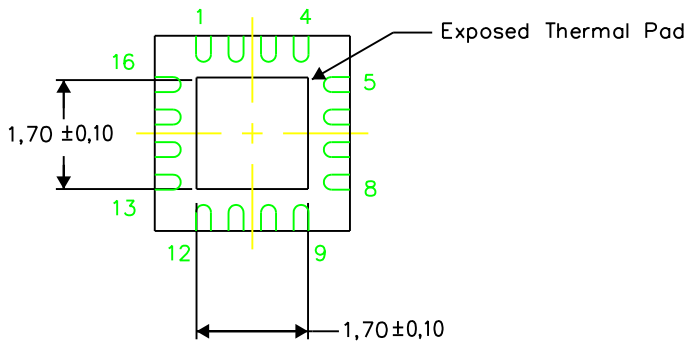
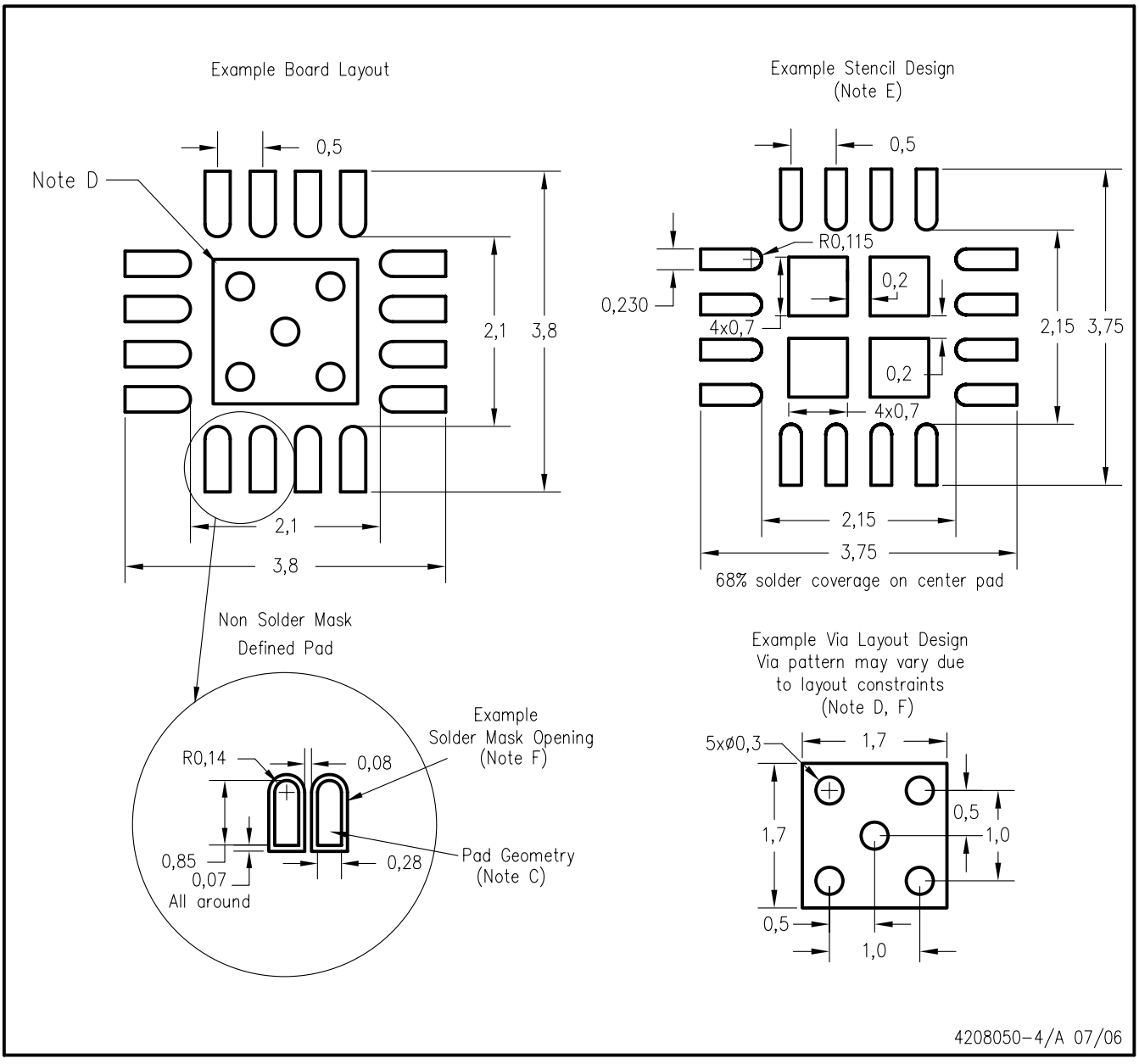


Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

RGT (S–PQFP–N16)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265