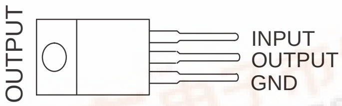
TLV1112
1.2-V, 0.8-A LOW-DROPOUT VOLTAGE REGULATOR

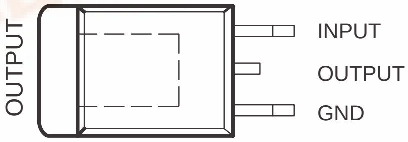
SLVS562B – DECEMBER 2004 – REVISED APRIL 2005

- **Output Current of Up to 800 mA**
- **Operates Down to 1.1-V Dropout**
- **Specified Dropout Voltage at Multiple Current Levels**
- **0.2% Line Regulation Maximum**
- **0.5% Load Regulation Maximum**

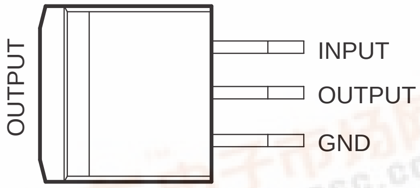
KCS (TO-220) PACKAGE
(TOP VIEW)



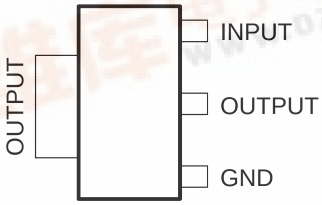
KTP (PowerFLEX™) PACKAGE
(TOP VIEW)



KTT (TO-263) PACKAGE
(TOP VIEW)



DCY (SOT-223) PACKAGE
(TOP VIEW)



description/ordering information

The TLV1112 is a low-dropout voltage regulator, designed to provide up to 800 mA of output current at 1.2 V (typ). All internal circuitry is designed to operate down to 1.1-V input-to-output differential. Dropout voltage is specified at a maximum of 1.3 V at 800 mA, decreasing at lower load currents.

ORDERING INFORMATION

T_J	V_OTYP (V)	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 125°C	1.2 V	PowerFLEX™ (KTP)	Reel of 2000	TLV1112IKTPR	
		SOT-223 (DCY)	Tube of 80	TLV1112IDCY	
			Reel of 2500	TLV1112IDCYR	
		TO-220 (KCS)	Tube of 50	TLV1112IKCS	
		TO-263 (KTT)	Tube of 50	TLV1112IKTT	
			Reel of 1000	TLV1112IKTTR	
0°C to 125°C	1.2 V	PowerFLEX (KTP)	Reel of 2000	TLV1112CKTPR	
		SOT-223 (DCY)	Tube of 80	TLV1112CDCY	
			Reel of 2500	TLV1112CDCYR	
		TO-220 (KCS)	Tube of 50	TLV1112CKCS	
		TO-263 (KTT)	Tube of 50	TLV1112CKTT	
			Reel of 1000	TLV1112CKTTR	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

PRODUCT PREVIEW

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PowerFLEX is a trademark of Texas Instruments.

PRODUCT PREVIEW

description/ordering information (continued)

The low-profile surface-mount KTP package allows the device to be used in applications where space is limited. The TLV1112 requires a minimum of 10 µF of output capacitance for stability. Output capacitors of this size or larger normally are included in most regulator designs.

Unlike pnp-type regulators, where up to 10% of the output current is wasted as quiescent current, the quiescent current of the TLV1112 flows into the load, increasing efficiency.

The TLV1112C is characterized for operation over the virtual junction temperature range of 0°C to 125°C. The TLV1112I is characterized for operation over the virtual junction temperature range of −40°C to 125°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Continuous input voltage . . . . 20 V
Operating virtual junction temperature, T_J . . . . 150°C
Storage temperature range, T_{stg} . . . . −65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

package thermal data (see Note 1)

PACKAGE	BOARD	θ_{JP}[‡]	θ_{JC}	θ_{JA}
PowerFLEX™/TO-252 (KTP)	High K, JESD 51-5	1.4°C/W	19°C/W	28°C/W
SOT (DCY)	High K, JESD 51-7		4°C/W	53°C/W
TO-220 (KCS)	High K, JESD 51-5	3°C/W	17°C/W	19°C/W
TO-263 (KTT)	High K, JESD 51-5	TBD		TBD

NOTE 1: Maximum power dissipation is a function of T_J(max), θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(\text{max}) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.

[‡] For packages with exposed thermal pads, such as QFN, PowerPAD, or PowerFLEX, θ_{JP} is defined as the thermal resistance between the die junction and the bottom of the exposed pad.

recommended operating conditions

			MIN	MAX	UNIT
V_{IN}	Input voltage		2.7	15	V
I_{OUT}	Output current			800	mA
T_J	Operating virtual junction temperature range	TLV1112I	−40	125	°C
		TLV1112C	0	125	

electrical characteristics, T_J = 0°C to 125°C, all typical values are at T_J = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS[†]	TLV1112C			UNIT
		MIN	TYP	MAX	
Output voltage, V_{OUT}	$V_{IN} - V_{OUT}$ = 2 V, I_{OUT} = 10 mA, T_J = 25°C	1.17	1.2	1.23	V
	10 mA ≤ I_{OUT} ≤ 800 mA, 1.4 V ≤ $V_{IN} - V_{OUT}$ ≤ 10 V	1.14	1.2	1.26	
Line regulation	I_{OUT} = 10 mA, 1.5 ≤ $V_{IN} - V_{OUT}$ ≤ 13.8 V		0.035	0.2	%
Load regulation	10 mA ≤ I_{OUT} ≤ 800 mA, $V_{IN} - V_{OUT}$ = 3 V		0.1	0.5	%
Dropout voltage (see Note 4)	I_{OUT} = 100 mA		1.1	1.2	V
	I_{OUT} = 500 mA		1.15	1.25	
	I_{OUT} = 800 mA		1.2	1.3	
Current limit	$V_{IN} - V_{OUT}$ = 5 V[‡], T_J = 25°C	0.8	1.2	1.5	A
Quiescent current	V_{IN} ≤ 15 V		5	10	mA
Thermal regulation	30 ms pulse, T_A = 25°C		0.01	0.1	%/W
Ripple rejection	$V_{IN} - V_{OUT}$ = 3 V, V_{ripple} = 1 V_{pp}, f = 120 Hz	60	75		dB
Minimum load current	V_{IN} = 15 V		1.7	5	mA
Temperature stability	T_J = 0°C to 125°C		0.5		%
Long-term stability	1000 hrs, No load, T_A = 125°C		0.3		%
Output noise voltage (% of V_{OUT})	f = 10 Hz to 100 kHz		0.003		%

[†] All characteristics are measured with a 10-μF capacitor across the input and a 10-μF capacitor across the output. Pulse testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible.

[‡] Current limit test specified under recommended operating conditions

NOTE 2: Dropout is defined as the input-to-output differential at which V_{OUT} drops 100 mV below the value of V_{OUT}, measured at $V_{IN} = V_{OUT(nom)}$ + 1.5 V.

electrical characteristics, T_J = −40°C to 125°C, all typical values are at T_J = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS[†]	TLV1112I			UNIT
		MIN	TYP	MAX	
Output voltage, V_{OUT}	$V_{IN} - V_{OUT}$ = 2 V, I_{OUT} = 10 mA, T_J = 25°C	1.17	1.2	1.23	V
	10 mA ≤ I_{OUT} ≤ 800 mA, 1.4 V ≤ $V_{IN} - V_{OUT}$ ≤ 10 V	1.14	1.2	1.26	
Line regulation	I_{OUT} = 10 mA, 1.5 ≤ $V_{IN} - V_{OUT}$ ≤ 13.8 V		0.035	0.3	%
Load regulation	10 mA ≤ I_{OUT} ≤ 800 mA, $V_{IN} - V_{OUT}$ = 3 V		0.2	0.5	%
Dropout voltage (see Note 4)	I_{OUT} = 100 mA		1.1	1.3	V
	I_{OUT} = 500 mA		1.15	1.35	
	I_{OUT} = 800 mA		1.2	1.4	
Current limit	$V_{IN} - V_{OUT}$ = 5 V[‡], T_J = 25°C	0.8	1.2	1.5	A
Quiescent current	V_{IN} ≤ 15 V		5	15	mA
Thermal regulation	30 ms pulse, T_A = 25°C		0.01	0.1	%/W
Ripple rejection	$V_{IN} - V_{OUT}$ = 3 V, V_{ripple} = 1 V_{pp}, f = 120 Hz	60	75		dB
Minimum load current	V_{IN} = 15 V		1.7	5	mA
Temperature stability	T_J = −40°C to 125°C		0.5		%
Long-term stability	1000 hrs, No load, T_A = 125°C		0.3		%
Output noise voltage (% of V_{OUT})	f = 10 Hz to 100 kHz		0.003		%

[†] All characteristics are measured with a 10-μF capacitor across the input and a 10-μF capacitor across the output. Pulse-testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible.

[‡] Current limit test specified under recommended operating conditions

NOTE 4: Dropout is defined as the input-to-output differential at which V_{OUT} drops 100 mV below the value of V_{OUT}, measured at $V_{IN} = V_{OUT(nom)}$ + 1.5 V.

PRODUCT PREVIEW

TYPICAL CHARACTERISTICS

Figure 1. Short-Circuit Current vs ($V_I - V_O$)

Figure 2. Load Regulation vs Temperature

Figure 3. Ripple Rejection vs Frequency

Figure 4. Ripple Rejection vs Current

Figure 5. Temperature Stability

Figure 6. GND Pin Current vs Temperature

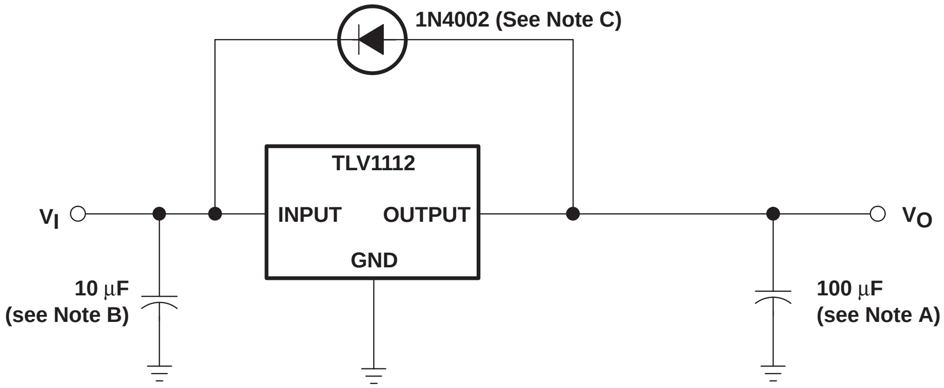
TYPICAL CHARACTERISTICS

Figure 7. Load-Transient Response

Figure 8. Line-Transient Response

PRODUCT PREVIEW

APPLICATION INFORMATION



NOTES: A. Output capacitor selection is critical for regulator stability. The recommended minimum is 10-µF tantalum or 50-µF aluminum electrolytic, with either one having an ESR between the range of 0.3 Ω to 22 Ω. Larger C_{OUT} values benefit the regulator by improving transient response and loop stability.

B. C_{IN} is recommended if TLV1112 is not located near the power-supply filter.

C. An external diode is recommended to protect the regulator if the input instantaneously is shorted to GND.

Figure 9. Typical Application Circuit

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
TLV1112IDCY	PREVIEW	SOT-223	DCY	4	80	TBD	Call TI	Call TI
TLV1112IDCYR	PREVIEW	SOT-223	DCY	4	2500	TBD	Call TI	Call TI
TLV1112IKCS	PREVIEW	TO-220	KCS	3	50	TBD	Call TI	Call TI
TLV1112IKTPR	PREVIEW	PFM	KTP	2	3000	TBD	Call TI	Call TI
TLV1112IKTT	PREVIEW	DDPAK/ TO-263	KTT	3	50	TBD	Call TI	Call TI
TLV1112IKTTR	PREVIEW	DDPAK/ TO-263	KTT	3	500	TBD	Call TI	Call TI

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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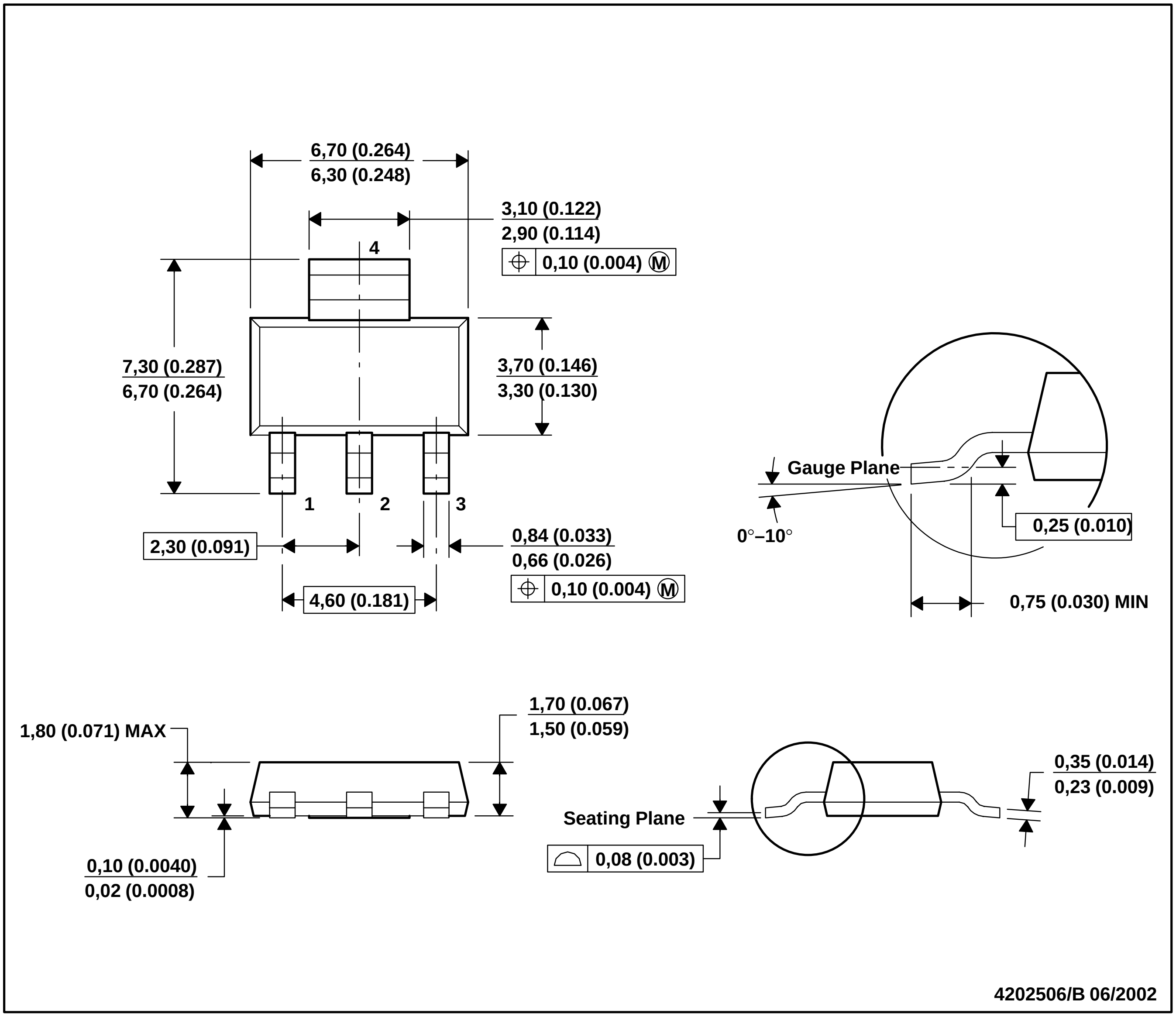
DCY (R-PDSO-G4) **PLASTIC SMALL-OUTLINE**



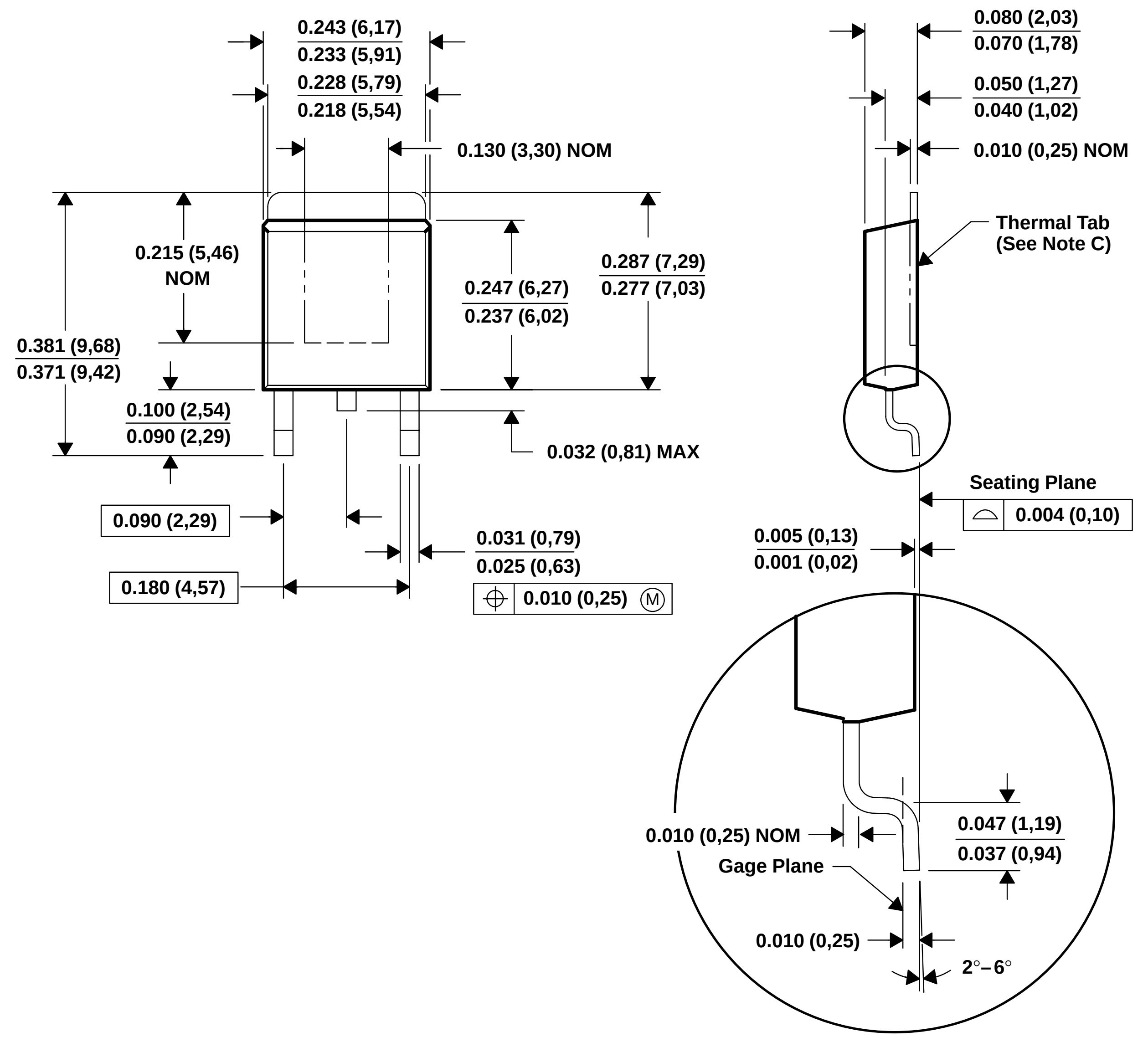
NOTES: A. All linear dimensions are in millimeters (inches).

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion.

D. Falls within JEDEC TO-261 Variation AA.

KTP (R-PSFM-G2) **PowerFLEX™ PLASTIC FLANGE-MOUNT PACKAGE**



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NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. The center lead is in electrical contact with the thermal tab.
D. Dimensions do not include mold protrusions, not to exceed 0.006 (0,15).
E. Falls within JEDEC TO-252 variation AC.

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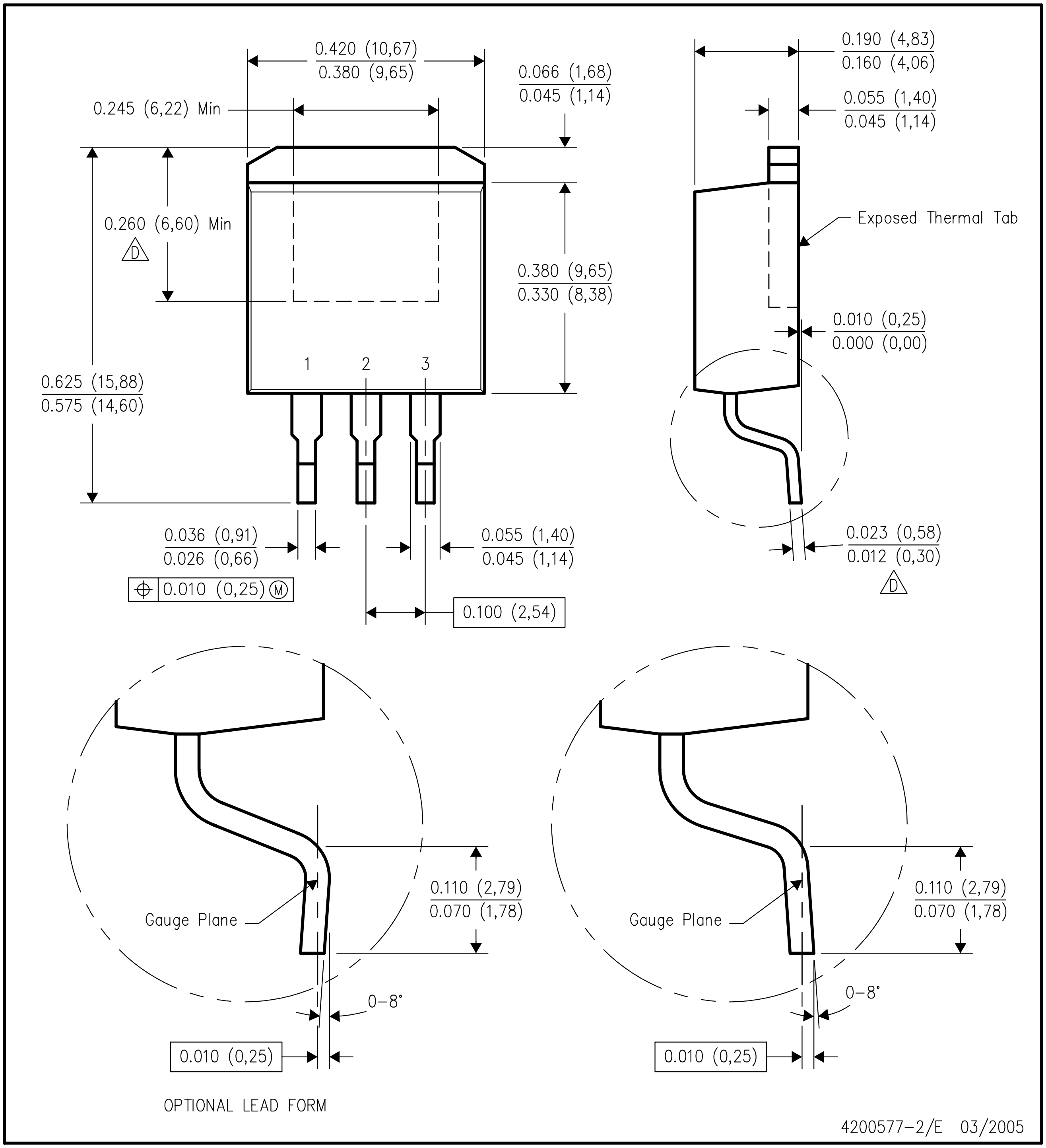
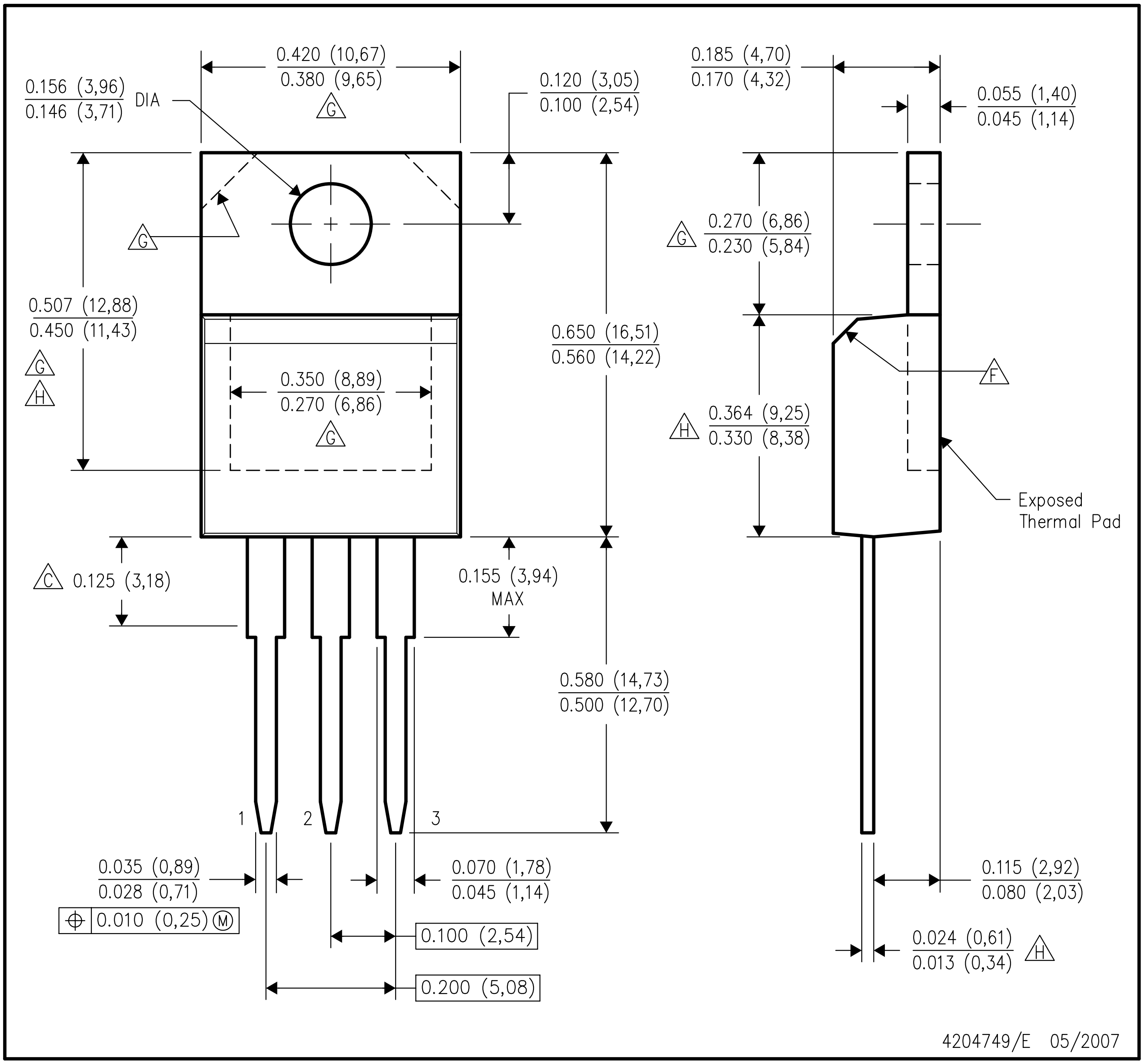
KTT (R–PSFM–G3) PLASTIC FLANGE–MOUNT PACKAGE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion. Mold flash or protrusion not to exceed 0.005 (0,13) per side.
- D Falls within JEDEC TO–263 variation AA, except minimum lead thickness and minimum exposed pad length.

KCS (R–PSFM–T3) PLASTIC FLANGE–MOUNT PACKAGE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Lead dimensions are not controlled within this area.
- D. All lead dimensions apply before solder dip.
- E. The center lead is in electrical contact with the mounting tab.
- F. The chamfer is optional.
- G. Thermal pad contour optional within these dimensions.
- H. Falls within JEDEC TO–220 variation AB, except minimum lead thickness, minimum exposed pad length, and maximum body length.

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