

# TLV7211 TLV7211A CMOS COMPARATORS WITH RAIL-TO-RAIL INPUT AND PUSH-PULL OUTPUT

SLCS149B–AUGUST 2006–REVISED JANUARY 2007

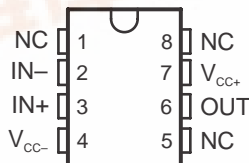
## FEATURES

- Parameters Specified at 2.7-V, 5-V, and 15-V Supplies
- Supply Current 7  $\mu$ A (Typ) at 5 V
- Response Time 4  $\mu$ s (Typ) at 5 V
- Push-Pull Output
- Input Common-Mode Range Beyond  $V_{CC-}$  and  $V_{CC+}$
- Low Input Current

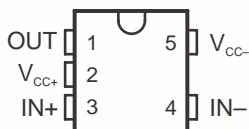
## APPLICATIONS

- Battery-Powered Products
- Notebooks and PDAs
- Mobile Communications
- Alarm and Security Circuits
- Direct Sensor Interface
- Replaces Amplifiers Used as Comparators With Better Performance and Lower Current

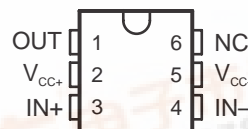
D PACKAGE  
(TOP VIEW)



DBV PACKAGE  
(TOP VIEW)



DCK PACKAGE  
(TOP VIEW)



NC – No internal connection

## DESCRIPTION/ORDERING INFORMATION

The TLV7211 and TLV7211A are micropower CMOS comparators available in the space-saving SOT-23-5 package. This makes the comparators ideal for space- and weight-critical designs. The TLV7211A features an input offset voltage of 5 mV, and the TLV7211 features an input offset voltage of 15 mV.

The main benefits of the SOT-23-5 package are most apparent in small portable electronic devices, such as mobile phones, pagers, notebook computers, personal digital assistants, and PCMCIA cards. The rail-to-rail input voltage makes the TLV7211 or TLV7211A a good choice for sensor interfacing, such as light detector circuits, optical and magnetic sensors, and alarm and status circuits.

The SOT-23-5 package's small size allows it to fit into tight spaces on PC boards.

## ORDERING INFORMATION

$T_A$	$V_{OS}$ (MAX)	PACKAGE <sup>(1)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING <sup>(2)</sup>
–40°C to 85°C	5 mV	SOIC – D	Reel of 2500	TLV7211AIDR	7211AI
			Tube of 75	TLV7211AID	
		SOT-23-5 – DBV	Reel of 3000	TLV7211AIDBVR	YBN_
		SOT (SC-70) – DCK	Reel of 3000	TLV7211AIDCKR	Y8_
			Reel of 250	TLV7211AIDCKT	
	15 mV	SOIC – D	Reel of 2500	TLV7211IDR	TY7211
			Tube of 75	TLV7211ID	
		SOT-23-5 – DBV	Reel of 3000	TLV7211IDBVR	YBK_
			Reel of 3000	TLV7211IDCKR	Y7_
		SOT (SC-70) – DCK	Reel of 250	TLV7211IDCKT	

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

(2) DBV/DCK: The actual top-side marking has one additional character that designates the assembly/test site.



# TLV7211, TLV7211A

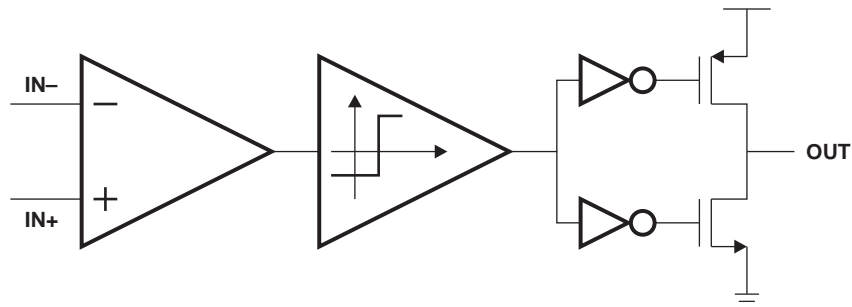
## CMOS COMPARATORS

### WITH RAIL-TO-RAIL INPUT AND PUSH-PULL OUTPUT

SLCS149B–AUGUST 2006–REVISED JANUARY 2007



#### FUNCTIONAL BLOCK DIAGRAM



#### Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_{CC+} - V_{CC-}$	Supply voltage <sup>(2)</sup>		16	V
$V_{ID}$	Differential input voltage <sup>(3)</sup>		±Supply voltage	V
$V_I$	Input voltage range (any input)	$V_{CC-} - 0.3$	$V_{CC+} + 0.3$	V
$V_O$	Output voltage range	$V_{CC-} - 0.3$	$V_{CC+} + 0.3$	V
$I_{CC}$	Supply current		40	mA
$I_I$	Input current		±5	mA
$I_O$	Output current		±30	mA
$\theta_{JA}$	Package thermal impedance <sup>(4)(5)</sup>	D package	97	°C/W
		DBV package	206	
		DCK package	259	
$T_J$	Operating virtual junction temperature		150	°C
$T_{stg}$	Storage temperature range	–65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values (except differential voltages and  $V_{CC}$  specified for the measurement of  $I_{OS}$ ) are with respect to the network GND.
- (3) Differential voltages are at IN+ with respect to IN–.
- (4) Maximum power dissipation is a function of  $T_J(\text{max})$ ,  $\theta_{JA}$ , and  $T_A$ . The maximum allowable power dissipation at any allowable ambient temperature is  $P_D = (T_J(\text{max}) - T_A)/\theta_{JA}$ . Operating at the absolute maximum  $T_J$  of 150°C can affect reliability.
- (5) The package thermal impedance is calculated in accordance with JESD 51-7.

#### ESD Protection

	TYP	UNIT
Human-Body Model	2000	V

#### Recommended Operating Conditions

	MIN	MAX	UNIT
$V_{CC+} - V_{CC-}$	2.7	15	V
$T_J$	–40	85	°C

## 2.7-V Electrical Characteristics

$V_{CC+} = 2.7\text{ V}$ ,  $V_{CC-} = \text{GND}$ ,  $V_{CM} = V_O = V_{CC+}/2$ , and  $R_L > 1\text{ M}\Omega$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$T_J$	TLV7211A			TLV7211			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
$V_{OS}$ Input offset voltage		25°C		3	5		3	15	mV
		–40°C to 85°C			8			18	
$TCV_{OS}$ Input offset voltage temperature drift		25°C		1			1		$\mu\text{V}/^\circ\text{C}$
Input offset voltage average drift <sup>(1)</sup>		25°C		3.3			3.3		$\mu\text{V}/\text{month}$
$I_B$ Input current		25°C		0.04			0.04		pA
$I_{OS}$ Input offset current		25°C		0.02			0.02		pA
CMRR Common-mode rejection ratio	$0 \leq V_{CM} \leq 2.7\text{ V}$	25°C		75			75		dB
PSRR Power-supply rejection ratio	$2.7\text{ V} \leq V_{CC+} \leq 15\text{ V}$	25°C		80			80		dB
$A_V$ Voltage gain		25°C		100			100		dB
CMVR Input common-mode voltage range	CMRR > 55 dB	25°C	2.9	3		2.9	3		V
		–40°C to 85°C	2.7			2.7			
	CMRR > 55 dB	25°C		–0.3	–0.2		–0.3	–0.2	
		–40°C to 85°C			0			0	
$V_{OH}$ High-level output voltage	$I_{load} = 2.5\text{ mA}$	25°C	2.4	2.5		2.4	2.5		V
		–40°C to 85°C	2.3			2.3			
$V_{OL}$ Low-level output voltage	$I_{load} = 2.5\text{ mA}$	25°C		0.2	0.3		0.2	0.3	V
		–40°C to 85°C			0.4			0.4	
$I_{CC}$ Supply current	$V_{OUT} = \text{Low}$	25°C		7	12		7	12	$\mu\text{A}$
		–40°C to 85°C			14			14	
	$V_{OUT} = \text{High-Idle}$	25°C		5	10		5	10	
		–40°C to 85°C			12			12	

(1) Input offset voltage average drift is calculated by dividing the accelerated operating life  $V_{OS}$  drift by the equivalent operational time. This represents worst-case input conditions and includes the first 30 days of drift.

# TLV7211, TLV7211A

## CMOS COMPARATORS

### WITH RAIL-TO-RAIL INPUT AND PUSH-PULL OUTPUT



SLCS149B–AUGUST 2006–REVISED JANUARY 2007

#### 5-V Electrical Characteristics

$V_{CC+} = 5\text{ V}$ ,  $V_{CC-} = \text{GND}$ ,  $V_{CM} = V_O = V_{CC+}/2$ , and  $R_L > 1\text{ M}\Omega$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$T_J$	TLV7211A			TLV7211			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
$V_{OS}$ Input offset voltage		25°C		3	5		3	15	mV
		–40°C to 85°C			8			18	
$TCV_{OS}$ Input offset voltage temperature drift		25°C		1			1		$\mu\text{V}/^\circ\text{C}$
Input offset voltage average drift <sup>(1)</sup>		25°C		3.3			3.3		$\mu\text{V}/\text{month}$
$I_B$ Input current		25°C		0.04			0.04		pA
$I_{OS}$ Input offset current		25°C		0.02			0.02		pA
CMRR Common-mode rejection ratio		25°C		75			75		dB
PSRR Power-supply rejection ratio	$5\text{ V} \leq V_{CC+} \leq 10\text{ V}$	25°C		80			80		dB
$A_V$ Voltage gain		25°C		100			100		dB
CMVR Input common-mode voltage range	CMRR > 55 dB	25°C	5.2	5.3		5.2	5.3		V
		–40°C to 85°C	5			5			
	CMRR > 55 dB	25°C		–0.3	–0.2		–0.3	–0.2	
		–40°C to 85°C			0			0	
$V_{OH}$ High-level output voltage	$I_{load} = 5\text{ mA}$	25°C	4.6	4.8		4.6	4.8		V
		–40°C to 85°C	4.45			4.45			
$V_{OL}$ Low-level output voltage	$I_{load} = 5\text{ mA}$	25°C		0.2	0.4		0.2	0.4	V
		–40°C to 85°C			0.55			0.55	
$I_{CC}$ Supply current	$V_{OUT} = \text{Low}$	25°C		7	14		7	14	$\mu\text{A}$
		–40°C to 85°C			18			18	
	$V_{OUT} = \text{High-Idle}$	25°C		5	10		5	10	
		–40°C to 85°C			13			13	
$I_{OH}$ Short-circuit output current	$I_{source}$	25°C	30			30			mA
$I_{OL}$ Short-circuit output current	$I_{sink}$ , $V_O < 12\text{ V}^{(2)}$	25°C	45			45			mA

(1) Input offset voltage average drift is calculated by dividing the accelerated operating life  $V_{OS}$  drift by the equivalent operational time. This represents worst-case input conditions and includes the first 30 days of drift.

(2) Do not short circuit the output to  $V_+$  if  $V_+$  is  $> 12\text{ V}$ .

## 15-V Electrical Characteristics

$V_{CC+} = 15\text{ V}$ ,  $V_{CC-} = \text{GND}$ ,  $V_{CM} = V_O = V_{CC+}/2$ , and  $R_L > 1\text{ M}\Omega$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$T_J$	TLV7211A			TLV7211			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
$V_{OS}$ Input offset voltage		25°C		3	5		3	15	mV
		–40°C to 85°C			8			18	
$TCV_{OS}$ Input offset voltage temperature drift		25°C		4			4		$\mu\text{V}/^\circ\text{C}$
Input offset voltage average drift <sup>(1)</sup>		25°C		4			4		$\mu\text{V}/\text{month}$
$I_B$ Input current		25°C		0.04			0.04		pA
$I_{OS}$ Input offset current		25°C		0.02			0.02		pA
CMRR Common-mode rejection ratio		25°C		82			82		dB
PSRR Power-supply rejection ratio	$5\text{ V} \leq V_{CC+} \leq 10\text{ V}$	25°C		80			80		dB
$A_V$ Voltage gain		25°C		100			100		dB
CMVR Input common-mode voltage range	CMRR > 55 dB	25°C	15.2	15.3		15.2	15.3		V
		–40°C to 85°C	15			15			
	CMRR > 55 dB	25°C		–0.3	–0.2		–0.3	–0.2	
		–40°C to 85°C			0			0	
$V_{OH}$ High-level output voltage	$I_{load} = 5\text{ mA}$	25°C	14.6	14.8		14.6	14.8		V
		–40°C to 85°C	14.45			14.45			
$V_{OL}$ Low-level output voltage	$I_{load} = 5\text{ mA}$	25°C		0.2	0.4		0.2	0.4	V
		–40°C to 85°C			0.55			0.55	
$I_{CC}$ Supply current	$V_{OUT} = \text{Low}$	25°C		7	14		7	14	$\mu\text{A}$
		–40°C to 85°C			18			18	
	$V_{OUT} = \text{High-Idle}$	25°C		5	12		5	12	
		–40°C to 85°C			14			14	
$I_{OH}$ Short-circuit output current	$I_{source}$	25°C	30			30			mA
$I_{OL}$ Short-circuit output current	$I_{sink}$ , $V_O < 12\text{ V}^{(2)}$	25°C	45			45			mA

(1) Input offset voltage average drift is calculated by dividing the accelerated operating life  $V_{OS}$  drift by the equivalent operational time. This represents worst-case input conditions and includes the first 30 days of drift.

(2) Do not short circuit the output to  $V+$  if  $V+$  is >12 V.

# TLV7211, TLV7211A

## CMOS COMPARATORS

### WITH RAIL-TO-RAIL INPUT AND PUSH-PULL OUTPUT



SLCS149B–AUGUST 2006–REVISED JANUARY 2007

#### Switching Characteristics

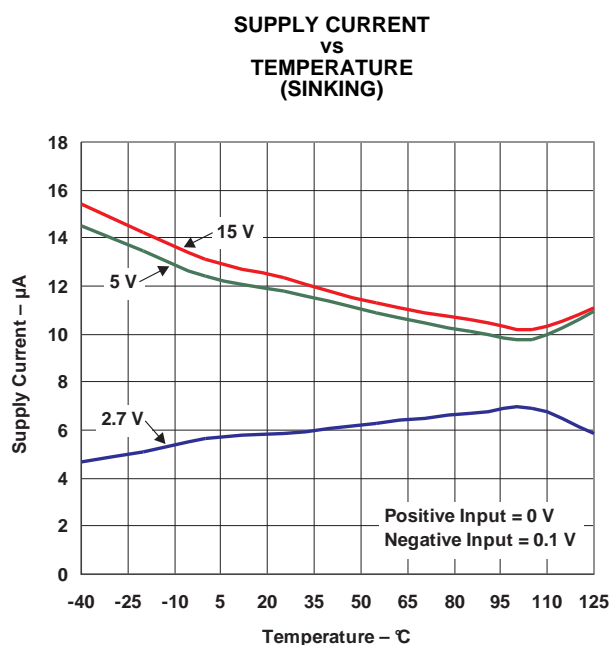
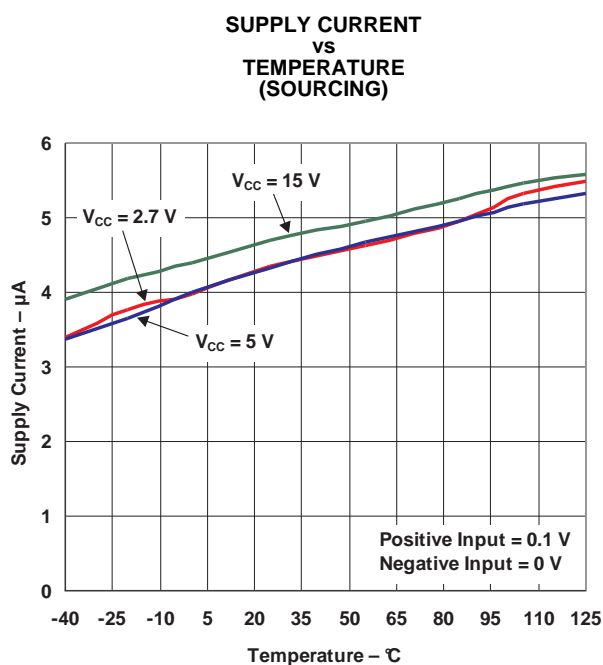
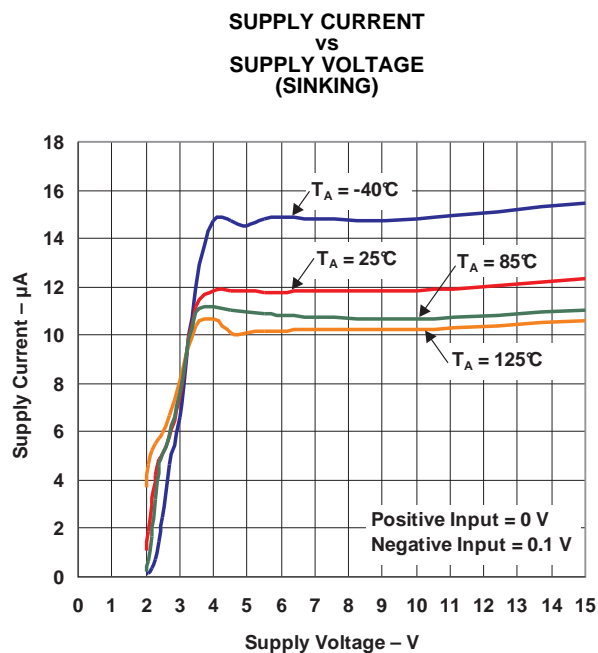
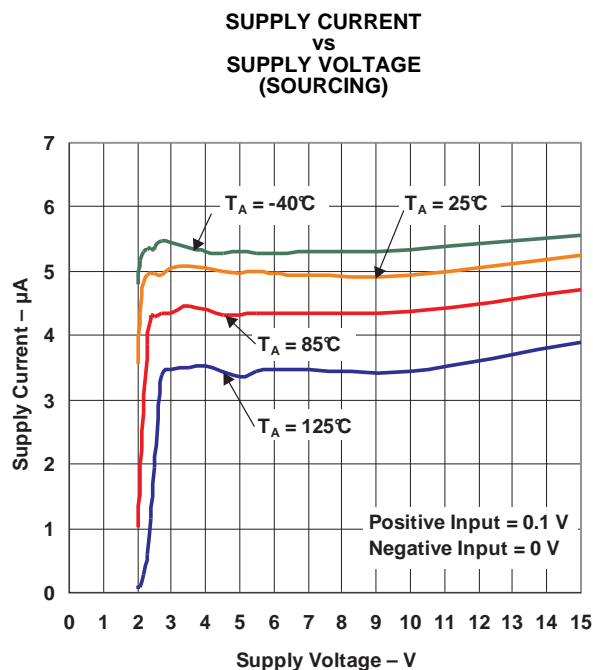
$T_J = 25^\circ\text{C}$ ,  $V_{CC+} = 5\text{ V}$ ,  $V_{CC-} = \text{GND}$ ,  $V_{CM} = V_O = V_{CC+}/2$ , and  $R_L > 1\text{ M}\Omega$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS		TYP	UNIT
$t_{\text{rise}}$	Rise time	$f = 10\text{ kHz}$ , $C_L = 50\text{ pF}^{(1)}$ , Overdrive = 10 mV		0.3	$\mu\text{s}$
$t_{\text{fall}}$	Fall time	$f = 10\text{ kHz}$ , $C_L = 50\text{ pF}^{(1)}$ , Overdrive = 10 mV		0.3	$\mu\text{s}$
$t_{\text{PHL}}$	Propagation delay time, high to low <sup>(2)</sup>	$f = 10\text{ kHz}$ , $C_L = 50\text{ pF}^{(1)}$	10 mV	10	$\mu\text{s}$
			100 mV	4	
		$V_{CC+} = 2.7\text{ V}$ , $f = 10\text{ kHz}$ , $C_L = 50\text{ pF}^{(1)}$	10 mV	10	
			100 mV	4	
$t_{\text{PLH}}$	Propagation delay time, low to high <sup>(2)</sup>	$f = 10\text{ kHz}$ , $C_L = 50\text{ pF}^{(1)}$	10 mV	6	$\mu\text{s}$
			100 mV	4	
		$V_{CC+} = 2.7\text{ V}$ , $f = 10\text{ kHz}$ , $C_L = 50\text{ pF}^{(1)}$	10 mV	7	
			100 mV	4	

(1)  $C_L$  includes probe and jig capacitance.

(2) Input step voltage for propagation delay measurement is 2 V.

## TYPICAL CHARACTERISTICS



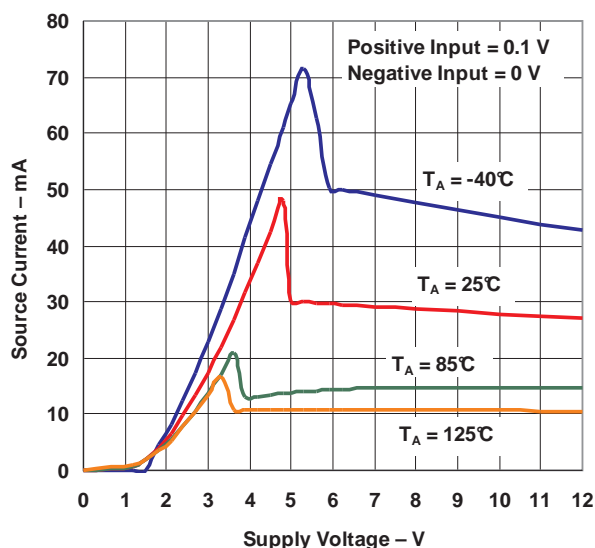
# TLV7211, TLV7211A CMOS COMPARATORS WITH RAIL-TO-RAIL INPUT AND PUSH-PULL OUTPUT

SLCS149B–AUGUST 2006–REVISED JANUARY 2007

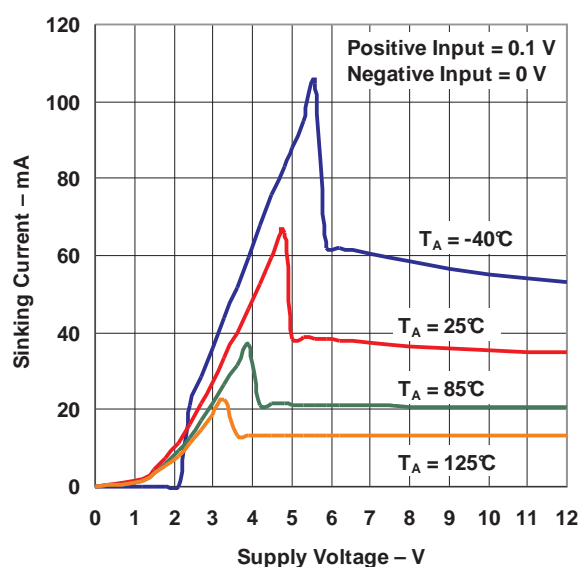


## TYPICAL CHARACTERISTICS (continued)

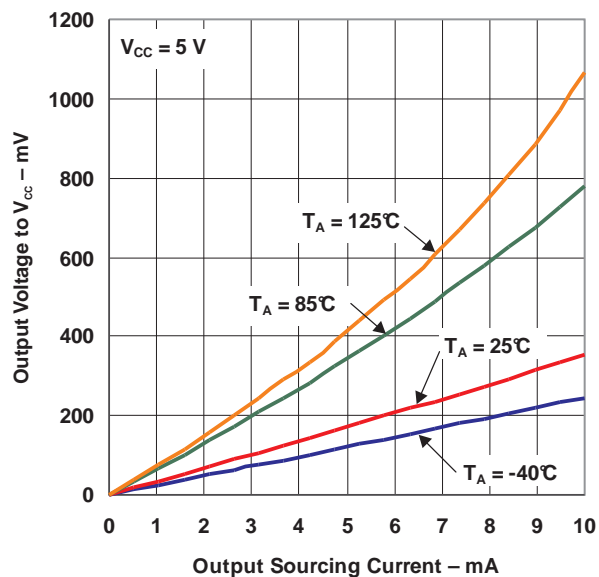
OUTPUT SOURCING CURRENT  
vs  
SUPPLY VOLTAGE



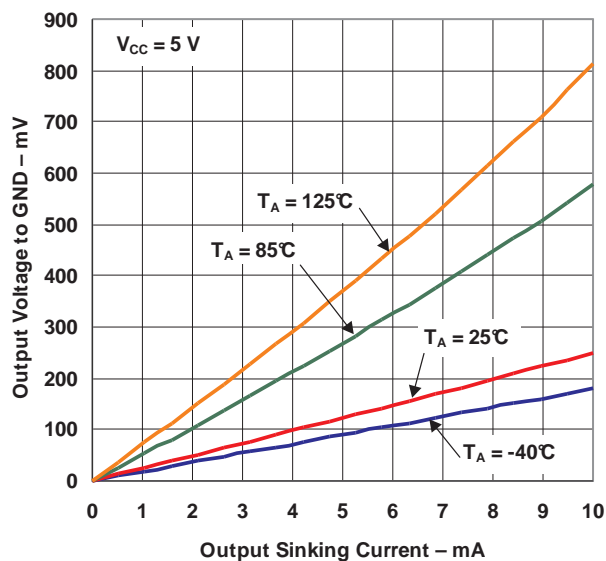
OUTPUT SINKING CURRENT  
vs  
SUPPLY VOLTAGE



OUTPUT VOLTAGE  
vs  
OUTPUT SOURCING CURRENT



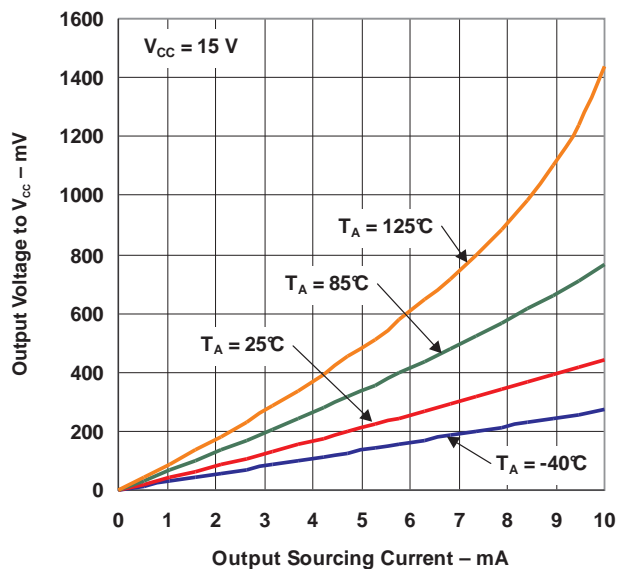
OUTPUT VOLTAGE  
vs  
OUTPUT SINKING CURRENT



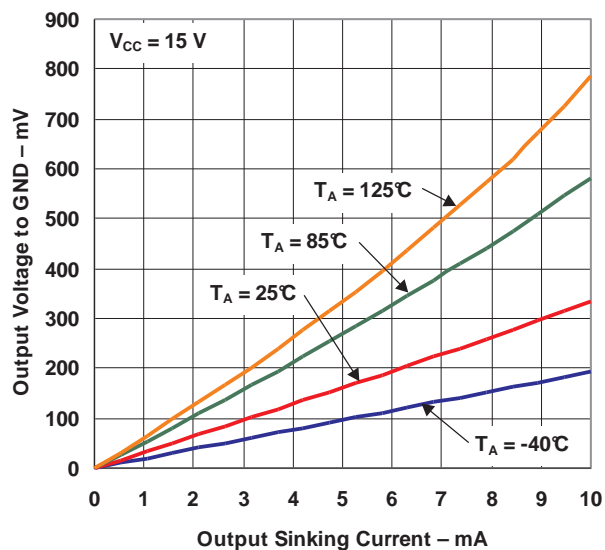


**TYPICAL CHARACTERISTICS (continued)**

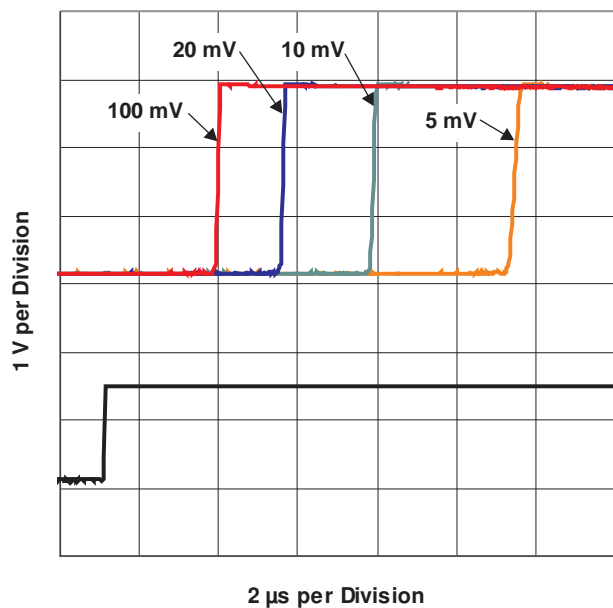
OUTPUT VOLTAGE  
 vs  
 OUTPUT SOURCING CURRENT



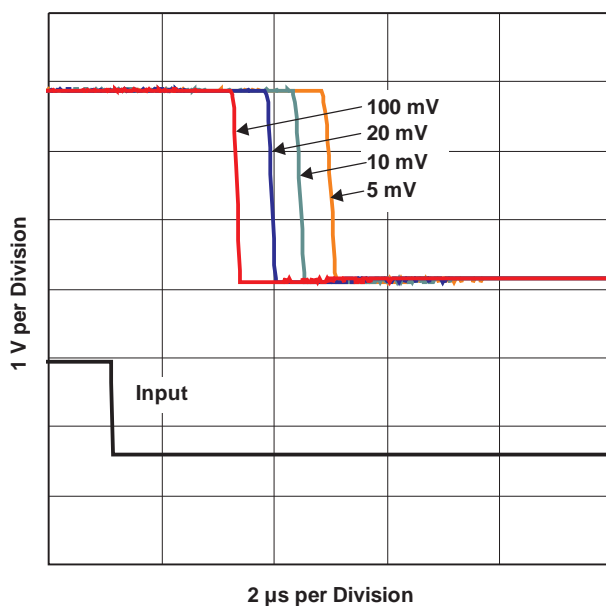
OUTPUT VOLTAGE  
 vs  
 OUTPUT SINKING CURRENT



Response Time ( $t_{PLH}$ ) for Various Input Overdrives  
 ( $V_{CC} = 2.7\text{ V}$ )



Response Time ( $t_{PHL}$ ) for Various Input Overdrives  
 ( $V_{CC} = 2.7\text{ V}$ )



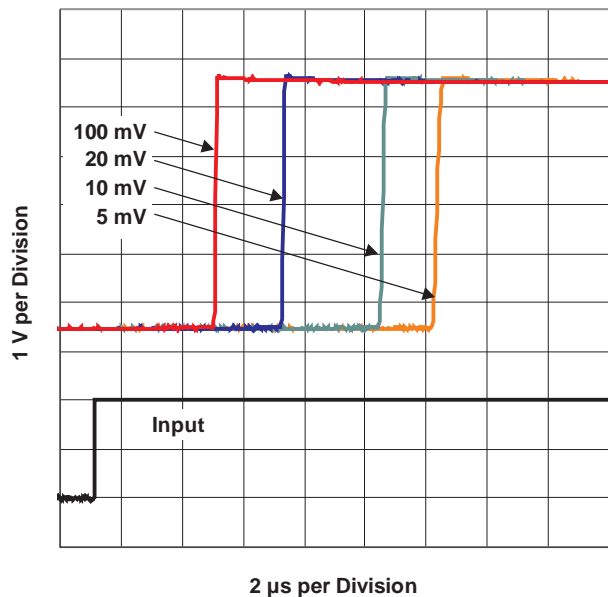
# TLV7211, TLV7211A CMOS COMPARATORS WITH RAIL-TO-RAIL INPUT AND PUSH-PULL OUTPUT

SLCS149B–AUGUST 2006–REVISED JANUARY 2007

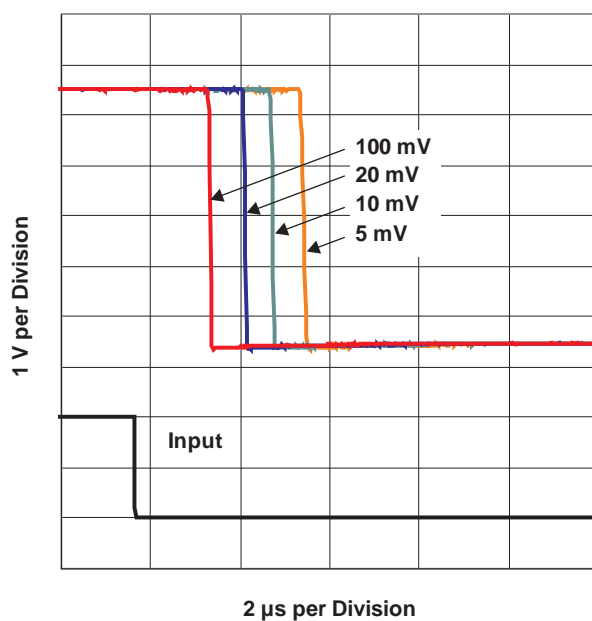


## TYPICAL CHARACTERISTICS (continued)

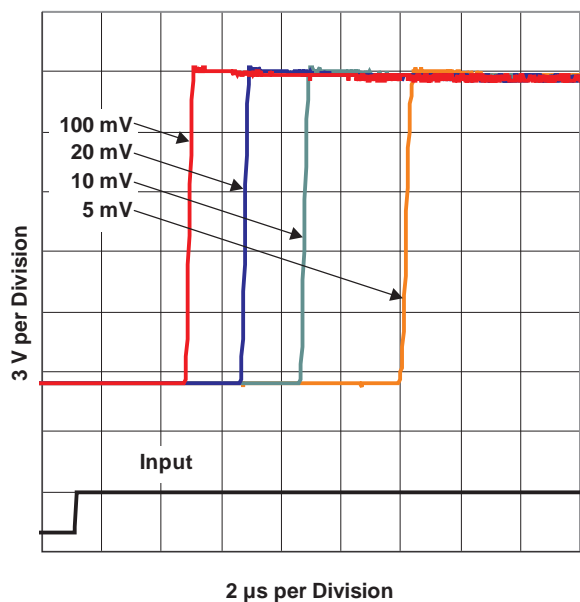
Response Time ( $t_{PLH}$ ) for Various Input Overdrives  
( $V_{CC} = 5\text{ V}$ )



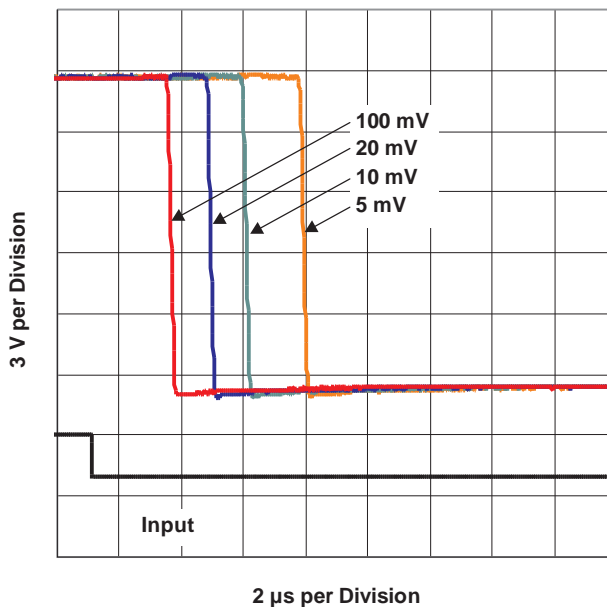
Response Time ( $t_{PHL}$ ) for Various Input Overdrives  
( $V_{CC} = 5\text{ V}$ )



Response Time ( $t_{PLH}$ ) for Various Input Overdrives  
( $V_{CC} = 15\text{ V}$ )



Response Time ( $t_{PHL}$ ) for Various Input Overdrives  
( $V_{CC} = 15\text{ V}$ )



## PACKAGING INFORMATION

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
TLV7211AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV7211AIDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV7211AIDBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV7211AIDCKR	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV7211AIDCKRG4	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV7211AIDCKT	ACTIVE	SC70	DCK	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV7211AIDCKTG4	ACTIVE	SC70	DCK	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV7211AIDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV7211AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV7211AIDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV7211ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV7211IDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV7211IDBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV7211IDCKR	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV7211IDCKRG4	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV7211IDCKT	ACTIVE	SC70	DCK	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV7211IDCKTG4	ACTIVE	SC70	DCK	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV7211IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV7211IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV7211IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

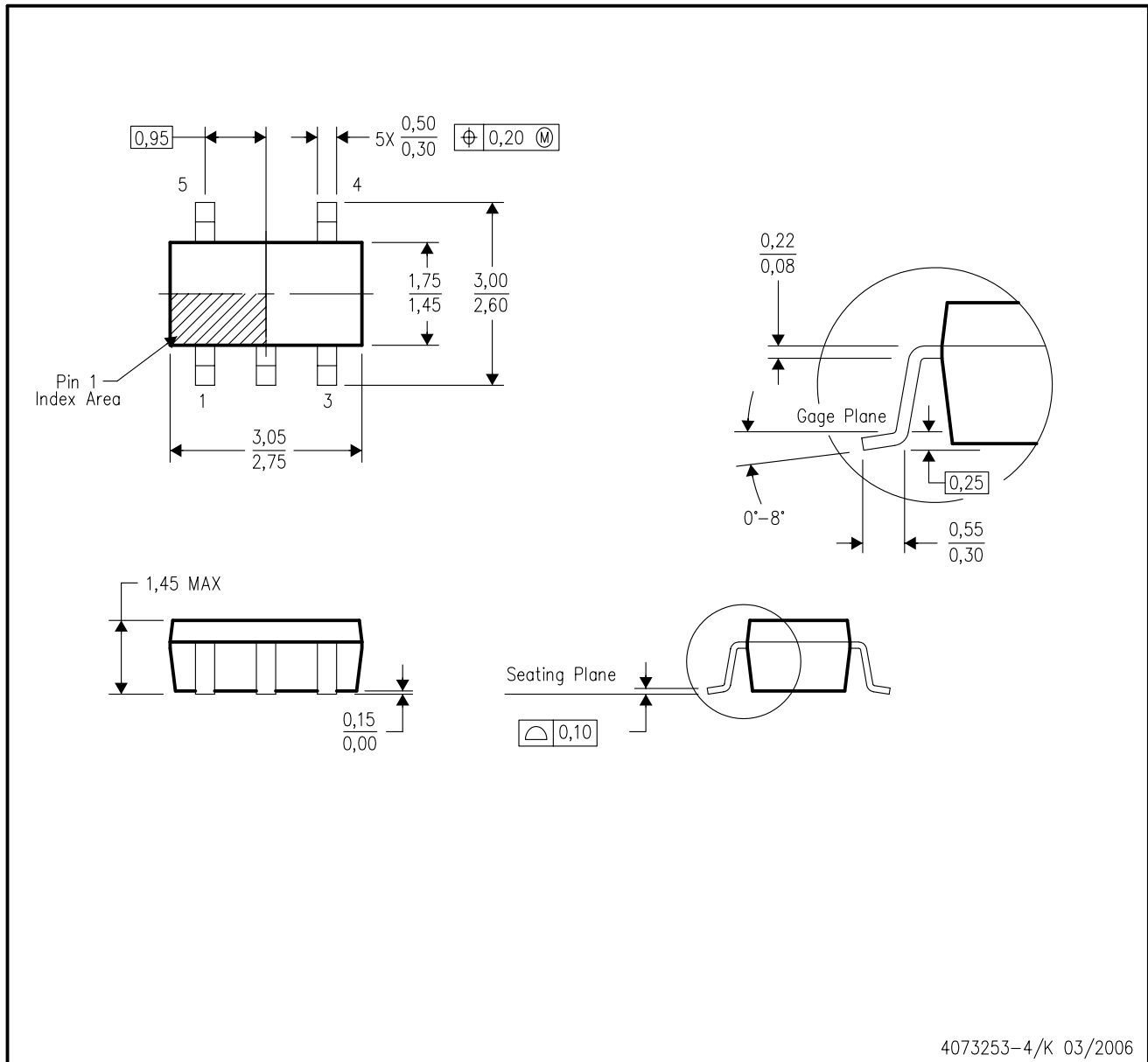
**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

# MECHANICAL DATA

DBV (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE

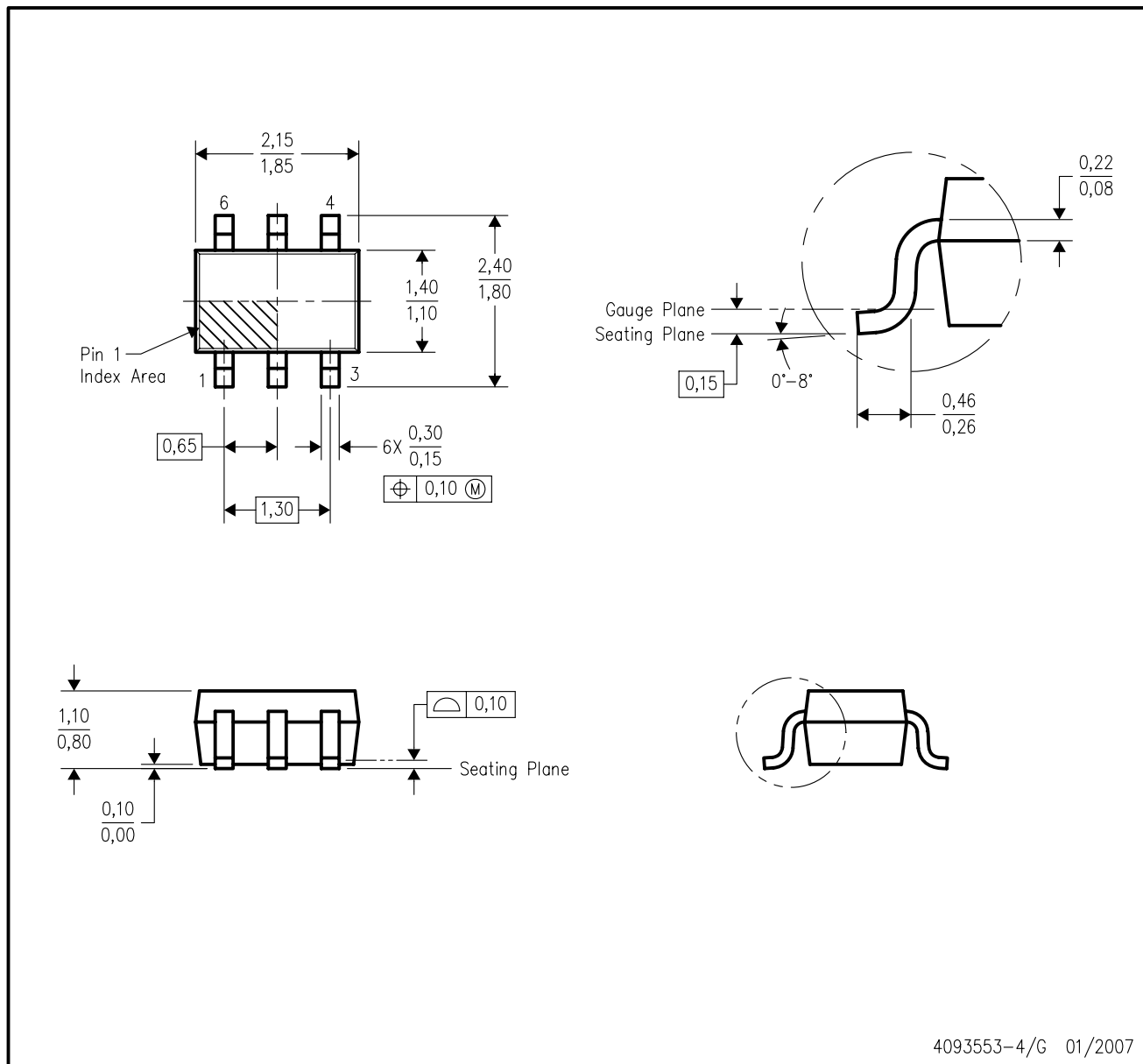


- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
  - Falls within JEDEC MO-178 Variation AA.

## MECHANICAL DATA

DCK (R-PDSO-G6)

PLASTIC SMALL-OUTLINE PACKAGE

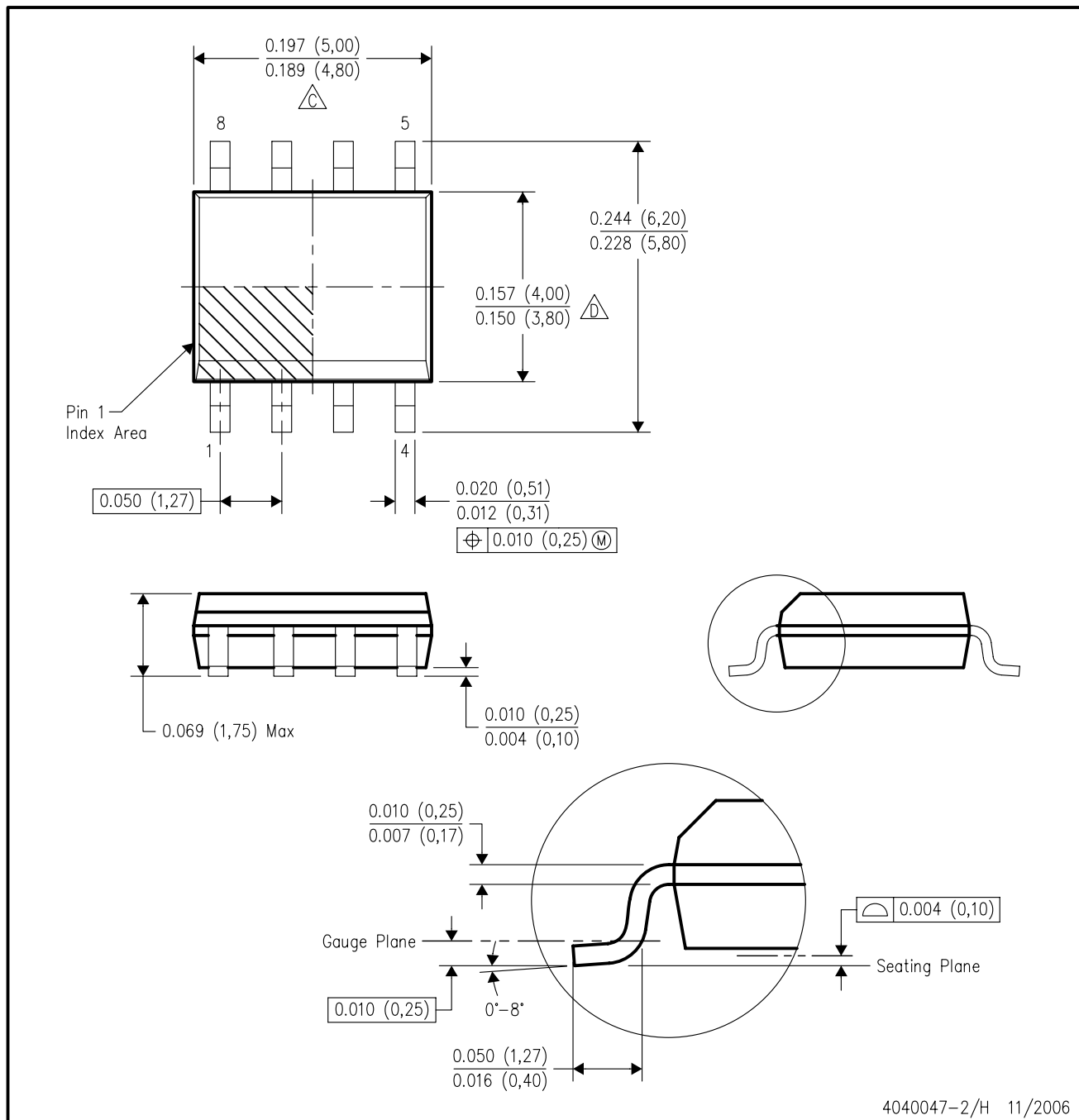


- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
  - Falls within JEDEC MO-203 variation AB.

# MECHANICAL DATA

## D (R-PDSO-G8)

## PLASTIC SMALL-OUTLINE PACKAGE



### NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
- D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
- E. Reference JEDEC MS-012 variation AA.

## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

### Products

Amplifiers	<a href="http://amplifier.ti.com">amplifier.ti.com</a>
Data Converters	<a href="http://dataconverter.ti.com">dataconverter.ti.com</a>
DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>
Interface	<a href="http://interface.ti.com">interface.ti.com</a>
Logic	<a href="http://logic.ti.com">logic.ti.com</a>
Power Mgmt	<a href="http://power.ti.com">power.ti.com</a>
Microcontrollers	<a href="http://microcontroller.ti.com">microcontroller.ti.com</a>
Low Power Wireless	<a href="http://www.ti.com/lpw">www.ti.com/lpw</a>

### Applications

Audio	<a href="http://www.ti.com/audio">www.ti.com/audio</a>
Automotive	<a href="http://www.ti.com/automotive">www.ti.com/automotive</a>
Broadband	<a href="http://www.ti.com/broadband">www.ti.com/broadband</a>
Digital Control	<a href="http://www.ti.com/digitalcontrol">www.ti.com/digitalcontrol</a>
Military	<a href="http://www.ti.com/military">www.ti.com/military</a>
Optical Networking	<a href="http://www.ti.com/opticalnetwork">www.ti.com/opticalnetwork</a>
Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
Telephony	<a href="http://www.ti.com/telephony">www.ti.com/telephony</a>
Video & Imaging	<a href="http://www.ti.com/video">www.ti.com/video</a>
Wireless	<a href="http://www.ti.com/wireless">www.ti.com/wireless</a>

Mailing Address: Texas Instruments  
Post Office Box 655303 Dallas, Texas 75265