

TMC2081

Digital Video Mixer

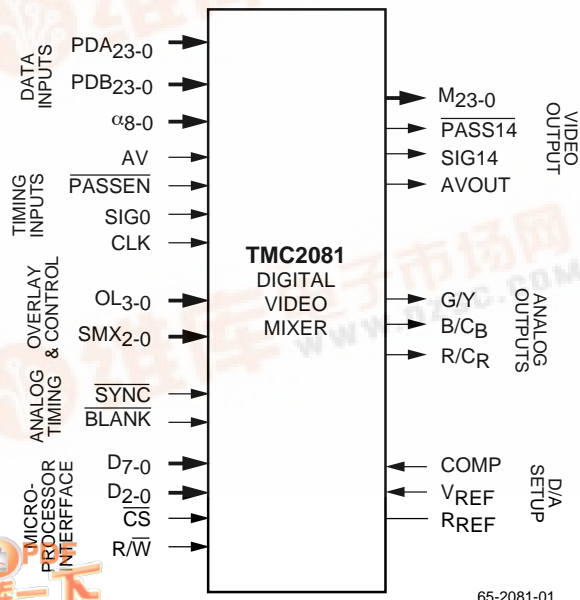
Features

- Mixes 24//16-bit GBR/YC_BCR444//YC_BCR422 and 8-bit color-index sources
- 24//16-bit GBR/YC_BCR444//YC_BCR422 output
- 255-step proportional mixing via α_{7-0} inputs
- 256-step mixing with α_{8-0} for $\alpha=100h$ unity gain
- 256 x 8-bit look-up table on α channel
- Lap-dissolve and fade effects
- α and crosspoint controls for soft and color-border wipe generation
- Mask register and three 256 x 8 bypassable CLUTs with overlay on A-channel
- Analog preview output with sync on Green/Y
- D/A power-down modes
- Single +5 volt power supply operation
- Pin compatible with TMC22080 Digital Mixer

Applications

- Mixing computer graphics and live video
- Lap-dissolve between video sources
- Fade to black or to user-selectable fill color
- Window/wipe processing

Logic Symbol



65-2081-01

Description

The TMC2081 is a Digital Video Mixer that performs

$$M = (\alpha) V_1 + (1-\alpha) V_2 \quad (0 \leq \alpha \leq 1)$$

cross-fading at speeds faster than 40 Mpps proportionally controlled by a 9-bit α -channel input. Variable rate dissolves and fades may be implemented with unity gain at the α endpoints. With the α -Look-Up Table (α LUT), mixing may be controlled by a single bit of the α -channel input. Setup is via a microprocessor interface.

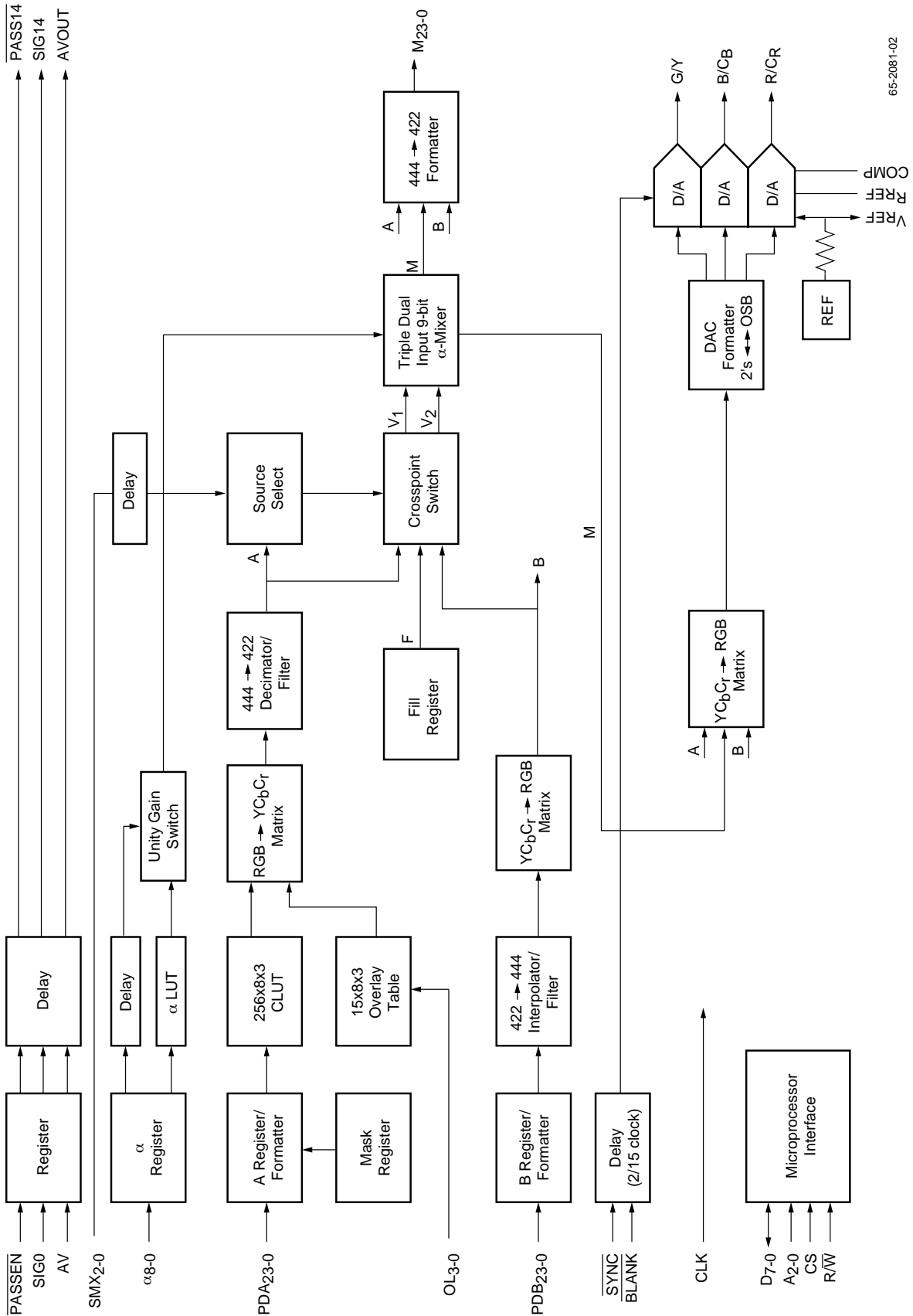
Supported video formats are 24-bit GBR, YC_BCR444, and 16-bit YC_BCR422 component video. Dissimilar pixel formats may be mixed using on-chip interpolation and decimation filters and GBR/YC_BCR and YC_BCR/GBR color-space conversion matrices.

An additional format accepted by the A-channel is 8-bit color-indexed pixel data which addresses three bypassable 256 x 8 color look-up tables (CLUTs). A 15 color overlay palette and a 24-bit fill register are also included.

Digital and Analog outputs may be programmed to view either mixer inputs, V_1 or V_2 or mixer output, M .

Packaged in a 128-lead plastic metric quad flat-pack (MQFP), the TMC2081 is fabricated with a sub-micron CMOS process. Performance is guaranteed over the commercial, 0°C to 70°C temperature range.

Block Diagram



Functional Description

The TMC2081 is a monolithic digital video processor that proportionally mixes digital video in GBR, YC_BCR, or color-index formats. Some of the variety of input and output data format combinations are shown in Table 1.

The A-channel data path has transformation circuits that can look up 24-bit GBR values from 8-bit color-index inputs, convert GBR-to-YC_BCR format, and decimate YC_BCR444 to YC_BCR422. The B-channel path includes circuits that convert YC_BCR to GBR and interpolate YC_BCR422 to YC_BCR444. Prior to mixing, incoming pixel data streams must be converted to matching formats by setting the A and B channel control registers.

Data enters the TMC2081 through the PDA₂₃₋₀, PDB₂₃₋₀, α₈₋₀, and OL₃₋₀ ports. Data and video controls ($\overline{\text{PASEN}}$ and AV) are simultaneously registered on the rising edge of PXCLK. Pipeline latency is 14 clock cycles to the mixed digital video output.

Although PDA₂₃₋₀, PDB₂₃₋₀, and M₂₃₋₀ data formats may be different, V₁ and V₂ data formats at the α-Mixer input must be matched: unsigned magnitude for GBR and Y components; 2's complement for C_B and C_R components.

Data formats converted within the TMC2081 are determined by the control bits programmed into the internal registers.

Output format may be GBR, YC_BCR444 or YC_BCR422. Either crosspoint switch input, A and B or the Mixer output may be selected at the M₂₃₋₀ port. Table 2, Table 3 and Table 4 show examples of the M₂₃₋₀ output for 9-bit α-mixing. In Table 3, C_BCR is accepted at the C_B input. Table 4 exemplifies format conversion.

Mixer output and inputs may be previewed by three video D/A converters. Analog outputs may be either GBR or YC_BCR.

For initialization and control, internal registers and tables may be accessed through a microprocessor interface.

Power may be conserved by disabling the D/A converters or sections of the TMC2081 via internal Control Registers. In the latter mode, the microprocessor interface remains active and Control Register settings are retained but CLUT locations are not accessible.

Table 1. Input and Output Data Format Examples

A Input Format	B Input Format	A CLUT	A GBR-YC _B CR	A Decimate	B Interpolate	B YC _B CR-GBR	M Format	M Output Format
YC _B CR444	YC _B CR444	Bypass	Bypass	Bypass	Bypass	Bypass	Low	YC _B CR444
YC _B CR444	YC _B CR422	Bypass	Bypass	Bypass	Enable	Bypass	Low	YC _B CR444
YC _B CR444	YC _B CR422	Bypass	Bypass	Enable	Bypass	Bypass	High	YC _B CR422
YC _B CR422	YC _B CR422	Bypass	Bypass	Bypass	Bypass	Bypass	High	YC _B CR422
YC _B CR422	YC _B CR422	Bypass	Bypass	Bypass	Bypass	Bypass	Low	YC _B CR444
GBR, CI	YC _B CR444	Enable	Bypass	Bypass	Bypass	Enable	Low	GBR
GBR, CI	YC _B CR444	Enable	Enable	Bypass	Bypass	Bypass	Low	YC _B CR444
GBR, CI	YC _B CR422	Enable	Bypass	Bypass	Enable	Enable	Low	GBR
GBR, CI	YC _B CR422	Enable	Enable	Enable	Bypass	Bypass	High	YC _B CR422
GBR, CI	GBR	Enable	Bypass	Bypass	Bypass	Bypass	Low	GBR

Table 2. GBR Mixing Example (9-bit α)

α (hex)	PDA (hex)			PDB (hex)			M (hex)		
	G	B	R	G	B	R	G	B	R
000	BB	CC	AA	EE	FF	DD	EE	FF	DD
040	BB	CC	AA	EE	FF	DD	E1	F2	D0
080	BB	CC	AA	EE	FF	DD	D5	E6	C4
100	BB	CC	AA	EE	FF	DD	BB	CC	AA

Table 3. Y_{C_BC_R}422 Mixing Example (C_B and C_R in 2's Complement)

α (hex)	PDA (hex)			PDB (hex)			M (hex)		
	Y	C _B	C _R	Y	C _B	C _R	Y	C _B	C _R
40	10	F4	XX	20	4	XX	1C	00	00
80	10	F4	XX	20	4	XX	18	00	00
40	10	F4	XX	20	4	XX	1C	00	00
40	10	FE	XX	20	2	XX	1C	01	00
A0	30	60	XX	40	70	XX	36	66	00
B0	30	80	XX	40	90	XX	35	86	00
A0	30	C0	XX	40	D0	XX	36	C6	00
B0	30	E0	XX	40	F0	XX	35	E5	00

Table 4. Y_{C_BC_R}422-to-Y_{C_BC_R}444 Mixing Example

α (hex)	PDA (hex)			PDB (hex)			M (hex)		
	Y	C _B	C _R	Y	C _B	C _R	Y	C _B	C _R
40	10	F4	XX	20	4	XX	1C	00	00
40	10	F4	XX	20	4	XX	1C	00	00
40	10	F4	XX	20	4	XX	1C	00	01
40	10	FE	XX	20	2	XX	1C	00	01
A0	30	60	XX	40	70	XX	36	66	86
B0	30	80	XX	40	90	XX	35	66	86
A0	30	C0	XX	40	D0	XX	36	C6	E5
B0	30	E0	XX	40	F0	XX	35	C6	E5

Input Formats

Data is accepted by PDA and PDB channels in one pair of the following formats:

1. Y_{C_BC_R}444
2. Y_{C_BC_R}422
3. GBR
4. 8-bit color-index mapped to a palette of 256x256x256 colors. (A-channel only)

Details of bits assignments are shown in Figure 1. Pixel Data Formats with the expected data ranges are shown in Table 5.

Table 5. Y_{C_BC_R} and GBR Data Types and Ranges

Signal	Min.	Max.	Format
GBR	0	255	Unsigned Binary
Y	16	235	Unsigned Binary
C _B C _R	-112	+112	2's Complement
			Offset Binary

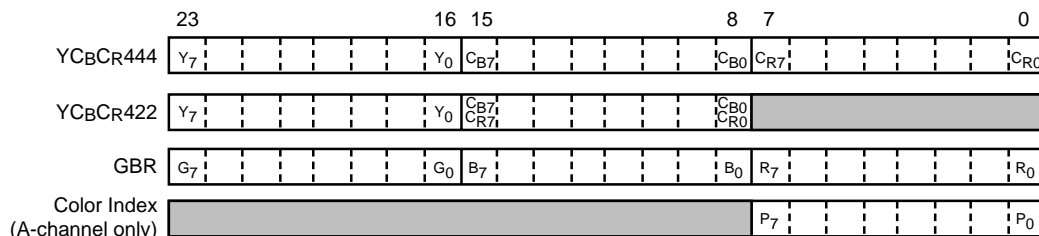


Figure 1. Pixel Data Formats

A-Channel Operation

A-channel pixel data, PDA, is registered on the rising edge of CLK. C_{BCR} data is either passed or format converted (from offset binary to 2’s complement) by MSB inversion. 16-bit YC_{BCR}422 data is converted to 24-bit YC_{BCR} data by pixel replication of C_{BCR} data. Each of the three A channel bytes is logically-ANDed with the contents of the Mask Register.

The CLUT in the A-channel pixel data path comprises three 256-word x 8-bit sections. When the CLUT is enabled, pixel data addresses the CLUT, which outputs the address contents for subsequent processing. The CLUT may also be bypassed, passing incoming pixel data directly to subsequent circuits.

For 24-bit GBR operation, each of the 256-word by 8-bit CLUTs is independently addressed by green, blue, and red bytes from PDA_{23:0}. For Color-index operation, each of the 256 x 8 CLUTs is addressed by the same pixel data from PDA_{7:0}.

CLUT locations may hold GBR or YC_{BCR} color values. V₁ and V₂ mixer input formats must match CLUT formats.

The PDA overlay palette is addressed by four Overlay inputs, OL_{3:0} and is enabled via the Control Register. Each valid Overlay address produces one of 15 24-bit colors selected from stored 8-bit red, green, and blue values. If all four overlay inputs are LOW, CLUT data is selected. If any overlay input is HIGH, OL_{3:0} is decoded into the corresponding color which is selected at the RGB/YC_{BCR} matrix. OL_{3:0} may be changed on a pixel-by-pixel basis.

Table 6. A-Channel GBR-to-YC_{BCR} Mapping for Fully-Saturated Colors

Color	Input Values			Output Values		
	R	G	B	Y	C _B	C _R
White	255	255	255	235	0	0
Yellow	255	255	0	210	-112	18
Cyan	0	255	255	169	38	-112
Green	0	255	0	144	-74	-94
Magenta	255	0	255	106	74	94
Red	255	0	0	81	-38	112
Blue	0	0	255	41	112	-18
Black	0	0	0	16	0	0

Table 7. B-Channel YC_{BCR}-GBR Mapping for Fully-Saturated Colors

Color	Input Values			Output Values		
	Y	C _B	C _R	R	G	B
White	235	0	0	255	255	255
Yellow	210	-112	18	255	255	0
Cyan	169	38	-112	0	255	255
Green	144	-74	-94	0	255	0
Magenta	106	74	94	255	0	255
Red	81	-38	112	255	0	0
Blue	41	112	-18	0	0	255
Black	16	0	0	0	0	0

B-Channel Operation

YC_{BCR}444, YC_{BCR}422, or GBR are accepted by the B-channel. PDB_{23:0} pixel data is registered on the rising edge of CLK. 16-bit YC_{BCR}422 data is converted to 24-bit YC_{BCR}444 data by pixel replication of C_{BCR} data in the Register/Formatter.

24-bit data is passed to an interpolation filter followed by a color-space converter to ensure that the B-channel data format matches that of the A-channel prior to mixing. Table 1 illustrates the setup of color-space converters, decimation, and interpolation filters. Pipeline latencies of the A and B-channels are matched.

Interpolation and Decimation Filters

Digital interpolation and decimation filters in the A- and B-channels suppress unwanted artifacts in the chrominance components. Maximum passband attenuation is 0.06 dB. Minimum stopband rejection is 41 dB.

When the input format is YC_{BCR}422, the incoming pixel following AV transitioning HIGH is assumed to be the C_B pixel. (See Figure 11.)

α-Channel Operation

Nine bits of α data are registered on a pixel-by-pixel basis from α_{8:0}. Either 9-bit or 8-bit α values can be selected by setting Control Register Bit αGAIN. Table 8 shows the differences between the 8-bit and 9-bit gain settings for a 0FF input.

Bits α_{7:0} address a 256 x 8-bit lookup table (αLUT). The αLUT may be used to redefine the function of incoming α data for special effects or low resolution dissolves and fades.

Bit α₈ controls a unity gain switch. If α₈ = 1, then α is set to unity gain. α₈ functions independently of the α gain bit register 0. For 8-bit α mixing, set α₈ = 0.

By setting control register bit αLUTEN = 0, the αLUT may be completely bypassed, allowing α_{8:0} to directly control the mixing of A, B and F. αLUT locations may be accessed via the D_{7:0} microprocessor port.

Table 8. Alpha Channel Gains

α value (hex)	8-bit Gain	9-bit Gain
000	0/256	0/256
001	1/256	1/256
..		
07F	127/256	127/256
080	128/256	128/256
..		
0FE	254/256	254/256
0FF	256/256	255/256
100	256/256	256/256
1XX	256/256	256/256

Fill Color Registers

Three registers, 03, 04, and 05, store a solid fill color, F. Either GBR values or YCBCR values may be stored but the format must match the data format of the A- and B-channels at the input to the crosspoint switch.

Fill color registers are accessed through the D7-0 microprocessor port. Fill color may be used as an alternative video source for fades.

α -Mixer

There are three sources of data for the mixer: A-channel pixels, B-channel pixels, and the stored fill color, F. One pair of inputs, either AB, BF or FA are selected by the Crosspoint Switch to be passed to the V₁ and V₂ inputs of the α -Mixer. Prior to mixing, V₁ and V₂ data formats must be matched (see Table 1).

Within the α -Mixer are three dual input 9-bit mixers which mix each of the component channels of V₁ and V₂. By varying the value on the α -channel from 000_h to 100_h, the Mixer performs a 256-step transition from one digital video source to the other.

Six dissolve transitions are supported: A-to-B, A-to-F, B-to-A, B-to-F, F-to-A, and F-to-B. Type of dissolve is selected by directing the A-, B-, or F pixels to the V₁ or V₂ mixer input via the ABF Crosspoint Switch. This is done either by internal Control Registers via the microprocessor port or directly through the SMX₂₋₀ inputs. SMX₂₋₀ input pins are enabled via SMX Control Register bits. When enabled, SMX₂₋₀ directly control the ABF Crosspoint Multi-plexer on a pixel-by-pixel basis, for externally derived wipe patterns.

Rate of dissolve is controlled directly through the α -channel. Transfer function of the mixer is:

$$M = (\alpha) V_1 + (1-\alpha) V_2$$

where V₁ and V₂ are two of the three inputs A, B or F selected by the crosspoint switch.

For an A-to-B dissolve transition, as the value of the eight LSBs of the α -channel change from 00_h to FF_h, (or 000_h to 100_h in the 9-bit mode), an increasing level of A-channel contribution and a decreasing level of B-channel contribution becomes evident at the output, M.

Bit α_8 of the α -channel can correct for the 255/256 gain factor in the A-channel that occurs when the 8-bit α value is FF_h. When $\alpha_8=1$, bits α_{7-0} are ignored, A-channel gain is set to 256/256 and B-channel gain is set to 0/256.

Modified transfer functions may be selected for background/foreground and drop-shadow effects by programming control register bits, MIXTFN.

A Foreground Key may be created such that:

$$M = (\alpha) V_1$$

A Background Key may be created such that:

$$M = (\alpha) V_1 + V_2$$

By using foreground and background mixers in series, drop shadow effects can be implemented.

α may change at pixel rates up to 40 Mpps on a pixel-by-pixel basis, allowing smooth transitions from one video source to another. Transition time interval may vary from many frames to only a few or a single pixel depending upon the α -channel data rate.

α_8 may be used like a key input. Either unity gain V₁ or (1- α)V₂ may be selected. A- and B-channel pixels may be mixed by switching α_8 on a pixel-by-pixel basis. Pipeline latencies of the α -, A- and B-channels are matched.

Passing of Non-Pixel Data

In the PASSON mode, the TMC2081 is transparent to data accepted during the PASSESN = LOW period (see Figure 10 and Figure 11). Either PDA or PDB data may be selected to pass on reference signals containing time codes, subcarrier phase and frequency data from upstream video processors.

Digital Outputs

Data at the M₂₃₋₀ output port, may be selected from either the mixer or, for digital preview, the A or B crosspoint switch inputs.

The 444-to-422 formatter may be bypassed for 24-bit output. To convert 24-bit YCBCR data to the 16-bit YCBCR422 format, the formatter needs to be enabled.

Except for color index, all data formats shown in Figure 1 are available:

- YCBCR444
- YCBCR422
- GBR

M₂₃₋₀ bits are clocked synchronously with the rising edge of CLK. M₂₃₋₀ data outputs may be disabled to a high-impedance state by setting the MOUT Control Register bit LOW.

Analog Preview

Either crosspoint switch input (A or B) or the mixed pixel data output (M₂₃₋₀) can be monitored by D/A converters. D/A outputs may be either YC_{BCR} or GBR. A YC_{BCR}-to-GBR matrix prior to the D/A converters can be selected for color-space conversion.

To view A or B data originating in the C_{BCR} format, the DACFRM Control Register bit must be set to convert 2's-complement data to the offset binary format.

With the DACSLP bit, D/A converters can be powered down and with the DACOVL bit, the D/A overlay RAM can be powered down.

D/A Converter Outputs

Each D/A converter comprises an array of current sources referenced to V_{DD} and controlled by the data, $\overline{\text{BLANK}}$, and $\overline{\text{SYNC}}$ inputs. When $\overline{\text{BLANK}} = \text{HIGH}$, the SETUP Control Register bit determines if a pedestal is activated. With nominal R_{REF} and V_{REF}, outputs match SMPTE 170M levels when terminated with a 37.5Ω resistive load (75Ω at the source and destination). By doubling R_{REF}, a 75Ω load can be accommodated.

Full scale current is set by an external resistor, R_{SET}, connected between the R_{REF} pin and AGND and the reference voltage, V_{REF}. V_{REF} may be derived from either a 1.235 volt internal source or an external voltage reference connected to V_{REF}.

Nominal outputs (see Figure 2 and Figure 3) are expressed in Current Units (IU) where 1 IU is equivalent to the current activated by one unit of D/A input data (Gdata/Ydata, Bdata/C_Rdata, or Rdata/C_Bdata). SETUP = HIGH activates a 21 IU pedestal when $\overline{\text{BLANK}} = \text{H}$. $\overline{\text{SYNC}} = \text{LOW}$ disables a 110 IU sync pulse. SETUP is programmed through Register 7 bit 2.

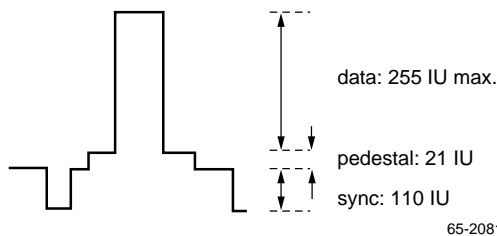
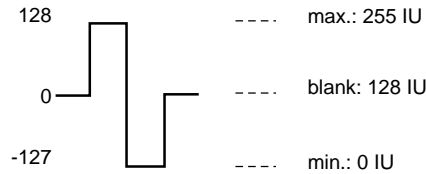


Figure 2. GBR/Y DAC Output Levels in Current Units



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Figure 3. C_{BCR} DAC Output Levels in Current Units

To translate IUs to millivolts, V_{REF} and R_{SET} must be set to the correct values, nominally V_{REF} = 1.235 volt and R_{SET} = 681 ohms. In each table below, G and the Y outputs have been normalized to 1000 mV with Data = 255.

Since V_{REF} and R_{REF} are common to all D/A converters, B and R full scale outputs track G. C_B C_R full scale outputs track Y. R_{REF} may be trimmed to set the G or Y full scale voltage to 1000 mV.

In the equations for the GBR and YC_{BCR} outputs that follow, symbols are defined as:

- + = plus
- * = multiply
- & = logical AND
- ! = logical complement

GBR Output

Expressed in IUs, the GBR transformation from data to current is as follows:

$$G = (\text{Gdata} + \text{SETUP} * 21) \& \overline{\text{BLANK}} + \overline{\text{SYNC}} * 110$$

$$B = (\text{Bdata} + \text{SETUP} * 21) \& \overline{\text{BLANK}}$$

$$R = (\text{Rdata} + \text{SETUP} * 21) \& \overline{\text{BLANK}}$$

Sample outputs are listed in Table 9 and Table 10.

Table 9. GBR DAC Transfer Characteristic without Pedestal (SETUP = L)

D/A Input Data	$\overline{\text{SYNC}}$	$\overline{\text{BLANK}}$	G		B or R	
			IU	mV	IU	mV
255	1	1	365	1000	255	699
128	1	1	238	652	128	351
0	1	1	110	301	0	0
X	1	0	110	301	0	0
X	0	0	0	0	0	0
128	0	1	128	351	128	351

Table 10. GBR DAC Transfer Characteristic with Pedestal (SETUP = H)

D/A Input Data	SYN \bar{C}	BLANK \bar{K}	G		B or R	
			IU	mV	IU	mV
255	1	1	386	1000	276	715
128	1	1	259	671	149	386
0	1	1	131	339	21	54
X	1	0	110	285	0	0
X	0	0	0	0	0	0
128	0	1	149	386	149	386

Y_{CB}C_R Output

Data inputs are unsigned Ydata and offset-binary format C_Bdata and C_Rdata. BLANK = L sets C_B and C_R outputs to 128, the value for zero chrominance data. Y_{CB}C_R transfer equations are:

$$Y = (Ydata + SETUP * 21) \& \overline{BLANK} + \overline{SYN} * 110$$

$$C_B = (Cdata + SETUP * 21) \& \overline{BLANK} + 128 \& !\overline{BLANK}$$

$$C_R = (Cdata + SETUP * 21) \& \overline{BLANK} + 128 \& !\overline{BLANK}$$

Sample outputs are listed in Table 11 and Table 12.

Table 11. YCrCb DAC Transfer Characteristic without Pedestal (SETUP = L)

D/A Input Data	SYN \bar{C}	BLANK \bar{K}	Y		C _B or C _R	
			IU	mV	IU	mV
255	1	1	365	1000	255	699
128	1	1	238	652	128	351
64	1	1	174	477	64	175
0	1	1	110	301	0	0
X	1	0	110	301	128	351
X	0	0	0	0	128	351
64	0	1	64	175	64	175

Table 12. YCrCb DAC Transfer Characteristic with Pedestal (SETUP = H)

D/A Data	SYN \bar{C}	BLANK \bar{K}	Y		C _B or C _R	
			IU	mV	IU	mV
255	1	1	386	1000	276	715
128	1	1	259	670	149	386
64	1	1	195	505	85	220
0	1	1	131	339	21	54
X	1	0	110	285	149	386
X	0	0	0	0	149	386
64	0	1	85	220	85	220

Dissolve and Crossfade Operation

Video transitions such as dissolve and fades may be executed by direct α -channel control. Rate and start time for the transition depends entirely upon the value of the α_{8-0} inputs. Transitions may be executed as quickly or slowly as values are presented to the α -channel. Transitions may remain partially executed by keeping α -values constant.

It is possible to mix modes, bringing data in either 444 or 422 format and outputting data in 422 or 444 format.

In the 444/444 mode (see Figure 7), α is applied to each Y_{CB}C_R or GBR pixel pair at the input of the mixer. The Y_{CB}C_R444 output is mixed at the full α rate.

In the 422/422 mode (see Figure 8), α mixes the Y component of incoming PDA and PDB pixels. Only odd indexed α values mix C_BC_R components. α -values applied to C_BC_R change synchronously with C_B data. Consequently, full bandwidth α data is applied to the luminance channel but the chrominance channel α values are decimated by dropping the even values that are synchronous with C_R data.

In the 422/444 mode (see Figure 9), Y_{CB}C_R422 data is accepted at the PDA and PDB port but the output at the M₂₃₋₀ port is Y_{CB}C_R444. α may change from pixel-to-pixel with mixing at the M₂₃₋₀ outputs tracking both Y and C_BC_R. Although odd values of C_B and C_R are repeated at half the pixel rate, α transitions are applied to C_B and C_R at the pixel rate.

Microprocessor Interface

Internal Control Registers, CLUT, α LUT, and the overlay palette are accessed through a bi-directional microprocessor port, D₇₋₀. Table 13 shows how address bits, A₂₋₀, select the registers to be accessed.

Table 13. Microprocessor Port Address Map

A ₂₋₀	Action
000	RAM Address Register for CLUT, α LUT, and overlay palette for write operations
001	Directs RAM R/W operations selected by the two MSBs of Control Address Register
010	Reserved
011	RAM Address Register for CLUT, α LUT, and overlay palette for read operations
100	Reserved
101	Directs Control Register R/W operations selected by the four LSBs of the Control Address Register
110	Mask Register (Default: Load with FF)
111	Control Address Register

As shown in Table 14, to access a control register, Control Address Register bits D₃₋₀ must be set to specify one of the nine control registers shown in Table 17. For access to LUTs and Overlay palettes, Control Address Register bits D₇₋₆ must be set to select the address of one of the four RAMs shown in Table 14.

Table 14. Control Address Register Bit Definitions

RAM Select		Reserved		Control Register Address			
D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
00		A-channel CLUT					
01		A-channel Overlay palette					
10		Reserved					
11		αLUT					

Figure 4 and Figure 5 show the microprocessor port read and write timing cycles. Table 15 shows the Control Register read and write sequences.

When loading or reading look-up tables or the overlay palette, with the exception of α-LUT write, the address pointer is auto-incremented after each read or write operation. For α-LUT write, the address pointer is pre-incremented, so that the address must be set one address before the required address. For α-LUT read, the address pointer is post-incremented.

When accessing the A-channel CLUT, or A-channel Overlay palette, each address location must be written/read three consecutive times for red (R/C_R), green (G/Y), and blue (B/C_B) data. After accessing the blue data, the address pointer auto-increments.

In Table 16, note that:

1. To read the α-LUT, Control Register 06h, bit 5 must be set to enable the α-LUT.
2. To read the CLUT and Overlay Table, Control Register 00h, bit 4 (CLUT) must be set to enable both the CLUT and Overlay Table.
3. Data may be written to the CLUT or αLUT with Control Register bits set to enable or bypass.
4. When writing to the α-LUT, the address pre-increments. The address pointer is set to FFh, one address before address 00h.
5. Load mask register to pass PDA data.

Power and Ground

The TMC2081 operates from a single +5 Volt power supply. Multiple power and ground pins are assigned and must be connected.

Table 15. Control Register Read/Write Sequences

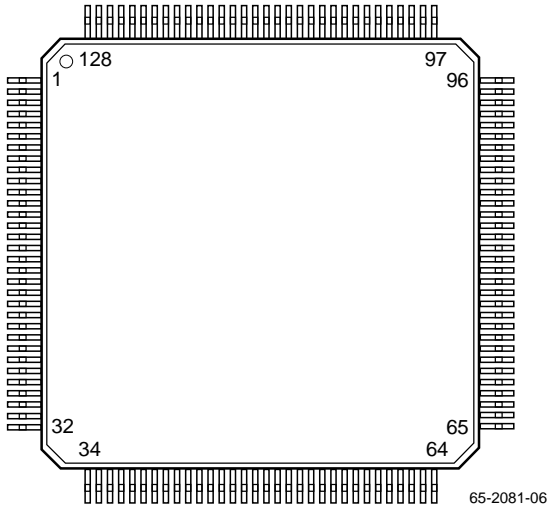
Step	R/W	A ₂₋₀	D ₇₋₀	Function
Write to all Control Registers				
1	0	111	x0	Writes 0 to Address Control Register (selects the A-channel Control Register)
2	0	101	aa	Writes aa into A-channel Control Register
.	Repeat steps 1 and 2 incrementing data to Address Control Register
15	0	111	07	Writes 07 to Address Control Register (selects the D/A Control Register)
16	0	101	bb	Writes bb into D/A Control Register
Read/Modify/Write Mixer Control Register				
1	0	111	x2	Writes 02 to Address Control Register (selects the Mixer Control Register)
2	1	101	aa	Mixer Control Register contents, aa, available on D ₇₋₀ .
.	System modifies aa to get bb.
3	0	101	bb	Writes bb into Mixer Control Register

Table 16. CLUT Read/Write Sequences

Step	R/ \bar{W}	A ₂₋₀	D ₇₋₀	Function
Write Entire A-Channel CLUT from Address 00				
1	0	111	0x	Selects A-CLUT for write.
2	0	000	00	Presets RAM Address Register to 00.
3	0	001	r0	r0 written into red (R/C _R) CLUT address 00.
4	0	001	g0	g0 written into green (G/Y) CLUT address 00.
5	0	001	b0	b0 written into blue (B/C _B) CLUT address 00.
.	repeat steps 3,4,5 until A-CLUT is full.
768	0	001	r255	r255 written into red (R/C _R) CLUT address FF.
769	0	001	g255	g255 written into green (G/Y) CLUT address FF.
770	0	001	b255	b255 written into blue (B/C _B) CLUT address FF.
Write GBR Data to A-Overlay Location Address				
1	0	111	4x	Select A-channel Overlay.
2	0	000	a _n	Write a _n into RAM Address Register.
3	0	001	r _n	r _n written into red (R/C _R) CLUT address.
4	0	001	g _n	g _n written into green (G/Y) CLUT address.
5	0	001	b _n	b _n written into blue (B/C _B) CLUT address.
Write all αLUT Locations starting from 00				
1	0	111	Cx	Select α LUT.
2	0	000	FF	Write FF into RAM Address Register (sets address to FF for pre-increment).
3	0	001	$\alpha\alpha$	Write $\alpha\alpha$ to α LUT location 00.
.	Repeat step 3, 254 times for locations 01h-FEh.
258	0	001	$\zeta\zeta$	Write $\zeta\zeta$, to α LUT location FF.
Read All αLUT Locations Starting from 00				
1	0	111	C6	Select α LUT and Register 06 in Address Control Register.
2	1	101	aa	Read Control Register 06. bb = (aa OR 20h) to set bit 5.
3	0	101	bb	Restores aa with α LUT enabled.
4	0	011	00	Write 00 into RAM Address Register (sets address to 00).
5	1	001	cc	Read contents of α LUT, cc, from location 00.
.	Repeat step 5, 254 times for locations 01h-FEh.
260	1	001	$\zeta\zeta$	Read contents of α LUT, $\zeta\zeta$, from last location FF.

Pin Assignments

128 Pin Plastic Quad Flat Pack (PQFP) Package



Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	D5	33	PDA11	65	R/CR	97	M22
2	D4	34	PDA10	66	B/CB	98	M21
3	D3	35	PDA9	67	AGND	99	M20
4	D2	36	PDA8	68	G/Y	100	M19
5	D1	37	PDA7	69	COMP	101	M18
6	D0	38	PDA6	70	VDDA	102	M17
7	CS	39	PDA5	71	VDDA	103	M16
8	R/W	40	PDA4	72	PDB23	104	DGND
9	A0	41	PDA3	73	PDB22	105	VDD
10	A1	42	PDA2	74	PDB21	106	M15
11	A2	43	PDA1	75	PDB20	107	M14
12	SIG0	44	PDA0	76	PDB19	108	M13
13	PASSEN	45	α 8	77	PDB18	109	M12
14	AV	46	α 7	78	PDB17	110	M11
15	OL3	47	VDD	79	PDB16	111	M10
16	VDD	48	DGND	80	PDB15	112	M9
17	DGND	49	α 6	81	PDB14	113	M8
18	OL2	50	α 5	82	PDB13	114	M7
19	OL1	51	α 4	83	PDB12	115	M6
20	OL0	52	α 3	84	PDB11	116	M5
21	PDA23	53	α 2	85	PDB10	117	M4
22	PDA22	54	α 1	86	PDB9	118	M3
23	PDA21	55	α 0	87	PDB8	119	M2
24	PDA20	56	SMX2	88	PDB7	120	M1
25	PDA19	57	SMX1	89	PDB6	121	M0
26	PDA18	58	SMX0	90	PDB5	122	AVOUT
27	PDA17	59	CLK	91	PDB4	123	PASS14
28	PDA16	60	BLANK	92	PDB3	124	SIG14
29	PDA15	61	SYNC	93	PDB2	125	DGND
30	PDA14	62	VREF	94	PDB1	126	VDD
31	PDA13	63	RREF	95	PDB0	127	D7
32	PDA12	64	AGND	96	M23	128	D6

Pin Descriptions

Name	Pin Number	Value	Pin Function Description																											
Clock																														
CLK	59	TTL	Clock Input. TTL-compatible clock. All pixel data is registered on the rising edge of CLK. CLK synchronizes the flow of pixel data through the TMC2081 and the operation of the α -input.																											
Pixel I/O																														
PDA ₂₃₋₀	21-44	TTL	A-Channel Pixel Inputs. A-channel pixel inputs are registered on the rising edge of CLK and specify which of the CLUT locations are addressed after masking. The CLUT in the A-Channel may be bypassed. PDA ₇₋₀ are applied to all three CLUT sections when color-index pixel data is used.																											
PDB ₂₃₋₀	72-95	TTL	B-Channel Pixel Inputs. B-channel pixel inputs are registered on the rising edge of CLK and are applied to the mixer after color-space conversion, and interpolation, if selected.																											
α ₈₋₀	45,46,49-55	TTL	α-Channel Inputs. The α -channel inputs are registered on the rising edge of CLK and control proportional mixing at pixel rates up to 40 Mpps. α_8 acts as a key input, switching A- and B-channel pixel data on a pixel-by-pixel basis. α_0 is the LSB.																											
SMX ₂₋₀	56-58	TTL	<p>ABF Crosspoint Mux Control. When enabled by setting the SMX Control Register bits to 111, these inputs control the ABF Crosspoint Switch which directs the A- or B-channel pixels or the fill color register values to the V₁ or V₂ inputs to the mixer. SMX₂₋₀ input pins are ignored when the SMX Control Register bits are not 111. SMX₂₋₀ are registered on the rising edge of CLK. ABF Crosspoint Switch control is according to the following:</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>SMX₂₋₀</th> <th>V₁</th> <th>V₂</th> </tr> </thead> <tbody> <tr> <td>000</td> <td>A</td> <td>B</td> </tr> <tr> <td>001</td> <td>A</td> <td>F</td> </tr> <tr> <td>010</td> <td>B</td> <td>A</td> </tr> <tr> <td>011</td> <td>B</td> <td>F</td> </tr> <tr> <td>100</td> <td>F</td> <td>A</td> </tr> <tr> <td>101</td> <td>F</td> <td>B</td> </tr> <tr> <td>110</td> <td>-</td> <td>-</td> </tr> <tr> <td>111</td> <td>-</td> <td>-</td> </tr> </tbody> </table>	SMX ₂₋₀	V ₁	V ₂	000	A	B	001	A	F	010	B	A	011	B	F	100	F	A	101	F	B	110	-	-	111	-	-
SMX ₂₋₀	V ₁	V ₂																												
000	A	B																												
001	A	F																												
010	B	A																												
011	B	F																												
100	F	A																												
101	F	B																												
110	-	-																												
111	-	-																												
OL ₃₋₀	15,18-20	TTL	Overlay Inputs. Overlay inputs select one of 15 overlay colors from the PDA overlay palette. OL ₃₋₀ are registered on the rising edge of CLK. When PDA or overlay is enabled and OL ₃₋₀ > 0, the contents of the addressed palette are selected in place of the pixel data. Overlay is inactive when OL ₃₋₀ = 0 _n or when disabled via the Control Registers. OL ₀ is the LSB.																											
M ₂₃₋₀	96-103, 106-121	TTL	Mixed Pixel Outputs. Mixer output or digital preview of the V ₁ and V ₂ Crosspoint Switch outputs are synchronized to the rising edge of CLK. M ₂₃₋₀ data is passed on for further processing (mixing, encoding, etc.). Pipeline latency is 14 clock cycles.																											

Pin Descriptions (continued)

Name	Pin Number	Value	Pin Function Description
Video Controls			
PASSEN	13	TTL	Pass Enable Input. Data selected by A/BPASS is enabled by PASSEN.
SIG0	12	TTL	Signal 0 Input. Input to a 14 CLK delay. Output is at SIG14.
PASS14	123	TTL	Pass Enable Output (14 Clock Delay). PASSEN delayed by 14 CLK cycles to match the pipeline latency of pixels
SIG14	124	TTL	Signal 0 Output (14 Clock Delay). SIG0 delayed to match the 14 CLK cycles pipeline latency of pixels
AV	14	TTL	Active Video Input. When HIGH, AV enables data from the PDA and PDB ports. When LOW, at the M ₂₃₋₀ output, GBR data is set to zero and YC _B C _R data is set to 10 _h 80 _h 80 _h in the offset binary format and 10 _h 00 _h 00 _h in 2's complement format. In the 422 mode, AV transitioning HIGH defines the next pixel to be the first C _B pixel.
AVOUT	122	TTL	Delayed AV Output. AV delayed by either 12 or 14 clock cycles. A 14 clock cycle delay matches the pipeline delay of the A and B channels. A 12 clock cycle delay is useful for interfacing with Fairchild Encoders.
SYNC	61	TTL	Sync Enable for G/Y D/A. D/A Converter sync enable. SYNC = LOW, disables a current source at the G/Y output, forcing the sync tip to zero volts. SYNC = HIGH, activates the sync current at the G/Y output. SYNC is delayed either 2 or 15 clock cycles according to the status of the DACDLY bit. To disable sync on G/Y, ground SYNC.
BLANK	60	TTL	Blanking Control for D/As. D/A Converter blanking input. BLANK = LOW disables the data and pedestal output currents. If BLANK = HIGH, data and pedestal currents are added to the SYNC current. BLANK is delayed either 2 or 15 clock cycles according to the status of the DACDLY bit. For blank levels, see Tables 9, 10, 11, and 12.
Microprocessor I/O			
R/W	8	TTL	Read/Write Control. Read-Write control input. R/W controls the direction of the D ₇₋₀ port. If R/W = HIGH and CS is LOW, registers or CLUTs may be read. If R/W = LOW and CS = LOW, data may be written to control registers or CLUTs via the D ₇₋₀ port. R/W is latched on the falling edge of CS.
CS	7	TTL	Chip Select. Chip Select Input. If CS = HIGH, port, D ₇₋₀ , is set to high-impedance. If CS = LOW, port D ₇₋₀ is enabled. Read data (R/W = HIGH) is enabled on the falling edge of CS. Write data is latched into the TMC2081 on the rising edge of the CS. CLUT, αLUT, or overlay read/write operations require CS to be HIGH for at least 4 CLK cycles after CS = LOW.
A ₂₋₀	11-9	TTL	Register Select Controls. Address bits input. A ₂₋₀ select registers or tables to be accessed (see Table 13) via D ₇₋₀ . A ₂₋₀ are latched on the falling edge of CS.
D ₇₋₀	127,128, 1-6	TTL	Data I/O Port. Bi-directional data port. D ₀ is the LSB. Control Registers, CLUT, αLUT and Overlay locations are accessed via D ₇₋₀ .
Video Output			
G/Y	68	1 V P-P	Green/Luminance Video. The green/luminance analog video output. Sync pulses are included on this output.
B/C _B	66	0.7 V P-P	Blue/C_B Video. Blue/C _B analog video output.
R/C _R	65	0.7 V P-P	Red/C_R Video. Red/C _R analog video output.

Pin Descriptions (continued)

Name	Pin Number	Value	Pin Function Description
Reference			
V _{REF}	62	+1.23 V	Voltage Reference Input/Output. An internal voltage source of +1.2 Volts (nominal) is applied to the V _{REF} terminal. This is the reference for all three D/A converters of the TMC2081. Decoupling V _{REF} to AGND with a 0.1 μF ceramic capacitor is recommended. This pin may also be used as an input for an external voltage reference source.
R _{REF}	63	681 Ω	Current-Setting Resistor. Full-scale output current of the TMC2081 is determined by the value of the resistor connected between R _{REF} and AGND. Varying this resistor will vary the “white” output level for all three D/A converters. The TMC2081 is not designed for operation with an external current reference.
COMP	69	0.1 μF	Compensation Capacitor. A 0.1 μF ceramic capacitor is connected between the COMP and V _{DDA} at pin 70 or 71.
Power, Ground			
V _{DDA}	70,71	+5 V	Analog Power Supply. The TMC2081 operates from a single +5V supply. All power pins must be connected. V _{DDA} and V _{DD} must be derived from a common power supply.
V _{DD}	16,47,105,126	+5 V	Digital Power Supply. The TMC2081 operates from a single +5V supply. All power pins must be connected. V _{DDA} and V _{DD} must be derived from a common power supply.
AGND	64,67	0.0 V	Analog Ground. All ground pins must be connected.
DGND	17,48,104,125	0.0 V	Digital Ground. All ground pins must be connected.

Control Register Map

Reg	Bit	Name	Function
A-Channel Control Register			
00	7	AOVLEN	A-channel Overlay enable/disable
00	6	ADEC	Decimator bypass/enable
00	5	AMAT	A-channel GBR-to-YC _B C _R bypass/enable
00	4	CLUT	Bypass/enable CLUT (power down)
00	3	AMSB	Inverts C _B /C _R MSB
00	2	αGAIN	Alpha Channel 9-/8-bit gain
00	1-0	AFORMAT	A Pixel data path setup (4 formats)
B-Channel/Mixer Control Register			
01	7		Reserved
01	6-5	MSOURCE	M ₂₃₋₀ pixel source
01	4	BMAT	Bypass/enable the B-channel YC _B C _R -to-GBR
01	3	BINT	Bypass/enable Interpolator
01	2	BMSB	Inverts C _B /C _R MSB
01	1-0	BFORMAT	B Pixel data path setup (4 formats)
Mixer Control Register			
02	7	MIXFMT	Mixer format select
02	6-5	DSOURCE	Selects data source for the internal D/A converters
02	4-2	SMX	Chooses video source to be directed to the mixer inputs, V ₁ and V ₂
02	1-0	MIXTFN	Used to alter the mixer transfer function
Fill Color Registers			
03	7-0	REDVAL	Value for Red/C _R
04	7-0	GRNVAL	Value for Green/Y
05	7-0	BLEVAL	Value for Blue/C _B

Reg	Bit	Name	Function
Output Control Register			
06	7	AVPIPE	Sets pipeline latency of AV
06	6		Reserved
06	5	αLUTEN	αLUTEN power down enable
06	4	PASSON	Sets pixel activity subject to mixer transfer function
06	3	A/BPASS	Selects A or B data in PASSON mode
06	2	MOUT	Bits M ₂₃₋₀ enable
06	1	MMSB	Inverts C _B , C _R MSBs
06	0	MFORMAT	Sets output data format
D/A Control Register			
07	7-6		Reserved
07	5	DACDLY	Selects SYNC and BLANK pipe delay
07	4	DACFMT	C _B /C _R translate from 2's complement to offset binary
07	3	AWAKE	D/A converters enable/disable
07	2	SETUP	Sets IRE blanking levels
07	1		Reserved
07	0	DMAT	D/A converter input data YC _B C _R /GBR conversion
Identification (read-only)			
08	7-0	REVID	Chip revision ID
09	7-0	CHIPID	Chip type ID = 2F

Control Register Definitions

A-Channel Control Register (00)

7	6	5	4	3	2	1	0
AOVLEN	ADEC	AMAT	CLUT	AMSB	α GAIN	AFORMAT	

Reg	Bit	Name	Description
00	7	AOVLEN	When HIGH, the Overlay palette in the PDA pixel path is enabled and controlled by the OL ₃₋₀ inputs. When LOW, the PDA Overlay palette is disabled.
00	6	ADEC	When HIGH, this bit causes A-channel pixel data to be decimated from Y _C B _C R ₄₄₄ to Y _C B _C R ₄₂₂ format. When LOW, no decimation takes place and the data is passed through.
00	5	AMAT	When HIGH, the A-channel pixel data is converted from GBR to Y _C B _C R format. When LOW, no conversion takes place and the data is passed through.
00	4	CLUT	When HIGH, the A-channel CLUT is enabled and addressed by pixel data. When LOW the CLUT is bypassed.
00	3	AMSB	When LOW, the MSBs of the A-channel C _B and C _R (PDA ₁₅ and PDA ₇) are passed through. When HIGH, the MSBs of the C _B and C _R are inverted.
00	2	α GAIN	α -channel gain. LOW selects 9-bit unity gain. HIGH selects 8-bit gain. For 8-bit α mixing, set $\alpha_8 = 0$.
00	1-0	AFORMAT	These two bits set up the A channel data path to accommodate four different formats: 0 0 Y _C B _C R ₄₄₄ 0 1 Y _C B _C R ₄₂₂ 1 0 8-bit color index 1 1 24-bit GBR

Control Register Definitions (continued)**B-Channel Control Register (01)**

7	6	5	4	3	2	1	0
Reserved	MSOURCE		BMAT	BINT	BMSB	BFORMAT	

Reg	Bit	Name	Description
01	7		Reserved.
01	6-5	MSOURCE	Source of pixels to be connected to port M ₂₃₋₀ . 0 0 Mixer Pixels 0 1 A pixels 1 0 B pixels 1 1 Reserved
01	4	BMAT	When HIGH, the B-channel pixel data is converted from Y _C B _C R to GBR format. When LOW, no conversion takes place and the data is passed through.
01	3	BINT	When HIGH, B-channel pixel data is interpolated from the Y _C B _C R ₄₂₂ to the Y _C B _C R ₄₄₄ format. When LOW, no interpolation takes place and the data is passed through.
01	2	BMSB	When LOW, the MSBs of the B-channel C _B and C _R bytes (PDB ₁₅ and PDB ₇) are passed through. When HIGH, the MSBs of the C _B and C _R bytes are inverted.
01	1-0	BFORMAT	B-channel pixel data format select bits. 0 0 Y _C B _C R ₄₄₄ 0 1 Y _C B _C R ₄₂₂ 1 0 Reserved 1 1 24-bit GBR

Control Register Definitions (continued)

Mixer Control Register (02)

7	6	5	4	3	2	1	0
MIXFMT	DSOURCE		SMX			MIXFTN	

Reg	Bit	Name	Description
02	7	MIXFMT	When LOW, the mixer is set for YC _B C _R format. When HIGH, the mixer expects GBR format.
02	6-5	DSOURCE	The data source for the internal D/A converters is selected by two control bits. 0 0 A-pixels 0 1 B-pixels 1 0 Mixed pixels 1 1 Reserved
02	4-2	SMX	These three control bits determine which video sources (A-pixels, B-pixels, fill color registers) are directed to the two mixer inputs, V ₁ and V ₂ , through the ABF Crosspoint Mux: 0 0 0 A to V ₁ , B to V ₂ 0 0 1 A to V ₁ , F to V ₂ 0 1 0 B to V ₁ , A to V ₂ 0 1 1 B to V ₁ , F to V ₂ 1 0 0 F to V ₁ , A to V ₂ 1 0 1 F to V ₁ , B to V ₂ 1 1 0 Reserved 1 1 1 Enables SMX ₂₋₀ inputs for external source select
02	1-0	MIXTFN	These two bits are used to alter the mixer transfer function: 0 0 (V ₁ - V ₂)α + V ₂ 0 1 (V ₁) α + V ₂ 1 0 (V ₁) α 1 1 Reserved

Fill Color Registers (03–05)

Reg	Bit	Name	Description
03	7-0	REDVAL	Value for Red/C _R
04	7-0	GRNVAL	Value for Green/Y
05	7-0	BLUVAL	Value for Blue/C _B

Control Register Definitions (continued)

Output Control Register (06)

7	6	5	4	3	2	1	0
AVPIPE	Reserved	α LUTEN	PASSON	A/BPASS	MOUT	MMSB	MFORMAT

Reg	Bit	Name	Description
06	7	AVPIPE	When LOW the pipeline latency from AV, to AVOUT is 14 CLK cycles. When HIGH, the pipeline latency is 12 CLK cycles.
06	6		Reserved.
06	5	α LUTEN	When LOW (write only), the α LUTEN is powered down. Data from α_{8-0} bypasses the α LUT to control the mixer directly. When HIGH, α_{7-0} addresses the α LUT which controls the mixer.
06	4	PASSON	When HIGH, either PDA or PDB data may be selected to pass through the mixer without modification. When LOW the mixer transfer function is enabled if the $\overline{\text{PASSEN}}$ input is HIGH. The PASSON feature allows Genlock or Decoder reference signals to be passed downstream for subsequent processing.
06	3	A/BPASS	Selects A or B data in PASSON mode. LOW allows all pixels from PDA_{23-0} during $\overline{\text{PASSEN}} = \text{LOW}$ to pass to M_{23-0} . HIGH allows all pixels from PDB_{23-0} during $\overline{\text{PASSEN}} = \text{LOW}$ to pass to M_{23-0} .
06	2	MOUT	Digital outputs M_{23-0} are enabled when this bit is HIGH. These outputs are in a high-impedance state when MOUT is LOW.
06	1	MMSB	When LOW, the MSBs of the C_B and C_R M_{23-0} output positions (M_{15} and M_7) are not inverted. When HIGH, the MSBs of the C_B and C_R output positions are inverted.
06	0	MFORMAT	When LOW, 24-bit GBR or $\text{Y}_{\text{C}_B\text{C}_R444}$ output data formats are enabled. When HIGH, the multiplexer in the M_{23-0} path is enabled producing 16-bit $\text{Y}_{\text{C}_B\text{C}_R422}$.

D/A Control Register (07)

7	6	5	4	3	2	1	0
Reserved		DACDLY	DACFMT	AWAKE	SETUP	DOVLEN	DMAT

Reg	Bit	Name	Description
07	7-6		Reserved.
07	5	DACDLY	Selects $\overline{\text{SYNC}}$ and $\overline{\text{BLANK}}$ pipe delay. LOW = 15 clocks, HIGH = 2 clocks.
07	4	DACFMT	Translates C_B/C_R format from 2's complement to C_B/C_R offset binary. LOW passes C_B/C_R unchanged. HIGH inverts C_B/C_R MSB.
07	3	AWAKE	D/A converters are enabled when HIGH. The D/A converters are powered-down when AWAKE is LOW.
07	2	SETUP	When LOW, 0 IRE blanking levels are present on the D/A converter outputs. When HIGH, blanking levels are 7.5 IRE units.
07	1		Reserved.
07	0	DMAT	When HIGH, D/A converter input data is converted from $\text{Y}_{\text{C}_B\text{C}_R}$ to GBR format. When LOW, no conversion takes place and the data is passed through.

Control Register Definitions (continued)

Identification Registers (08-09)

Reg	Bit	Name	Description
08	7-0	REVID	Chip revision identification.
09	7-0	PARTID	Chip type identification = 2F.

Absolute Maximum Ratings

(beyond which the device may be damaged)¹

Parameter	Min.	Max.	Unit
Power Supply Voltage	-0.5	+7.0	V
Input Voltage	-0.5	(V _{DD} + 0.5)	V
Digital Inputs			
Applied voltage ²	-0.5	(V _{DD} + 0.5)	V
Externally forced current ^{3, 4}	-20.0	20.0	mA
Digital Outputs			
Applied voltage ²	-0.5	(V _{DD} + 0.5)	V
Externally forced current ^{3, 4}	-20.0	20.0	mA
Short Circuit Duration (Single output in HIGH state to GND)		1 second	
Analog Output Short Circuit Duration (Single output to GND)		infinite	
Temperature			
Operating, case	-60	+130	°C
Operating, Junction, Plastic package		+150	°C
Lead, soldering (10 seconds)		300	°C
Vapor phase soldering (1 minute)		+220	°C
Storage	-65	150	°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied. Performance and reliability are guaranteed only if Operating Conditions are not exceeded.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.

Operating Conditions

Parameter		Min.	Nom	Max.	Units
V _{DD}	Power Supply Voltage	4.75	5.0	5.25	V
V _{IH}	Input Voltage, Logic HIGH	2.0		V _{DD}	V
	TTL Inputs, all but CLK, \overline{CE} CLK, \overline{CE}	2.4		V _{DD}	V
V _{IL}	Input Voltage, Logic LOW TTL Inputs	GND		0.8	V
I _{OH}	Output Current, Logic HIGH			-2.0	mA
I _{OL}	Output Current, Logic LOW			4.0	mA
V _{REF}	External Reference Voltage		1.235		V
I _{REF}	D/A Converter Reference Current (I _{REF} = V _{REF} / R _{REF} , sourced from R _{REF} pin)		1.8		mA
R _{REF}	Reference Resistor @ V _{REF} = Nom.		681		Ω
R _{OUT}	Total Output Load Resistance		37.5		Ω
T _A	Ambient Temperature, Still Air	0		70	°C

Electrical Characteristics

Parameter		Conditions	Min.	Typ.	Max.	Units
I _{DD}	Power Supply Current ¹	f _{CLK} = 25MHz, DAC, CLUT and αLUT enabled		300	360	mA
I _{DDQ}	Power Supply Current ¹	f _{CLK} = 0 DAC, CLUT and αLUT enabled		260	330	mA
I _{DAC}	DAC Supply Current	f _{CLK} = 25MHz		80	100	mA
I _{CLUT}	CLUT Supply Current			85	100	mA
I _{αLUT}	αLUT Supply Current			30	45	mA
I _{DDSE}	Power Supply Current	Sleep Mode (D/A, CLUT, αLUT, and D/A overlay disabled)		5	15	mA
V _{RO}	Voltage Reference Output		0.98	1.2	1.48	V
I _{BR}	Input Bias Current, V _{REF}	V _{REF} = Nom	-100		40	μA
I _{IH}	Input Current, Logic HIGH	V _{DD} = Max, V _{IN} = 4.0V	-5		5	μA
I _{IL}	Input Current, Logic LOW	V _{DD} = Max, V _{IN} = 0.4V	-5		5	μA
V _{OH}	Output Voltage, Logic HIGH	I _{OH} = Max	2.4			V
V _{OL}	Output Voltage, Logic LOW	I _{OL} = Max			0.4	V
I _{OZH}	High-Z Leakage Current, HIGH	V _{DD} = Max, V _{IN} = V _{DD}	-5		5	μA
I _{OZL}	High-Z Leakage Current, LOW	V _{DD} = Max, V _{IN} = GND	-5		5	μA
C _I	Digital Input Capacitance	T _A = 25°C, f = 1MHz		15		pF
C _O	Digital Output Capacitance	T _A = 25°C, f = 1MHz		15		pF
V _{OC}	Video Output Compliance Voltage		-0.4		2.0	V
R _{OUT}	Video Output Resistance			15		KΩ
C _{OUT}	Video Output Capacitance	I _{OUT} = 0mA, f = 1MHz		15	25	pF

Note:

1. Typical I_{DD} measured at V_{DD} = +5.0 Volts and T_A = 25°C, Maximum I_{DD} measured at V_{DD} = + 5.25 Volts and T_A = 0°C.

Switching Characteristics

Parameter		Min.	Nom.	Max.	Units
Microprocessor Interface					
t _{PWLCS}	$\overline{\text{CS}}$ Pulse Width, LOW	95			ns
t _{PWHCS}	$\overline{\text{CS}}$ Pulse Width, HIGH		4/f _{PXL}		ns
t _{SA}	Address Setup Time	0			ns
t _{HA}	Address Hold Time	4			ns
t _{SD}	Data Setup Time (write)	6			ns
t _{HD}	Data Hold Time (write)	3			ns
t _{DOZ}	Output Delay, $\overline{\text{CS}}$ to low-Z	16			ns
t _{DOM}	Output Delay, $\overline{\text{CS}}$ to Data Valid			110	ns
t _{HOM}	Output Hold Time, $\overline{\text{CS}}$ to High-Z	7			ns
Pixel Interface					
f _{PXL}	Pixel Rate			40	Mpps
t _{CYPX}	Pixel Cycle Period	25			ns
t _{PWH}	CLK Pulse Width, HIGH	6			ns
t _{PWL}	CLK Pulse Width, LOW	6			ns
	For PDA, PDB, α , SMX, OL, $\overline{\text{PASSEN}}$, SIG0, AV inputs:				
t _{SP}	Setup Time	6			ns
t _{HP}	Hold Time	2			ns
t _{HO}	Output Hold Time, CLK to data disabled	6			ns
t _{DO}	Output Delay, CLK to data valid			17	ns
Analog Outputs					
PIPES	Pipeline Delay		15		CLKs
t _R	D/A Output Current Risettime (10% - 90%)		6		ns
t _F	D/A Output Current Falltime (10% - 90%)		3		ns
t _{DOV}	Analog Output Delay		20		ns
SKEW	D/A to D/A Output Skew			1	ns

Notes:

1. Timing reference points are at the 50% level.
2. Analog and digital C_{LOAD} = 15pF.
3. TTL input levels are 0.0 and 3.0 Volts, 10% - 90% rise and fall times < ns.

System Performance Characteristics

Parameter	Conditions	Min.	Typ.	Max.	Units
V _{VID}	Video Amplitude with 37.5 Ω load		0.7		Volt
V _{SYNC}	Sync Amplitude with 37.5 Ω load		0.3		Volt
RES	D/A Converter Resolution		8		Bits
ELI	D/A Integral Linearity Error			0.75	LSB
ELD	D/A Differential Linearity Error			0.75	LSB
E _G	D/A Gain Error			± 11	% FS

Timing Diagrams

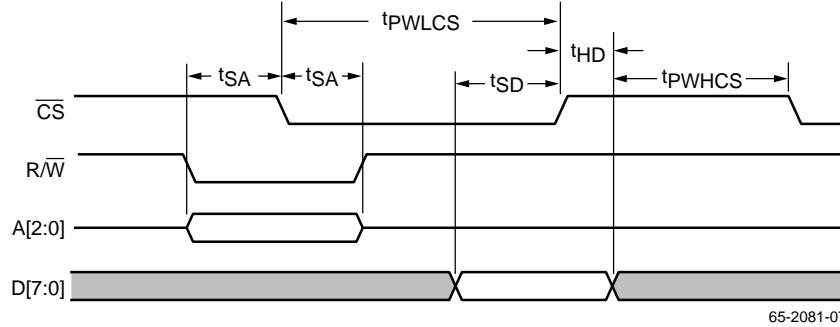


Figure 4. Microprocessor Port Write Timing

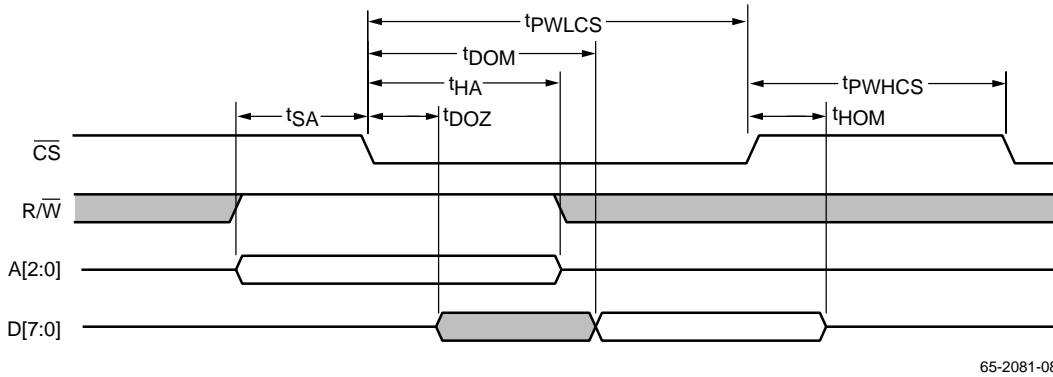


Figure 5. Microprocessor Port Read Timing

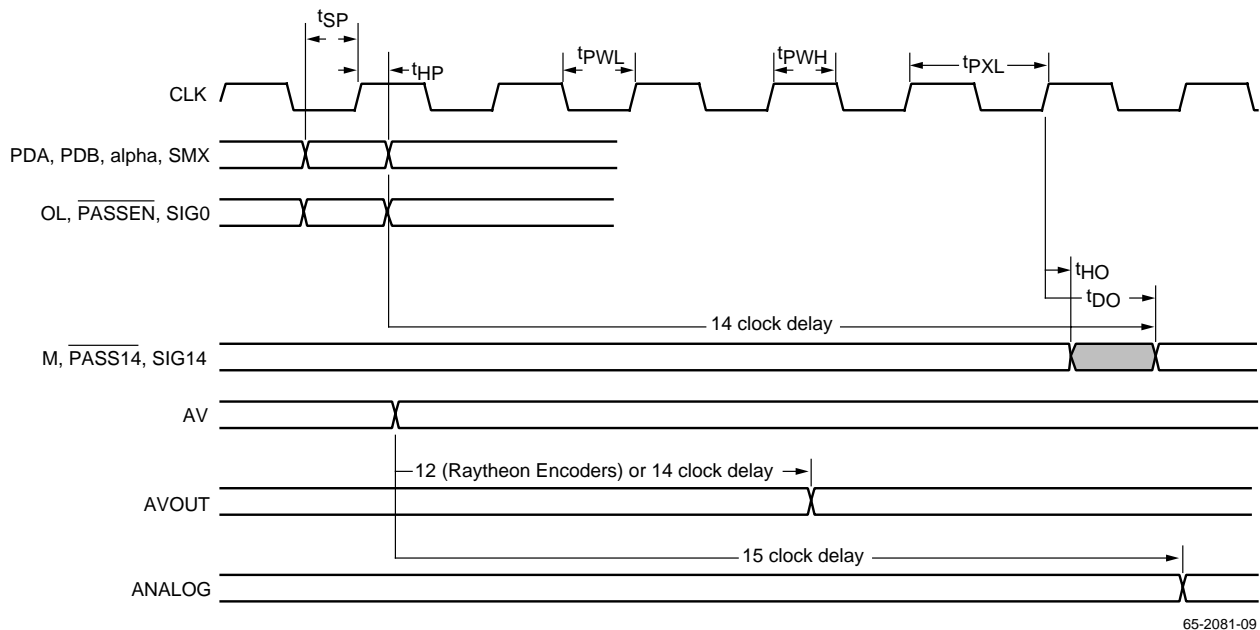
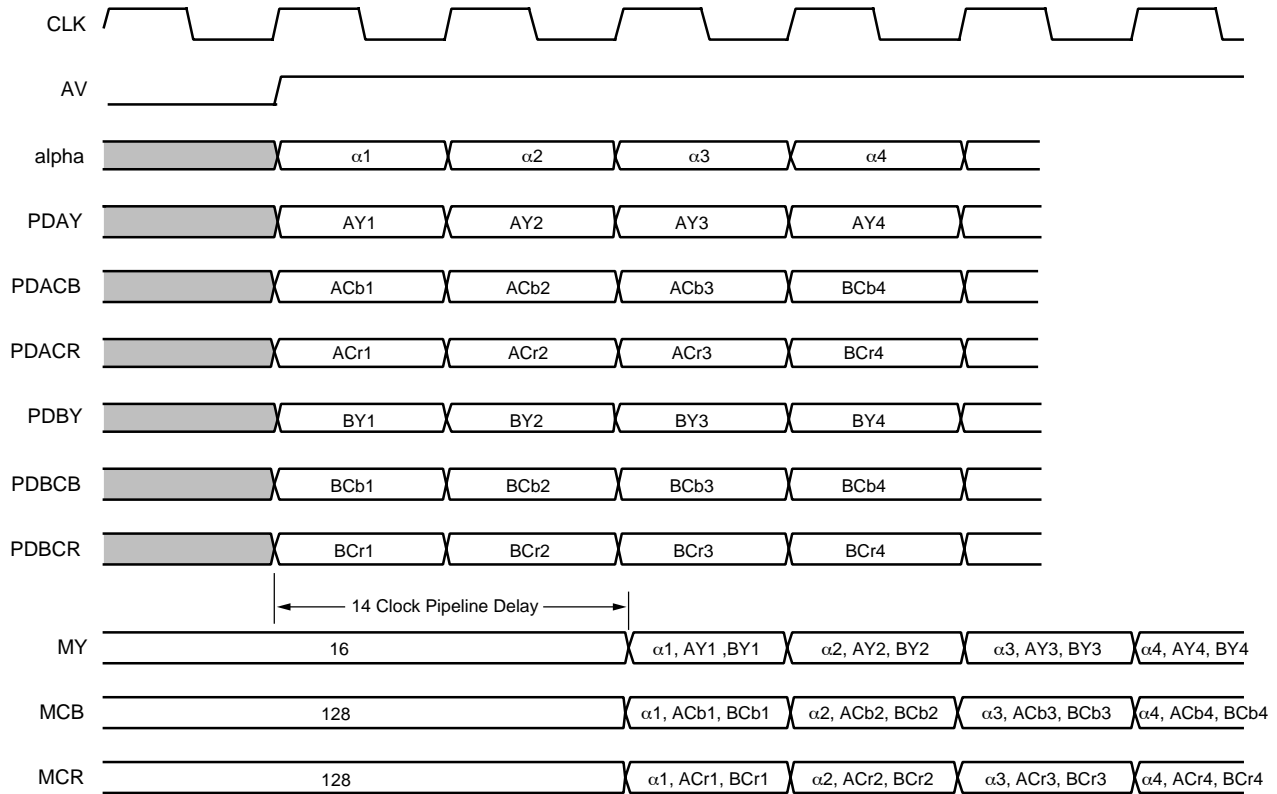


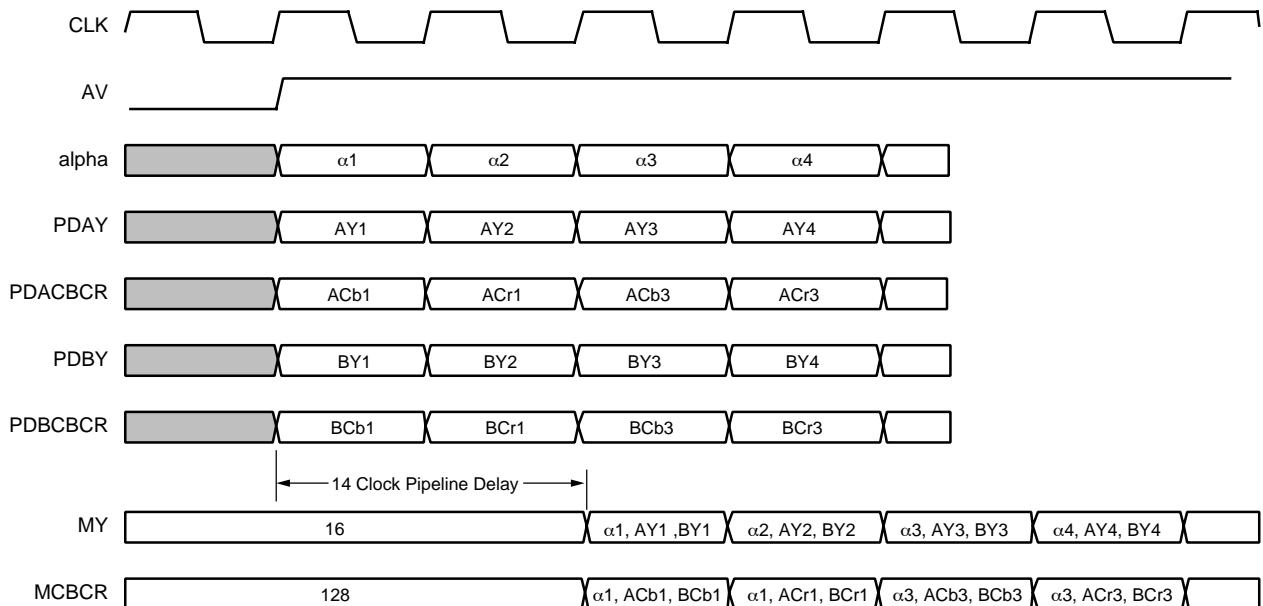
Figure 6. Pixel Timing

Timing Diagrams (continued)



65-3701-05

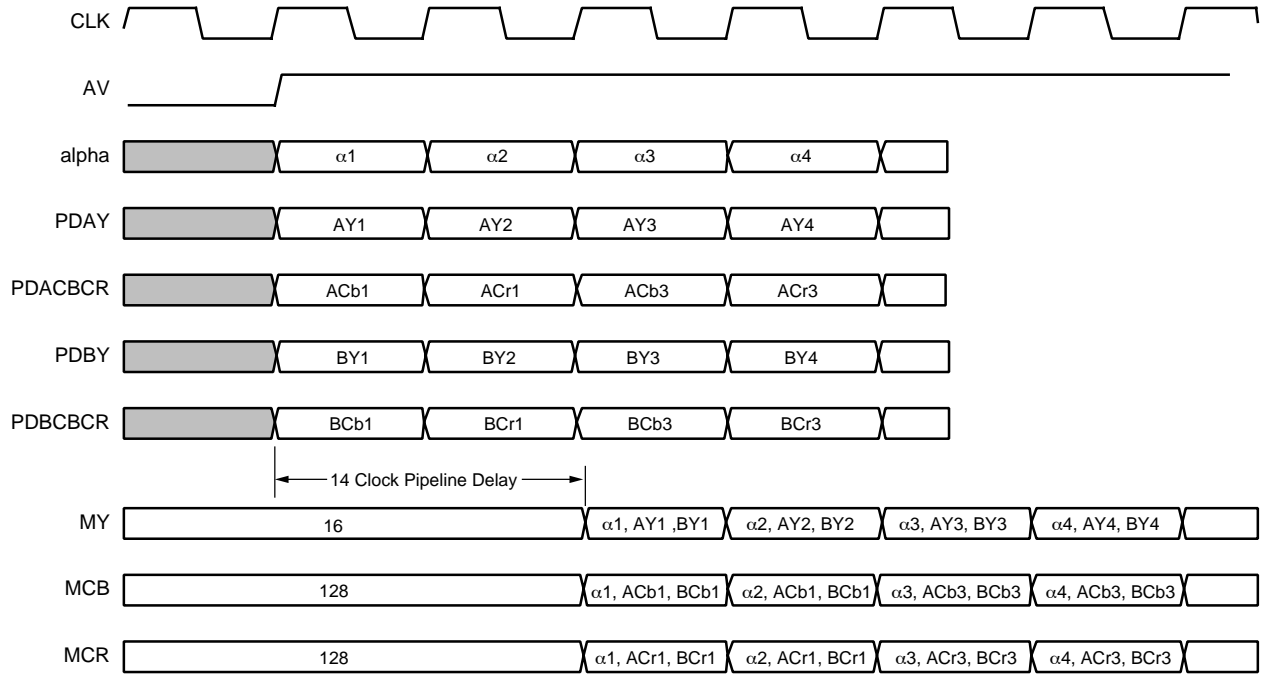
Figure 7. Pixel/Alpha Data Timing – 444/444 Mode



65-3701-06

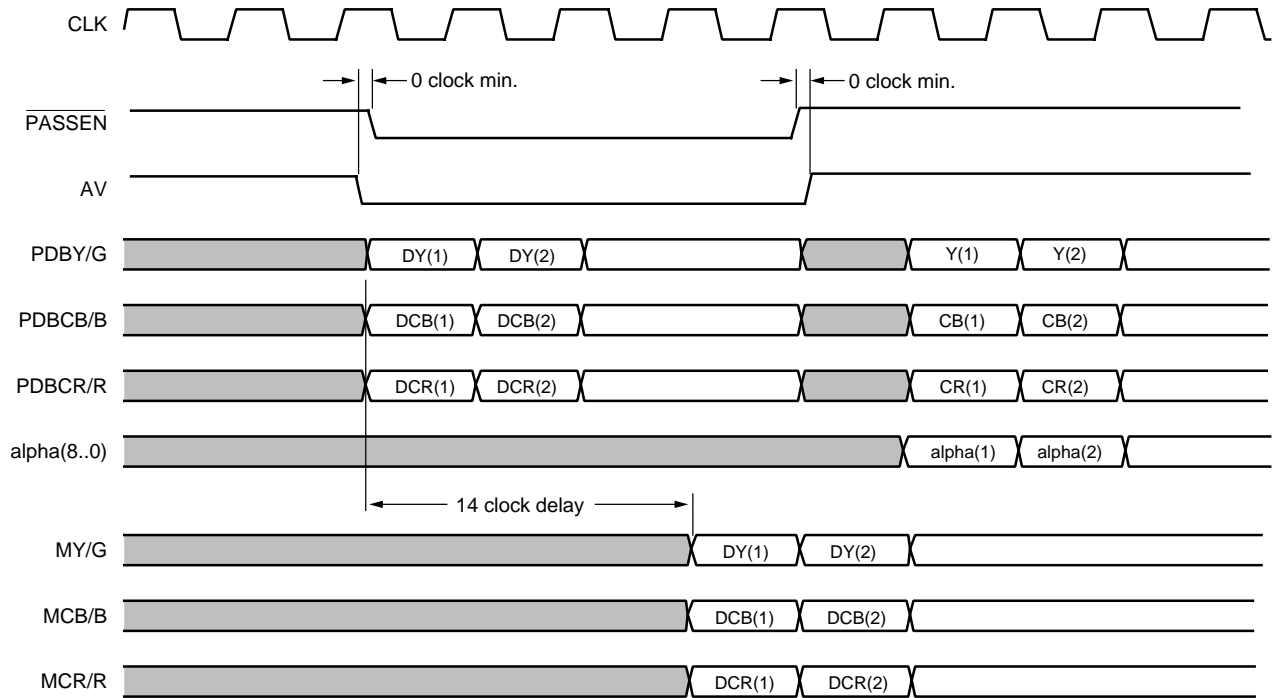
Figure 8. Pixel/Alpha Data Timing – 422/422 Mode

Timing Diagrams (continued)



65-3701-07

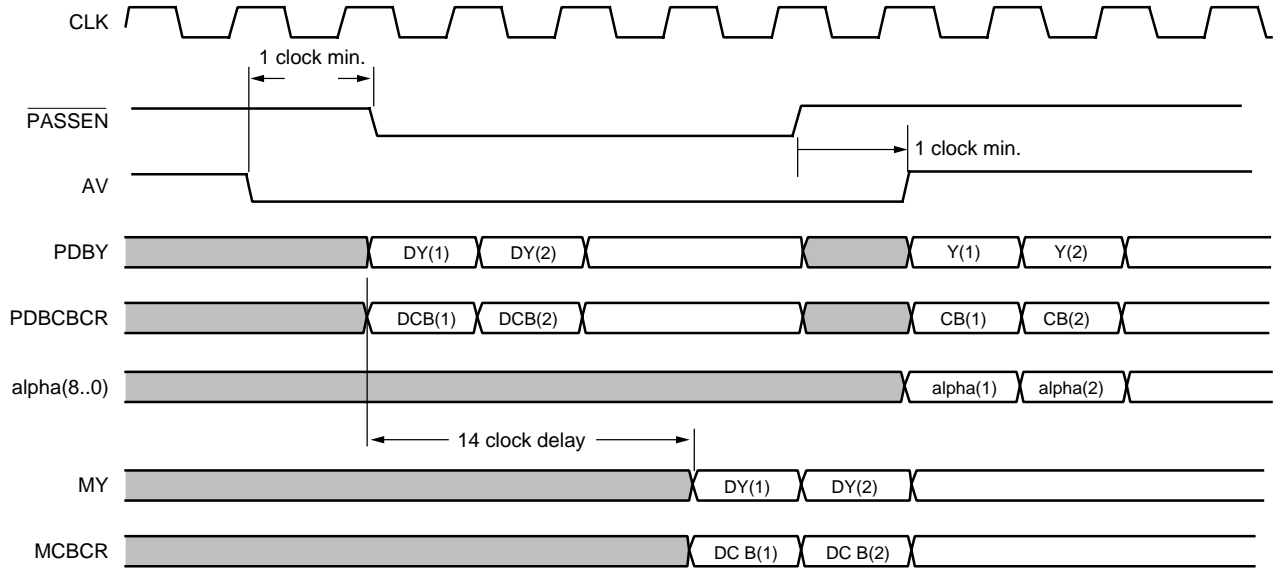
Figure 9. Pixel/Alpha Data Timing – 422/444 Mode



65-3701-08

Figure 10. PASSON Timing – 444 Mode
(Control bits: PASSON = HIGH, A/BPASS = HIGH)

Timing Diagrams (continued)



65-3701-09

Figure 11. PASSON Timing – 422 mode
 (Control bits: PASSON = HIGH, A/BPASS = HIGH)

Equivalent Circuits

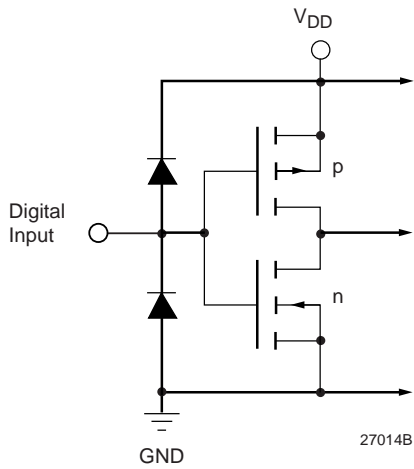


Figure 12. Equivalent Digital Input Circuit

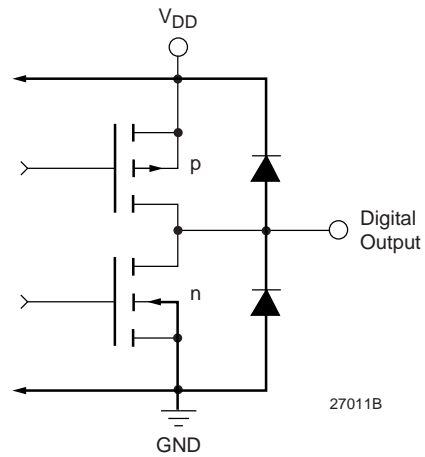


Figure 13. Equivalent Digital Output Circuit

Equivalent Circuits (continued)

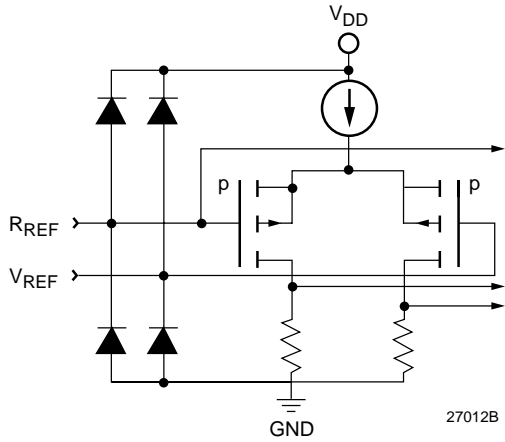


Figure 14. Equivalent Analog Input Circuit

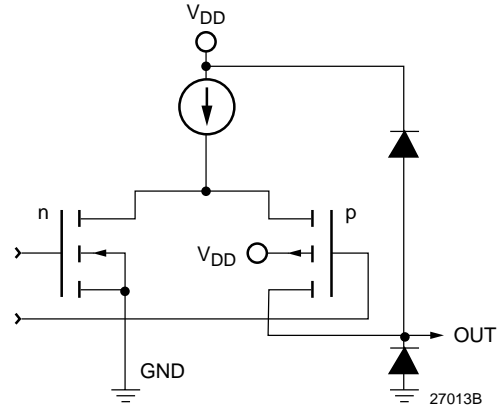


Figure 15. Equivalent Analog Output Circuit

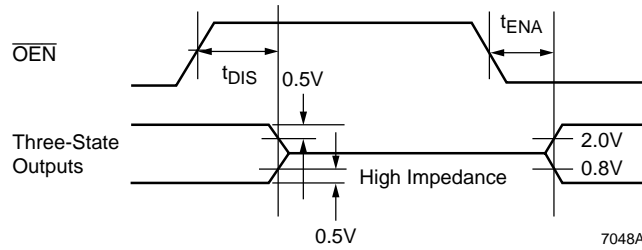


Figure 16. Threshold Levels for Three-State Measurement

Application Information

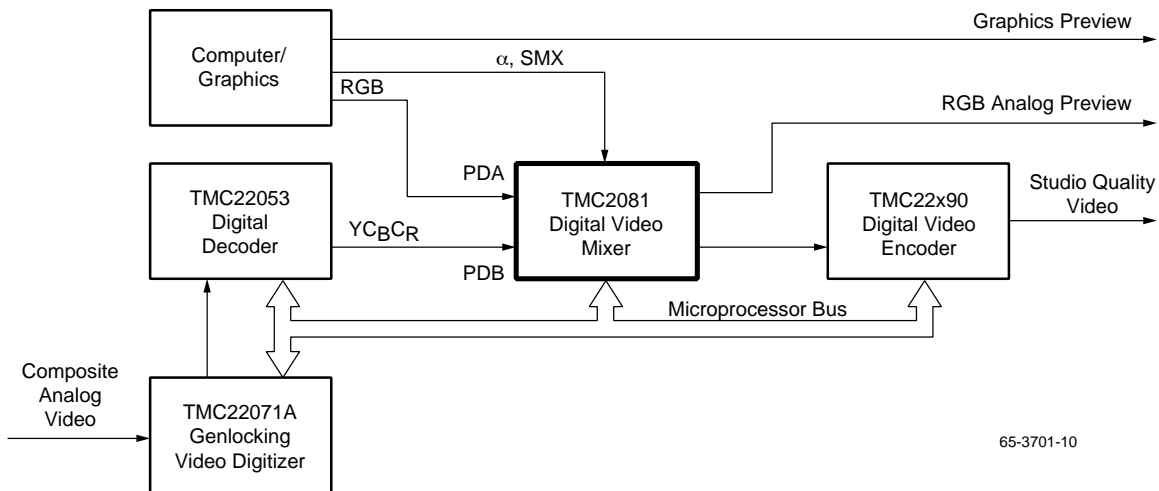


Figure 17. Mixing Video and Computer Graphics – Basic Multimedia System

Application Notes (continued)

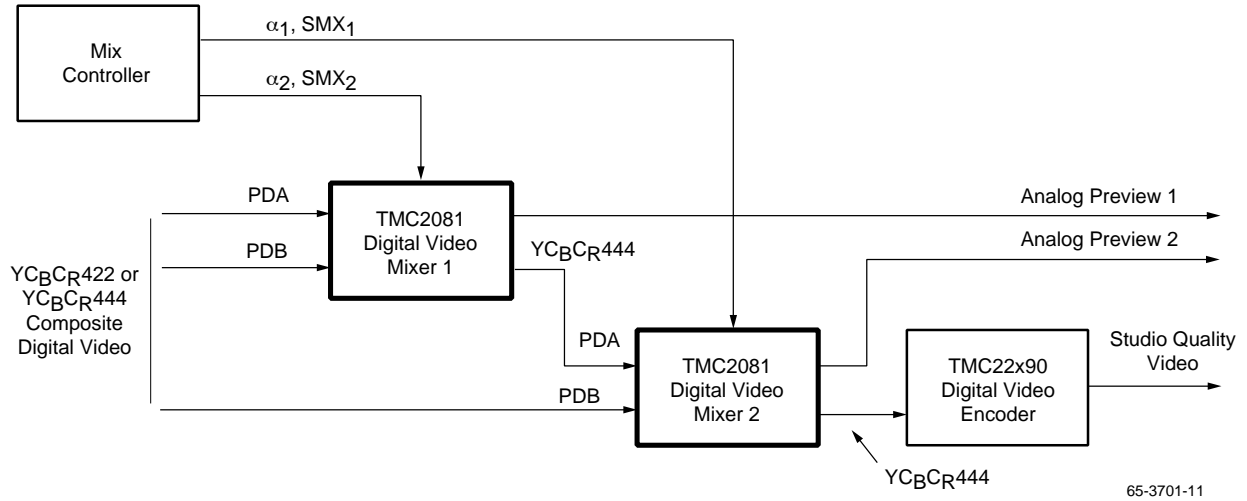


Figure 19. Multilevel Video Mixer with Special Effects

65-3701-11

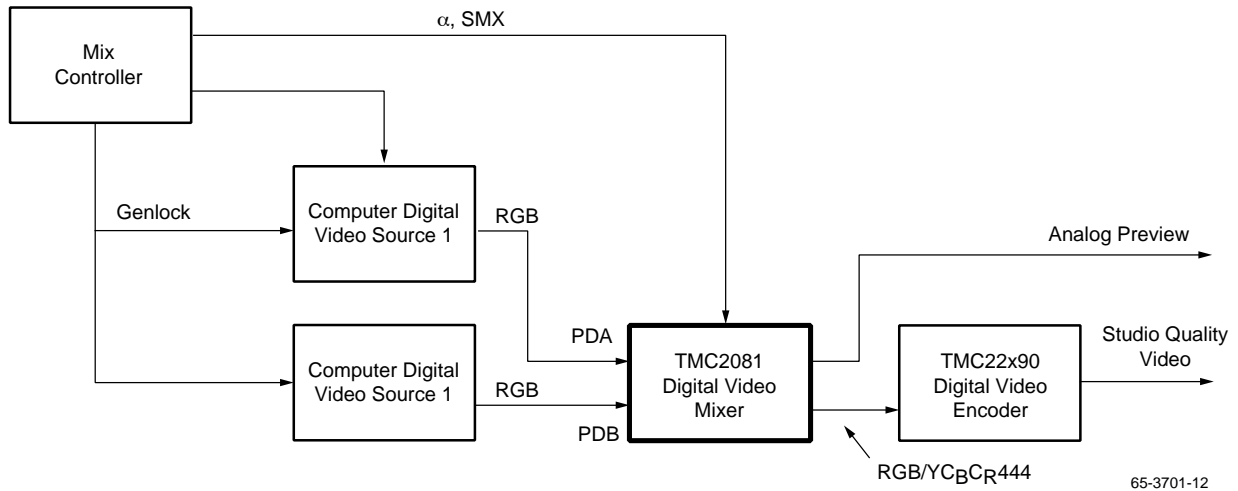
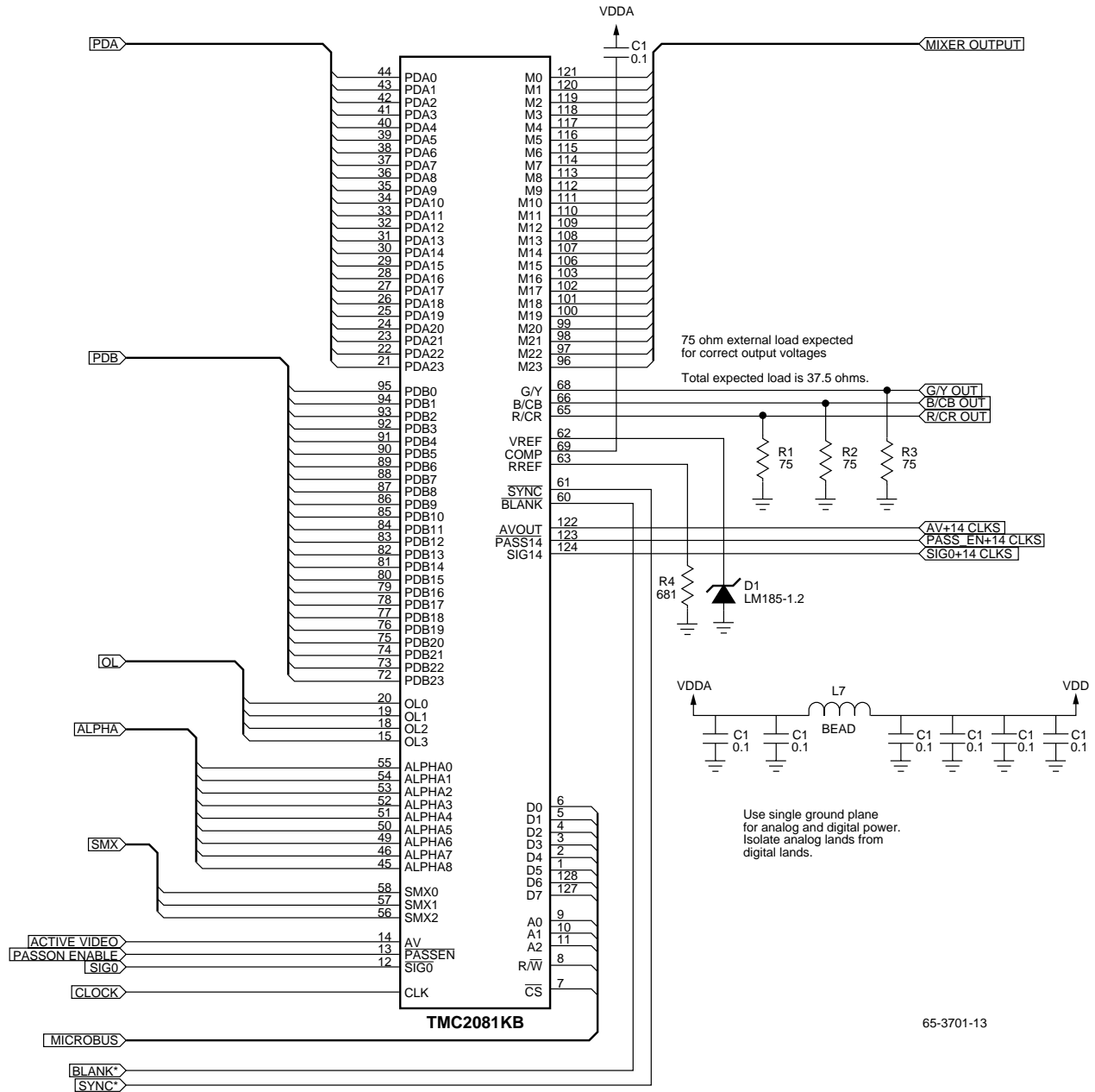


Figure 20. Mixing Two Computer Graphics Sources

65-3701-12

Application Notes (continued)



65-3701-13

Figure 21. Recommended TMC2081 Connections

Related Products

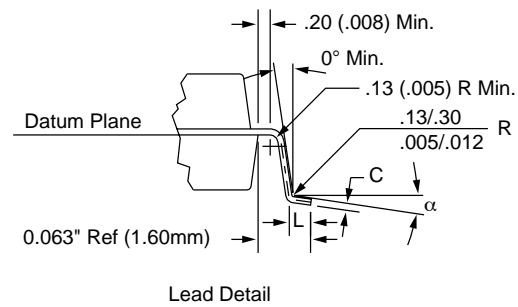
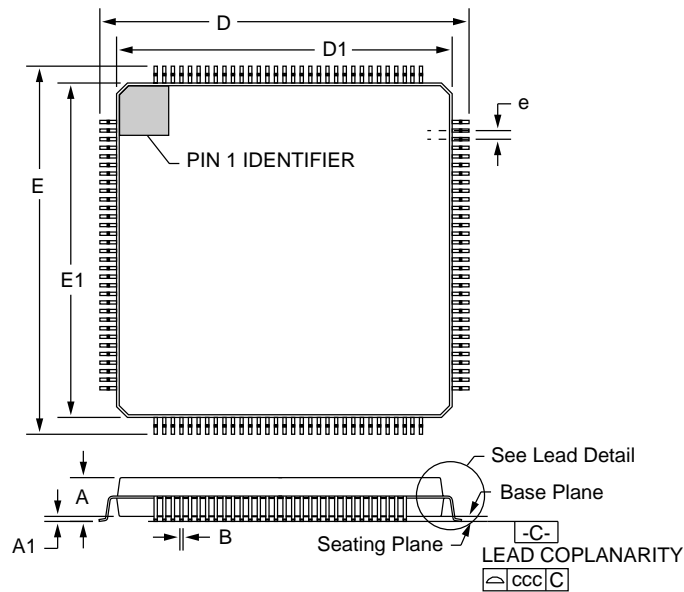
- TMC2072 Genlocking Video Digitizer
- TMC22190/191 Digital Video Encoder
- TMC2242A/TMC2246A Digital Filter
- TMC2272A Color Space Converter
- TMC22053 Decoder

Mechanical Dimensions – 128-Lead MQFP Package

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	—	.160	—	4.07	
A1	.010	—	.25	—	
B	.012	.018	.30	.45	3, 5
C	.005	.009	.13	.23	5
D/E	1.219	1.238	30.95	31.45	
D1/E1	1.098	1.106	27.90	28.10	
e	.0315 BSC		.80 BSC		
L	.029	.041	.73	1.03	4
N	128		128		
ND	32		32		
α	0°	7°	0°	7°	
ccc	—	.004	—	0.10	

Notes:

1. All dimensions and tolerances conform to ANSI Y14.5M-1982.
2. Controlling dimension is millimeters.
3. Dimension "B" does not include dambar protrusion. Allowable dambar protrusion shall be .08mm (.003in.) maximum in excess of the "B" dimension. Dambar cannot be located on the lower radius or the foot.
4. "L" is the length of terminal for soldering to a substrate.
5. "B" & "C" includes lead finish thickness.



Notes:

Notes:

Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TMC2081KBC	T _A = 0°C to 70°C	Commercial	128-Lead MQFP	2081KBC

LIFE SUPPORT POLICY

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.