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TMC2084

Standalone Mode CircLink™ Controller

Datasheet

PRODUCT FEATURES

- Low Power CMOS, 3.3 Volt Power Supply with 5 Volt Tolerant I/O
- Enhanced Token Passing Protocol from ARCNET
  - Maximum 15 node per network
  - Token Retry Mechanism
  - 64/128 Byte Per Packet
  - Consecutive Node ID Assignment
- Memory Mirror
  - Shared Memory Within Network
- Network Standard Time
  - Network Time Synchronization
  - Automatic Time Stamping
- Coded Mark Inversion
  - Intelligent 1-Bit Error Correction
  - Magnetic Saturation Prevention
- Standalone I/O Mode Operates without MCU
  - Supports 16 Bit Input and 16 Bit Output
- Up to 14 Intelligent Remote I/O Ports:
  - Programmable with 8-bit basis (16 to 32 outputs; 0 to 16 inputs)
  - Selectable output type (push-pull or open-drain)
  - The part of port is definable as strobe outputs and/or external trigger inputs
  - The anti-chatter circuit on the input port can be set in ON/OFF
  - The sampling frequency of the anti-chatter circuit can be set (19.1Hz/1.22KHz)
- Feature Rich Transmit Trigger:
  - After receiving OUTPUT DATA packet or expiring on-chip timer
  - Continuous transmission
  - External trigger input
- Flexible Transceiver Interface:
  - RS-485 transceiver + twist pair cable
  - RS-485 transceiver + pulse transformer + twist pair cable
  - Hybrid transceiver (HYC4000 or HYC2000 from SMSC Japan)
  - Fiber Optics also supported
- 48-Pin TQFP Package; Green, Lead-free Package also available
  - Body size: 7 × 7mm; pitch: 0.5mm; lead-free
- Temperature Range from 0 to 70 degrees C

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DATASHEET

ORDERING INFORMATION

Order Number(s):

TMC2084-HD for 48 pin TQFP package
TMC2084-HT for 48 pin TQFP package (green, lead-free)

80 Arkay Drive
Hauppauge, NY 11788
(631) 435-6000
FAX (631) 273-3123

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Chapter 1 General Description

1.1 About CircLink

The CircLink networking controller was developed for small control-oriented local network data communication based on ARCNET's token-passing protocol that guarantees message integrity and calculatable maximum delivery times.

In a CircLink network, when a node receives the token it becomes the temporary master of the network for a fixed, short period of time. No node can dominate the network since token control must be relinquished when transmission is complete. Once a transmission is completed the token is passed on to the next node (logical neighbor), allowing it to be come the master.

Because of this token passing scheme, maximum waiting time for network access can be calculated and the time performance of the network is predictable or deterministic. Industrial network applications require predictable performance to ensure that controlled events occur when required.

However, reconfiguration of a regular ARCNET network becomes necessary when the token is missed due to electronic and magnetic noise. In these cases, the maximum wait time for sending datagrams can not be guaranteed and the real-time characteristic is impaired. CircLink makes several modification to the original ARCNET protocol (such as maximum and consecutive node ID assignment) to avoid token missing as much as possible and reduce the network reconfiguration time.

CircLink implements other enhancements to the ARCNET protocol including a smaller-sized network , shorter packet size, and remote buffer mode operation that enable more efficient and reliable small, control-oriented LANs. In addition, CircLink introduces several unique features for reducing overall system cost while increasing system reliability.

CircLink can operate under a special mode called "Standalone" or "I/O" mode. In this mode, CircLink does not need an administrating CPU for each node. Only one CPU is needed to manage a CircLink network composed of several nodes, reducing cost and complexity.

In a CircLink network, the data sent by the source node is received by all other nodes in the network and stored according to node source ID. For the target node the received data is executed per ARCNET flow control and the data is stored in its buffer RAM. The receiving node processes the data while the remaining nodes on the network discard the data when the receiving node has completed. This memory-mirroring function assures higher reliability and significantly reduces network traffic.

Network Standard Time (NST) is also a unique CircLink feature. NST is realized by synchronizing the individual local time on each network node to the clock master in the designated node from which the packet is sent. CircLink also uses CMI code for transmitting signals, rather than the dipulse or bipolar signals that are the standard ARCNET signals. Since CMI encoding eliminates the DC element, a simple combination of a standard RS485 IC and a pulse transformer can be used to implement a transformer-coupled network.

1.2 About TMC2084

The TMC2084 is CircLink's standalone mode controller acting as an intelligent remote I/O controller that uses the enhanced token passing protocol. TMC2084 I/O nodes are controlled by the Host node (TMC2074/72) via the network. Thus, TMC2084 enables a single-processor with multi-remote I/O controllers environment at reasonable cost.

The TMC2084 has thirty-two I/O port lines featuring programmable direction, with 8-bit basis (output: 16 to 32 bit; input: 0 to 16 bit). The maximum number of nodes per network is fifteen, including the host node. This configuration enables a processor to control a total of 448 (14 × 32) remote I/O lines.

The Output Port type is selectable from either open-drain or push-pull, while one part of the I/O ports is definable as either output pins for network status monitoring, strobe output pins to handshake with AD or DA converter, or input pins for external trigger.

TMC2084 also has additional functions including the function to notify the host of its status, the states of its Output Ports and settings, the function to send packets with timestamp, and the function to synchronize the on-chip timer to the host.

This rich feature set is contained in a single 48-pin TQFP package.

1.3 Block Diagram

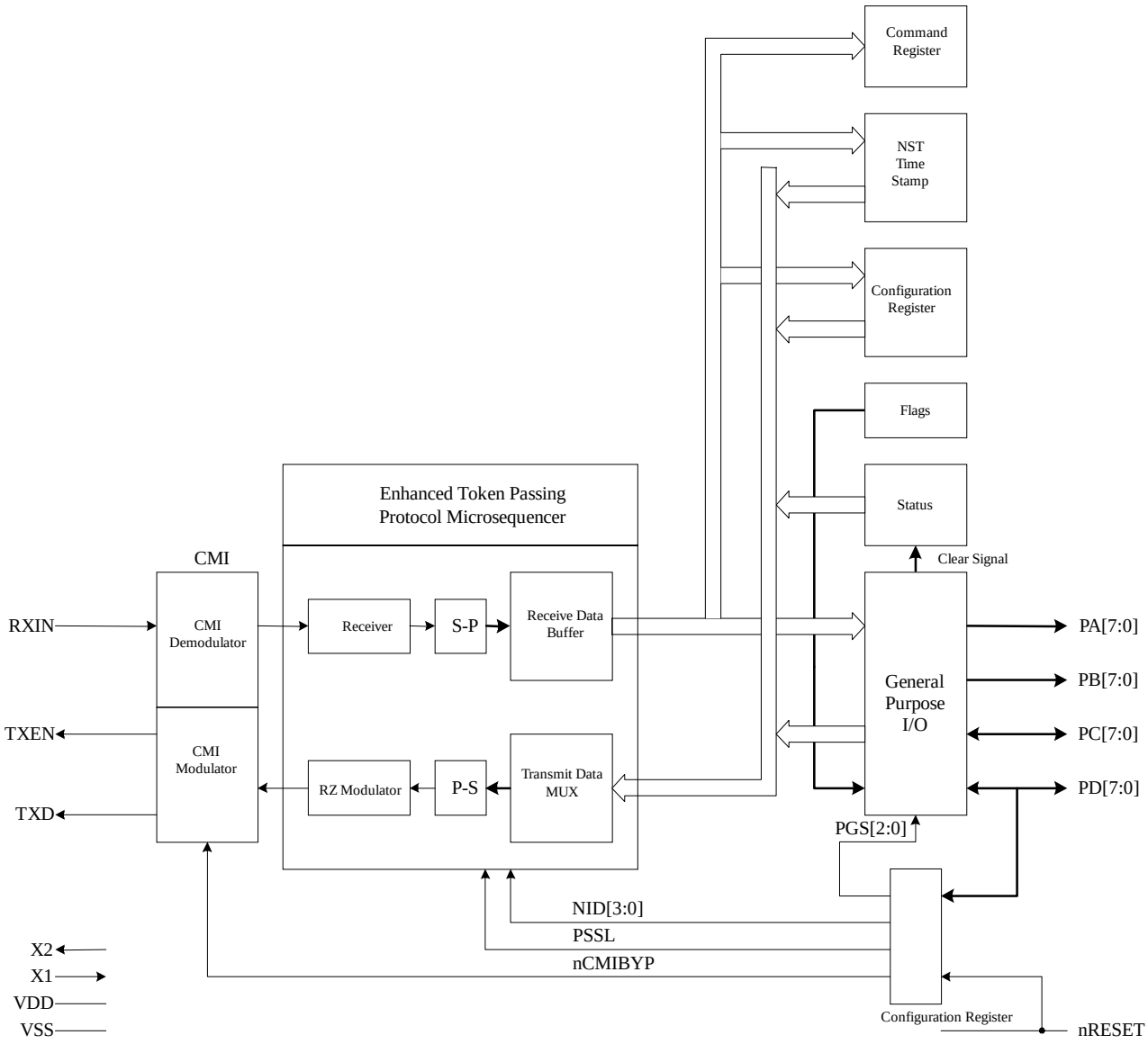


Figure 1 - TMC2084 Block Diagram

1.4 Pin List

PIN NO.	SIGNAL NAME	PIN NAME	BUFFER TYPE BY FUNCTION	DETAILED DESCRIPTION
General Purpose I/O Group A				
2 - 9	Port A bit 0 - 7 (output-only)	PA0 - 7	O42/OD4	General Purpose I/O Port A. An output-only port. The type of output can be selected using the PAOD bit, configured through the network. PAOD = 0 selects push-pull; PAOD = 1 selects open-drain (default).
General Purpose I/O Group B				
10-11, 14-19	Port B bit 0 - 7 (output-only)	PB0 - 7	O42/OD4	General Purpose I/O Port B. An output-only port. The type of output can be selected using PBOD bit, configured through the network. PBOD = 0 selects push-pull; PBOD = 1 selects open-drain (default).
General Purpose I/O Group C				
20	Port C bit 0	PC0	IT/O42/OD4	General Purpose I/O Port Bit 0. A bi-directional port. The port direction can be specified using the shared pin PGS0. PGS0 = L specifies input; PGS0 = H specifies output. The type of output can be selected using PCOD bit, configured through the network. PCOD = 0 selects push-pull; PCOD = 1 selects open-drain (default).
	External Trigger Input 1	nPISTR1	IT	External Trigger Input 1 The input pin for external trigger signal. If the shared pin PGS0 is set to L while "6h" or “7” is set using TXTRG3 - 0 bits that are configured through network then this port is configured for the external trigger input.
21-23, 26-29	Port C bit 1 - 7	PC1 - 7	IT/O42/OD4	General Purpose I/O port C bit 1 to 7. A bi-directional port. The direction of port and the type of output are configured using the same way as PC0.

PIN NO.	SIGNAL NAME	PIN NAME	BUFFER TYPE BY FUNCTION	DETAILED DESCRIPTION
General Purpose I/O Group D				
30	Port D bit 0	PD0	IT/O42	The bit 0 of Port D. A bi-directional port. The port direction can be specified using the shared pin PGS1. PGS1 = L specifies input; PGS1 = H specifies output.
	External Trigger Input 2	nPISTR2	IT	External Trigger Input 2 The input port of external trigger signal. If the shared pins PGS0 and PGS1 are set to L and H respectively while either "6h" or "7h" is set using TXTRG3 – 0 bits that are configured through network, then this port is configured for the external trigger input port.
	(Node ID Configuration Bit 0)	(NID0)	(IT)	The configuration bit 0 of the own node ID. For detailed information, see the section on Configuration Using Shared Pins.
31	Port D bit 1	PD1	IT/O42	The bit 1 of Port D. A bi-directional port. The port direction is configured using the same way as PD0.
	(Node ID Configuration Bit 1)	(NID1)	(IT)	The configuration bit 1 of the own node ID For detailed information, see the section on Configuration Using Shared Pins.
32	Port D bit 2	PD2	IT/O42	The bit 2 of Port D. A bi-directional port. The port direction is configured using the same way as PD0.
	(Node ID Configuration Bit 2)	(NID2)	(IT)	The configuration bit 2 of the own node ID For detailed information, see the section on Configuration Using Shared Pins.
33	Port D bit 3	PD3	IT/O42	The bit 3 of Port D. A bi-directional port. The port direction is configured using the same way as PD0.
	(Node ID Configuration Bit 3)	(NID3)	(IT)	The configuration bit 3 of the own node ID For detailed information, see the section on Configuration Using Shared Pins.
34	Port D bit 4	PD4	IT/O42	The bit 4 of Port D. A bi-directional port. The port direction can be specified using the shared pin PGS1. PGS1 = L specifies input; PGS1 = H specifies output. PGS2 should be set to L.
	FLAG OUTPUT bit0	FO0	O42	The bit0 of FLAG OUTPUT. A bi-directional port. Setting the shared pin PGS2 to H configures FLAG OUTPUT mode. For detailed information of the flag, see the section on Configuration Through Network.
	(Page Size Selection)	(PSSL)	(IT)	Page Size Selection. For detailed information, see the section on Configuration Using Shared Pins.

PIN NO.	SIGNAL NAME	PIN NAME	BUFFER TYPE BY FUNCTION	DETAILED DESCRIPTION
35	Port D bit 5	PD5	IT/O42	The bit 5 of Port D. A bi-directional port. The port direction is configured using the same way as PD4.
	FLAG OUTPUT bit1	FO1	O42	The bit1 of FLAG OUTPUT. The FLAG OUTPUT mode is configured using the same way as PD4. For detailed information of the flag, see the section on Configuration Through Network.
	(Port Direction Configuration - bit 0)	(PGS0)	(IT)	Configuration bit 0 of port direction. For detailed information, see the section on Configuration Using Shared Pins.
37	Port D bit6	PD6	IT/O42	The bit 6 of Port D. A bi-directional port. The port direction is configured using the same way as PD4.
	FLAG OUTPUT bit2	FO2	O42	The bit2 of FLAG OUTPUT. The FLAG OUTPUT mode is configured using the same way as PD4. For detailed information of the flag, see the section on Configuration Through the Network.
	(Port Direction Configuration - bit 1)	(PGS1)	(IT)	Configuration bit 1 of port direction. For detailed information, see the section on Configuration Using Shared Pins.
38	Port D bit 7	PD7	IT/O42	The bit 7 of Port D. A bi-directional port. The port direction is configured using the same way as PD4.
	Network Status Monitoring output	nRCNERR	O42	Network Status Monitoring output. The FLAG OUTPUT mode is configured using the same way as PD4. For detailed information see the section on Configuration Through the Network.
	(Port Direction Configuration - bit 2)	(PGS2)	(IT)	The configuration bit 2 of port direction. For detailed information, see the section on Configuration Using Shared Pins.
Reset and Clock				
41	Reset Input	nRESET	ICS	The input for the reset signal. The signal for hardware reset is connected to this active low pin.
43	Oscillator/ External Clock Input	X1	IC	This pin functions as the input for either the oscillator or the external clock.
44	Oscillator Output	X2	OX	Oscillator output.
Transceiver Interface				
46	Transmit Enable Output	TXEN	O42	Transmit enable output (active high)
47	Transmit Data Output (CMI bypass configuration)	TXD (nCMIBYP)	O42 (IT)	Transmit data output. Specifies bypassing of CMI encoder/ decoder. For detailed information, see the section on Configuration Using Shared Pins.

PIN NO.	SIGNAL NAME	PIN NAME	BUFFER TYPE BY FUNCTION	DETAILED DESCRIPTION
48	Receive Data Input	RXIN	IT	Receive data input.
Test Pin				
39, 40	Test Mode	nTMODE nSMODE	IT_PU	Test mode. **This pin must be tied to Vdd.**
Power Supply Pin				
13, 25, 42	Power Supply	Vdd	-	Power supply pin. This pin is connected to the power supply voltage (3.3V).
1, 12, 24, 36, 45	Ground	Vss	-	Ground pin. This pin is connected to the ground level (0V).

Description of buffer types:

IC	Input, CMOS Level
IT	Input, TTL Level
IT_PU	Input, TTL Level with pull-up
ICS	Input, CMOS Level with Schmitt Trigger
O42	Output, I_{OL} = 4 mA, I_{OH} = -2 mA
OD4	Open-drain Output, I_{OL} = 4 mA
OX	Oscillator Output

1.5 Pinout

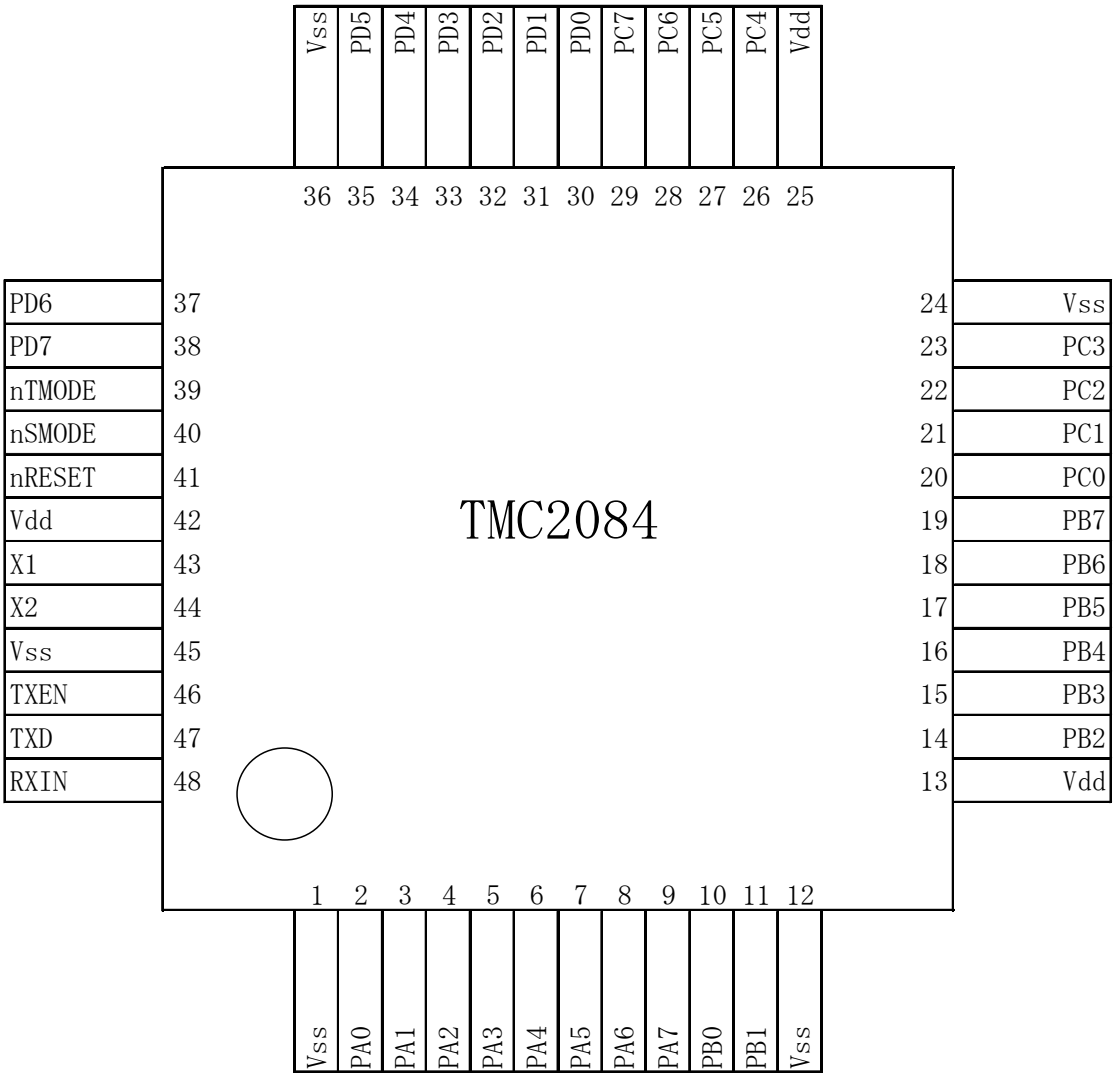


Figure 2 - TMC2084 Pin Configuration

Chapter 2 Functional Description

2.1 Network Configuration

2.1.1 General

Host Node and I/O Node

A CircLink network can consist of a single host node/multi I/O node, or multiple host nodes/single I/O, or multiple host nodes and multiple I/O nodes. The host node is directly connected to the system (external) CPU, which controls all communications to or from it. The device that can be used for the host node should be a TMC2072/74 that is configured to operate in Peripheral mode; the TMC2084 is dedicated for the use as an I/O node only (Standalone mode). The I/O nodes do not require the CPU and they are controlled indirectly via the network by the CPU through the host node.

The CircLink network allows a combination of host nodes and I/O nodes up to 15 nodes total. Every CircLink network must have at least one host node.

The host node controls the following I/O node functions:

- Input and output activities on a port (sending and receiving data and initializing the port)
- Setting various configuration data
- Request for configuration data
- Activation of transmission activity
- Software reset

These functions are controlled through the network.

Section 2.1.2 shows two examples: network configuration example 1 (single host) that includes one host node and fourteen I/O nodes, and network configuration example 2 (dual host) that includes two host nodes and four I/O nodes. When multiple hosts are used, I/O nodes should be grouped so that each host can control its corresponding group as shown in network configuration example 2: Host 1 controls both I/O-1 and -2; Host 2 controls both I/O-3 and -4.

Node ID

Any node that belongs to a network should have a unique identification number (ID). The ID is configured using shared pins NID3 - 0. When shared pin PSSL is set to L, the allowable range of the node ID is 1 trough 7; it is 1 through 15 when the PSSL pin is set to H. 0 is not allowed for any node ID.

Consecutive node ID numbers (beginning with 1) are assigned to nodes in a network. Consecutive node ID numbers should be used, because each unused ID number between 2 working node IDs causes a latency of 93.6 μs (2.5 Mbps operation) every time a token is sent and thus degrades overall network performance.

MAXID

The MAXID defines the maximum node ID of the network and is configured through the network using the MAXID3 – 0 bits. Configuring the MAXID for the network when the number of nodes is less than the upper limit that is defined as 7 for PSSL = L and 15 for PSSL = H in the protocol enables tokens to circulate only among the existing nodes. The allowable MAXID range is 2 through 7 for PSSL = L and 2 through 15 for PSSL = H. Both 0 and 1 are not allowed. The node ID should be assigned consecutively starting with 1 and the MAXID should be equal to the number of nodes.

Typically, all nodes should have the same value for MAXID. However, the node that requires MAXID is the node that has the largest ID number in the network and the remaining nodes can be left to use the default value: 7 for PSSL = L and 15 for PSSL = H (in this case the maximum ID is assigned to the host node). In the case where configuration items other than MAXID also can use their corresponding default values, configuration through the network is not required.

Transmission Rate

Transmission Rate defines a common rate for all nodes. The transmission rate for TMC2072/74 is configured using either an internal register or an external pin; for TMC2084, it is configured by the value that is equal to one eighth of the input clock.

TRANSMISSION RATE	CLOCK FREQUENCY	CLOCK SOURCE
5 Mbps	40 MHz	External clock only
4 Mbps	32 MHz	External clock or crystal resonator
2.5 Mbps	20 MHz	External clock or crystal resonator
2 Mbps	16 MHz	External clock or crystal resonator
1.25 Mbps	10 MHz	External clock or crystal resonator
1 Mbps	8 MHz	External clock only
625 Kbps	5 MHz	External clock only
500 Kbps	4 MHz	External clock only
312.5 Kbps	2.5 MHz	External clock only

The acceptable frequency of an external crystal resonator is limited to the range of 10 MHz to 32 MHz due to the limitation of the onchip oscillator's performance. Please use the external clock module if a frequency other than the above is needed.

2.1.2 Configuration Examples

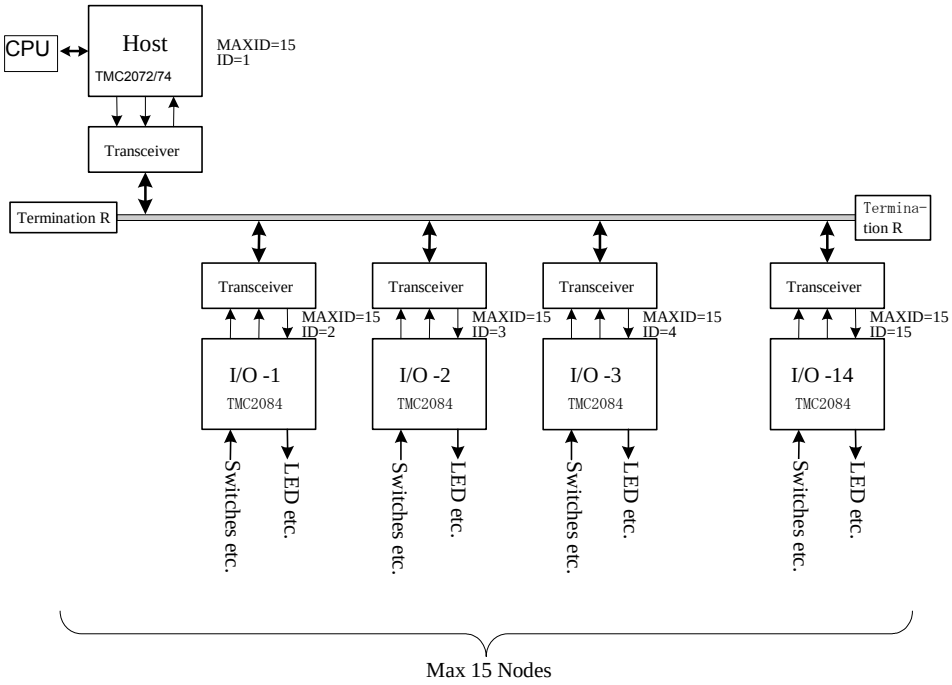
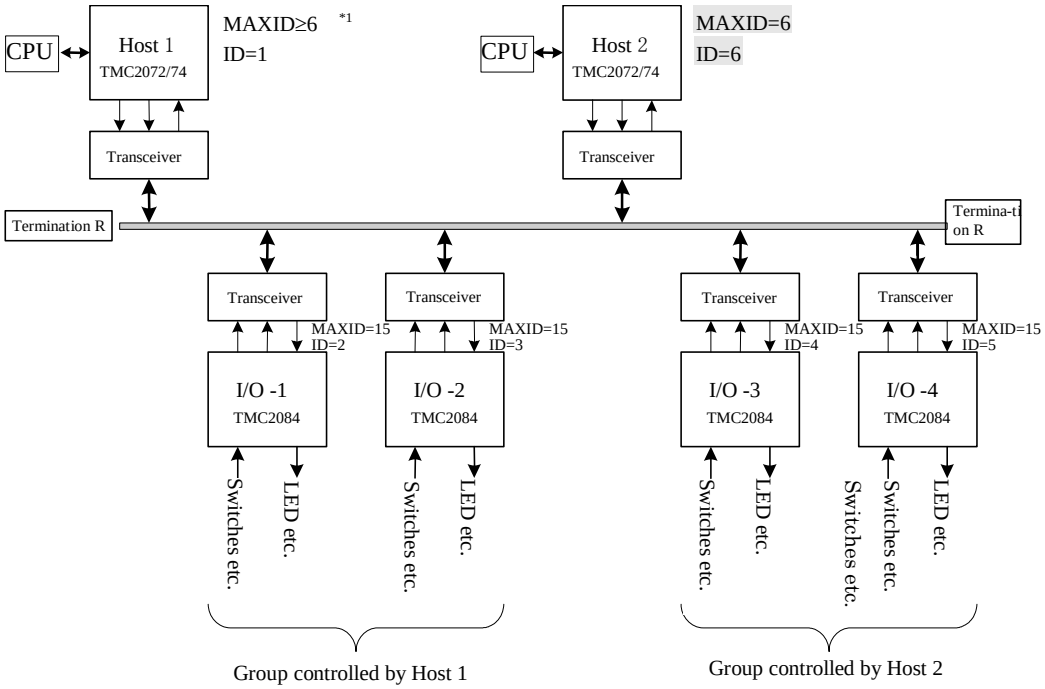


Figure 3 - Network Configuration Example 1: S Single Host and 15 Nodes



*1 Because a token is still passed to node 6 even if nodes 2 to 5 are off.

Figure 4 - Network Configuration Example 2: Dual Hosts and 6 Nodes

2.2 Initial Configuration

Initial configuration can be performed two ways: through shared pins or through the network.

2.2.1 Configuration Using Shared Pins

Basic items related to communication are configured using the shared pins. The configuration is performed after reading the states of pins PD7 - 0 and TXD at the rising edge of the reset signal. Since these pins remain in their high-impedance states (input states) during reset, connecting pull-up resisters to them causes High level input and connecting pull-down resisters to them causes Low level input. The items configured here are essential to send or receive packets within the network. Additional detail items may be configured if necessary using configuration through the network as described below.

nCMIBYP This pin specifies whether CMI coding is bypassed.

(Shared with TXD) Low: the CMI coding is bypassed (RZ coding for HYC4000/2000)

High: the CMI coding is not bypassed. (CMI coding for RS-485/CAN transceiver)

NID3 - 0 These three pins specify the node ID within the range 1 through 15.

(Shared with PD3 - 0) NID3 and NID0 correspond to MSB and LSB respectively. Low causes 0; High causes 1. When PSSL is set to Low, NID3 causes 0.

Note: DO NOT set low level for all pins.

PSSL This pin selects the page size.

(Shared with PD4) Low: 128 bytes/page (the maximum number of nodes = 7): All of the NID3, MAXID3 and CMID3 bits are fixed to 0.

Burst Transmission Period = 1.07 ms × 2.5/R (R = Transmission Rate in Mbps)

High: 64 bytes/page (the maximum number of nodes = 15)

Burst Transmission Period = 0.79 ms × 2.5/R (R = Transmission Rate in Mbps)

Two types of page sizes out of the four types that TMC2072/74 supports can be configured for TMC2084: 64-byte and 128-byte modes. A common page size must be configured for all nodes including host nodes. The data size that TMC2084 can send to or receive from the host in all modes is only the 8 bytes that are taken from the page; 64 bytes or 128 bytes of data can be transmitted only between host nodes.

PGS2 - 0 These three pins specify I/O port direction as shown in the table below.

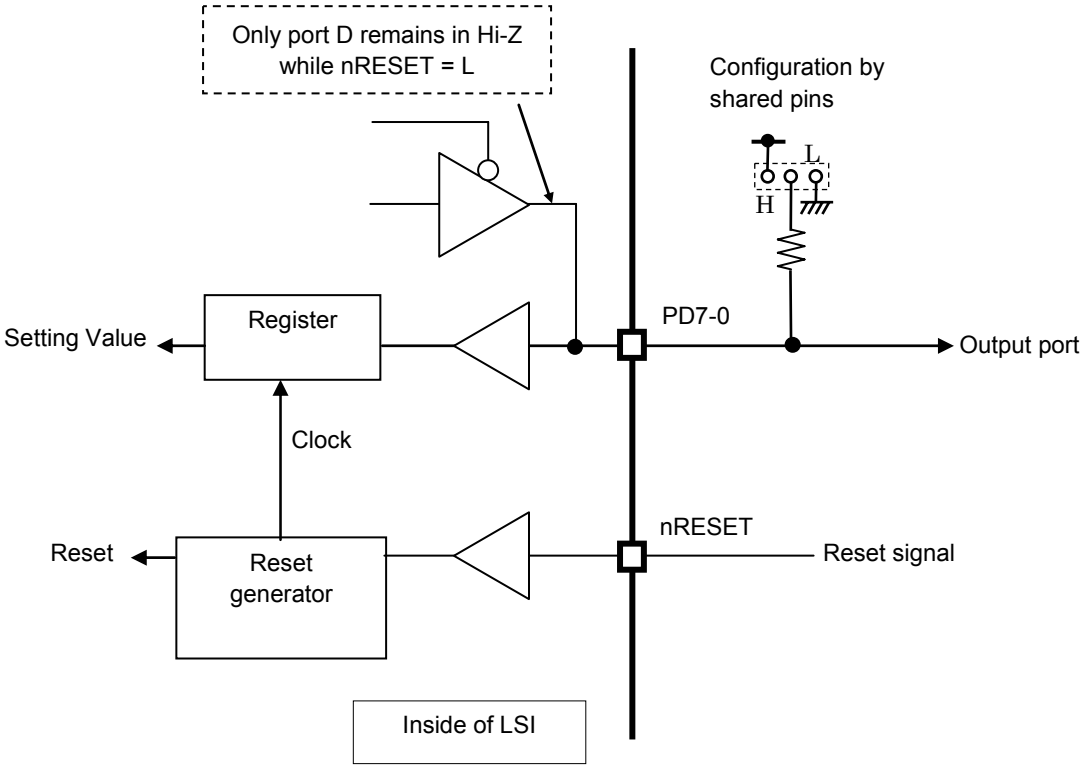
(Shared with PD7 - 5)

PGS2	PGS1	PGS0	Push-pull only		O.D / Push-pull			Input Pins for External Trigger
			PD7 - 4	PD3 - 0	PC7 - 0	PB7 - 0	PA7 - 0	
L	L	L	Input	Input	Input	Output	Output	nPISTR1
L	L	H			Output			nPISTR2
L	H	L	Output	Output	Input			nPISTR1
L	H	H			Output			-
H	L	L	FLAG OUTPUT	Input	Input			nPISTR1
H	L	H			Output			nPISTR2
H	H	L		Output	Input			nPISTR1
H	H	H			Output			-
L : Low ; H : High			O.D : Open-drain. The pins PA7 – 0 and PB7 – 0 are output-only.					

Port D Considerations

Example 1: Configuring Port D as OUTPUT PORT or FLAG OUTPUT - The case where the configuration by the shared pins is the same as the initial data from the OUTPUT PORT configured

The figure below shows the case where the initial data from the OUTPUT PORT does not conflict with the configuration by shared pins even if port D is configured as the OUTPUT PORT or FLAG OUTPUT. Port D remains in high-impedance state while the reset signal (nRESET) remains low. OUTPUT PORT remains in high-impedance state during the period from the falling edge of reset to the beginning of the first output data received. During these high-impedance periods, each input to port D is defined by the external pull-up (High) or pull-down (Low) resister. When port D is configured as FLAG OUTPUT, it starts driving right after the deassertion of the reset signal.

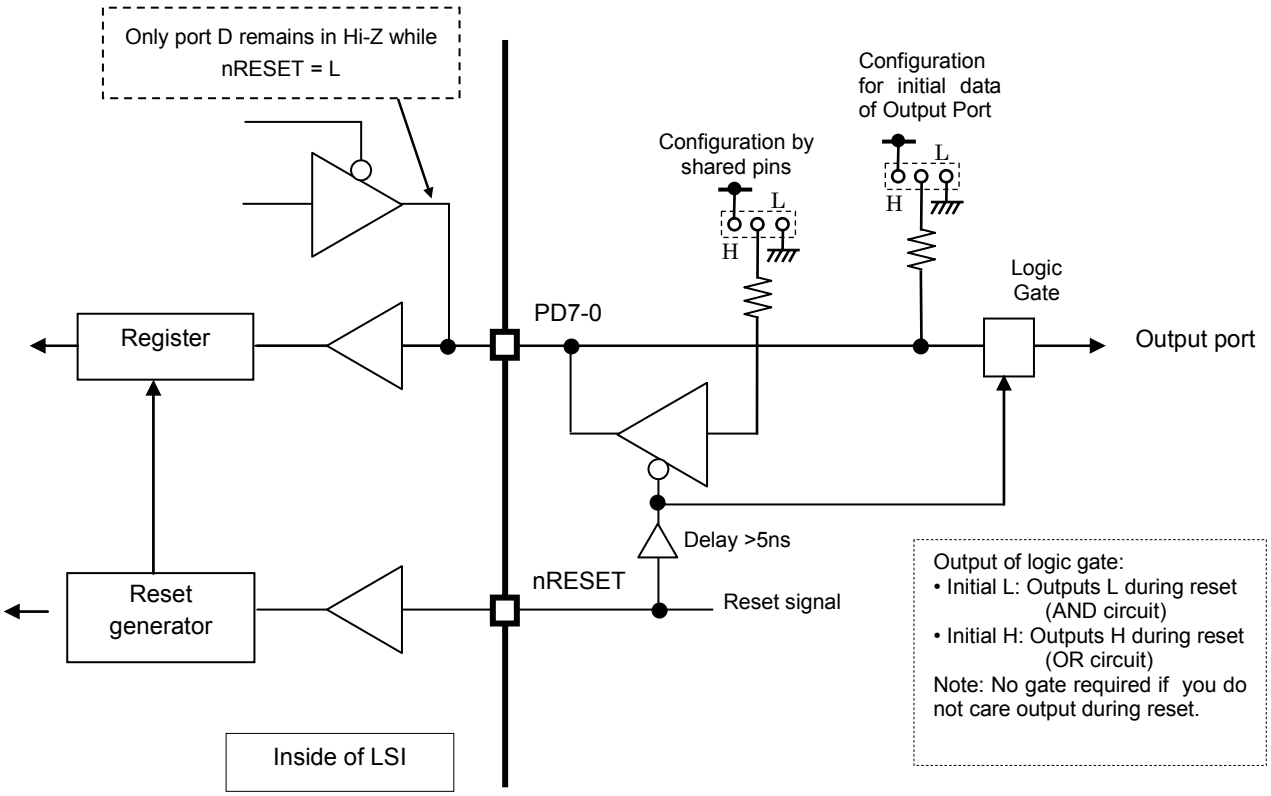


Example 2: Configuring Port D as OUTPUT PORT - The case where the configuration by the shared pins is different from the initial data from the OUTPUT PORT configured**.**

The figure below shows the case where the initial data from the OUTPUT PORT does conflict with the configuration by shared pins when port D is configured as an OUTPUT PORT. Port D remains in high - impedance state while the reset signal (nRESET) remains low. Also, the OUTPUT PORT remains in high-impedance state during the period from the falling edge of reset to the beginning of the first output data received.

During reset, the external tri-state buffer is enabled and the values configured by the shared pins are inputted to port D. After the reset signal is deasserted, the tri-state buffer is disabled and the initial data from the OUTPUT PORT is defined by an external pull-up (High) or pull-down (Low) resister. If initial data from the OUTPUT PORT is needed during the reset, use an external gate as shown in the figure below to define the data from OUTPUT PORT while the nRESET remains at low level.

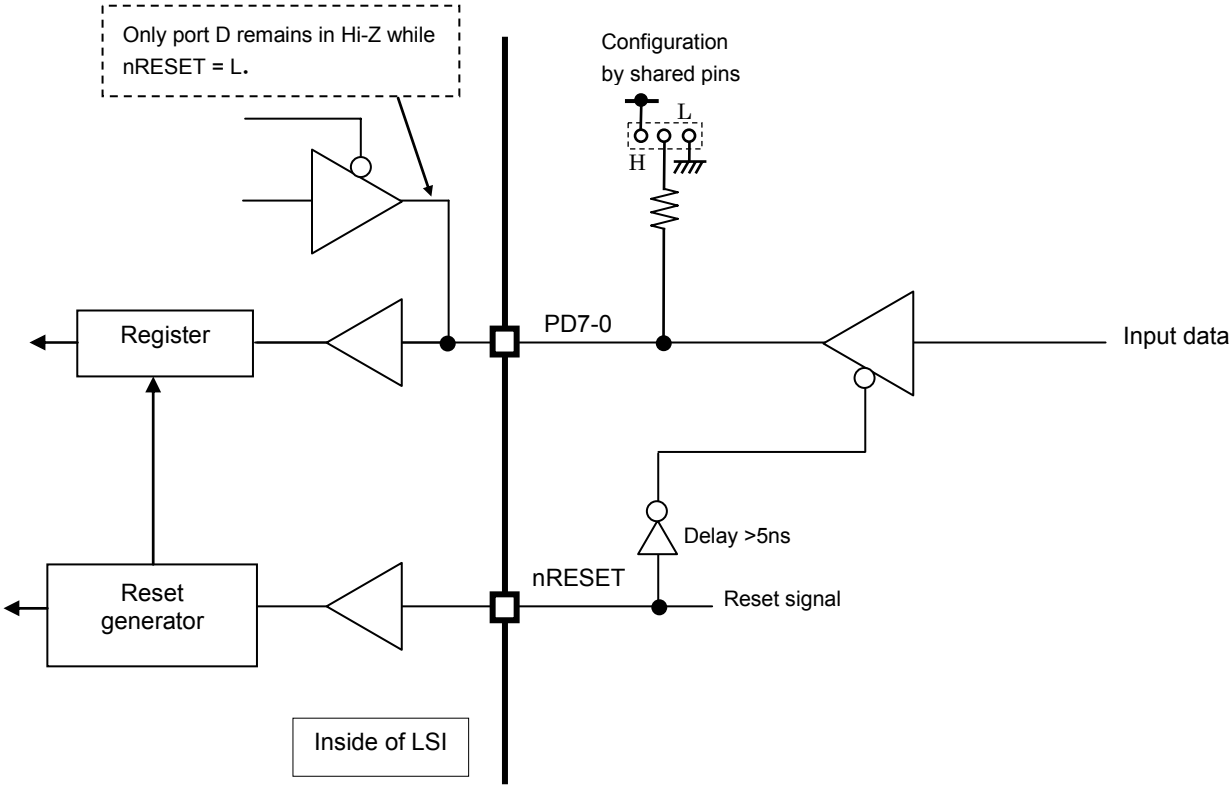
A hold time greater than 5 ns is required to retrieve the data configured by the shared pins and place it in the onchip memory. Thus, a buffer is added to provide a delay time for the control signal of an external tri-state buffer.


Only port D remains in Hi-Z while nRESET = L
Configuration for initial data of Output Port
Configuration by shared pins
L
H
L
H
Logic Gate
Register
PD7-0
Output port
Delay >5ns
nRESET
Reset generator
Reset signal
Inside of LSI
Output of logic gate:
• Initial L: Outputs L during reset (AND circuit)
• Initial H: Outputs H during reset (OR circuit)
Note: No gate required if you do not care output during reset.

Example 3: Configuring Port D as an INPUT PORT

The figure below shows the case where the port D is configured as INPUT PORT. The port D remains in high impedance state while the reset signal (reset) remains low level. During this high-impedance state, data defined by an external pull-up (High) or pull-down (Low) resister must be inputted to port D and any external input data to port D should be inhibited to avoid conflict. This requires the external tri-state buffer to inhibit input data during the reset period.

A hold time greater than 5 ns is required to retrieve the data configured by the shared pins and place it on the onchip memory. Thus, the buffer is added to provide a delay time for the control signal of the external tri-state buffer.



2.2.2 Configuration Through the Network

Additional items configured using this feature. The configuration is performed with an INITIAL SETTING packet received from the host node.

If the default is acceptable for all items that require configuration via the network and the NST carry output (i.e. nNSTCOUT described later) is not used, then configuration by the INITIAL SETTING packet is unnecessary. The configuration by INITIAL SETTING packet is valid only before receiving the START TRANSMIT command (described later). After receiving the START TRANSMIT command, the INITIAL SETTING packet is ignored.

Format of INITIAL SETTING Packet

From host node (transmit) to I/O node (receive)

Name	Adrs. *	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Initial value
SID	00h	Host node ID								--
DID	01h	I/O node ID or 00h (broadcasted)								--
C.P	02h	C.P = 38h/78h *								--
	⋮	⋮				⋮				--
		PACKET ID code								--
DATA0	38h/78h	**0**	**1**	**0**	0					--
DATA1	39h/79h	0	PCOD	PBOD	PAOD	BSTSEND	CMIERRMD	EMGYMD	BRE	7Fh
DATA2	3Ah/7Ah	POSTRMD	POSTRDLY	ACHTBYP	0	MAXID3 - 0				0Fh
DATA3	3Bh/7Bh	FOSL3 - 0				TXTRG3 - 0				00h
DATA4	3Ch/7Ch	NSTCOMD	ACHTFRQ	0	0	NSTC3 - 0				80h
DATA5	3Dh/7Dh	NSTPRE2 - 0			0	CMID3 - 0				00h
NST-L	3Eh/7Eh	NST7 - 0								--
NST-H	3Fh/7Fh	NST15 - 8								--

Note: *Addresses in 64-byte mode/Addresses in 128-byte mode

Register Description (DATA1: Various Configurations)

Name	Drs.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DATA1	39h/79h	0	PCOD	PBOD	PAOD	BSTSEND	CMIERRMD	EMGYMD	BRE

BRE Enables or disables receiving broadcast

0: Receiving broadcast is disabled.

1: Receiving broadcast is enabled (default).

When the broadcast packet is received by the BRE=0 setting, it is disregarded. (It doesn't become a receiving error.)

EMGYMD Configures emergency mode (Assertion of MYRECON causes dropping from network).

0: Does not initialize OUTPUT PORT (high-impedance state) when MYRECON is asserted.

1: Initializes OUTPUT PORT (high-impedance state) when MYRECON is asserted (default).

CMIERRMD Configures the CMI error mode.

0: Does not discard the packet when CMIECC is asserted in it.

1: Discards the packet when CMIECC is asserted in it (default)

BSTSEND Configures Recon-burst signal transmit (Assertion of MYRECON causes dropping from network).

0: Does not transmit Recon-burst signal when MYRECON is asserted.

1: Transmits Recon-burst signal when MYRECON is asserted (default).

PAOD Configures port A pins (PA7 - 0) as open-drain outputs.

0: Configures port A pins (PA7 - 0) as push-pull outputs (totem pole).

1: Configures port A pins (PA7 - 1) as open-drain outputs (default).

PBOD Configures port B pins (PB7 - 0) as open-drain outputs.

0: Configures port B pins (PB7 - 0) as push-pull output (totem pole).

1: Configures port B pins (PB7 - 1) as open-drain outputs (default).

PCOD Configures port D pins (PD7 - 0) as open-drain outputs.

0: Configures port D pins (PD7 - 0) as push-pull output (totem pole).

1: Configures port D pins (PD7 - 1) as open-drain outputs (default).

Register Description (DATA2: MAXID and nPOSTR Related)

Name	Adrs.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DATA2	3Ah/7Ah	POSTRMD	POSTRDLY	ACHTBYP	0	0			

MAXID3 - 0 Configure the maximum ID number with range 1 to 15 (MAXID4 is fixed to 0)

MAXID3: MSB; MAXID0: LSB

Configuring PSSL = Low causes MAXID3 to be fixed to 0.

Default: MAXID3 - 0 = 1111

ACHTBYP Configures the bypass or not for Anti-chatter circuit on input ports.

0: Enable the anti-chatter circuit (default)

1: Bypass (Disable) the anti-chatter circuit

Note: When the transmit trigger (TXTRG3-0) setting is set to “By the external trigger”, bypass is automatic.

POSTRDLY Configures delay time for the OUTPUT PORT strobe (nPOSTR).

0: From the transition of port A to the falling edge of strobe at least 11 times of Tx (default)

1: From the transition of port A to the falling edge of strobe at least 43 times of Tx.

Note: Tx = Period of input clock (11 × Tx = 550 ns and 43 × Tx = 2.15 μs @20 MHz input)

POSTRMD Configures output mode for the OUTPUT PORT strobe signal (nPOSTR).

0: Asserts OUTPUT PORT strobe signal after initializing OUTPUT PORT and after receiving the OUTPUT DATA packet (default).

1: Asserts only after receiving the OUTPUT DATA packet.

Note: Initializing OUTPUT PORT means Initialization by both the INITIALIZE OUTPUT PORT command and the assertion of MYRECON in emergency mode (EMGYMD = 1).

Register Description (DATA3: This register selects the transmit trigger in FLAG OUTPUT.)

Name	Adrs.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DATA3	3Bh/7Bh	FOSL3 - 0				TXTRG3 - 0			

TXTRG3 - 0 These bits select the transmit trigger.

The trigger condition to send the INPUT DATA packet is configured. The transmit trigger is enabled after receiving the START TRANSMIT command.

TXTRG				The transmit trigger to send the INPUT DATA packet is generated upon ...
3	2	1	0	
0	0	0	0	Receiving the OUTPUT DATA packet
0	0	0	1	Receiving the OUTPUT DATA packet or expiring on-chip timer (3.3 ms)
0	0	1	0	Receiving the OUTPUT DATA packet or expiring on-chip timer (6.6 ms)
0	0	1	1	Receiving the OUTPUT DATA packet or expiring on-chip timer (13.1 ms)
0	1	0	0	Receiving the OUTPUT DATA packet or expiring on-chip timer (26.2 ms)
0	1	0	1	Receiving the OUTPUT DATA packet or expiring on-chip timer (104.8 ms)
0	1	1	0	By the external trigger (with NST latch)
0	1	1	1	By the external trigger (without NST latch)
1	0	0	0	Reserved (unused)
1	0	0	1	Reserved (unused)
1	0	1	0	Reserved (unused)
1	0	1	1	Reserved (unused)
1	1	0	0	Reserved (unused)
1	1	0	1	Reserved (unused)
1	1	1	0	Receiving own token
1	1	1	1	Receiving the COMMAND packet

Receiving the OUTPUT DATA packet:

A single transmit trigger is generated after receiving the OUTPUT DATA packet that is destined for this node or broadcasted is received. The INPUT DATA packet is transmitted after receiving the token (i.e., the token destined for this node).

Receiving the OUTPUT DATA packet or expiring on-chip timer:

A single transmit trigger is generated after either receiving the OUTPUT DATA packet that is destined for this node or broadcasted, or expiring on-chip timer. The INPUT DATA packet is then transmitted after receiving the token.

Note: This on-chip timer is cleared by an of three events: receiving the START TRANSMIT command; receiving the INITIALIZE OUTPUT PORT command; or transmitting an INPUT DATA packet after receiving a data packet.

By the external trigger:

The rising edge on the external trigger input pin (nPISTR1 or nPISTR2) latches the input data and generates the trigger. The INPUT DATA packet is then transmitted after receiving the token.

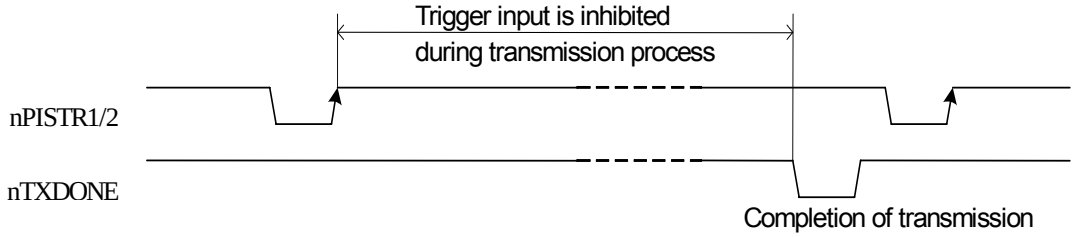
Either nPISTR1 or nPISTR2 is selected as the external trigger input pin depending on the I/O port direction configured by pins PGS2 - 0. If all of ports are configured as OUTPUT PORTs by the configuration feature for I/O port direction, then this external trigger cannot be used.

When the NST value latch is used, both the NST value and input data are latched simultaneously and the latched NST value is transmitted. When the NST value latch is not used, the last NST value is transmitted regardless to latching the input data.

(Both the input data and NST value latches are cleared to zero by hardware at initialization.)

Receiving the token allows the actual transmission of packets. Thus, the delay time from the trigger to the actual transmission can vary. If two consecutive external triggers are inputted, it can not be determined which trigger caused the data transmission since it depends on when the token was received.

Using nTXDONE (transmit completion flag) of the FLAG OUTPUT allows an easy handshake.



Whenever the token is received:

With this condition, the trigger is always generated. The INPUT DATA packet is transmitted whenever own token is received.

Receiving COMMAND packet:

A single transmit trigger is generated whenever either the START TRANSMIT or INITIALIZE OUTPUT PORT command that is destined for this node or broadcasted is received. The INPUT DATA packet is then transmitted upon receiving the token (The transmit trigger caused by the INITIALIZE OUTPUT PORT command is valid after receiving the START TRANSMIT command).

Note that the Return Setting and SOFTWARE RESET commands do not cause any transmit trigger. For detail information on each command, see section 2.4 COMMAND packet.

NOTE: A single transmit trigger is generated each time the START TRANSMIT command is received regardless of the configuration for the transmit trigger. Additionally, a single transmit trigger is generated at the time the INITIALIZE OUTPUT PORT command is received after receiving the START TRANSMIT command.

FOSL3 - 0 Select FLAG OUTPUT.

These bits select the flags that are outputted to the upper 4 bits of port D. For detailed information, see section of 2.7 FLAG OUTPUT.

	FOSL				FO3 (PD7)	FO2 (PD6)	FO1 (PD5)	FO0 (PD4)
	3	2	1	0				
Default	0	0	0	0	nRCNERR	nPOSTR	nTXDONE	nNSTCOUT
	0	0	0	1				NSTUNLOC
	0	0	1	0				nTKN2ME
	0	0	1	1			nNSTCOUT	NSTUNLOC
	0	1	0	0				nTKN2ME
	0	1	0	1			NSTUNLOC	
	0	1	1	0		nTXDONE	nNSTCOUT	NSTUNLOC
	0	1	1	1				nTKN2ME
	1	0	0	0			NSTUNLOC	
	1	0	0	1		nNSTCOUT		
	1	0	1	0		(Fixed to High)	(Fixed to High)	(Fixed to High)
	1	0	1	1				
	1	1	0	0				
	1	1	0	1				
	1	1	1	0				
	1	1	1	1				

Register Description (DATA4: NST carry-related configuration)

Name	Adrs.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DATA4	3Ch/7Ch	NSTCOMD	ACHTFRQ	0	0	NSTC3 – 0			

NSTC3 - 0 These bits select the NST carry (default: NSTC3 - 0 = 0000)

0000: 1st digit (carry period = NST resolution X 2^1)

0001: 2nd digit (carry period = NST resolution X 2^2)

0010: 3rd digit (carry period = NST resolution X 2^3)

0011: 4th digit (carry period = NST resolution X 2^4)

: : :

1110: 15th digit (carry period = NST resolution X 2^15)

1111: 16th digit (carry period = NST resolution X 2^16)

ACHTFRQ Configures the sampling frequency for Anti-chatter circuit on input ports.

0: Sampling frequency is 1.22 kHz (default)

1: Sampling frequency is 19.1Hz (52 ms period)

NOTE: When the transmit trigger (TXTRG3-0) setting is set to “By the external trigger”, bypass is automatic. The above-mentioned sampling frequency is the value when the input clock is 20 MHz. The sampling frequency doubles when the input clock is 40 MHz, and half when the input clock is 10 MHz.

NSTCOMD Configures the output mode of NST carry (NST carry is outputted via nNSTCOUT)

0: Active low pulse output with the pulse Level Width resolution selected by the bits NSTPRE2 – 0

1: Clock output with the duty ratio 50% (default)

Register Description (DATA5: Clock master ID and NST resolution)

Name	Adrs.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DATA5	3Dh/7Dh	NSTPRE2 - 0			0	CMID3 - 0			

CMID3 - 0 These bits define the clock master ID in the range of 1 to 15 (CMID4 is fixed to 0)

CMID3: MSB; CMID0: LSB

PSSL = Low causes CMID3 = 0.

Default: CMID3 - 0 = 0000 (Asynchronous to NST: free running)

If a non-zero value is set in bits CMID3 – 0, the synchronization to NST begins when a packet is received from the next CMID.

NSTPRE2 - 0 These bits define the NST resolution (default： NSTPRE2 - 0 = 000)

000: 1.6 μs (Maximum period = 104.9 ms)

001: 3.2 μs (Maximum period = 209.7 ms)

010: 6.4 μs (Maximum period = 419.4 ms)

011: 12.8 μs (Maximum period = 838.9 ms)

100: 25.6 μs (Maximum period = 1.68 s)

101: 51.2 μs (Maximum period = 3.35 s)

110: 102.4 μs (Maximum period = 6.71 s)

111: 204.8 μs (Maximum period = 13.42 s)

NOTE: The above data are for 20 MHz input.

(For 40 MHz input they are half; for 10 MHz input they double)

2.2.3 Returning Configuration Data

When the RETURN SETTING command is received before receiving the START TRANSMIT command, the RETURN SETTING packet is broadcasted upon receiving the next own token. Items configured using the INITIAL SETTING packet are transmitted as the RETURN SETTING packet.

After receiving the START TRANSMIT command, any RETURN SETTING command is ignored. For detail information on each command, see the section of 2.4 COMMAND packets.

Format of the RETURN SETTING Packet

From I/O node (transmit) to host node (receive)

Name	Adrs. *	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SID	00h	ID of I/O node							
DID	01h	00h (always broadcasted)							
C.P	02h	C.P = 38h/78h *							
	⋮	⋮							
		PACKET ID code							
DATA0	38h/78h	**0**	**1**	**1**	0	0	000 / PGS2-0 *2		
DATA1	39h/79h	0	PCOD	PBOD	PAOD	BSTSEND	CMIERRMD	EMGYMD	BRE
DATA2	3Ah/7Ah	POSTRMD	POSTRDLY	ACHTBYP	0	0			
DATA3	3Bh/7Bh	FOSL3 - 0				TXTRG3 - 0			
DATA4	3Ch/7Ch	NSTCOMD	ACHTFRQ	0	0	NSTC3 - 0			
DATA5	3Dh/7Dh	NSTPRE2 - 0			0	CMID3 - 0			
NST-L	3Eh/7Eh	NST7 - 0							
NST-H	3Fh/7Fh	NST15 - 8							

* Addresses in 64-byte mode/Addresses in 128-byte mode

*2 “000” or “PGS2-0” is selected using the RETURN SETTING command.

PGS2-0 sets status of the I/O ports direction for the configuration using shared pins.

2.3 Types of Packets

2.3.1 Packets TMC2084 Can Receive

TMC2084 can receive the three types of packets from the host node: the Initial Setting, Command and OUTPUT DATA packets. The packet is identified using the packet ID code included in the first data byte (DATA0) of it and any packet that has undefined code is discarded.

Packet's RAM image on the host node is shown below.

Adrs. *1	Name	INITIAL SETTING Packet	COMMAND Packet	OUTPUT DATA Packet
00h	SID	ID of host node		
01h	DID	ID of I/O node or 00h (broadcasted)		
02h	C.P	C.P = 38h/78h *1		
⋮		⋮		
38h/78h	DATA0	PACKET ID code = 010	PACKET ID code = 100	PACKET ID code = 000, OPICDONE clear
39h/79h	DATA1	Various configuration data	0	Status clear
3Ah/7Ah	DATA2	MAXID, nPOSTR-related	Command code	Port A output data
3Bh/7Bh	DATA3	Transmit trigger , FLAG OUTPUT selection	0	Port B output data
3Ch/7Ch	DATA4	NST carry -related	Command code	Port C output data
3Dh/7Dh	DATA5	Clock master ID, NST resolution	0	Port D output data
3Eh/7Eh	NST-L	Lower byte of NST (for the time synchronization use*2)		
3Fh/7Fh	NST-H	Upper byte of NST (for the time synchronization use*2)		

*1 Addresses in 64-byte mode/Addresses in 128-byte mode

*2 In the case where the originator of the packet is the clock master (CM) node. If the originator of the packet is not the clock master (CM) node, then the time synchronization is not used.

2.3.2 Packets TMC2084 Can Transmit

TMC2084 can send two types of packets: the Return Setting and INPUT DATA packets. It sends the RETURN SETTING packet during the period from the deassertion of reset signal to receiving the START TRANSMIT command. After receiving the START TRANSMIT command it sends INPUT DATA packets. For more information, see section of 2.4 COMMAND packets.

Packet's RAM image on the host node is shown below.

Adrs. *	Name	RETURN SETTING Packet	INPUT DATA Packet
00h	SID	ID of I/O node	
01h	DID	00h (always broadcasted)	
02h	C.P	C.P = 38h/78h *	
⋮		⋮	
38h/78h	DATA0	PACKET ID code = 011	PACKET ID code = 001, OPICDONE, configuration data of PGS2 – 0 pins
39h/79h	DATA1	Various configuration data	Status
3Ah/7Ah	DATA2	MAXID, nPOSTR-related configuration data	Port A OUTPUT PORT data
3Bh/7Bh	DATA3	Transmit trigger, FLAG OUTPUT selections	Port B OUTPUT PORT data
3Ch/7Ch	DATA4	NST carry-related configurations	Port C input data or port C OUTPUT PORT data
3Dh/7Dh	DATA5	Clock master ID, NST resolution configurations	Port D input data or port D OUTPUT PORT data
3Eh/7Eh	NST-L	Lower byte of NST (time stamp)	
3Fh/7Fh	NST-H	Upper byte of NST (time stamp)	

* Addresses in 64-byte mode/Addresses in 128-byte mode

2.4 Command Packets

2.4.1 Format of COMMAND Packets

From host node (transmit) to I/O node (receive)

Name	Adrs. *	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SID	00h	ID of host node							
DID	01h	ID of I/O node or 00h (broadcasted)							
C.P	02h	C.P = 38h/78h *							
	⋮	⋮							
		PACKET ID code							
DATA0	38h/78h	**1**	**0**	**0**	0				
DATA1	39h/79h	00h							
DATA2	3Ah/7Ah	CMD7 - 0							
DATA3	3Bh/7Bh	00h							
DATA4	3Ch/7Ch	CMD7 - 0 (repeat the same data twice)							
DATA5	3Dh/7Dh	00h							
NST-L	3Eh/7Eh	NST7 - 0							
NST-H	3Fh/7Fh	NST15 - 8							

* Addresses in 64-byte mode/Addresses in 128-byte mode

RETURN SETTING Command (CMD7 - 0 = 000P - 0001 = 01h or 11h)

Operation: Requests sending the configuration data configured via the network (i.e., RETURN SETTING packet).

3bit Data of Bit2-0 on DATA0 in the RETURN SETTING packet, is selected by the "P" option.

P=0 (CMD=01h) : Bit2-0 is all zero (Compatible with TMC20080)

P=1 (CMD=11h) : Bit2-0 is PGS2-0 which is I/O ports direction status

This command is ignored after receiving the Start Transmit packet.

Response: The RETURN SETTING packet is broadcasted upon receiving own token. (Refer to 2.2.3)

START TRANSMIT command (CMD7 - 0 = 0000 - 0011 = 03h)

Operation: Enables the transmit trigger and starts the transmission of the INPUT DATA packet. After receiving this command, packets the TMC2084 can transmit are limited to INPUT DATA packets. The SOFTWARE RESET command disables transmission from the TMC2084.

Response: The INPUT DATA packet is broadcasted only one time upon receiving own token regardless of the transmit trigger configuration. After that the transmissions depend on the transmit trigger configuration.

NOTE: If the transmit trigger is configured for the external trigger and:

If the external trigger input (either nPISTR1 or 2) is low when TMC2084 comes out of reset, then both the input data and the NST are returned with zeroes set as their values. If the external trigger input is High, it returns the data taken from the INPUT PORTs and NST at the time the INITIAL SETTING packet is received. However, when the NST latch is not used, typically current contents of the counter are transmitted as the NST value.

For the START TRANSMIT commands that are received after the first START TRANSMIT command, it returns the data that are taken from the input data and the NST at the time the preceding external trigger is inputted. However, when the NST latch is not used, usually the current contents of the counter are transmitted as NST value.

INITIALIZE OUTPUT PORT command (CMD7 - 0 = 0000 to 0111 = 07h)

Operation: Places all of OUTPUT PORTs in high-impedance state.

Response: If any START TRANSMIT command is already received, then TMC2084 sends the INPUT DATA packet upon receiving own token. Otherwise, it sends nothing.

SOFTWARE RESET command (CMD7 - 0 = 1000 to 1111 = 8Fh)

Operation: Executes the software reset (i.e., it resets the communication section of the TMC2084), sets all I/O ports to high-impedance state and initializes the configuration data configured through the network to default values, then adds TMC2084 to the network automatically. The transmit trigger is also disabled (disabled transmission).

Response: None

***NOTE:** After receiving the software reset command, software reset is executed within 100 µS (@2.5 Mbps) or less.

(The100 µS becomes 50 µS at 5 Mbps, and 200 µS at 1.25 Mbps)

2.5 OUTPUT PORTs

These ports output the data included in the OUTPUT DATA packet received from the host node. The received data are outputted to the OUTPUT PORTs that are configured using the I/O port direction configuration feature, and the data destined for the INPUT PORT and FLAG OUTPUT are not outputted to pins. The output type is only available for the port A, B and C: Either push-pull or open-drain output type is selectable for them through network using the PAOD, PBOD and PCOD bits.

OUTPUT DATA packets also include the area to clear NST and various status bits.

All ports that are configured for the FLAG OUTPUT mode, except for pins PD7 – 4, are placed in the high-impedance state until the first OUTPUT DATA packet is received, regardless the output type configured. Dropping from the network causes high-impedance state for them (depending on the EMGYMD configured). Initializing OUTPUT PORTs to high-impedance is also possible using a command.

In addition, the output port is initialized (high-impedance state) by the hardware reset and the software reset command.

2.5.1 Format of OUTPUT DATA Packets

From host node (transmit) to I/O node (receive)

Name	Adrs. *	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SID	00h	ID of host node							
DID	01h	ID of I/O node or 00h (broadcasted)							
C.P	02h	C.P = 38h/78h *							
	⋮	⋮							
		PACKET ID code							
DATA0	38h/78h	**0**	**0**	**0**	0	OPICDONE	0		
DATA1	39h/79h	RXERR	CMIECC	NSTUNLOC	MRCV	TKNRETF	RCPUM	POR	MYRECON
DATA2	3Ah/7Ah	PA7 - 0							
DATA3	3Bh/7Bh	PB7 - 0							
DATA4	3Ch/7Ch	PC7 - 0							
DATA5	3Dh/7Dh	PD7 - 0							
NST-L	3Eh/7Eh	NST7 - 0							
NST-H	3Fh/7Fh	NST15 - 8							

* Addresses in 64-byte mode/Addresses in 128-byte mode

PA7 - 0, PB7 - 0, PC7 – 0 and PD7 - 0

These pins accept data that are outputted to the corresponding port. However, data on the bits that are configured as both the INPUT PORTs and the FLAG OUTPUTs (PD7 - 4) are not outputted to pins.

RXERR	1: Clears RXERR flag	0: Unaffected
CMIECC	1: Clears CMIECC flag	0: Unaffected
NSTUNLOC	1: Clears NSTUNLOC flag	0: Unaffected
MRCV	1: Clears MRCV flag	0: Unaffected
TKNRETF	1: Clears TKNRETF flag	0: Unaffected
RCPUM	1: Clears RCPUM flag	0: Unaffected
POR	1: Clears POR flag	0: Unaffected
MYRECON	1: Clears MYRECON flag	0: Unaffected
OPICDONE	1: Clears OPICDONE flag	0: Unaffected

2.5.2 Configuring I/O Port Directions

The direction of each I/O port is configured using shared pins PGS2 - 0. For detailed information, see the section on Configuration Using Shared Pins.

2.5.3 Open-Drain Mode

Either push-pull or open-drain output type is configurable for ports A, B, and C through the network using PAOD, PBOD, and PCOD. For detailed information, see the section on Configuration Through Network.

2.5.4 Initializing OUTPUT PORTs

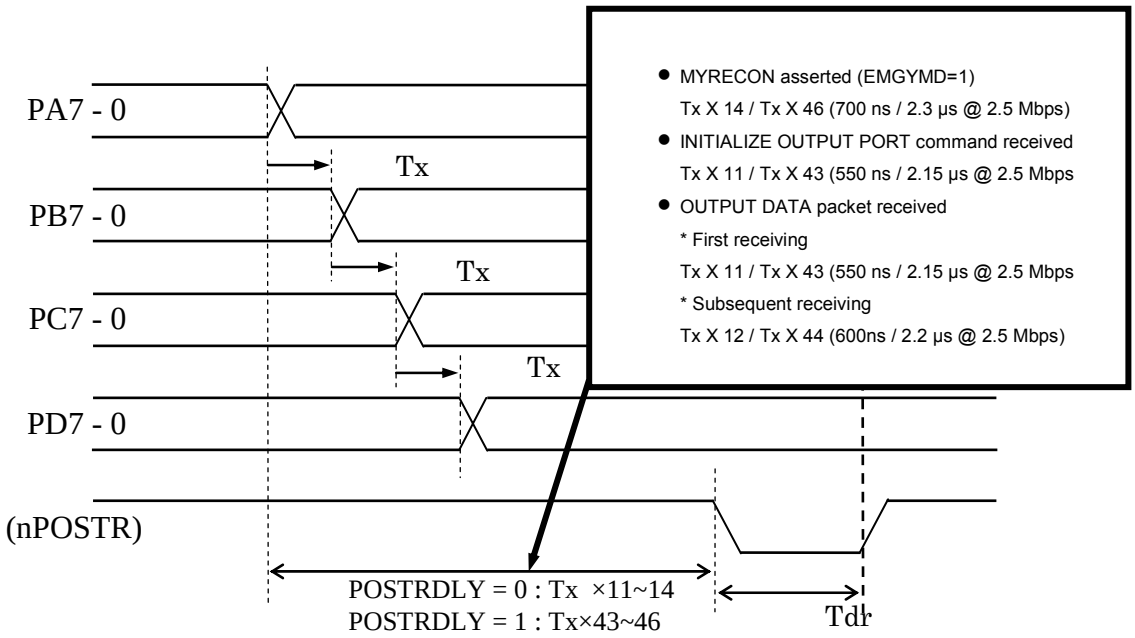
OUTPUT PORTs are initialized to high-impedance by the following events:

- Node dropped from network (EMGYMD = 1; MYRECON asserted)
- For detailed information, see EMGYMD in the section on Configuration Through Network.
- The INITIALIZE OUTPUT PORT command is received
- Hardware reset
- The SOFTWARE RESET command is received

The data from the OUTPUT DATA packet are outputted to the corresponding port again when the OUTPUT DATA packet is received.

2.5.5 Switching Timing In OUTPUT PORTs

To prevent simultaneously switching OUTPUT PORTs which would generate noise, a time delay is provided for each group ports. The delay time depends on the input clock: 50 ns at 20 MHz clock. The figure below shows timing relationships between the OUTPUT PORT and the output strobe flag, nPOSTR.



Tdr: Period of transmission rate (400 ns @ 2.5 Mbps)
Tx: Period of input clock (50 ns @ 20 MHz) Tdr = 8 × Tx

2.6 INPUT PORT

In the following events, Data from the INPUT PORTs are broadcasted using the INPUT DATA packet:

- Own token is received immediately after the START TRANSMIT command is received.
- Own token is received after the transmit trigger is issued.
- Own token is received immediately after the OUTPUT PORT command is received.

Also, the following data are transmitted together with the data from INPUT PORTs:

- Various statuses
- PGS2 – 0 — Configuration data of I/O direction (see the section of Configuration Using Shared Pins)
- NST15 – 0 — Time stamp (see the section of NST)

The data from the OUTPUT PORTs are retransmitted (feed backed) to the bits that are configured as OUTPUT PORTs. However, if bits PD7 – 4 are configured as FLAG OUTPUT, ”1” is transmitted to each corresponding bit. Additionally, if the transmit trigger is configured as the external trigger, ”0” is transmitted to the corresponding trigger input pin: PC0 or PD0.

No INPUT DATA packet is transmitted before the START TRANSMIT command is received from the host (i.e., the transmission function is activated). Once the START TRANSMIT command is received, the transmission of the INPUT DATA packet commences depending on the transmit trigger mode configured through network using bits TXTRG3 - 0. For detailed information, see sections 2.2.2 Configuration Through Network and 2.4 Command Packets.

2.6.1 Format of Input Data Packets

From I/O node (transmit) to host node (receive)

Name	Adrs. *	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SID	00h	ID of I/O node							
DID	01h	00h (always broadcasted)							
C.P	02h	C.P = 38h/78h *							
	⋮	⋮ PACKET ID code							
DATA0	38h/78h	**0**	**0**	**1**	0	OPICDONE	PGS2 - 0		
DATA1	39h/79h	RXERR	CMIECC	NSTUNLOC	MRCV	TKNRETF	RCPUM	POR	MYRECON
DATA2	3Ah/7Ah	PA7 - 0							
DATA3	3Bh/7Bh	PB7 - 0							
DATA4	3Ch/7Ch	PC7 - 0							
DATA5	3Dh/7Dh	PD7 - 0							
NST-L	3Eh/7Eh	NST7 - 0							
NST-H	3Fh/7Fh	NST15 - 8							

* Addresses in 64-byte mode/Addresses in 128-byte mode

PA7 - 0, PB7 - 0, PC7 – 0 and PD7 - 0

Each of these bits transmits the state of a port. The data from the OUTPUT PORTs are transmitted (feedback) to the bits that are configured as OUTPUT PORTs. However, if bits PD7 – 4 are configured as FLAG OUTPUT, ”1” is transmitted to the corresponding bit. Additionally, if the transmit trigger is configured as the external trigger, ”0” is transmitted to either PC0 or PD0 pin that corresponds to the trigger input pin, nPISTR1 or nPISTR 2 respectively.

PGS2 - 0	Configuration data of I/O port direction For detail information, see the section of Configuration Using Shared Pins.	
RXERR	1: Receiving error was detected.	0: No error was detected.
CMIECC	1: Error correction was performed during CMI decoding.	0: No error was detected.
NSTUNLOC	1: NST unlock state was detected.	0: No error was detected.
MRCV	1: Own packet was received.	0: No own packet was received.
TKNRETF	1: Token retry was encountered.	0: No token retry was encountered.
RCPUM	1: The C.P value in the received packet was different from 38h/78h.	
	0: The C.P value in the received packet was equal to 38h/78h.	
POR	1: Either hardware or software reset was asserted.	
	0: No reset was asserted.	
MYRECON	1: Dropping from network caused the RECON timer to expire.	
	0: No timeout was encountered.	
OPICDONE	1: The INITIALIZE OUTPUT PORT command was executed.	
	0: The INITIALIZE OUTPUT PORT command was not executed.	

After receiving the START TRANSMIT command, TMC2084 commences the transmission of the above data: configuration data (3 bits), status data (9 bits) input data (32 bits) and NST(16 bits).

For detail information on each status bit, see the section 2.8 Status Bits.

NST15 - 0 (Time stamp)

TMC2084 sends the INPUT DATA packet with time information (NST value) attached. When the transmit trigger is configured as the external trigger mode that uses NST latch, the NST value taken at the time the input data is latched is transmitted. In the external trigger mode that does not use the NST latch, the preceding NST value is transmitted regardless of the input data latch (For detail information on the transmit trigger, see the section on Configuration Through the Network).

2.7 FLAG OUTPUT

Tying the shared pin PGS2 to high level configures the upper four bits of port D to be FLAG OUTPUT port. When the FLAG OUTPUT configuration is used, the OUTPUT PORT feature using the OUTPUT DATA packet is not available. The flags start to drive within two system clock cycles after the de-assertion of reset.

The FLAG OUTPUT port outputs six different flags: MSB (FO3) always outputs nRCNERR; the lower three bits (FO2 – 0) output a set of three flags that is selected from five flags using the bits FOSL3 – 0 that are configured through network.

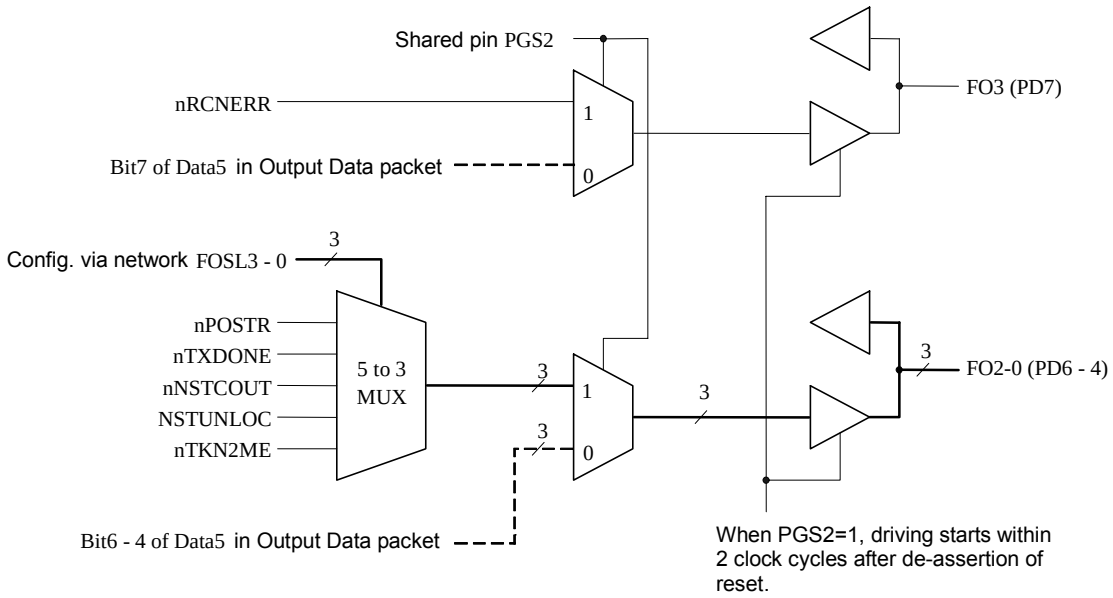


Figure 5 - Functional Diagram Of FLAG OUTPUT

Table 1 - Truth Table Of Bits FOSL3 - 0

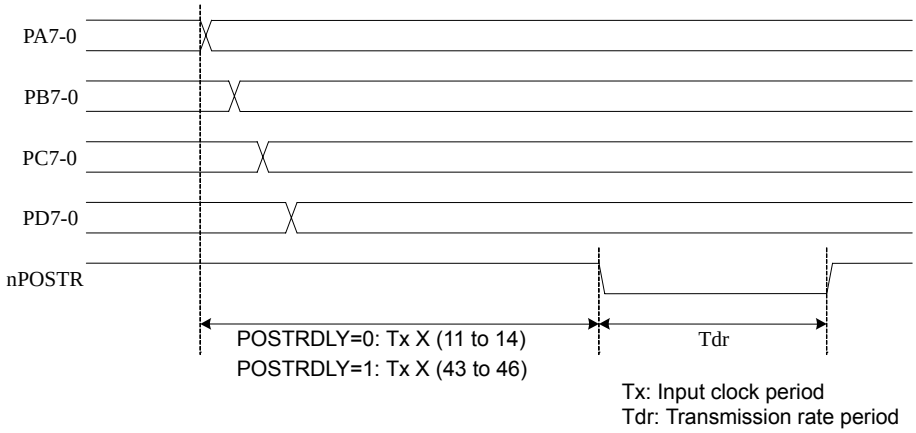
	FOSL				FO3 (PD7)	FO2 (PD6)	FO1 (PD5)	FO0 (PD4)
	3	2	1	0				
Default	0	0	0	0	nRCNERR	nPOSTR	nTXDONE	nNSTCOUT
	0	0	0	1				NSTUNLOC
	0	0	1	0				nTKN2ME
	0	0	1	1			nNSTCOUT	NSTUNLOC
	0	1	0	0				nTKN2ME
	0	1	0	1			NSTUNLOC	
	0	1	1	0		nTXDONE	nNSTCOUT	NSTUNLOC
	0	1	1	1				nTKN2ME
	1	0	0	0			NSTUNLOC	
	1	0	0	1		nNSTCOUT		
	1	0	1	0		(Fixed to High)	(Fixed to High)	(Fixed to High)
	1	0	1	1				
	1	1	0	0				
	1	1	0	1				
	1	1	1	0				
	1	1	1	1				

2.7.1 Flag Descriptions

nPOSTR The strobe pulse for the OUTPUT PORT (active low). This can be used as the strobe signal for such as an external DA converter (see the examples of application circuits in the section of the Appendix). The following events assert nPOSTR:

- OUTPUT DATA packet was received.
- The INITIALIZE OUTPUT PORT command was received when POSTRMD = 0 had been configured through network.
- Dropped from network due to EMGYMD = 1 (MYRECON asserted) when POSTRMD = 0 had been configured through network.

The nPOSTR outputs a pulse after the OUTPUT DATA packet is received and the state of OUTPUT PORT is stabled. As the delay time from the settling of OUTPUT PORT state to the output of strobe pulse, one of two delay times is selectable using the POSTRDLY bit that is configured through network.



nTXDONE The pulse that indicates the completion of transmitting the INPUT DATA packet (active low). The pulse Level Width is Tdr (= transmission rate period). This can be used as the trigger signal for such as an external AD converter (see the example of application circuits in the section of the Appendix).

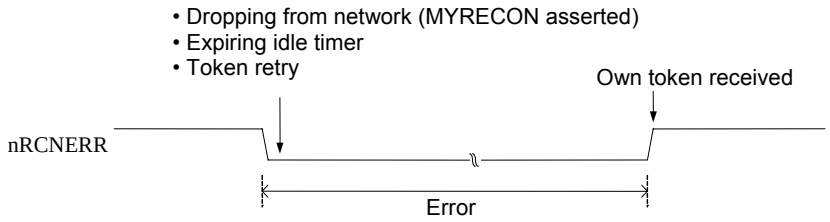
nNSTCOUT NST carry pulse (active low or clock). For detail information, see the section of NST.

NSTUNLOC The output flag that indicates the synchronization status between own and clock master's NSTs (active high). The asynchronous state (unlocked state) causes High level. For detail information, see the section of NST.

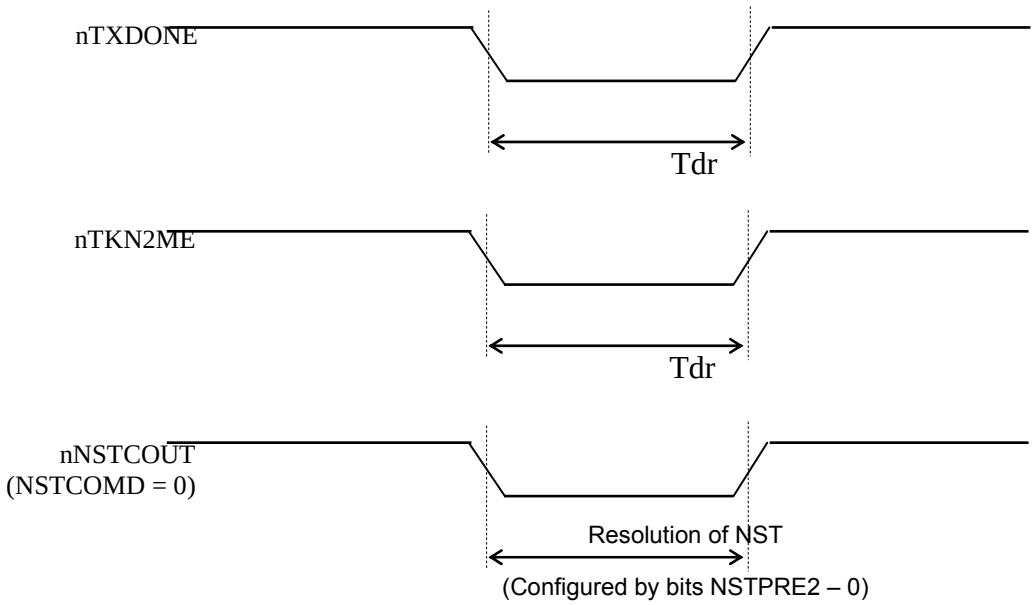
nTKN2ME The pulse that indicates that own token was received (active low). The pulse Level Width is Tdr (= transmission rate period).

nRCNERR The output flags that indicates network error (active low).

This is asserted in the event of dropping from network (MYRECON asserted), expiring idle timer or token retry and it is reset upon receiving own token.



2.7.2 Pulse Level Width Of Each Output Flag



Tdr: Transmission rate period

2.8 Status Bits

TMC2084 has multiple status bits that indicate its various states and transmits them as a part of the INPUT DATA packet. Setting anyone of these statuses bits to "1" causes it to keep its value until it is cleared. Any status bit is cleared when the OUTPUT DATA packet in which its corresponding status bit is set to "1" is received. Also, they are cleared by the hardware reset and receiving the SOFTWARE RESET command.

RXERR Indicates that the device stopped receiving a packet since it detected an error during it (the packet was discarded).

1: Receiving error is detected

0: Non error

This flag is asserted in the following events:

a) CP error

The C.P in the received packet exceeded the Page Size (40h or 80h) or it was equal to the value (01h or 02h) that means the header area. Potential causes： Incorrect configuration in host node side.

b) Frame error

The packet data of which frame format violated the token passing protocol was received. Potential causes： Mismatch in the configuration for such as transmission rate or coding scheme.

c) Length error

The data size that was actually received was different from the value C.P indicated. The device failure is only potential cause.

d) CRC error

The received packet data had incorrect CRC code. Potential causes： Unreliable physical line.

e) CMI decoding error (CMIERRMD = 1)

The CMI demodulator encountered error correction. (This is considered as an error only if CMIERRMD = 1 is configured through network)

NOTE: No error source bit is available for RXERR.

CMIECC Indicates that CMI decoder corrected an error in the received data.

1: An error was corrected.

0: Non error

NOTE: The state transition diagram for CMI describes that no potential symbol received is regarded as the nearest potential symbol received. For an example, receiving no potential symbol 10 allows the CMI receiver to interpret that the correct symbol either 11 or 00 was changed to 10 due to an error. Receiving another 11 illegally immediately after symbol 11 enables the CMI receiver to think that the correct symbol would be 00, inversely if the preceding 00 is received then the correct symbol would be 11. On the other hand, receiving another 11 (00) immediately after 11 (00) allows selecting 01 as correct symbol. For more information, see section 2.10 CMI Coding.

NSTUNLOC Indicates the NST synchronization state between the CM and own nodes. For detail information, see the section 2.9 NST Time Stamps.

1: Not locked to NST of the CM node.

0: Locked (synchronized) to NST of the CM node.

Although this flag has the same meaning as the NSTUNLOC bit of the FLAG OUTPUT, it acts differently:

This status bit: Once It is set to ”1,” it remains in the ”1” state until it is cleared.

FLAG OUTPUT: The Lock/Unlock sate is reflected to the output pin immediately.

If own node is the CM node, this flag always is ”0.”

If other node is CM node, this flag is ”1” by default. Be sure to clear this bit before you use it to confirm the synchronization to the CM node.

*About approval condition for Synchronous lock /unlock state

- Unlock to lock state (NSTUNLOC=0)

The difference between own NST and NST from CM node enters within +/-2. And NST from CM node must be received three times or more continuously, and all of those differences must be within +/-2.

- Lock to unlock state (NSTUNLOC=1)

The difference between own NST and NST from CM node doesn't enter within +/-2. Or NST from CM node must be received three times or more continuously, and all of those differences are not within +/-2.

MRCV Indicates that own packet was received normally.

1: Own packet was received.

0: Own packet was not received.

Receiving the broadcasted packet or others packet does not affect this bit.

TKNRETF Indicates that a token was retransmitted (Token retry).

1: Token retry was performed;

0: No token retry was performed

When a token did not arrive at the destination (own ID + 1), TMC2084 transmit it to the same destination one more time. This may happen when the next node does not exist or some reason like noise prevents token to arrive at the destination (own ID + 1). When non-consecutive node ID numbers are used, this always happen at the neighboring node of unused ID number.

RCPUM Indicates that the C.P in the received packet had an invalid value; the correct value is 38h for PSSL = H or 78h for PSSL = L. Potential cause: the host node has an incorrect configuration. The received packet is discarded.

1: The C.P in the received packet had a value other than 38h/78h.

0: It had 38h/78h.

In the event that the C.P in the received packet exceeded the Page Size (40h for PLLS = H or 80h for PSSL = L) or it was equal to the value (01h or 02h) that means the header area, RXERR is asserted instead of RCPUM.

RCPUM=1 is generated by receiving the broadcast packet that it transmits when the TMC2072/74 is set to Standalone mode when BRE=1 is set.

POR Indicates that hardware reset or receiving the SOFTWARE RESET command caused software reset.

1: Either hardware or software reset was performed.

0: No reset was performed.

MYRECON Indicates that RECON timer has expired, dropping the node from the network. When no node recognized its own node, i.e., no own token received during the time period of 52 ms (@2.5 Mbps), the RECON timer expires.

1: The RECON timer expired.

0: The RECON timer did not expire.

OPICDONE Indicates that the INITIALIZE OUTPUT PORT command was executed.

1: The INITIALIZE OUTPUT PORT command was executed.

0: It was not executed.

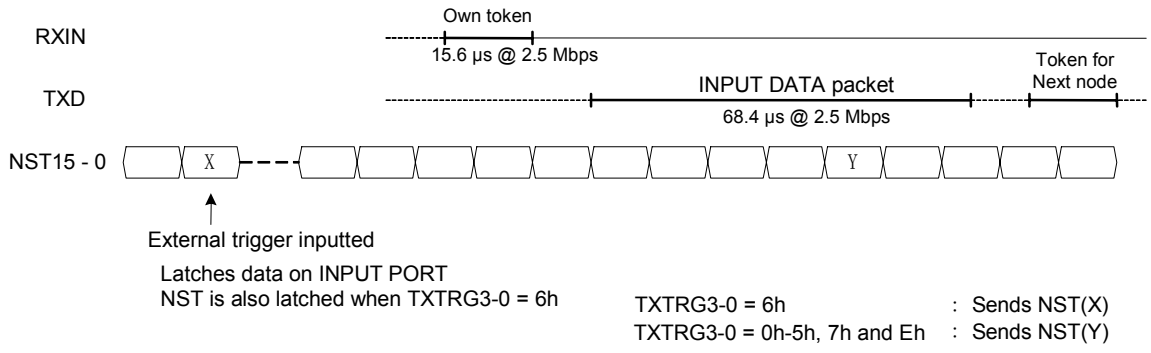
2.9 NST Time Stamps

TMC2084 can handle packets with an attached time stamp. The time stamp is known as NST (Network Standard Time). Every node in the network has its own clock that is synchronized to the NST of the clock master node (CM node). Only one clock master node is allowed to exist in a network.

NST has 16-bit length and is included in the last two bytes of the packet that is sent or received. The NST has a different meaning depending on whether it is in a received or transmitted packet.

Packet Type	Usage of NST
Received packet (transmitted from CM node)	Synchronization with CM node
Received packet (transmitted from non-CM node)	Receiving time stamp
Transmitted packet	Transmitting time stamp

The NST used in the time stamp usually represents the time at which the packet is transmitted (see Y in the figure shown below). If you need the time stamp that represents the time at which data on an INPUT PORT is taken using the external trigger, please configure bits TXTRG3 – 0 = 6h (i.e., external trigger using NST latch). The time stamp represents the time at which the external trigger is inputted (see X in the figure shown below).



2.9.1 Time Synchronization

Receiving the packet from the clock master after configuring both bit sets CMID3 – 0 and NSTPRE2 - 0 to the appropriate values enables synchronization with NST.

CMID3 - 0 The ID number for the clock master. It must be in the range 1 to 15 (1 to 7 for PSSL = L).

NSTPRE2 - 0 The resolution of NST. Its range must be the system clock period multiplied by 32 to 4096.

NOTE: All nodes must have a common resolution. (Except for the asynchronous case).

Table 2 - Bits NSTPRE2 – 0 And NST Resolution

NSTPRE			Dividing Ratio	Resolution and NST Period @ 20 MHz Clock	
2	1	0			
0	0	0	1: 32	1.6 μs	105 ms
0	0	1	1: 64	3.2 μs	210 ms
0	1	0	1: 128	6.4 μs	409 ms
0	1	1	1: 256	12.8 μs	839 ms
1	0	0	1: 512	25.6 μs	1,680 ms
1	0	1	1: 1024	51.2 μs	3,360 ms
1	1	0	1: 2048	102.4 μs	6,710 ms
1	1	1	1: 4096	204.8 μs	13,420 ms

The local time is synchronized each time with unicasted or broadcasted packet received from the CM node that is specified by bits CMID3 – 0 and even with any packet that the CM node transmits. The NSTUNLOC pin of FLAG OUTPUT and the NSTUNLOC status bit indicate whether the device is synchronized to the NST of CM node. For detailed information, see the sections on FOSL3 – 0 in Configuration Through the Network and the Status Bits.

2.9.2 Carry Output

Configuring both the bit sets FOSL3 - 0 (flag selection) and NSTC3 – 0 through the network enables the nNSTCOUT pin (NST carry output) of the FLAG OUTPUT to output the operating state of NST counter. Additionally, configuring the NSTCOMD bit through the network enables the selection of output type from either pulse (NSTCOMD = 0) or clock (NSTCOMD = 1: default).

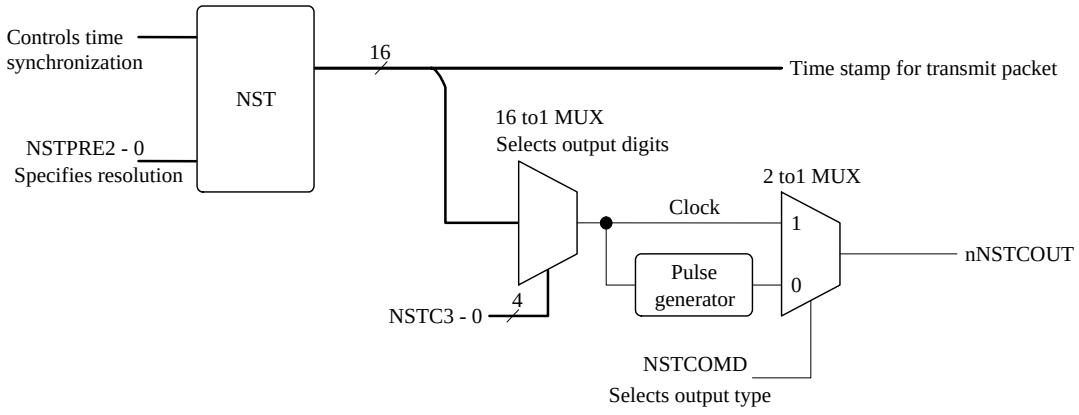


Figure 6 - Functional Diagram of NST Carry Output Generation Section

Table 3 - Bits NSTC3 – 0 vs. Carry Output Bit

NSTC				Carry Output Bits	Output period of Carry
3	2	1	0		
0	0	0	0	NST bit 0	Resolution X 2^1
0	0	0	1	NST bit 1	Resolution X 2^2
0	0	1	0	NST bit 2	Resolution X 2^3
. . .				. . .	
1	1	1	1	NST bit 15	Resolution X 2^{15}

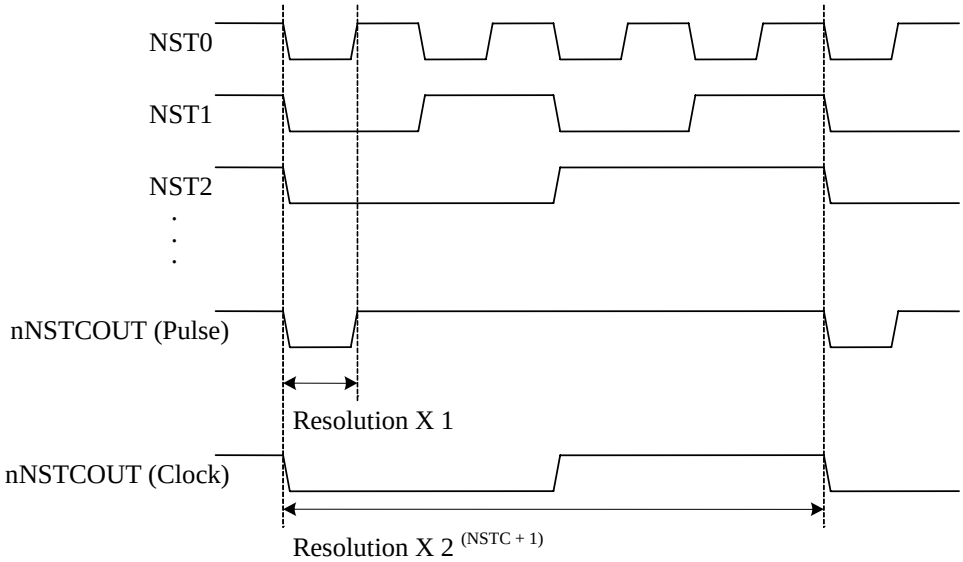
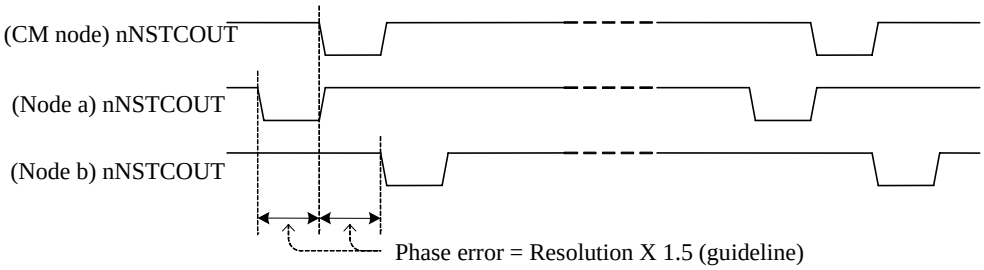


Figure 7 - nNSTCOUT Output Timing Example For Bits NSTC3 - 0 = 2h

The NST feature as a network standard time allows multiple nodes to output the synchronous NST carry. It is suitable for LED lamp controlling applications.



The carry output starts driving with High level when the devise comes out of reset. The condition for the pin to start driving the carry output depends on the configuration of bits CMID3 – 0 as shown in the table below:

Bits CMID3 - 0	Start Condition Of Carry Output
Own ID or 0	When the INITIAL SETTING packet is received
ID of other node	When a packet is received from CM node (regardless the destination of packet)

2.10 CMI Coding

TMC2084 supports CMI coding and RZ coding as the coding scheme for media interface.

Features of CMI Coding:

- Low DC component

  This makes external circuitry to prevent the pulse transformer from magnetic saturation unnecessary when it is used for isolation in RS485, since in CMI coding the same bit is never repeated more than two consecutive times.

- Limited possible states allows easy self-correction

  The self-correction capability of CMI may correct an error caused by jitter or one shot noise. The CMIECC status bit reports whether the self-correction was made.

  The bit CMIERMD that is configured through the network specifies whether the self-corrected packet is treated as a normally-received packet. Usually it is not a problem to treat it as a normal packet [*1] Faulty correction made by CMI causes the assertion of CRC check and the RXERR status bit reports this event. In this case, the received packet should be discarded.

[*1] The CMIERRMD bit is by default configured to "The packet is discarded."

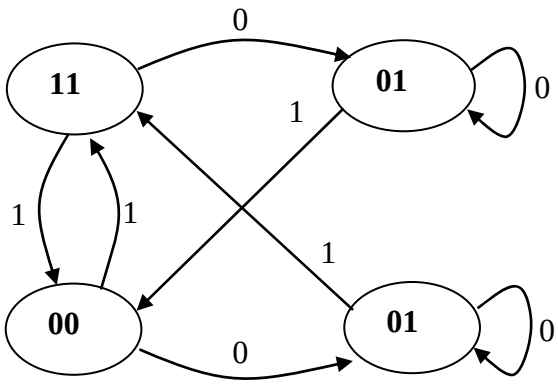


Figure 8 - State Transition Diagram for CMI

The shared pin nCMIBYP is used to select either the CMI or RZ coding: nCMIBYP = H selects CMI coding; nCMIBYP = L selects RZ coding.

For detail information on CMI coding, see the data sheet for TMC2072 or TMC2074.

2.11 RAM Image On Host Side

The image of on-chip RAM in the host node is shown below. The area labeled as ”I/O-n” shows the packet data received from each I/O node and the area labeled as ”host ” shows the state of the transmission page of host node.

I. Page Size configuration: 64 byte/page (PSSL = H)

The following conditions apply:

- Host node ID = MAXID

- The number of I/O nodes = m (possible setting: m = 14 max, ID = 1 to 14 and MAXID = 15)
- One host node (required setting: ID = m + 1 and MAXID = m+1)

		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
Page: 1 (ID = 1) **I/O-1**	00	01h	00h	38h													
	10																
	20																
	30									DATA0	DATA1	DATA2	DATA3	DATA4	DATA5	NST-L	NST-H
Page: 2 (ID = 2) **I/O-2**	00	02h	00h	38h													
	10																
	20																
	30									DATA0	DATA1	DATA2	DATA3	DATA4	DATA5	NST-L	NST-H
Page: 3 (ID = 3) **I/O-3**	00	03h	00h	38h													
	10																
	20																
	30									DATA0	DATA1	DATA2	DATA3	DATA4	DATA5	NST-L	NST-H
⋮											⋮						
Page: m (ID = m) **I/O-m**	00	m	00h	38h													
	10																
	20																
	30									DATA0	DATA1	DATA2	DATA3	DATA4	DATA5	NST-L	NST-H
Page: m + 1 (ID = m + 1) Host	00	m + 1	DID	38h													
	10																
	20																
	30									DATA0	DATA1	DATA2	DATA3	DATA4	DATA5	Reserved	Reserved

II. Page Size configuration: 128 byte/page (PSSL = L)

The following conditions apply:

- Host node ID = 1
- The number of I/O nodes = m (required setting: m = 6 max, ID = 2 to 6 and MAXID = m + 1)
- One host node (required setting: ID = 1 and MAXID = m+1)

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
Page: 1 (ID = 1) **Host**	00	01h	DID	78h												
	10															
	20															
	30															
	40															
	50															
	60															
	70								DATA0	DATA1	DATA2	DATA3	DATA4	DATA5	NST-L	NST-H
Page: 2 (ID = 2) **I/O-1**	00	02h	00h	78h												
	10															
	20															
	30															
	40															
	50															
	60															
	70								DATA0	DATA1	DATA2	DATA3	DATA4	DATA5	NST-L	NST-H
Page: 3 (ID = 3) **I/O-2**	00	03h	00h	78h												
	10															
	20															
	30															
	40															
	50															
	60															
	70								DATA0	DATA1	DATA2	DATA3	DATA4	DATA5	NST-L	NST-H
⋮										⋮						
Page: m (ID = m+1) **I/O-m**	00	m+1	00h	78h												
	10															
	20															
	30															
	40															
	50															
	60															
	70								DATA0	DATA1	DATA2	DATA3	DATA4	DATA5	NST-L	NST-H

2.12 Configuration Flow

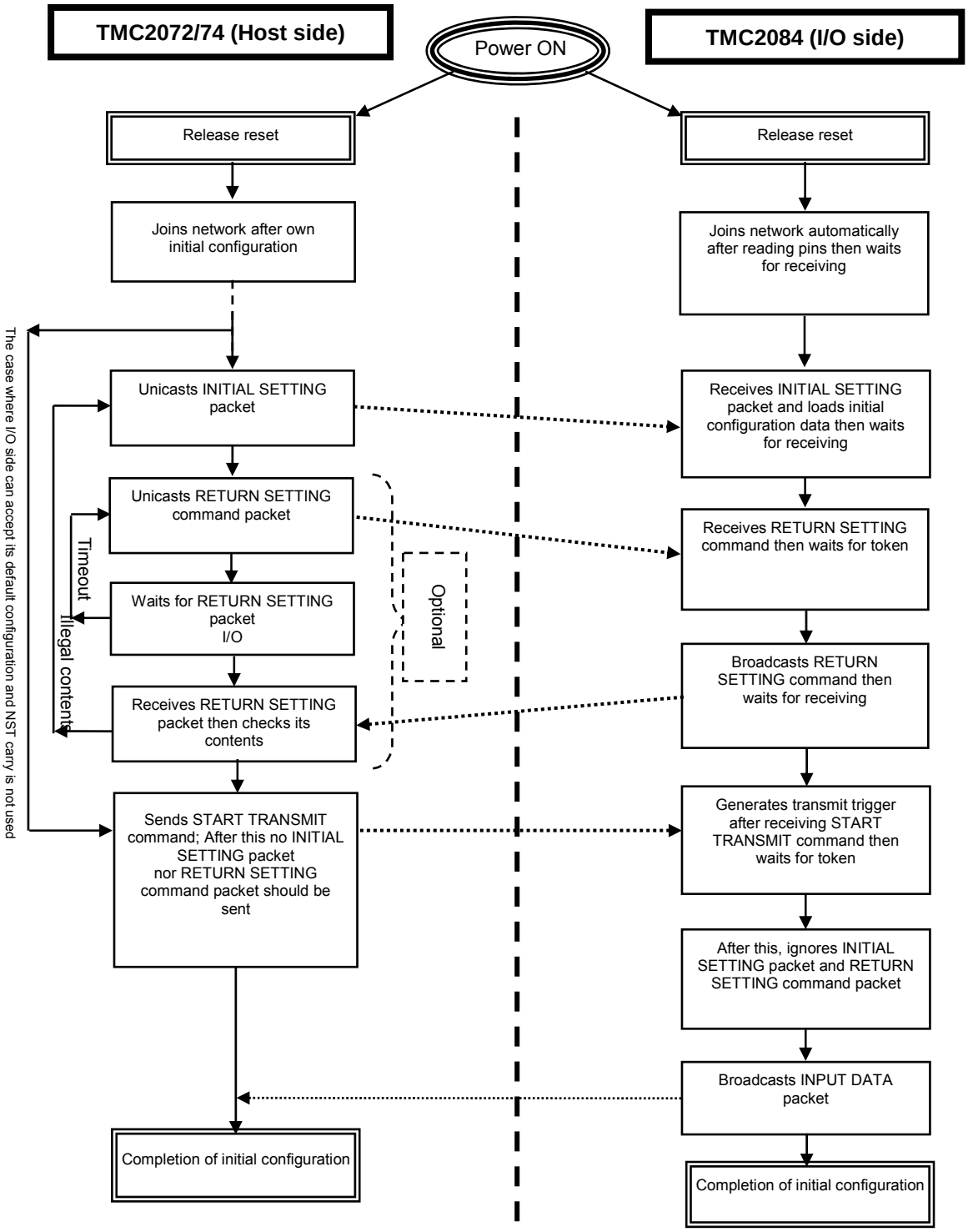


Figure 9 - Initialization Procedure

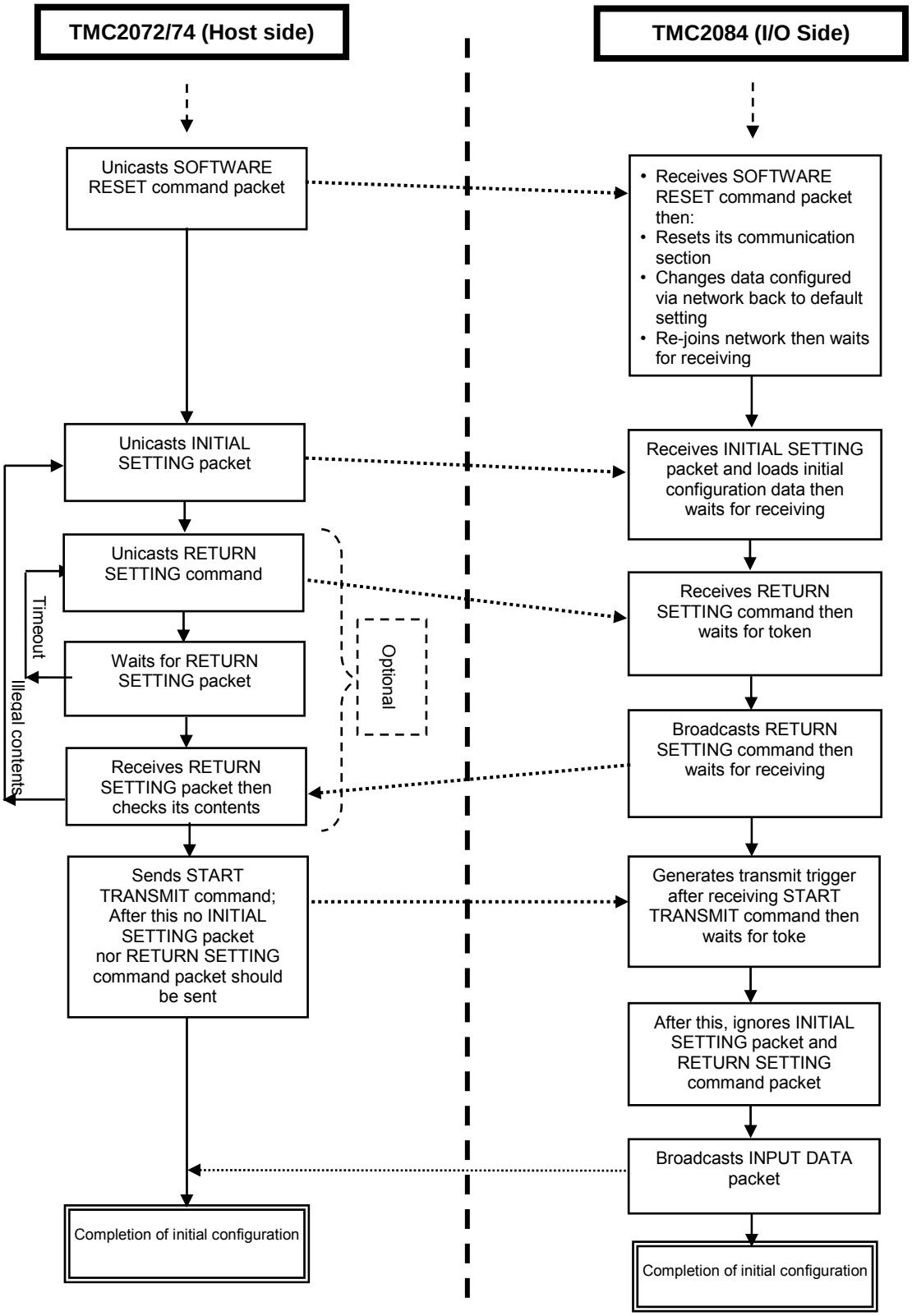


Figure 10 - Procedure to change the configuration through the network during operation

Chapter 3 Operating Conditions

3.1 Absolute Maximum Ratings

(Vss = 0 V)

Parameter	Symbol	Rating	Unit
Supply Voltage	Vdd	–0.3 to +5.0	V
Input Voltage (X1 pin)	Vin	–0.3 to Vdd +0.3	V
Input Voltage (except X1 pin)	Vin	–0.3 to +7.0	V
Output Voltage	Vout	–0.3 to Vdd +0.3	V
Input Current	Iin	±10	mA
Maximum Power Dissipation	Pd (MAX)	350	mW
Average Power Dissipation Note	Pd (AVE)	200	mW
Storage Temperature	Tstg	–40 to +125	°C

NOTE: Pd (AVE) is average per a day.

3.2 Typical Operating Conditions

(Vss = 0 V)

Parameter	Symbol	Rating	Unit
Supply Voltage	Vdd	3.0 to 3.6	V
Operating Ambient temperature	Ta	0 to +70	°C
Input Voltage (except X1 pin)	Vin	–0.3 to +5.5	V
Input Rising or Falling time Note	dt/dV	0 to 5	ns/V
Input Clock Frequency	fX1	25 to 40	MHz
Input Clock Frequency Tolerance	ΔfX1	±100	ppm

NOTE: dt/dV applies to pins nPISTR1, nPISTR2, RXIN and X1 (configured for the external clock input).

3.3 DC Characteristics

Symbol	Parameter	Buffer Type	Conditions	Min	Typ	Max	Unit
V_{IH1}	High Level Input Voltage	IT		2.2			V
	(TTL Level)						
V_{IL1}	Low Level Input Voltage	IT				0.8	V
	(TTL Level)						
V_{IH2}	High Level Input Voltage	IC		0.8 X Vdd			V
	(CMOS Level)	ICS		0.8 X Vdd			
V_{IL2}	Low Level Input Voltage	IC				0.2 X Vdd	V
	(CMOS Level)	ICS				0.2 X Vdd	

Symbol	Parameter	Buffer Type	Conditions	Min	Typ	Max	Unit
I_{IH}	High Level Input Current	Common	Vin = Vdd	–10		10	µA
I_{IL}	Low Level Input Current	Except IT_PU	Vin = Vss	–10		10	µA
		IT_PU		–200		10	
I_{OZ}	Output Off State Leakage Current	Common	Vout = Vdd or Vss	–10		10	µA
V_{HY}	Schmitt Trigger Hysteresis Voltage	ICS			1.0		V
V_{OH} Note	High Level Output Voltage	O42	I_{OH} = -1mA	Vdd-0.5			V
			I_{OH} = -2mA	0.8 X Vdd			
V_{OL} Note	Low Level Output Voltage	O42/OD4	I_{OL} = 1mA			Vss + 0.5	V
			I_{OL} = 4mA			0.4	
I_{OHM} Note	Maximum High Level Output Current	O42	(absolute value)			2	mA
I_{OLM} Note	Maximum Low Level Output Current	O42/OD4				4.5	mA
I_{DD}	Operating Current (No Load)		f_{X1} = 20MHz		15		mA
			f_{X1} = 40MHz		25		

NOTE: Excludes X2 pin.

3.4 AC Characteristics

3.4.1 Timing Measurement Points

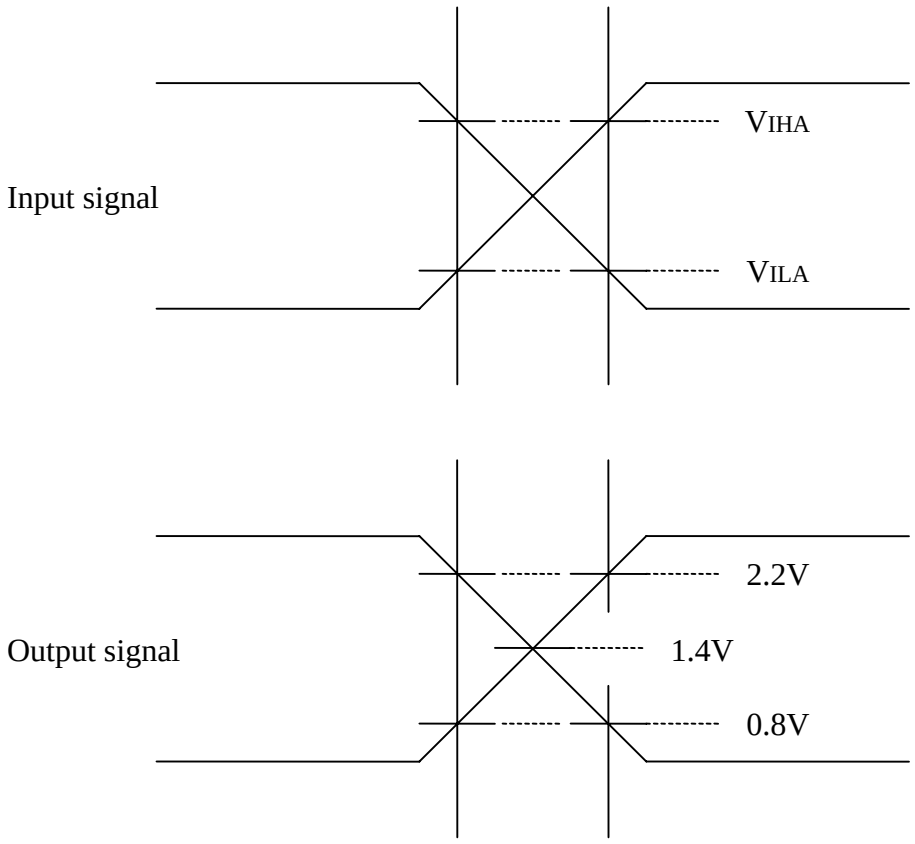


Figure 11 - Input Signal Measurement Points

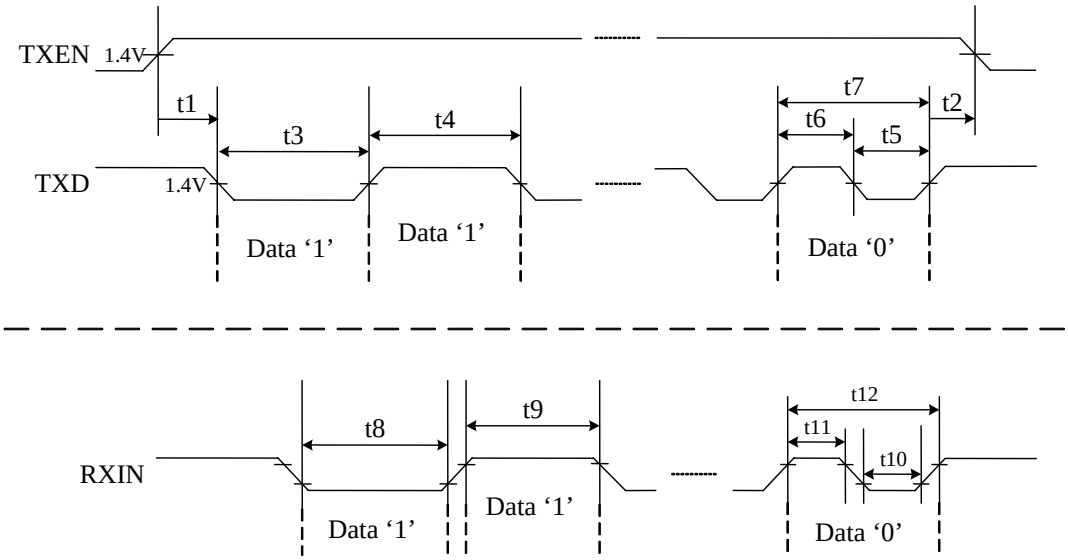
Buffer type:

IC : V_{IHA} = 0.8 X Vdd , V_{ILA} = 0.2 X Vdd (X1)

ICS : VI_{IHA}= 0.8 X Vdd , V_{ILA} = 0.2 X Vdd (nRESET)

IT : V_{IHA} = 2.2V, V_{ILA} = 0.8V (excluding both nRESET and X1)

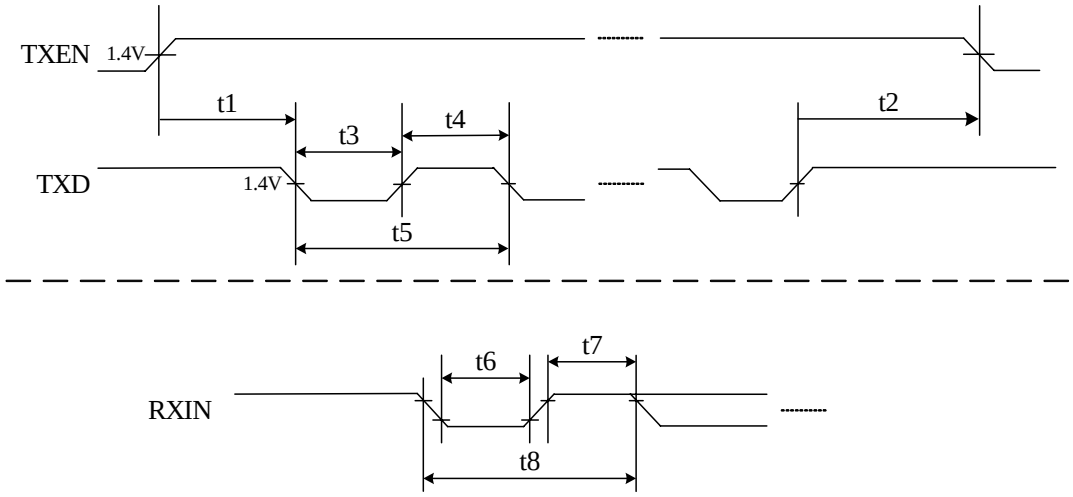
3.4.2 CMI Transmit And Receive Waveforms (nCMIBYP = H)



Symbol	Parameter	MIN	TYP	MAX	Unit	Comments
t1	TXEN Active to First TXD Low	2Tdr - 40	2Tdr		ns	Note 1
t2	Last TXD High to TXEN Inactive	3Trd / 8 - 40	3Tdr / 8		ns	Note 1
t3	Data ' 1 : Low Level Width of TXD		Tdr		ns	Note 1
t4	Data ' 1 ' : High Level Width of TXD		Tdr		ns	Note 1
t5	Data ' 0 ' : Low Level Width of TXD		Tdr / 2		ns	Note 1
t6	Data ' 0 ' : High Level Width of TXD		Tdr / 2		ns	Note 1
t7	Data ' 0 ' : Period of TXD		Tdr		ns	Note 1
	Data ' 0 ' : Duty Ratio of TXD		1 / 2			
t8	Data ' 1 ': Low Level Width of RXIN	7Tdr / 8	Tdr	9Tdr / 8	ns	Note 1
t9	Data ' 1 ' : High Level Width of RXIN	7Tdr / 8	Tdr	9Tdr / 8	ns	Note 1
t10	Data ' 0 ' : Low Level Width of RXIN	3Tdr / 8	Tdr / 2	5Tdr / 8	ns	Note 1
t11	Data ' 0 ' : High Level Width of RXIN	3Tdr / 8	Tdr / 2	5Tdr / 8	ns	Note 1
t12	Data ' 0 ' : Period of RXIN	7Tdr / 8	Tdr	9Tdr / 8	ns	Note 1
	Data ' 0 ' : Duty Ratio of RXIN	3 / 8	1 / 2	5 / 8		

Note 1: Tdr represents the period of communication rate (transmission rate). (2.5 Mbps: Tdr = 400 ns)

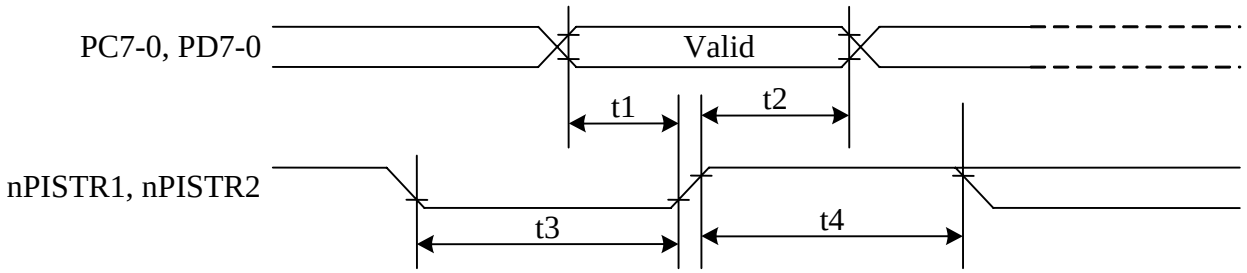
3.4.3 RZ Transmit And Receive Waveforms (nCMIBYP = L)



Symbol	Parameter	MIN	TYP	MAX	Unit	Comments
t1	TXEN Active to First TXD Low	7Tdr / 4 to 40	7Tdr / 4		ns	Note 1
t2	Last TXD High to TXEN Inactive	3Trd / 4 to 40	3Tdr / 4		ns	Note 1
t3	Low Level Width of TXD		Tdr / 2		ns	Note 1
t4	High Level Width of TXD		Tdr / 2		ns	Note 1
t5	Period of TXD		Tdr		ns	Note 1
t6	Low Level Width of RXIN	20	Tdr / 2		ns	Note 1
t7	High Level Width of RXIN	20	Tdr / 2		ns	Note 1
t8	Period of RXIN	3Tdr / 4	Tdr	5Tdr / 4	ns	Note 1

Note 1: Tdr represents the period of communication rate (transmission rate). (2.5 Mbps: Tdr = 400 ns)

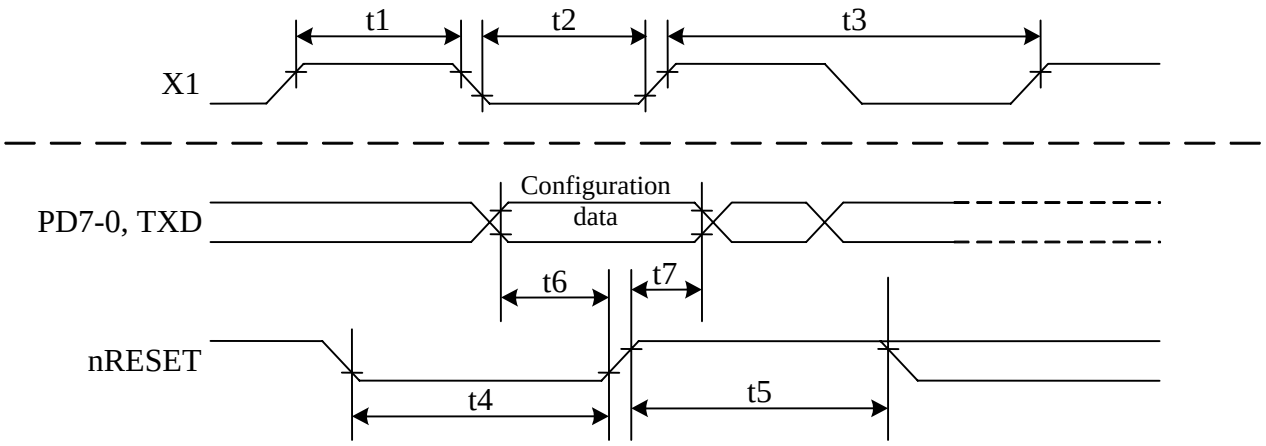
3.4.4 External Trigger Input



Symbol	Parameter	MIN	TYP	MAX	Unit	Comments
t1	Setup Time Of Data (Referenced to rising edge of nPISTR1 or nPISTR2)	30			ns	Note1
t2	Hold Time Of Data (Referenced to rising edge of nPISTR1 or nPISTR2)	30			ns	Note1
t3	Active Period Of nPISTR1 or nPISTR2	50			ns	
t4	Inactive Period Of nPISTR1 or nPISTR2	50			ns	

NOTE 1: When the transmit trigger is configured as the external trigger (TXTRG = 6 or 7), this applies to the timing to capture the transmit data.

3.4.5 Other Timing Specifications



Symbol	Parameter	MIN	TYP	MAX	Unit	Comments
t1	Clock High Level Width (External Clock)	10			ns	
t2	Clock Low Level Width (External Clock)	10			ns	
t3	Clock Period (External Clock)	25		400	ns	
f3	Clock Frequency (External Clock)	2.5		40	MHz	
t3x	Clock Period (Crystal Resonator)	31.25		100	ns	Note 1
f3x	Clock Frequency (Crystal Resonator)	10		32	MHz	Note 1
∆f3	Clock Frequency Tolerance	–100		+100	PPM	
t4	nRESET Low Level Width	6Tx			ns	Note 2, Note 3
t5	nRESET High Level Width	3Tx			ns	Note 2, Note 3
t6	Data Setup Time (Referenced To Rising Edge Of nRESET)	30			ns	Note 4
t7	Data Hold Time (Referenced To Rising Edge Of nRESET)	5			ns	Note 4

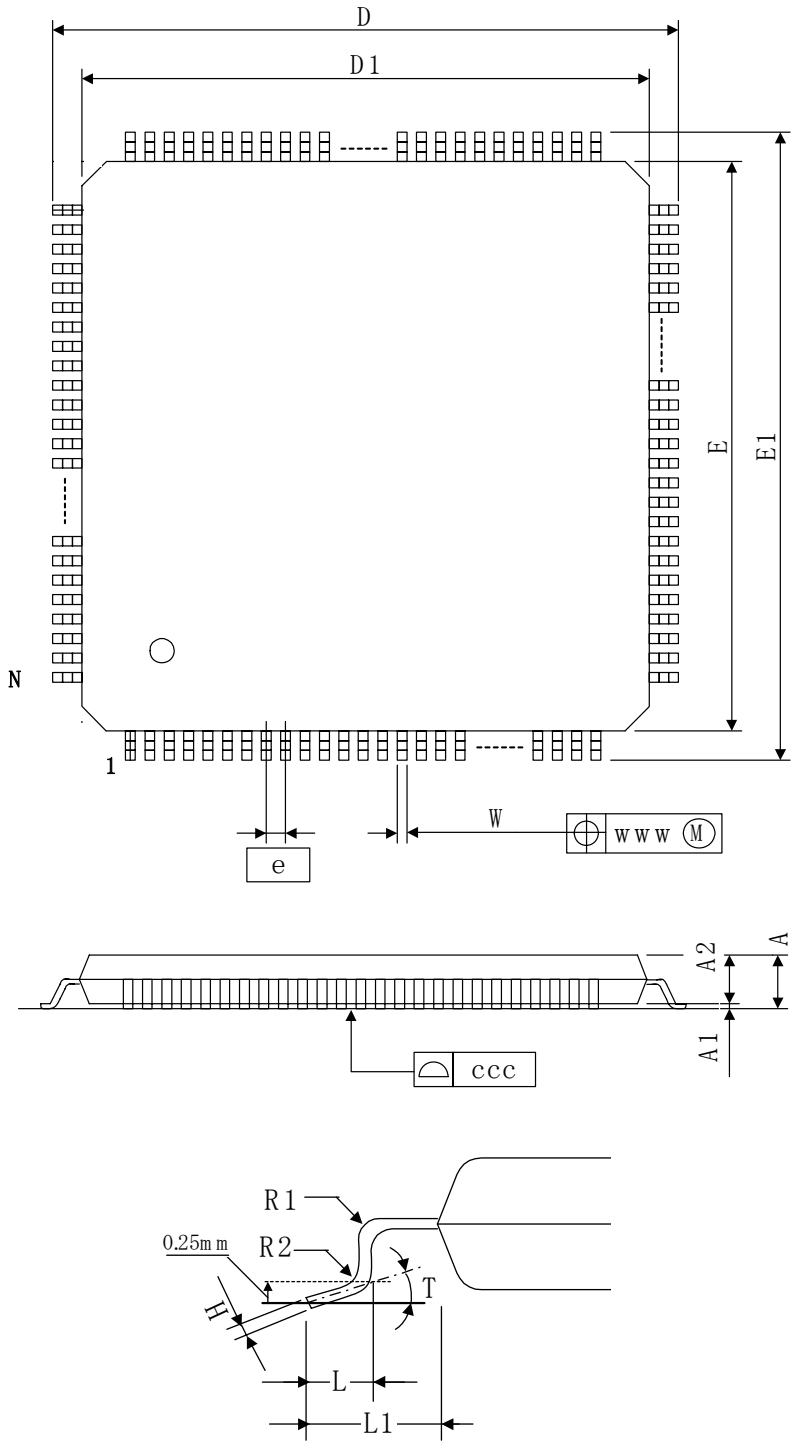
Note 1: For oscillator circuit component values, see the section 3.7 Oscillator Circuit.

Note 2: Tx represents the clock period that is applied to X1. (Tx = 50 ns @20 MHz)

Note 3: This applies to the stable crystal oscillator after the power supply voltage exceeds Vdd (min). Vdd (min) = 3.0 V for TMC2084.

Note 4: This specifies the read timing of shared pins.

3.5 Package Outline



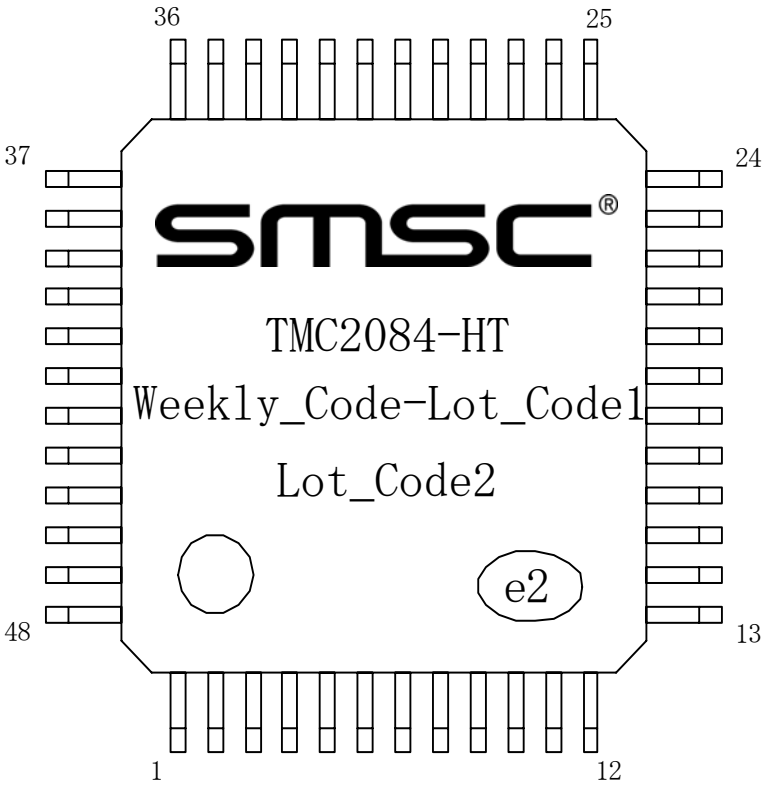
TMC2084 OUTLINE				
SYMBOL	**ITEMS**	**MIN**	**TYP**	**MAX**
A	Overall Package Height	-	-	1.6
A1	Standoff	0.05	-	0.15
A2	Body Thickness	1.35	-	1.45
D	X Span	8.8	-	9.2
D1	X body Size	6.9	-	7.1
E	Y Span	8.8	-	9.2
E1	Y body Size	6.9	-	7.1
H	Lead Frame Thickness	0.09	-	0.2
L	Lead Foot Length	0.45	0.6	0.75
L1	Lead Length	-	1.0	-
e	Lead Pitch	0.5 Basic		
T	Lead Foot Angle	0°	-	7°
W	Lead Width	0.17	0.22	0.27
www	Lead position Tolerance	-0.04	-	0.04
R1	Lead Shoulder Radius	0.08	-	-
R2	Lead Foot Radius	0.08	-	0.2
ccc	Coplanarity	-	-	0.08
N	Pin count	48		

NOTES:

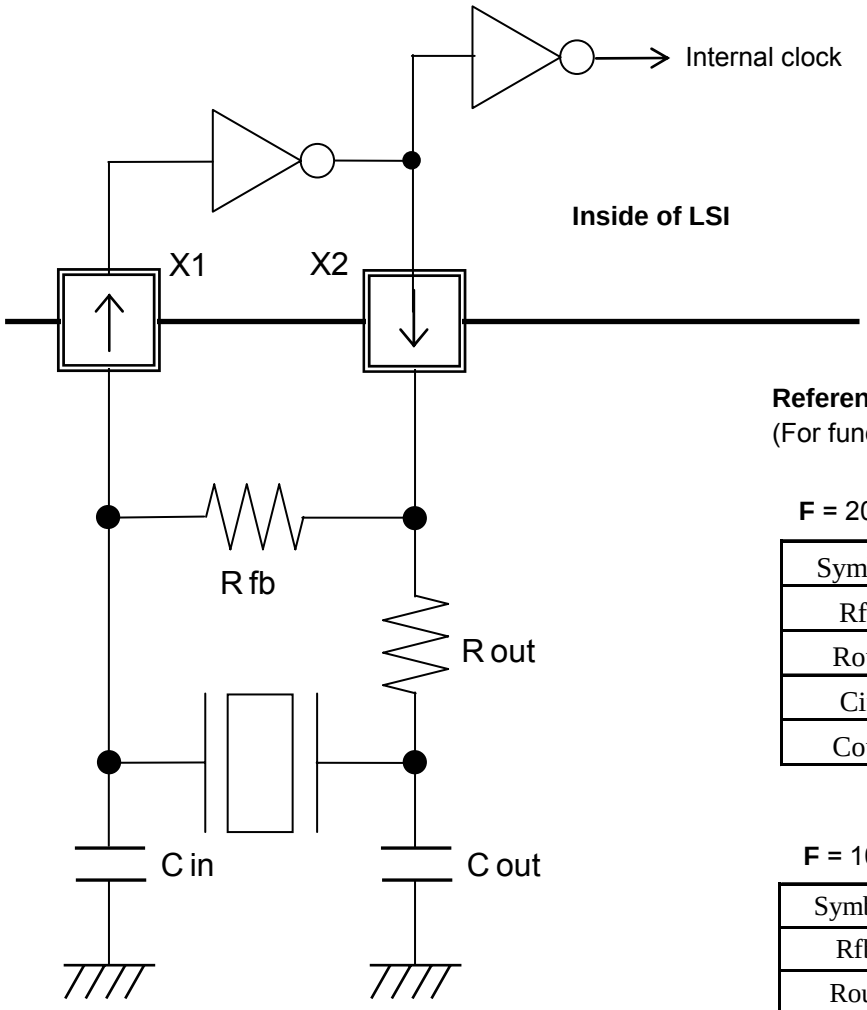
1) Controlling Unit: millimeter.
2) Package body dimensions D1 and E1 do not include the mold protrusion.
   Maximum mold protrusion is 0.25 mm.

3.6 Device Marking

NOTE: The character style may be slightly different from that of actual devices.



3.7 Oscillator Circuit



Reference Values
(For fundamental tone)

F = 20 to 32 MHz

Symbol	Reference Value
Rfb	51 Kohm
Rout	51 Ohm
Cin	22 pF
Cout	22 pF

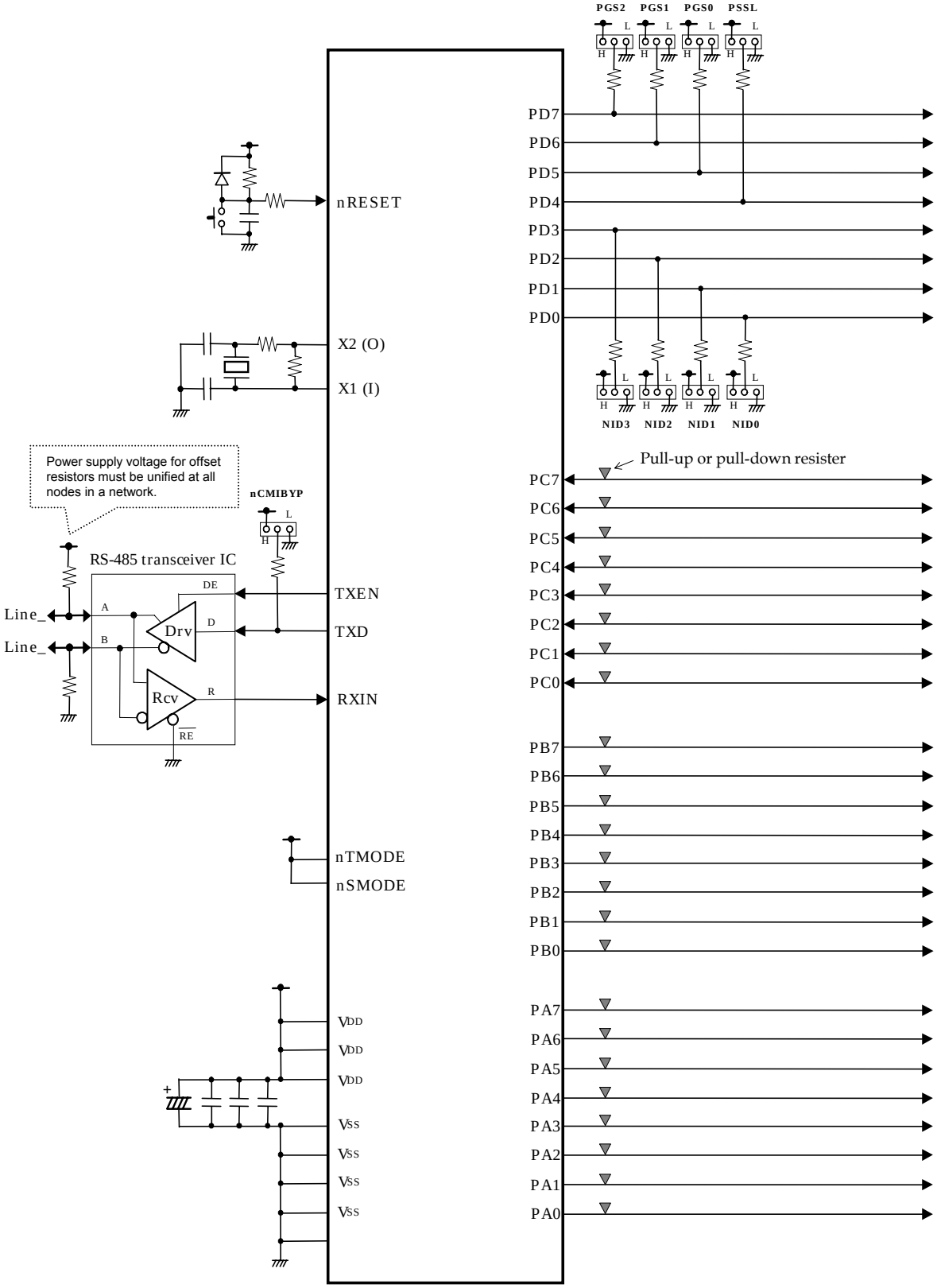
F = 10 MHz

Symbol	Reference Value
Rfb	51 Kohm
Rout	51 Ohm
Cin	22 pF
Cout	22 pF

[CAUTION]

Above R, C values may not be correct for a crystal you select. You may have to determine the correct values. If you use an overtone type crystal, follow the manufacturer's recommendations for connection details.

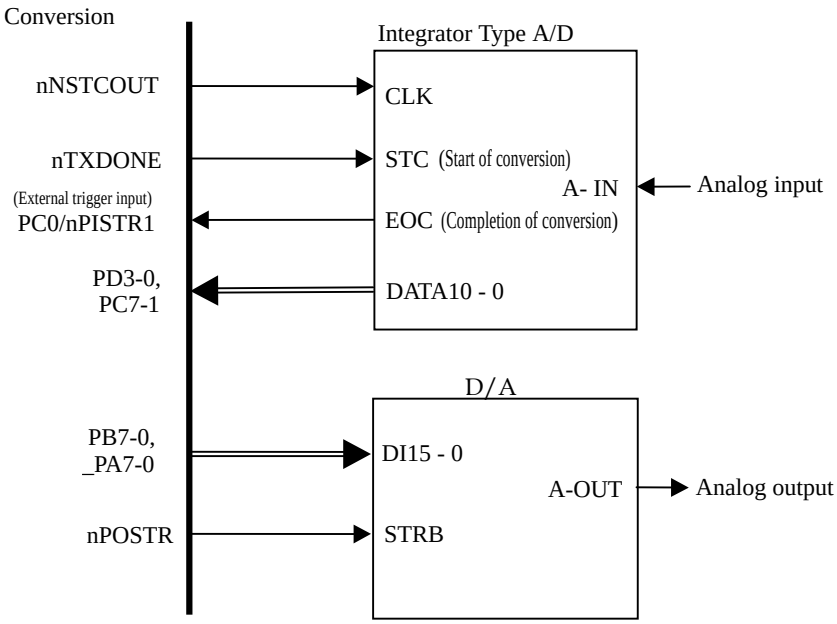
3.8 Basic Device Connections



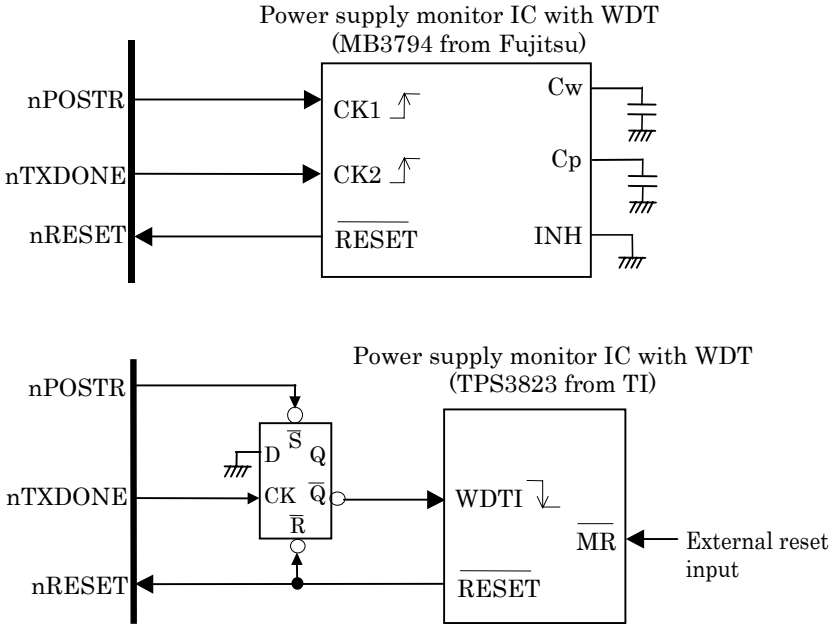
Chapter 4 APPENDIX

4.1 Application Circuit Examples

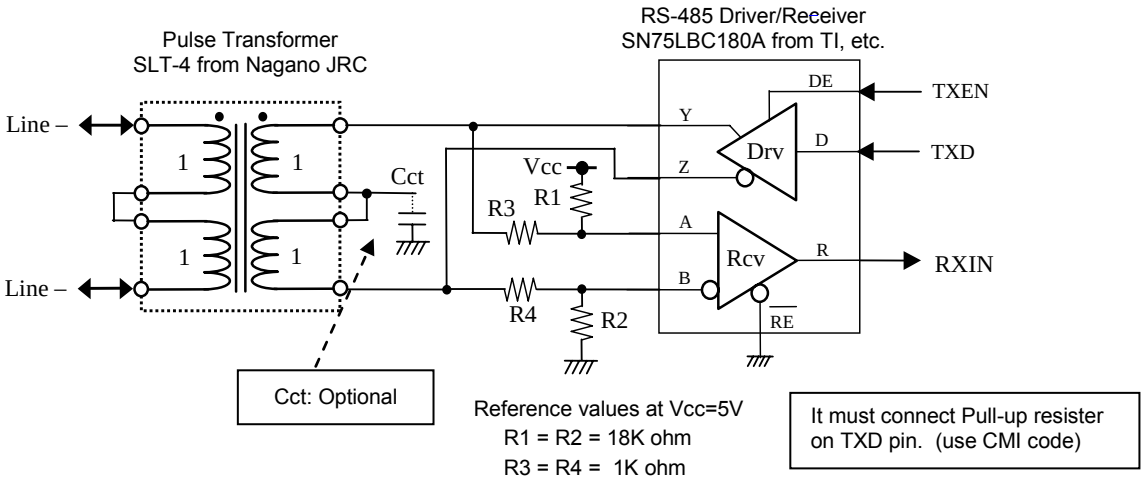
4.1.1 Connecting A/D and D/A



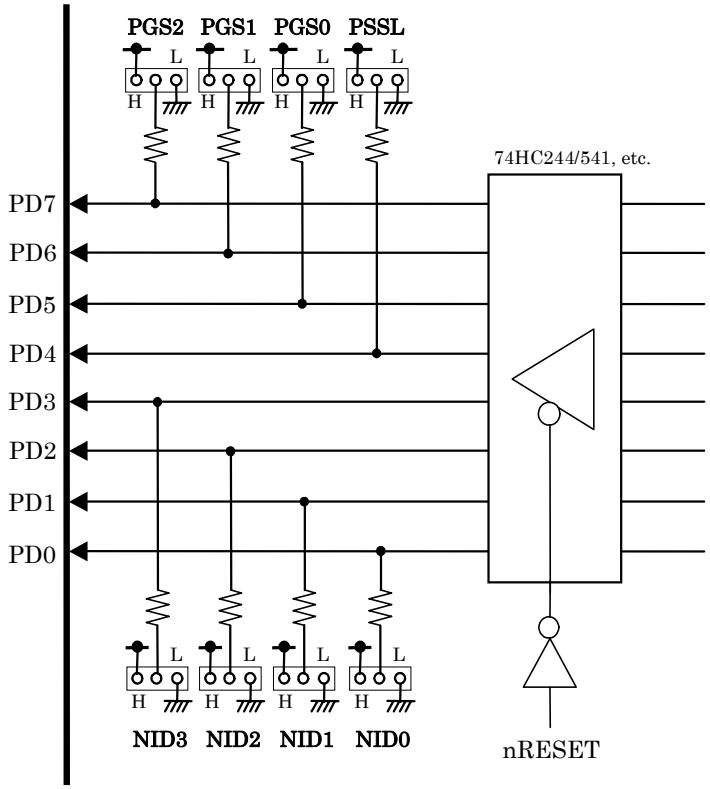
4.1.2 Connecting Watchdog Timer



4.1.3 Using SLT4 Plus RS485

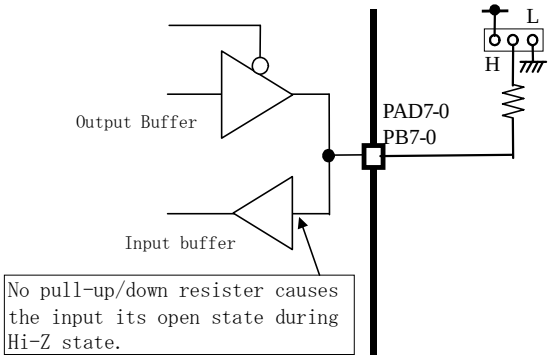


4.1.4 Considerations for Shared Pins When Port D is Configured as INPUT PORT

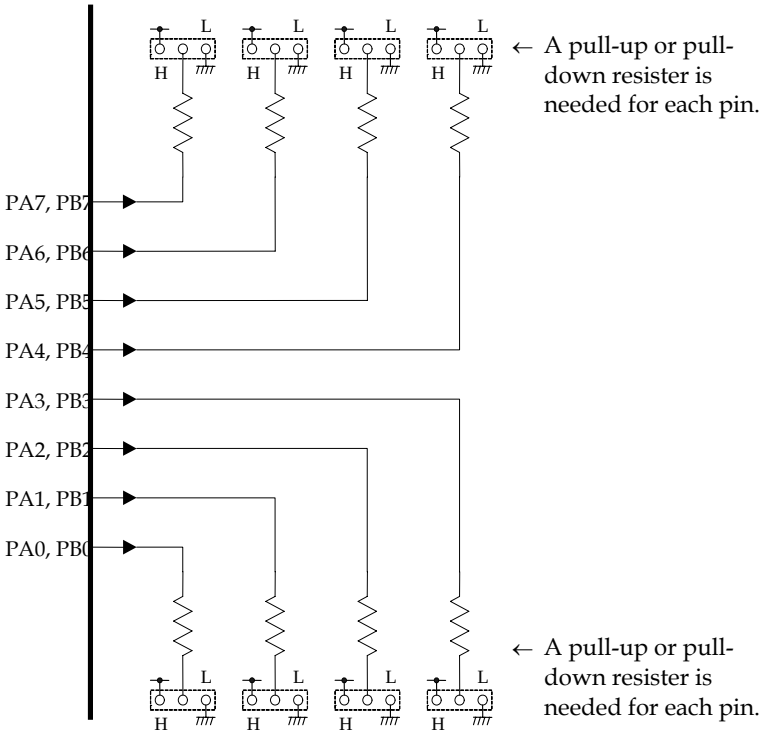


4.1.5 Case Where Port A and B are Unused

Although both port A (PA7 - 0) and port B (PB7 - 0) are output-only ports, input buffers exist to send (feedback) the states of the OUTPUT PORT to the host node. The OUTPUT PORT remains in its high-impedance (floating) state during both reset (nRESET = Low) and the period from de-assertion of reset (nRESET = High) to the first OUTPUT DATA packet received. Thus, the input node of the input buffer may be placed in the open state (undefined) during the high-impedance state. This can cause a punch-through current through the input buffer. To avoid this, either a pull-up or a pull-down resister should be added externally to each pin of both ports A and B so that each added resister can define the input sate of the corresponding input buffer during the high-impedance state.

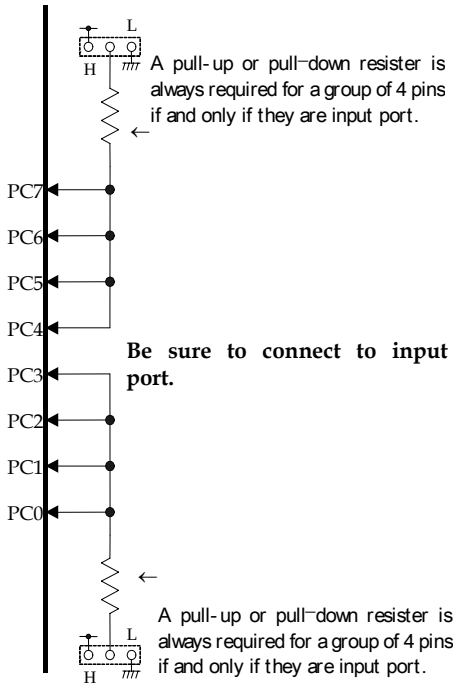


Either a pull-up or a pull-down resister is required externally connected to each pin of both unused ports A and B as described above.



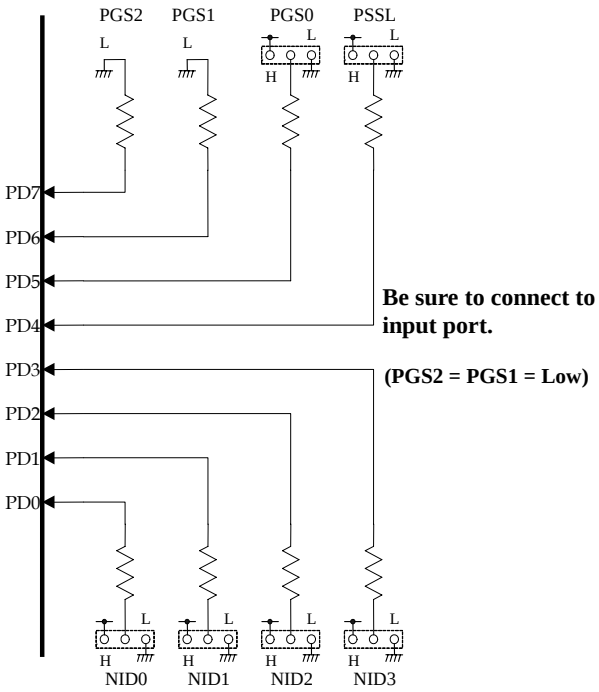
4.1.6 Case Where Port C is Unused

When the port C (PC7 - 0) is unused, its I/O port direction bits (PGS2 - 0) must be configured so that they specify **INPUT PORT** and either a pull-up or pull-down resister should be added externally to each pin of the INPUT PORT to define the state of the corresponding pin as shown below:



4.1.7 Case Where Port D is Unused

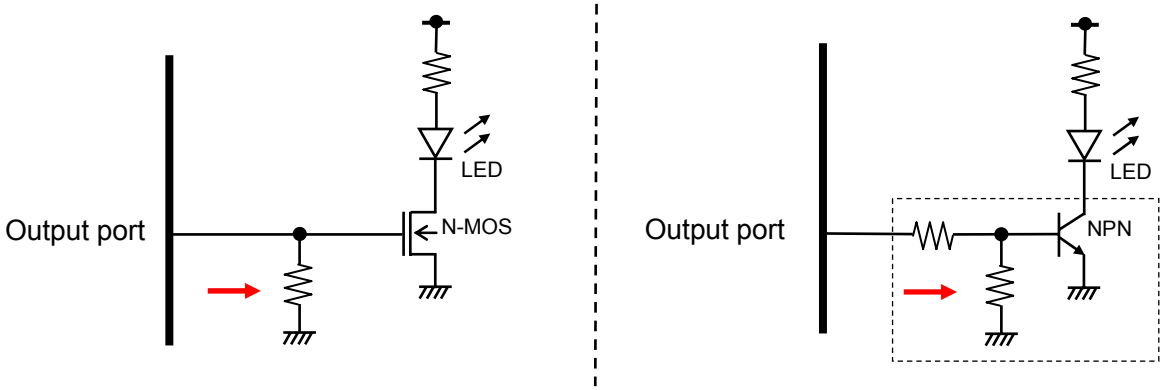
When port D (PD7 - 0) is unused, its I/O port direction bits (PGS2 - 0) must be configured so that they specify **INPUT PORT** and either a pull-up or a pull-down resister should be added externally to each pin of the INPUT PORT to define the state of the corresponding pin as shown below:



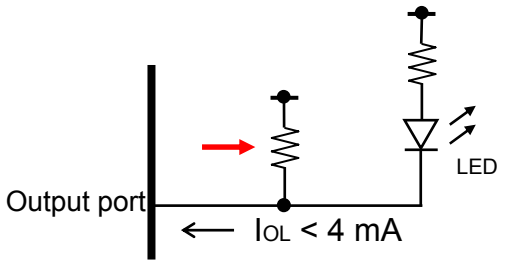
4.1.8 Initial Configuration for OUTPUT PORT (LED Display Example)

The initial state of OUTPUT PORT is high-impedance (floating) state. It remains in its high-impedance (floating) state during both reset (nRESET = Low) and the period from de-assertion of reset (nRESET = High) to the first OUTPUT DATA packet received. To avoid this, either a pull-up or a pull-down resister should be added externally to each pin of the OUTPUT PORT to ensure the inactive sate of the corresponding pin during the high-impedance state.

* If the low level causes inactive state (LED turns off), an external pull-down resister is required.



* If the high level causes inactive state (LED turns off), an external pull-up resister is required.



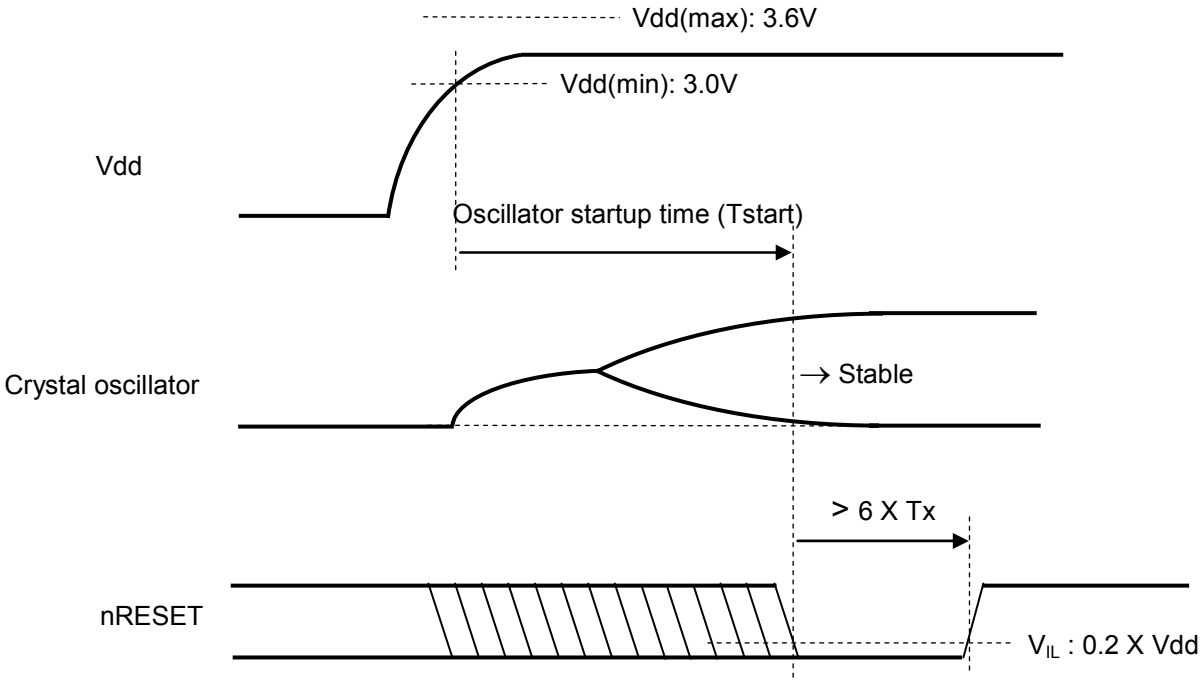
4.1.9 Width of Reset Signal

In an actual operating environment, the following considerations are needed for the width of the reset signal that is applied to the nRESET pin:

Oscillator Startup Time at Power-up (Tstart)

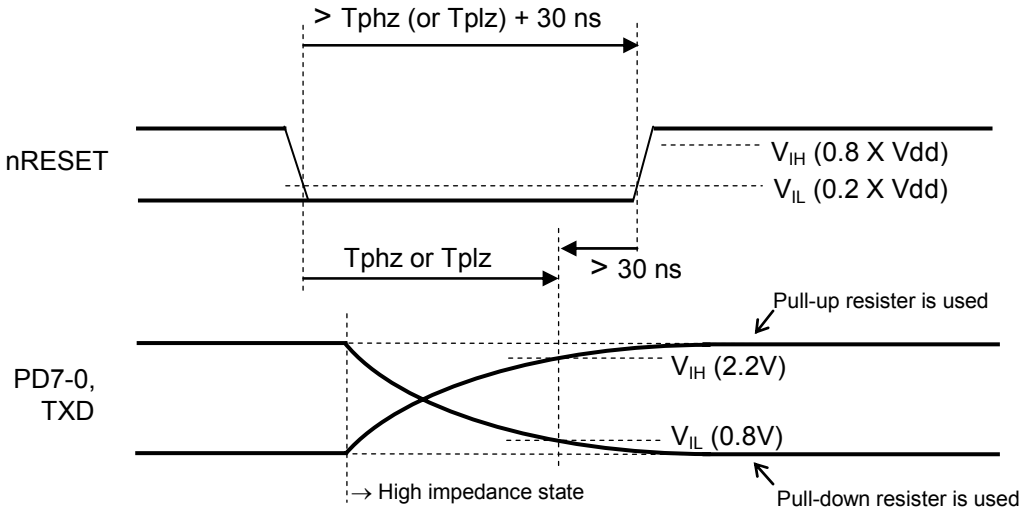
The oscillator startup time (Tstart) is required for the crystal oscillator to stabilize. The startup time is required for TMC2084 regardless of whether a crystal oscillator or an external clock is used. After the oscillator startup time, the input clock to X1 pin becomes normal (after approximately 20 ms).

The reset signal must stay low longer than 6(Tx) is required after Tstart.



Output Stabilization Time for Shared Pins (Tphz and Tplz)

The low level on reset input pin (nRESET) sets the high-impedance state for shared pins (PD7 - 0 and TXD). Since each pin has either a pull-up or a pull-down resister, it stabilizes to high or low level after sufficient time. The length of stabilization time (Tphz and Tplz) depends on the resister value connected. Therefore, the duration of reset signal must be longer than Tphz + Tplz + setup time (30 ns).



4.2 Output Current from Shared Pins

The output current from the PD7/nRCNERR pin is specified as I_{OL} = 4 mA (Max). However, this pin should drain no current when it is used as the OUTPUT PORT pin (PD7) (PGS2 = Low). Otherwise, configuration by the shared pin can not be performed correctly.

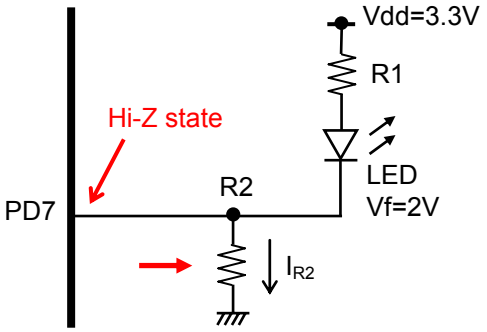
In the following example, the low level on PD7 pin turns on the LED; R1 limits LED current; and the pull-down resister R2 is used for configuration (PGS2 = Low) using the shared pin during reset. The voltage level on PD7 pin during the reset (PD7 is in high-impedance state) will be as follows:

Assuming Vdd = 3.3 V, Vf = 2 V, R1 = 330 Ω and R2 = 10 kΩ, the current (I_{R2}) flows in R1 and R2 from Vdd is:

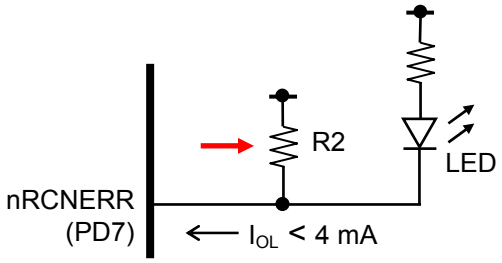
I_{R2} = (Vdd - Vf) ÷ (R1 + R2)

= (3.3 V - 2 V) ÷ (330 Ω + 10000 Ω) ≒ 126 μA.

Thus, the voltage level of PD7 pin during reset is I_{R2} × R2 = 126μA × 10 kΩ ≒ 1.3V and this exceeds the maximum low level input voltage 0.8V. This makes the configuration PGS2 = Low impossible.



The pull-up resister R2 in the figure below allows the configuration PGS2 = High correctly because no current flows through R2 during high-impedance state in reset phase. This enables LED to monitor the nRCNERR signal.



The same considerations are needed for other shared pins (PD6 - 0 and TXD). In the high-impedance state during reset, careful attention should be paid for the current and voltage caused by the pull-up and pull-down resisters.

4.3 Values of Pull-Up and Pull-Down Resisters

Care must be taken when selecting the values of the pull-up and pull-down resisters used for ports A, B, C and D and shared pins (PD7 - 0 and TXD):

Higher resistance values result in longer stabilization time for the transition from the active state to the high-impedance state. Shorter stabilization time follows from use of less resistance. However, lower resistance allows a higher output current in the drive state and wastes output current, limiting the necessary load current.

As a guideline, a 10 kΩ resister can typically be used; If shorter transition time from the active state to the high-impedance state is needed, use 4.7 kΩ.

Table 4 - CircLink Controller Comparison Table

ITEMS	CircLink		
	TMC2072	TMC2074	TMC2084
* Common			
Power supply voltage	3.3V +/-0.3V 5V tolerant I/O	3.3V +/-0.3V 5V tolerant I/O	3.3V +/-0.3V 5V tolerant I/O
Temperature range	0 to +70C	0 to +70C	0 to +70C
Package	TQFP-100 pin 14x14x1.4mm Body 0.5mm Pitch	VTQFP-128 pin 14x14x1.0mm Body 0.4mm Pitch	TQFP-48 pin 7x7x1.4mm Body 0.5mm Pitch
Maximum Data Rate	5 Mbps	5 Mbps	5 Mbps
HUB function	External 2 ports	External 2 ports	none
Transmission code	CMI / RZ code	CMI / RZ code	CMI / RZ code
TXEN polarity setting	Pin setting	Pin setting	Active-High Only
NodeID, MaxID, PageSize setting	Pin / Bit setting	Pin / Bit setting	Shared Pins
Data Rate Prescaler setting	Pin / Bit setting	Pin / Bit setting	none
Page-Size	32/64/128/256 bytes	32/64/128/256 bytes	64/128 bytes
Max. Node count	31/15/7/3 nodes	31/15/7/3 nodes	15/7 nodes
Operation Mode	Peripheral mode Only	Peripheral/Standalone mode	Standalone mode Only
* Peripheral Mode (With CPU mode)			
Internal RAM size	1 kBytes	1 kBytes	-
Data Bus width	8/16 bit	8/16 bit	-
Support CPU	CPU Type: nRD&nWR/DIR&nDS Bus Type: MUX/Non-MUX	CPU Type: nRD&nWR/DIR&nDS Bus Type: MUX/Non-MUX	- -
New Flag for Warning Timer	none	none	-
General Purpose-I/O	8 bit	8 bit	-
* Standalone Mode (No CPU control mode)			
Number of I/O Port	-	IN : 16 OUT : 16	IN : 0/ 8/16 OUT : 32/24/16
Variable Settings by	-	Pins	Shared Pins and a Packet
Tx Trigger	-	7 kinds	10 kinds
Receive Broadcast	-	No	Yes
Send Status	-	No	Yes
Anti-Chatter Sampling Freq.	-	2.44 kHz	1.22 kHz/19.1 Hz