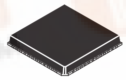


HDMI HIDER

FEATURES

- Supports 2.25 Gbps Signaling Rate for 480i/p, 720i/p, and 1080i/p Resolution to 12-Bit Color Depth
- Compatible with HDMI 1.3a
- Integrated Receiver Termination
- 8-dB Equalizer Compensates Losses from 5-m or Longer HDMI Cables
- Selectable Output De-Emphasis Supports 1-m HDMI Transmission
- I²C Repeater Isolates Bus Capacitance at Both Ends
- High Impedance Outputs When Disabled
- TMDS Inputs HBM ESD Protection Exceeds 6 kV
- 3.3-V Supply Operation
- 40-Pin QFN Package (RHA)
- ROHS Compatible and 260°C Reflow Rated

APPLICATIONS

- Digital TV
- DVD Player
- Set-Top-Box
- Audio Video Receiver
- Digital Projector
- DVI or HDMI cable

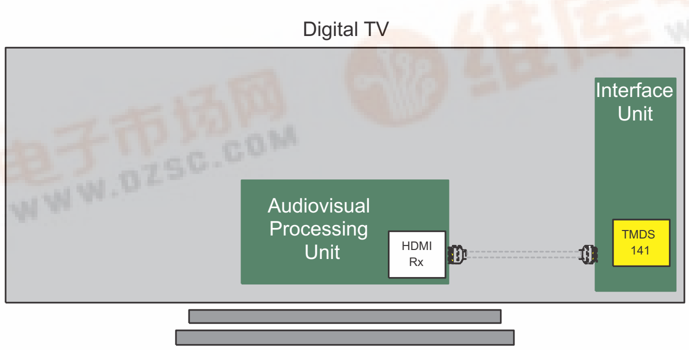
DESCRIPTION

The TMDS141 HDMI hider is designed to accommodate a 1-m HDMI cable between a HDMI connector and a receiver. The internal cable causes signal distortion to high-speed TMDS signals, as well as increasing capacitance to the DDC channel. Each TMDS141 contains four TMDS repeaters to transmit digital content with signaling rates of up to 2.25-Gbps, and an I²C repeater to link extended display identification data (EDID) reading and high-bandwidth digital content protection (HDCP) key exchange under I²C standard mode operations.

The device includes four TMDS compliant differential receivers with 50-Ω termination resistors and 3.3-V termination voltage integrated at each receiver input pin. External terminations are not required. A built-in frequency response equalization circuit, 8 dB at 825 MHz, compensates inter-symbol interference (ISI) losses from a 5-m or longer input cable link.

The device also includes four TMDS compliant differential drivers. A precision resistor is connected externally from the VSADJ pin to ground for setting the differential output voltage to be compliant with the TMDS standard. A selectable de-emphasis circuit is available via the PRE input to drive long PCB traces or cables. When PRE is high, the 3.5-dB high frequency gain offsets the losses due to the FR4 trace. PRE can be left open or kept low when the de-emphasis function is not desired.

TYPICAL APPLICATION

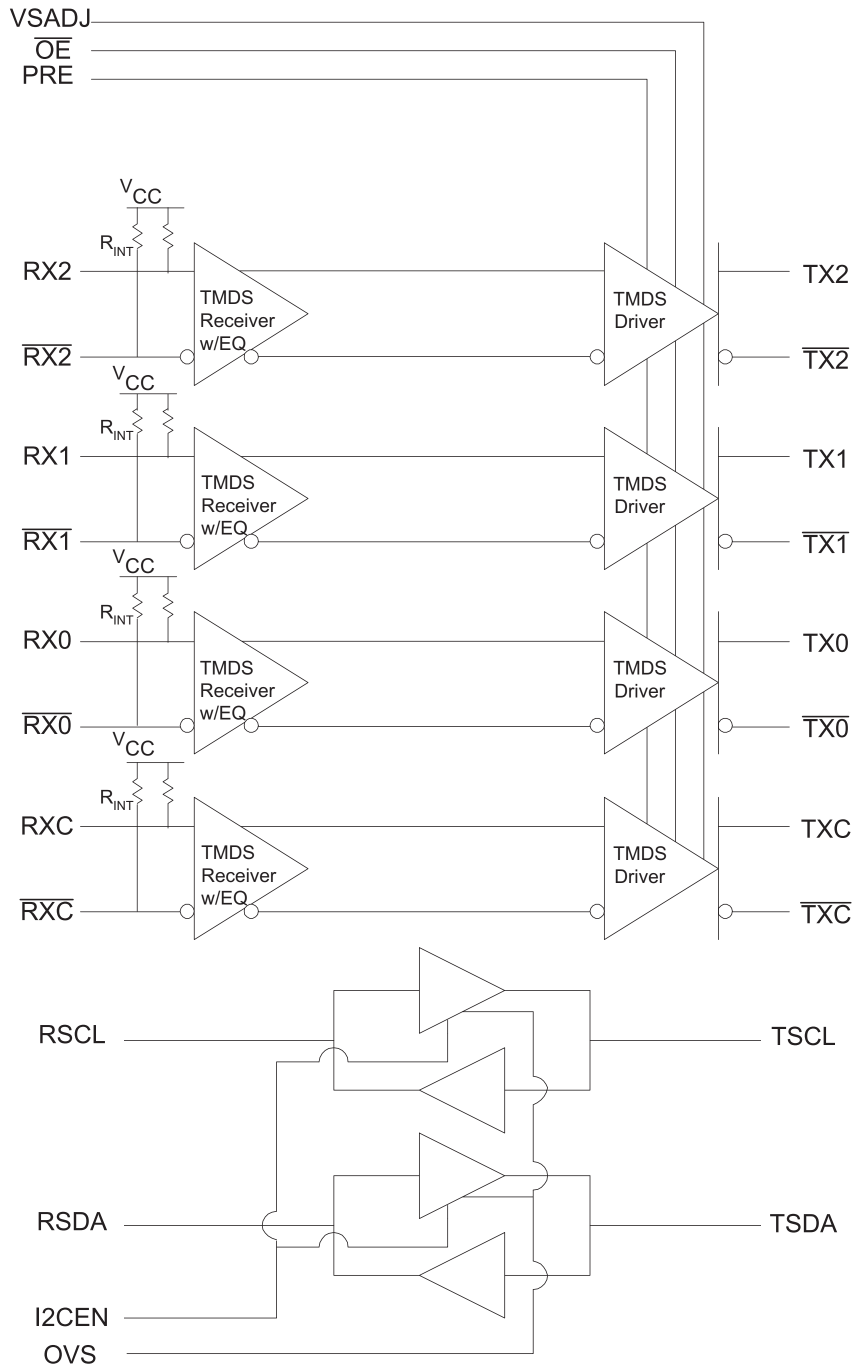


Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

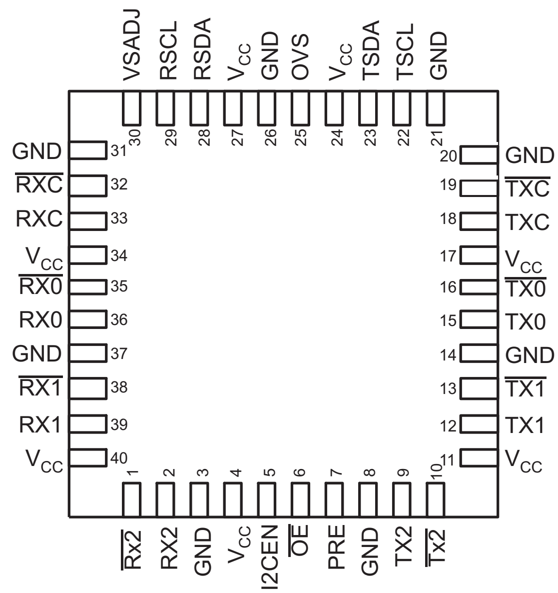
With standard TMDS terminations at the outputs, all TMDS outputs are forced high-impedance when $\overline{OE}$ is set high. The I^2C repeater isolates the buses without accumulating the capacitance of both sides. It allows DDC capacitance to be controlled under the desired load. The I^2C outputs are high-impedance when device supply voltage is less than 1.5 V or I2CEN is low. The OVS pin, output voltage select, provides the flexibility of adjusting the output voltage level of the TSCL and TSDA side to optimize noise margins while interfacing to different HDMI receivers. The device is characterized for operation from 0°C to 70°C.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

FUNCTIONAL BLOCK DIAGRAM



RHA PACKAGE
(TOP VIEW)

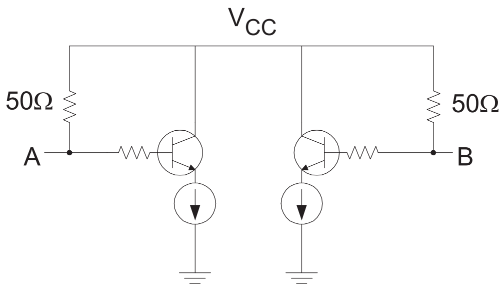


TERMINAL FUNCTIONS

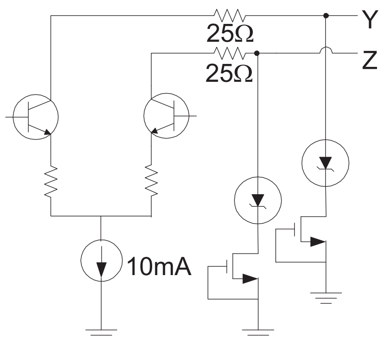
TERMINAL		I/O	DESCRIPTION
NAME	NO.		
$\overline{RX2}$, $\overline{RX1}$, $\overline{RX0}$, $\overline{RXC}$	1, 38, 35, 32	I	TMDS Negative inputs
RX2, RX1, RX0, RXC	2, 39, 36, 33	I	TMDS Positive inputs
$\overline{TX2}$, $\overline{TX1}$, $\overline{TX0}$, $\overline{TXC}$	10, 13, 16, 19	O	TMDS Negative outputs
TX2, TX1, TX0, TXC	9, 12, 15, 18	O	TMDS Positive outputs
RSCL	29	I/O	DDC Bus clock line to source
RSDA	28	I/O	DDC Bus data line to source
TSCL	22	I/O	DDC Bus clock line to sink
TSDA	23	I/O	DDC Bus data line to sink
VSADJ	30	I	TMDS Compliant voltage swing control
I2CEN	5	I	I^2C Repeater enable Low: High-Z High: Active
OVS	25	I	TSCL/TSDA Output voltage select
$\overline{OE}$	6	I	TMDS Output enable Low: Active High: High-Z
PRE	7	I	TMDS Output de-emphasis adjustment Low: 0 dB High: 3.5 dB
V_{CC}	4, 11, 17, 24, 27, 34, 40		Power supply
GND	3, 8, 14, 20, 21, 26, 31, 37		Ground

EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS

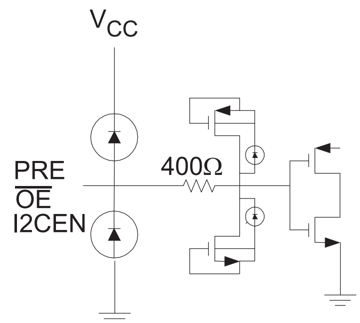
TMDS Input Stage



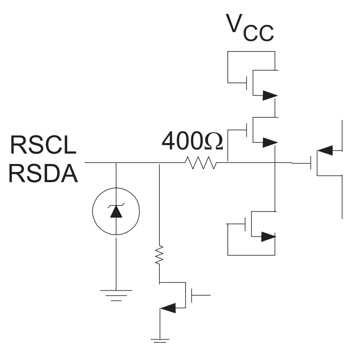
TMDS Output Stage



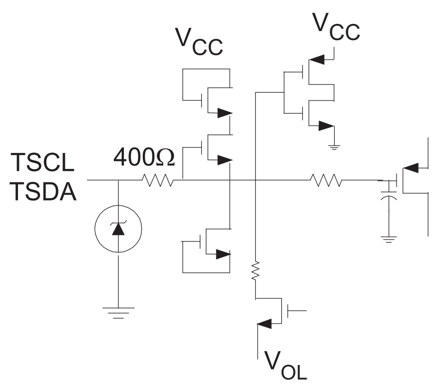
Control Input Stage



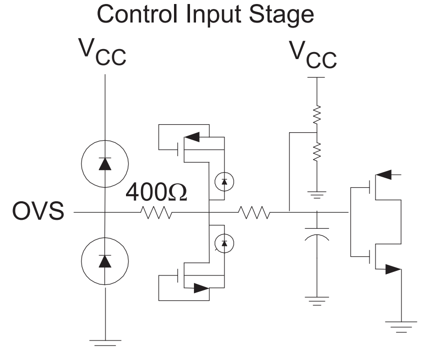
R-Side I2C Input/Output Stage



T-Side I2C Input/Output Stage



Control Input Stage



ORDERING INFORMATION(1)

PART NUMBER	PART MARKING	PACKAGE
TMDS141RHAR	TMDS141	40-PIN QFN Tape/Reel

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)[1]

				UNIT
V_{CC}	Supply voltage range[2]			–0.5 V to 4 V
	Voltage range	RX, $\overline{RX}$		2.0 V to 4 V
		TX, $\overline{TX}$, PRE, VSADJ, $\overline{OE}$, I2CEN, OVS, HPDn		–0.5V to 4 V
		RSCL, RSDA, TSCL, TSDA		–0.5 V to 6 V
	Electrostatic discharge	Human body model[3]	RX, $\overline{RX}$	±6 kV
			All pins	±4 kV
		Charged-device model[4] (all pins)		±1500 V
		Machine model [5] (all pins)		± 200 V
	Continuous power dissipation			See Dissipation Rating Table

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.
(3) Tested in accordance with JEDEC Standard 22, Test Method A114-B
(4) Tested in accordance with JEDEC Standard 22, Test Method C101-A
(5) Tested in accordance with JEDEC Standard 22, Test Method A115-A

DISSIPATION RATINGS

PACKAGE	PCB JEDEC STANDARD	$T_A \le 25°C$	DERATING FACTOR [1] ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
40-QFN RHA	Low-K[2]	839.7 mW	8.39 mW/°C	461.8 mW
40-QFN RHA	High-K[3]	3030.3 mW	30.3 mW/°C	1666.6mW

(1) This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.
(2) In accordance with the Low-K thermal metric definitions of EIA/JESD51-3
(3) In accordance with the High-K thermal metric definitions of EIA/JESD51-7

THERMAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$R_{\theta JB}$	Junction-to-board thermal resistance				30.96		°C/W
$R_{\theta JC}$	Junction- to-case thermal resistance				32.42		°C/W
P_D	Device power dissipation	$V_{IH} = V_{CC}$, $V_{IL} = V_{CC}$ - 0.5 V, $R_T = 50\ \Omega$, $V_{CC} = AV_{CC} = 3.3V$, $R_{vsadj} = 4.64\ k\Omega$	PRE = Low		344	370	mW
			PRE = High		381	407	
		$V_{IH} = V_{CC}$, $V_{IL} = V_{CC}$ - 0.6 V, $R_T = 50\ \Omega$, $V_{CC} = 3.6$ V, $AV_{CC} = 3.3V$, $R_{vsadj} = 4.6\ k\Omega$	PRE = Low			484	mW
			PRE = High			526	

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	3	3.3	3.6	V
T_A	Operating free-air temperature	0		70	°C
TMDS DIFFERENTIAL PINS (RX/ RXC)					
V_{IC}	Input common mode voltage	V_{CC}–400		V_{CC}+10	mV
V_{ID}	Receiver peak-to-peak differential input voltage	150		1560	mVp-p
R_{VSADJ}	Resistor for TMDS compliant voltage swing range	4.6	4.64	4.68	kΩ
AV_{CC}	TMDS Output termination voltage, see Figure 1	3	3.3	3.6	V
R_T	Termination resistance, see Figure 1	45	50	55	Ω
	Signaling rate	0		2.25	Gbps

RECOMMENDED OPERATING CONDITIONS (continued)

		MIN	NOM	MAX	UNIT
CONTROL PINS (PRE, $\overline{OE}$, I2CEN)					
V_{IH}	LVTTL High-level input voltage	2		V_{CC}	V
V_{IL}	LVTTL Low-level input voltage	GND		0.8	V
CONTROL PINS (OVS)					
V_{IH}	LVTTL High-level input voltage	3		3.6	V
V_{IL}	LVTTL Low-level input voltage	-0.5		0.5	V
I^2C PINS (TSCL, TSDA)					
V_{IH}	High-level input voltage	$0.7V_{CC}$		5.5	V
V_{IL}	Low-level input voltage	-0.5		$0.3V_{CC}$	V
V_{ICL}	Low-level input voltage contention (1)	-0.5		0.4	V
I^2C PINS (RSCL, RSDA)					
V_{IH}	High-level input voltage	2.1		5.5	V
V_{IL}	Low-level input voltage	-0.5		1.5	V

(1) V_{IL} specification is for the first low level seen by the SCL/SDA lines. V_{ICL} is for the second and subsequent low levels seen by the TSCL/TSDA lines.

ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP (1)	MAX	UNIT
I_{CC}	Supply current	$V_{IH} = V_{CC}$, $V_{IL} = V_{CC} – 0.4$ V, $R_T = 50\ \Omega$, $AV_{CC} = 3.3$ V, $R_{VSADJ} = 4.64\ k\Omega$, 1.65-Gbps HDMI data pattern, 165-MHz Pixel clock, PRE = Low		108	130 (2)	mA
P_D	Power dissipation	$V_{IH} = V_{CC}$, $V_{IL} = V_{CC} – 0.4$ V, $R_T = 50\ \Omega$, $AV_{CC} = 3.3$ V, $R_{VSADJ} = 4.64\ k\Omega$, 1.65-Gbps HDMI data pattern, 165-MHz Pixel clock, PRE = Low			497 (2)	mW
TMDS DIFFERENTIAL PINS (TX, TXC)						
V_{OH}	Single-ended high-level output voltage	See Figure 2, $AV_{CC} = 3.3$ V, $R_T = 50\ \Omega$	AV_{CC}–10		AV_{CC}+10	mV
V_{OL}	Single-ended low-level output voltage		AV_{CC}–600		AV_{CC}–400	mV
V_{swing}	Single-ended output swing voltage		400		600	mV
$V_{OD(O)}$	Overshoot of output differential voltage				15%	2× V_{swing}
$V_{OD(U)}$	Undershoot of output differential voltage				25%	2× V_{swing}
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage between logic states				5	mV
$I_{(O)OFF}$	Single-ended standby output current	$0\ V \le V_{CC} \le 1.5$ V, $AV_{CC} = 3.3$ V, $R_T = 50\ \Omega$	–10		10	µA
$V_{OD(pp)}$	Peak-to-peak output differential voltage	See Figure 3, PRE = High, $AV_{CC} = 3.3$ V, $R_T = 50\ \Omega$	800		1200	mVp-p
$V_{ODE(SS)}$	Steady state output differential voltage with de-emphasis		600		820	
$I_{(OS)}$	Short circuit output current	See Figure 4	-12		12	mA
$V_{I(open)}$	Single-ended input voltage under high impedance input or open input	$I_I = 10$ µA	V_{CC}–10		V_{CC}+10	mV
R_{INT}	Input termination resistance	$V_{IN} = 2.9$ V	45	50	55	Ω
CONTROL PINS (PRE, $\overline{OE}$, I2CEN, OVS)						
$\lvert I_{IH}\rvert$	High-level digital input current	$V_{IH} = 2$ V or V_{CC}	-10		10	µA
$\lvert I_{IL}\rvert$	Low-level digital input current	V_{IL} = GND or 0.8 V	-10		10	µA
I^2C PINS (TSCL, TSDA)						
$\lvert I_{lkg}\rvert$	Input leakage current	$V_I = 5.5$ V	-50		50	µA
		$V_I = V_{CC}$	-10		10	
$\lvert I_{OH}\rvert$	High-level output current	$V_O = 3.6$ V	-10		10	µA

(1) All typical values are at 25°C and with a 3.3-V supply.
(2) The maximum rating is characterized under 3.6 V V_{CC} and 600 mV V_{ID}.

ELECTRICAL CHARACTERISTICS (continued)

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
$\|I_{IL}\|$	Low-level input current	V_{IL} = GND		-40		40	µA
V_{OL}	Low-level output voltage	I_{OL} = 400 µA or 4 mA	OVS = NC(3)	0.47		0.6	V
			OVS = GND(3)	0.6		0.75	
			OVS = V_{CC}(3)	0.75		0.95	
V_{OL}-V_{ILC}	Low-level input voltage below output low-level voltage level	Ensured by design	OVS = NC(3)		70		mV
			OVS = GND(3)		220		
			OVS = V_{CC}(3)		370		
C_{IO}	Input/output capacitance	V_I = 5.0 V or 0 V, Freq = 100 kHz				25	pF
		V_I = 3.0 V or 0 V, Freq = 100 kHz				10	
I^2C PINS (RSCL, RSDA)							
$\|I_{lkg}\|$	Input leakage current	V_I = 5.5 V		-50		50	µA
		V_I = V_{CC}		-10		10	
$\|I_{OH}\|$	High-level output current	V_O = 3.6 V		-10		10	µA
$\|I_{IL}\|$	Low-level input current	V_{IL} = GND		-10		10	µA
V_{OL}	Low-level output voltage	I_{OL} = 4 mA				0.2	V
C_I	Input capacitance	V_I = 5.0 V or 0 V, Freq = 100 kHz				25	pF
		V_I = 3.0 V or 0 V, Freq = 100 kHz				10	

(3) The patent of the OVS pin is filed.

SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
TMDS DIFFERENTIAL PINS (TX/TXC)						
t_{PLH}	Propagation delay time, low-to-high-level output	See Figure 2, AV_{CC} = 3.3 V, R_T = 50 Ω	100		500	ps
t_{PHL}	Propagation delay time, high-to-low-level output		100		500	ps
t_r	Differential output signal rise time (20% - 80%)		75		240	ps
t_f	Differential output signal fall time (20% - 80%)		75		240	ps
$t_{sk(p)}$	Pulse skew ($\|t_{PHL} - t_{PLH}\|$)(2)				50	ps
$t_{sk(D)}$	Intra-pair differential skew, see Figure 5				60	ps
$t_{sk(o)}$	Inter-pair channel-to-channel output skew(3)				80	ps
$t_{sk(pp)}$	Part-to-part skew (4)				200	ps
t_{en}	Enable time	See Figure 6			10	ns
t_{dis}	Disable time				10	ns
$t_{jit(pp)}$	Peak-to-peak output jitter from TXC, residual jitter(5)	See Figure 7, RXC = 165-MHz clock, RX = 1.65-Gbps HDMI pattern, Input: 5m 28AWG HDMI cable, Output: 1m 28AWG HDMI cable, PRE = high		14	30	ps
$t_{jit(pp)}$	Peak-to-peak output jitter from TX0 - TX2, residual jitter(5)			30	88	ps
$t_{jit(pp)}$	Peak-to-peak output jitter from TXC, residual jitter(5)	See Figure 7, RXC = 225-MHz clock, RX = 2.25-Gbps HDMI pattern, Input: 5m 28AWG HDMI cable, Output: 1m 28AWG HDMI cable, PRE = high		25		ps
$t_{jit(pp)}$	Peak-to-peak output jitter from TX0 - TX2, residual jitter(5)			42	88	

(1) All typical values are at 25°C and with a 3.3-V supply.
(2) $t_{sk(p)}$ is the magnitude of the time difference between t_{PLH} and t_{PHL} of a specified terminal.
(3) $t_{sk(o)}$ is the magnitude of the difference in propagation delay times between any specified terminals of channel 2 to 4 of a device when inputs are tied together.
(4) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of channel 2 to 4 of two devices, or between channel 1 of two devices, when both devices operate with the same source, the same supply voltages, at the same temperature, and have identical packages and test circuits.
(5) Jitter specifications are ensured by design and characterization and measured in BER^{-12}

SWITCHING CHARACTERISTICS (continued)

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
I2C PINS (RSCL, RSDA, TSCL, TSDA)						
t_{PLH}	Propagation delay time, low-to-high-level output TSCL/TSDA to RSCL/RSDA	See Figure 8, OVS = NC	204		459	ns
t_{PHL}	Propagation delay time, high-to-low-level output TSCL/TSDA to RSCL/RSDA		35		120	ns
t_{PLH}	Propagation delay time, low-to-high-level output RSCL/RSDA to TSCL/TSDA		194		351	ns
t_{PHL}	Propagation delay time, high-to-low-level output RSCL/RSDA to TSCL/TSDA		35		120	ns
t_r	TSCL/TSDA Output signal rise time		500		800	ns
t_f	TSCL/TSDA Output signal fall time		30		72	ns
t_r	RSCL/RSDA Output signal rise time		796		999	ns
t_f	RSCL/RSDA Output signal fall time		20		72	ns
t_{set}	Enable to start condition	See Figure 9	100			ns
t_{hold}	Enable after stop condition		100			ns

PARAMETER MEASUREMENT INFORMATION

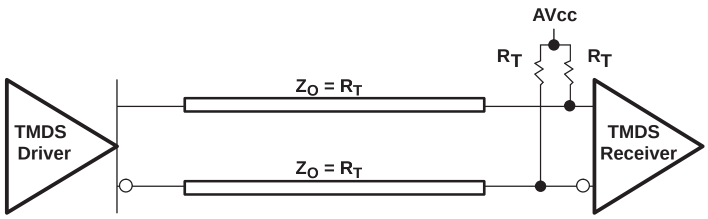
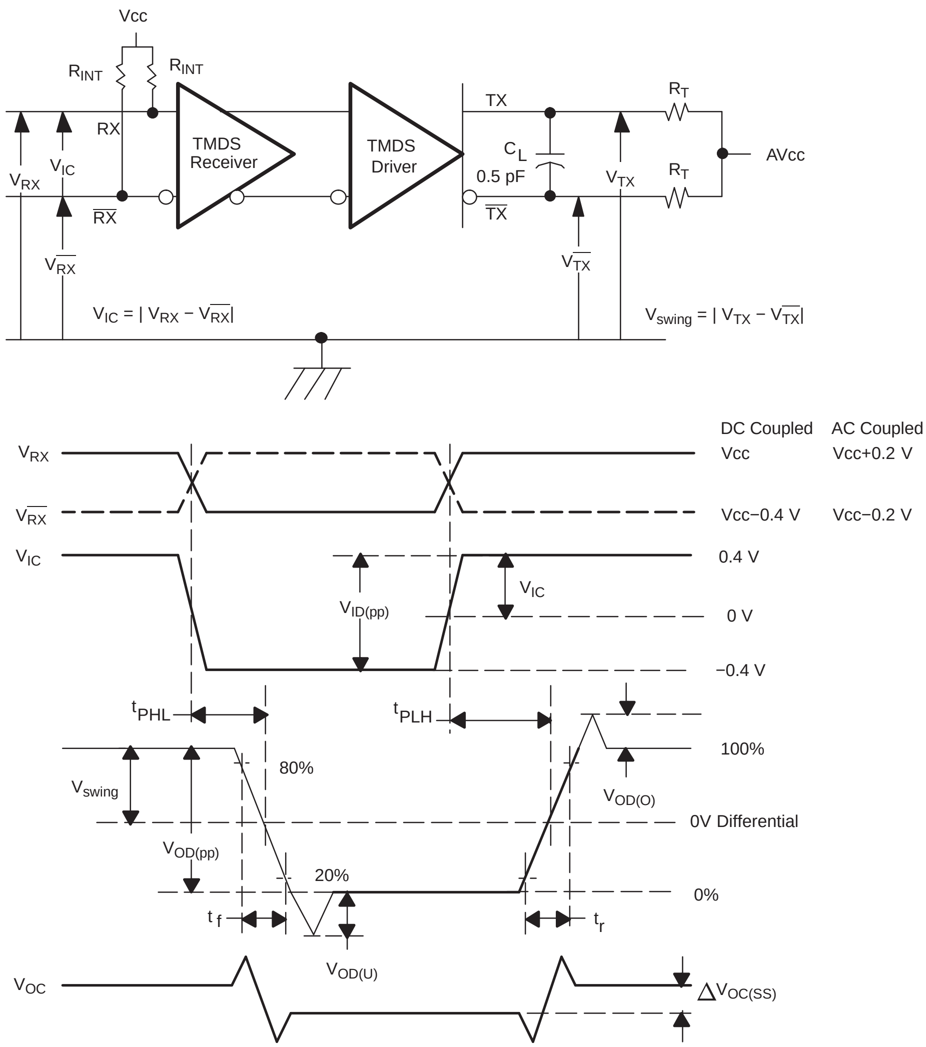


Figure 1. Typical Termination for TMDS Output Driver



NOTE: PRE = low. All input pulses are supplied by a generator having the following characteristics: t_r or t_f < 100 ps, 100 MHz from Agilent 81250. C_L includes instrumentation and fixture capacitance within 0.06 m of the D.U.T. Measurement equipment provides a bandwidth of 20 GHz minimum.

Figure 2. TMDS Timing Test Circuit and Definitions

PARAMETER MEASUREMENT INFORMATION (continued)

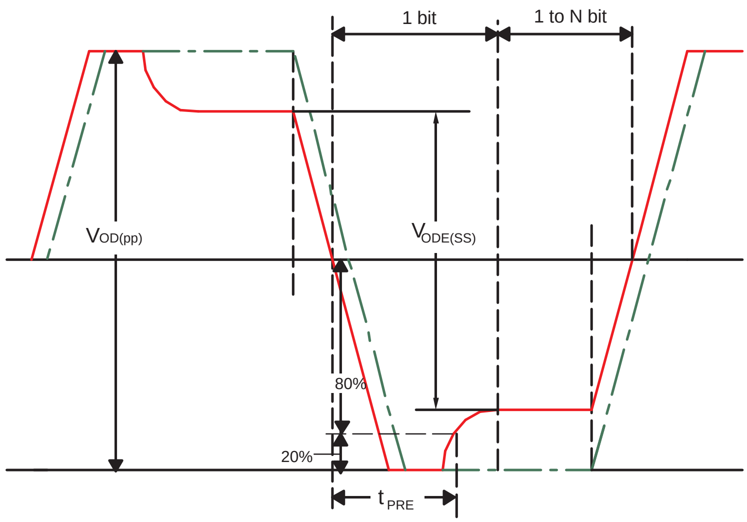


Figure 3. De-Emphasis Output Voltage Waveforms and Duration Measurement Definitions

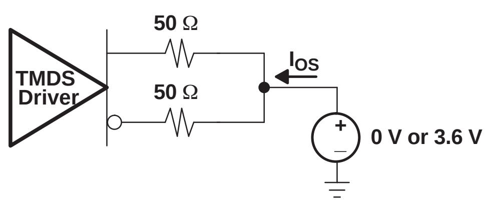


Figure 4. Short Circuit Output Current Test Circuit

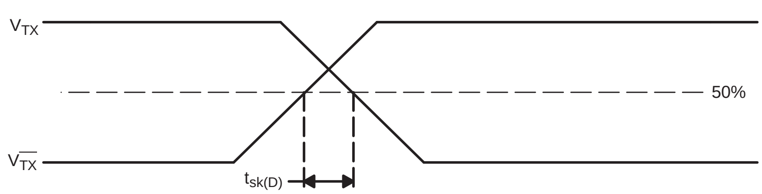


Figure 5. Definition of Intra-Pair Differential Skew

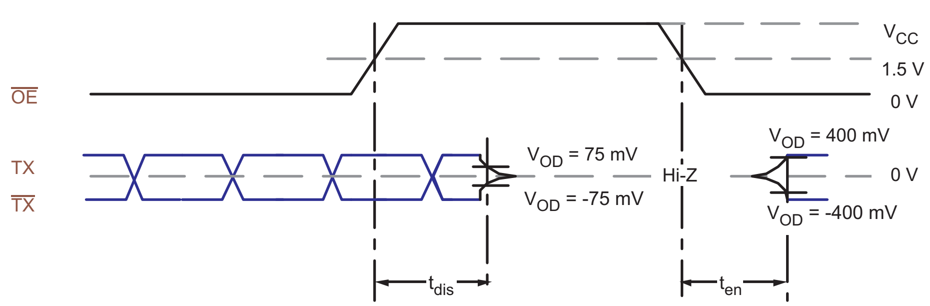
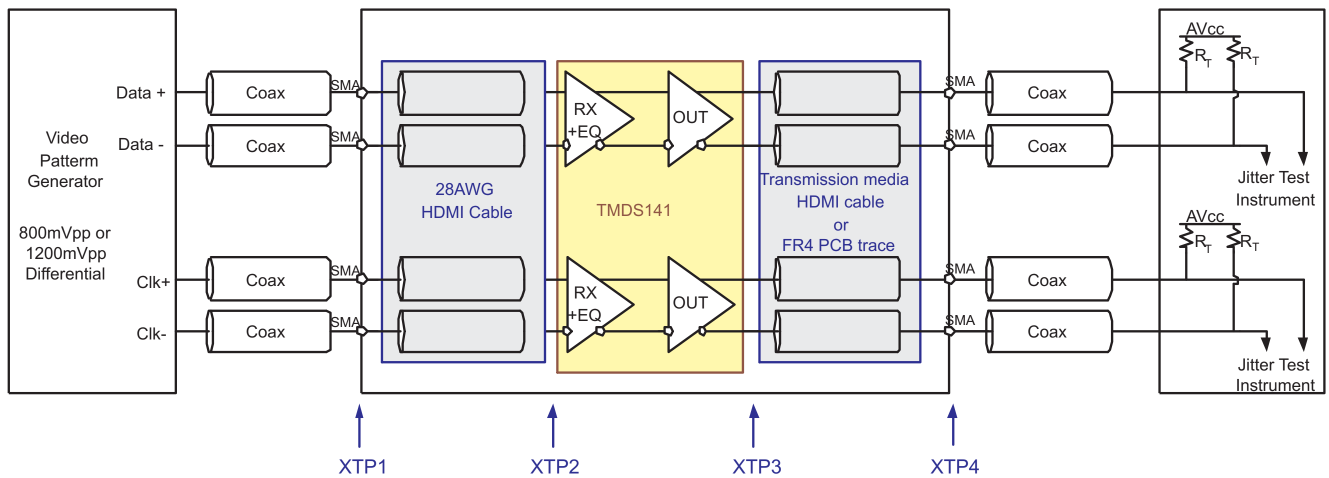


Figure 6. TMDS Enable and Disable Timing Definitions

PARAMETER MEASUREMENT INFORMATION (continued)



A. All jitters are measured in BER of 10^{-12}

B. The residual jitter reflects the total jitter measured at XTP4, subtract the total jitter at XTP1

Figure 7. Jitter Test Circuit

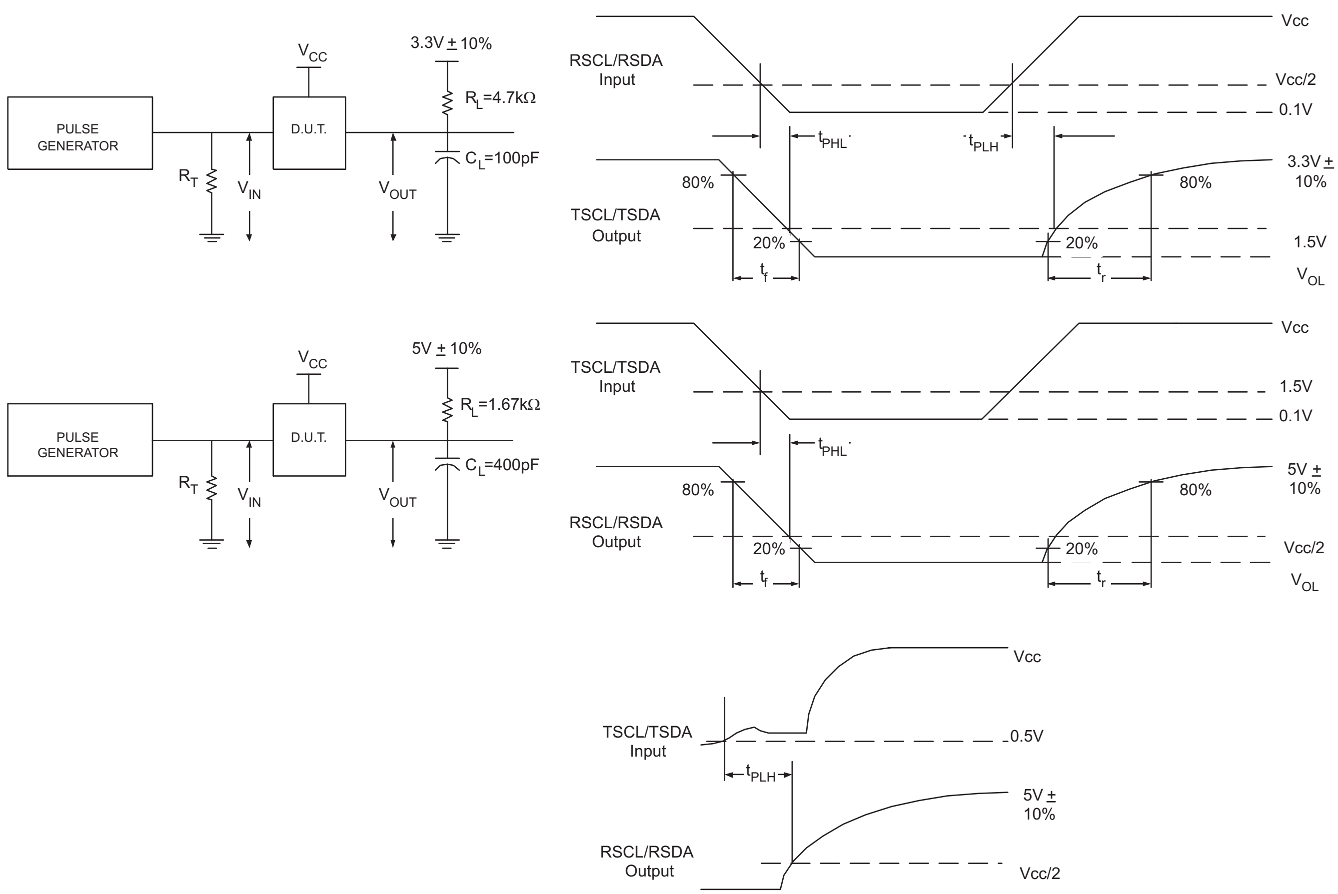


Figure 8. I²C Timing Test Circuit and Definition

PARAMETER MEASUREMENT INFORMATION (continued)

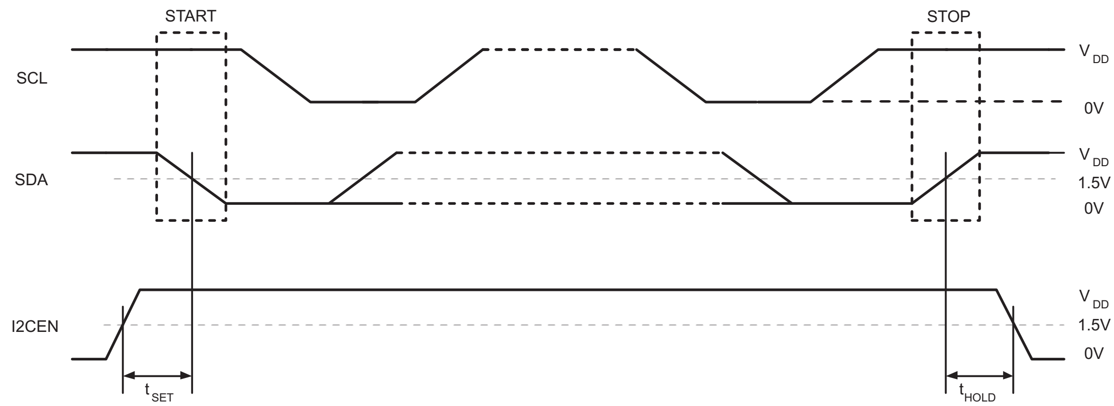


Figure 9. I²C Setup and Hold Definition

TYPICAL CHARACTERISTICS

SUPPLY CURRENT vs FREQUENCY

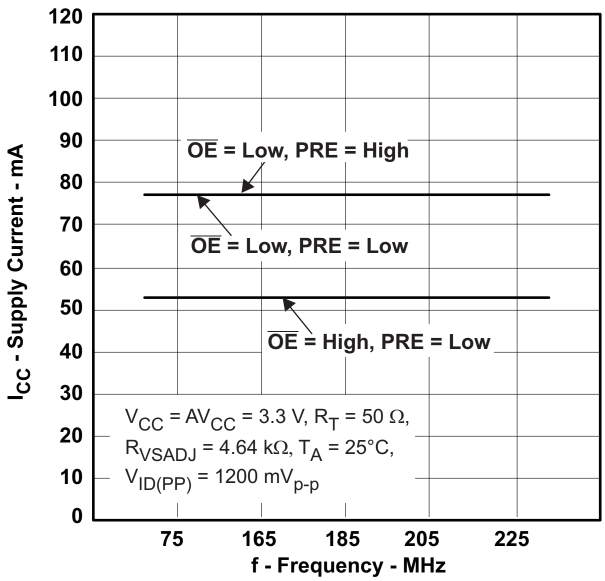


Figure 10.

SUPPLY CURRENT vs FREE-AIR TEMPERATURE

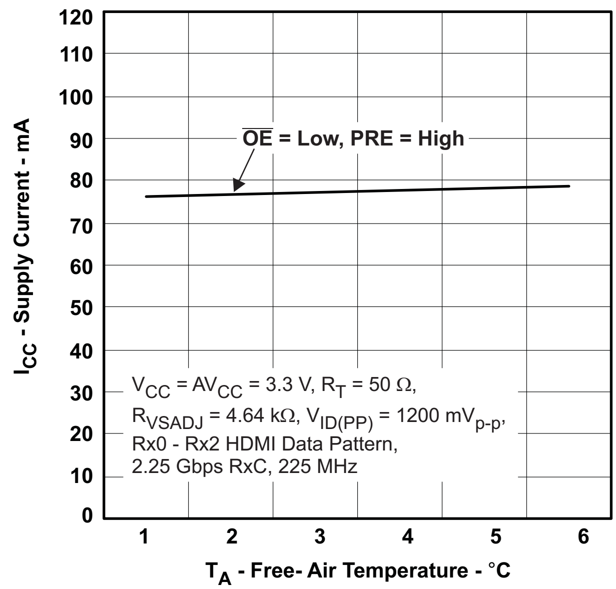


Figure 11.

RESIDUAL PEAK-TO-PEAK JITTER vs DATA RATE (DC Coupled Input: 5m 28AWG, Output: 1m 28AWG)

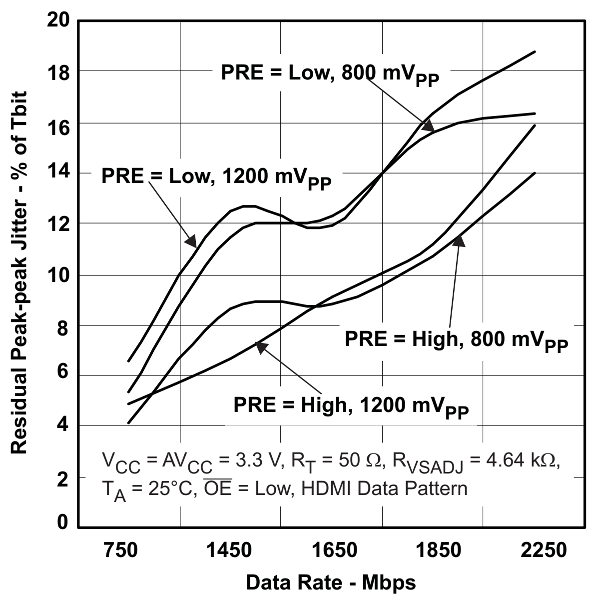


Figure 12.

RESIDUAL PEAK-TO-PEAK JITTER vs DATA RATE (DC Coupled Input: 3m 30AWG, Output: 1m 28AWG)

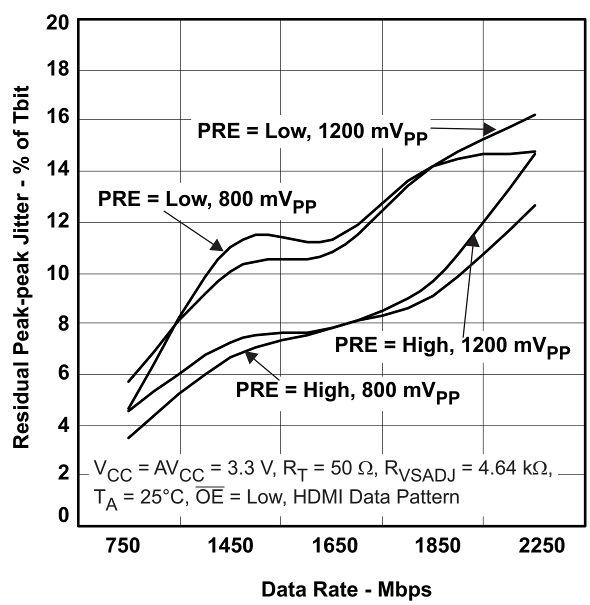


Figure 13.

TYPICAL CHARACTERISTICS (continued)

RESIDUAL PEAK-TO-PEAK JITTER
vs
DATA RATE
(AC Coupled Input: 3m 30AWG, Output: 1m 28AWG)

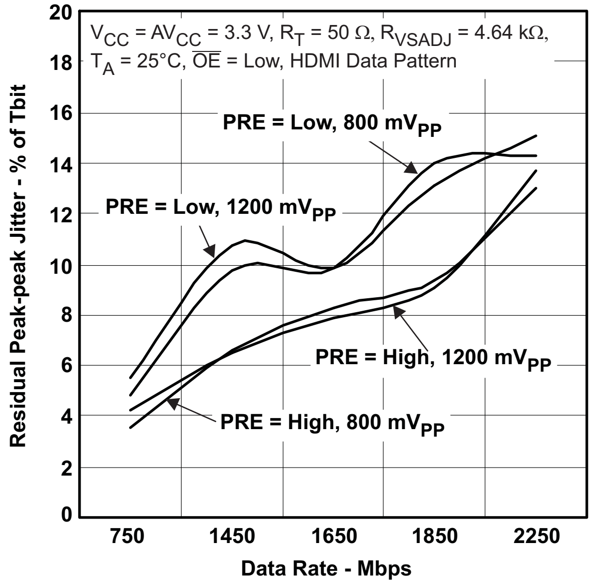


Figure 14.

RESIDUAL PEAK-TO-PEAK JITTER
vs
8-MIL FR4 TRACE OUTPUT
(DC Coupled Input: 5m 28AWG)

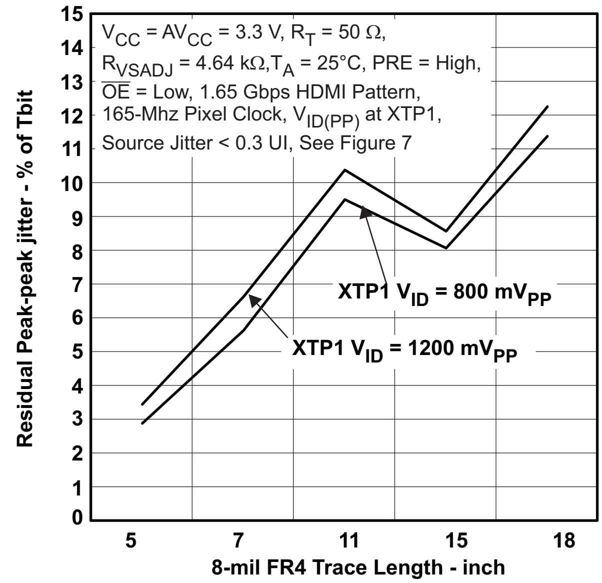


Figure 15.

RESIDUAL PEAK-TO-PEAK JITTER
vs
PEAK-TO-PEAK DIFFERENTIAL INPUT VOLTAGE
(at XTP2)

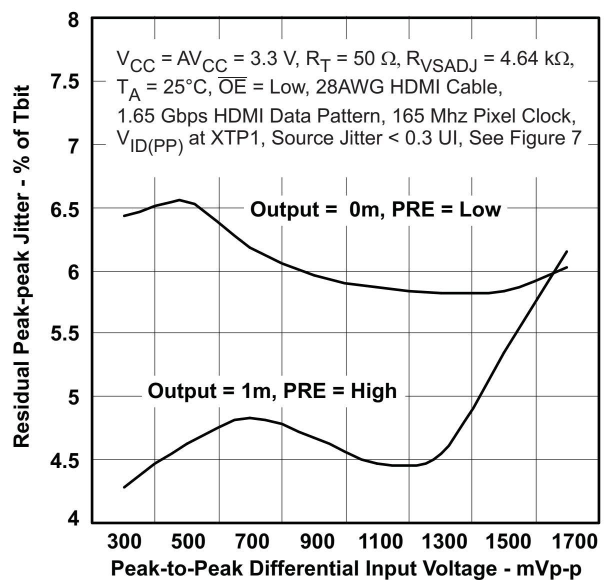


Figure 16.

APPLICATION INFORMATION

Supply Voltage

All V_{CC} pins can be tied to a single 3.3-V power source. A 0.01-µF capacitor is connected from each V_{CC} pin directly to ground to filter supply noise.

TMDS Inputs

Standard TMDS terminations are integrated on all TMDS inputs. External terminations are not required. Each input channel contains an 8-dB equalization circuit to compensate for cable losses. The voltage at the TMDS input pins must be limited per the absolute maximum ratings. An unused input should not be connected to ground as this would result in excessive current flow damaging the device. TMDS input pins do not incorporate failsafe circuits. An unused input channel can be externally biased to prevent output oscillation. The complementary input pin is recommended to be grounded through a 1-kΩ resistor and the other pin left open.

TMDS Outputs

A 1% precision resister, 4.64-kΩ, connected from VSADJ to ground is recommended to allow the differential output swing to comply with TMDS signal levels. The differential output driver provides a typical 10-mA current sink capability, which provides a typical 500-mV voltage drop across a 50-Ω termination resistor.

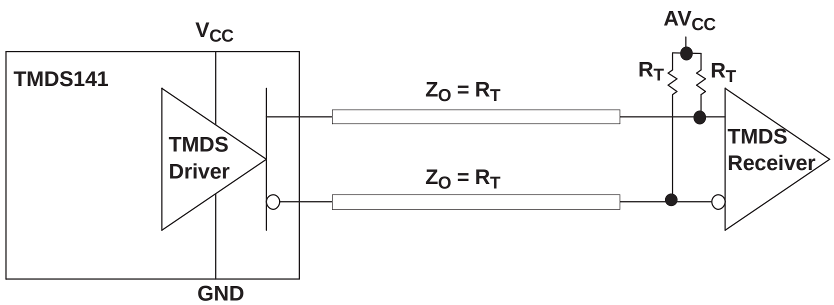


Figure 17. TMDS Driver and Termination Circuit

Referring to Figure 17, if both V_{CC} (TMDS141 supply) and AV_{CC} (sink termination supply) are both powered, the TMDS output signals is high impedance when OEB = high. Both supplies being active is the normal operating condition.

Again refer to Figure 17, if V_{CC} is on and AV_{CC} is off, the TMDS outputs source a typical 5-mA current through each termination resistor to ground. A total of 10-mW of power is consumed by the terminations independent of the OEB logical selection. When AV_{CC} is powered on, normal operation (OEB controls output impedance) is resumed.

When the power source of the device is off and the power source to termination is on, the $I_{O(off)}$, output leakage current, specification ensures the leakage current is limited 10-µA or less.

The PRE pin provides 3dB de-emphasis, allowing output signal pre-conditioning to offset interconnect losses from the TMDS141 outputs to a TMDS receiver. PRE is recommended to be set low while connecting to a receiver throw short PCB route.

I²C Function Description

The RSCL/RSDA and TSCL/TSDA pins are 5-V tolerant when the device is powered off and high impedance under low supply voltage, 1.5 V or below. If the device is powered up and the I^2C circuits are enabled, and I2CEN = high, the driver T (see Figure 18) is turned on or off depending up on the corresponding R side voltage level.

When the R side is pulled low below 1.5 V, the corresponding T side driver turns on and pulls the T side down to a low level output voltage, V_{OL}. The value of V_{OL} depends on the input to the OVS pin. When OVS is left floating

APPLICATION INFORMATION (continued)

or not connected, V_{OL} is typically 0.5 V. When OVS is connected to GND, V_{OL} is typically 0.65 V. When OVS is connected to V_{CC}, V_{OL} is typically 0.8 V. V_{OL} is always higher than the driver R input threshold, V_{IL}, which is typically 0.4 V, preventing lockup of the repeater loop. The V_{OL} value can be selected to improve or optimize noise margins between V_{OL} and the V_{IL} of the repeater itself or the V_{IL} of some external device connected on the T side.

When the R side is pulled up, above 1.5 V, the T side driver turns off and the T side pin is high impedance.

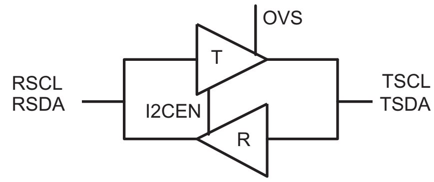


Figure 18. I²C Drivers in TMDS141

When the T side is pulled below 0.4 V by an external I²C driver, both drivers R and T are turned on. Driver R pulls the R side to near 0 V, and driver T is on, but is overridden by the external I²C driver. If driver T is already on, due to a low on the R side, driver R just turns on.

When the T side is released by the external I²C driver, driver T is still on, so the T side is only able to rise to the V_{OL} of driver T. Driver R turns off, since V_{OL} is above its 0.4-V V_{IL} threshold, releasing the R side. If no external I²C driver is keeping the R side low, the R side rises, and driver T turns off once the R side rises above 1.5 V, see Figure 19.

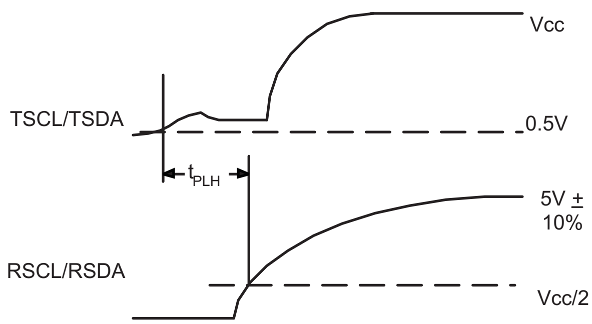


Figure 19. Waveform of Turning Driver T Off

It is important that any external I²C driver on the T side is able to pull the bus below 0.4 V to ensure full operation. If the T side cannot be pulled below 0.4 V, driver R may not recognize and transmit the low value to the R side.

I²C Enable

The I2CEN pin is active high with an internal pull-up to V_{CC}. It can be used to isolate a badly behaved slave during power up. It should never change state during an I²C operation because disabling during a bus operation may hang the bus and enabling part way through a bus cycle could confuse the I²C parts being enabled.

I²C Behavior

The typical application of the TMDS141 is as a repeater in a TV connecting the HDMI input connector and an internal HDMI Rx through flat cables. The I²C repeater is 5-V tolerant, and no additional circuitry is required to translate between 3.3-V to 5-V bus voltages. In the following example, the system master is running on an R-side I²C-bus while the slave is connected to a T-side bus. Both buses run at 100 kHz supporting standard-mode I²C operation. Master devices can be placed on either bus.

APPLICATION INFORMATION (continued)

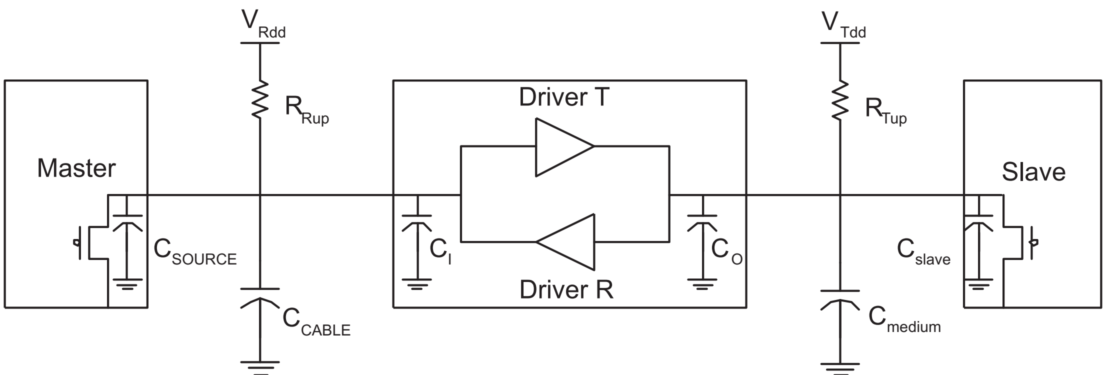


Figure 20. Typical Application

Figure 21 illustrates the waveforms seen on the R-side I²C-bus when the master writes to the slave through the I²C repeater circuit of the TMDS141. This looks like a normal I²C transmission, and the turn on and turn off of the acknowledge signals are slightly delayed.

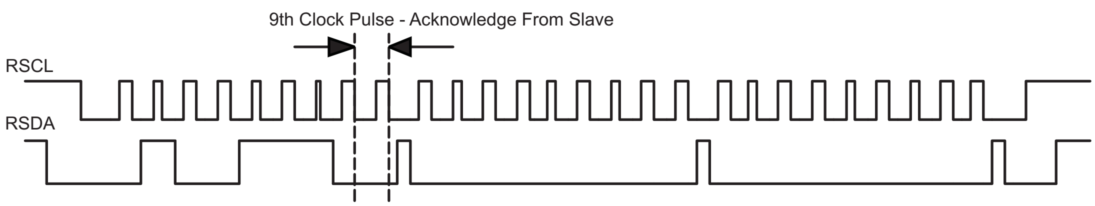


Figure 21. Bus R Waveform

Figure 22 illustrates the waveforms seen on the T-side I²C-bus under the same operation in Figure 21. On the T-side of the I²C repeater, the clock and data lines would have a positive offset from ground equal to the V_{OL} of the driver T. After the 8th clock pulse, the data line is pulled to the V_{OL} of the slave device which is very close to ground in this example. At the end of the acknowledge, the slave device releases and the bus level rises back to the V_{OL} set by the driver until the R-side rises above $V_{CC}/2$, after which it continues to high. It is important to note that any arbitration or clock stretching events require that the low level on the T-side bus at the input of the TMDS141 I²C repeater is below 0.4 V to be recognized by the device and then transmitted to the R-side I²C bus.

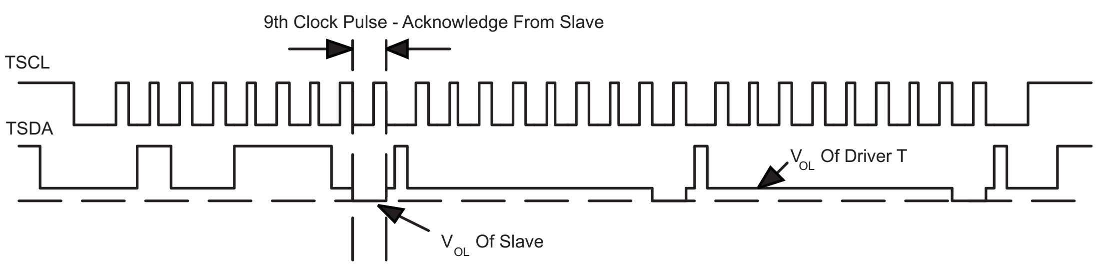


Figure 22. Bus T Waveform

The I²C circuitry inside the TMDS141 allows multiple stage operation as shown in Figure 23. I²C-Bus slave devices can be connected to any of the bus segments. The number of devices that can be connected in series is limited by repeater delay/time of flight considerations for the maximum bus speed requirements.

APPLICATION INFORMATION (continued)

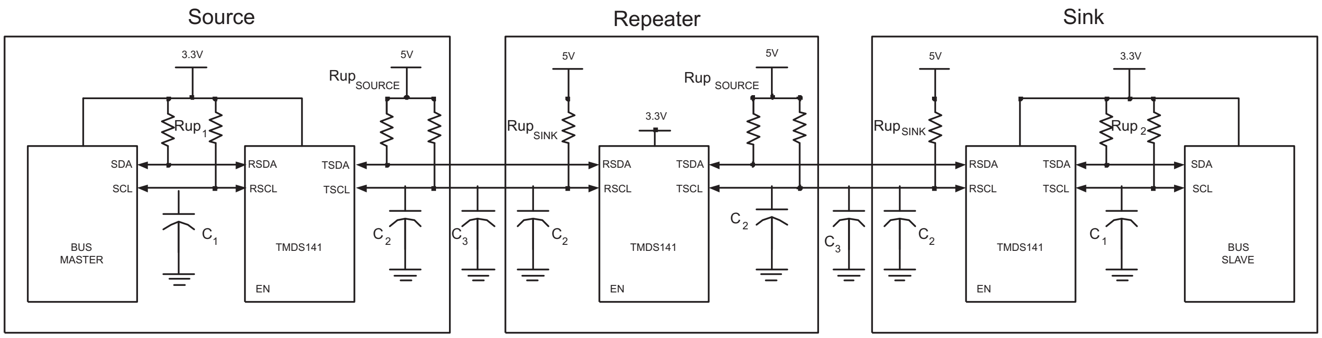


Figure 23. Typical Series Application

I^2C Pull-up Resistors

The pull-up resistor value is determined by two requirements:

1. The maximum sink current of the I^2C buffer:

   The maximum sink current is 3 mA or slightly higher for an I^2C driver supporting standard-mode I^2C operation.

   $$R_{up(min)} = V_{DD}/Isink \quad (1)$$

2. The maximum transition time on the bus:

   The maximum transition time, T, of an I^2C bus is set by an RC time constant, where R is the pull-up resistor value, and C is the total load capacitance. The parameter, k, can be calculated from equation 3 by solving for t, the times at which certain voltage thresholds are reached. Different input threshold combinations introduce different values of t. Table 1 summarizes the possible values of k under different threshold combinations.

   $$T = k \times RC \quad (2)$$

   $$V(t) = V_{DD}(1 - e^{-t/RC}) \quad (3)$$

Table 1. Value k Upon Different Input Threshold Voltages

$V_{th-}\backslash V_{th+}$	$0.7V_{DD}$	$0.65V_{DD}$	$0.6V_{DD}$	$0.55V_{DD}$	$0.5V_{DD}$	$0.45V_{DD}$	$0.4V_{DD}$	$0.35V_{DD}$	$0.3V_{DD}$
$0.1V_{DD}$	1.0986	0.9445	0.8109	0.6931	0.5878	0.4925	0.4055	0.3254	0.2513
$0.15V_{DD}$	1.0415	0.8873	0.7538	0.6360	0.5306	0.4353	0.3483	0.2683	0.1942
$0.2V_{DD}$	0.9808	0.8267	0.6931	0.5754	0.4700	0.3747	0.2877	0.2076	0.1335
$0.25V_{DD}$	0.9163	0.7621	0.6286	0.5108	0.4055	0.3102	0.2231	0.1431	0.0690
$0.3V_{DD}$	0.8473	0.6931	0.5596	0.4418	0.3365	0.2412	0.1542	0.0741	-

From equation 1, $R_{up(min)}$ = 5.5V/3mA = 1.83 kΩ to operate the bus under a 5-V pull-up voltage and provide less than 3 mA when the I^2C device is driving the bus to a low state. If a higher sink current, for example 4 mA, is allowed, $R_{up(min)}$ can be as low as 1.375 kΩ.

Given a 5-V I^2C device with input low and high threshold voltages at 0.3 V_{dd} and 0.7 V_{dd}, the valued of k is 0.8473 from Table 1. Taking into account the 1.83-kΩ pull-up resistor, the maximum total load capacitance is $C_{(total-5V)}$ = 645 pF. $C_{cable(max)}$ should be restricted to be less than 545 pF if C_{source} and C_i can be as heavy as 50 pF. Here the C_i is treated as C_{sink}, the load capacitance of a sink device.

Fixing the maximum transition time from Table 1, T = 1 µs, and using the k values from Table 1, the recommended maximum total resistance of the pull-up resistors on an I^2C bus can be calculated for different system setups.

To support the maximum load capacitance specified in the HDMI spec, $C_{cable(max)}$ = 700pF/C_{source} = 50pF/C_i = 50pF, $R_{(max)}$ can be calculated as shown in Table 2.

Table 2. Pull-Up Resistor Upon Different Threshold Voltages and 800-pF Loads

V_{th-}\V_{th+}	$0.7V_{DD}$	$0.65V_{DD}$	$0.6V_{DD}$	$0.55V_{DD}$	$0.5V_{DD}$	$0.45V_{DD}$	$0.4V_{DD}$	$0.35V_{DD}$	$0.3V_{DD}$	UNIT
$0.1V_{DD}$	1.14	1.32	1.54	1.80	2.13	2.54	3.08	3.84	4.97	kΩ
$0.15V_{DD}$	1.20	1.41	1.66	1.97	2.36	2.87	3.59	4.66	6.44	kΩ
$0.2V_{DD}$	1.27	1.51	1.80	2.17	2.66	3.34	4.35	6.02	9.36	kΩ
$0.25V_{DD}$	1.36	1.64	1.99	2.45	3.08	4.03	5.60	8.74	18.12	kΩ
$0.3V_{DD}$	1.48	1.80	2.23	2.83	3.72	5.18	8.11	16.87	-	kΩ

Or, limiting the maximum load capacitance of each cable to be 400 pF to accommodate with I^2C spec version 2.1. $C_{cable(max)}$ = 400pF/C_{source}=50pF/C_i = 50pF, the maximum values of $R_{(max)}$ are calculated as shown in Table 3.

Table 3. Pull-Up Resistor Upon Different Threshold Voltages and 500-pF Loads

V_{th-}\V_{th+}	$0.7V_{DD}$	$0.65V_{DD}$	$0.6V_{DD}$	$0.55V_{DD}$	$0.5V_{DD}$	$0.45V_{DD}$	$0.4V_{DD}$	$0.35V_{DD}$	$0.3V_{DD}$	UNIT
$0.1V_{DD}$	1.82	2.12	2.47	2.89	3.40	4.06	4.93	6.15	7.96	kΩ
$0.15V_{DD}$	1.92	2.25	2.65	3.14	3.77	4.59	5.74	7.46	10.30	kΩ
$0.2V_{DD}$	2.04	2.42	2.89	3.48	4.26	5.34	6.95	9.63	14.98	kΩ
$0.25V_{DD}$	2.18	2.62	3.18	3.92	4.93	6.45	8.96	13.98	28.99	kΩ
$0.3V_{DD}$	2.36	2.89	3.57	4.53	5.94	8.29	12.97	26.99	-	kΩ

Obviously, to accommodate the 3-mA drive current specification, a narrower threshold voltage range is required to support a maximum 800-pF load capacitance for a standard-mode I^2C bus.

When the input low and high level threshold voltages, V_{th-} and V_{th+}, are 0.7 V and 1.9 V, which is 0.15 V_{DD} and 0.4 V_{DD} approximately with V_{DD} = 5 V, from Table 2, the maximum pull-up resistor is 3.59 kΩ. The allowable pull-up resistor is in the range of 1.83 kΩ and 3.59 kΩ.

Thermal Dissipation

On a high-K board – It is always recommended to solder the PowerPAD onto the thermal land. A thermal land is the area of solder-tinned-copper underneath the PowerPAD package. On a high-K board the TMDS141 can operate over the full temperature range by soldering the PowerPAD onto the thermal land without vias.

On a low-K board – In order for the device to operate across the temperature range on a low-K board, a 1-oz Cu trace connecting the GND pins to the thermal land must be used. A simulation shows $R_{\theta JA}$ = 100.84°C/W allowing 545 mW power dissipation at 70°C ambient temperature.

A general PCB design guide for PowerPAD packages is provided in the document SLMA002 - PowerPAD Thermally Enhanced Package.

TEXAS INSTRUMENTS
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PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION 11-August-2006

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TMDS141RHAR	ACTIVE	QFN	RHA	40	2500	Green (RoHS & no Sb/ Br)	CU NIPDAU	Level-3-260C-168 HR
TMDS141RHARG4	ACTIVE	QFN	RHA	40	2500	Green (RoHS & no Sb/ Br)	CU NIPDAU	Level-3-260C-168 HR

1. The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

2. Eco Plan -The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) -please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

3. MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from A Revision (August 2006) to B Revision	Page
• Changed Features	1
• Changed Signaling rate from 1.65 Gbps to 2.25 Gbps	5
• Added PRE = Low to supply current test conditions	6
• Added PRE = Low to power dissipation test conditions	6
• Deleted TTL high- and low-level output voltages	7
• Changed Peak-to-peak output jitter from TX0 - TX2, residual jitter from 90 to 88 ps	7
• Added Peak-to-peak output jitter from TXC, residual jitter	7
• Added Peak-to-peak output jitter from TX0 - TX2, residual jitter	7
• Changed Figure 10	13
• Changed Figure 11	13
• Changed Figure 12	13
• Changed Figure 13	13
• Changed Figure 14	14

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

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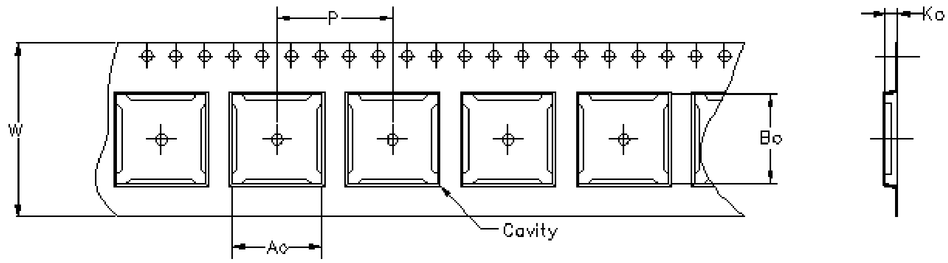
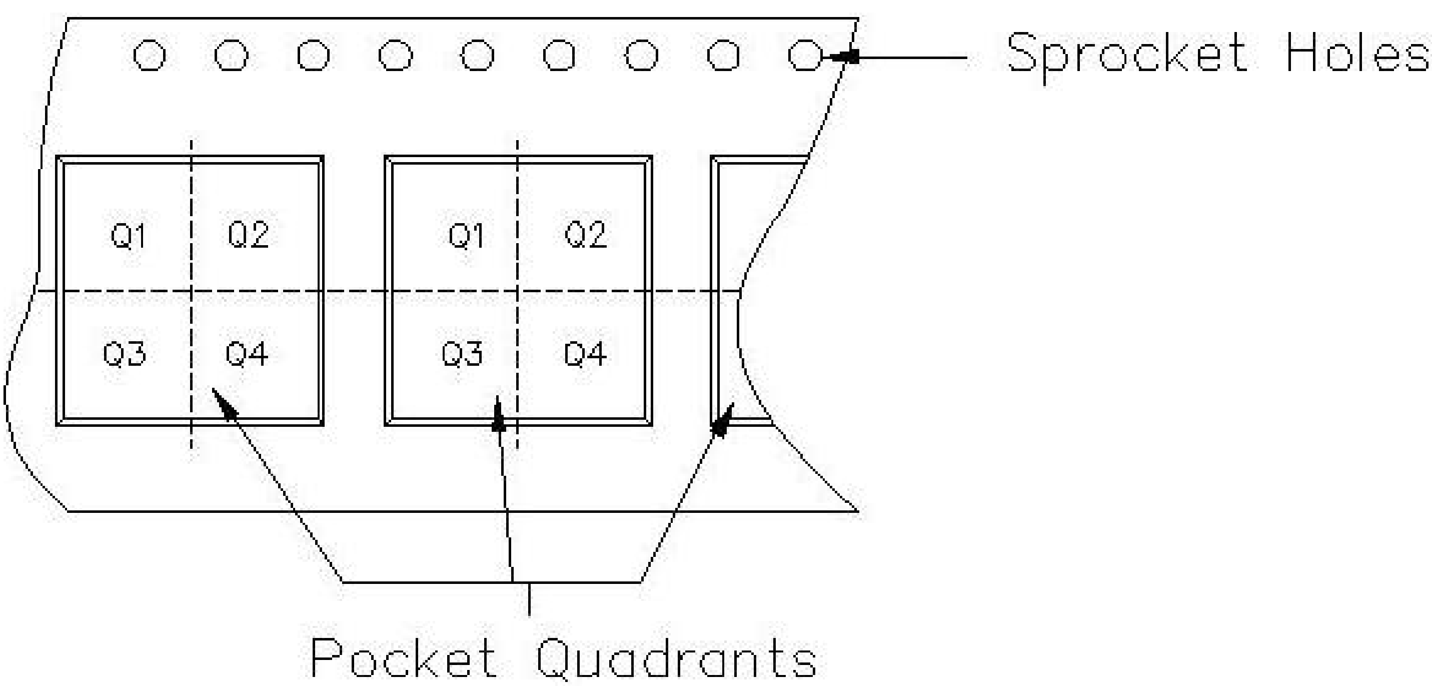


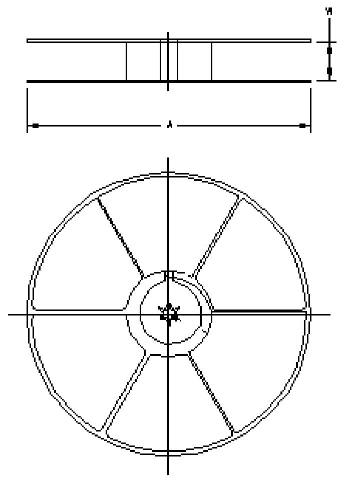
Carrier tape design is defined largely by the component lentgh, width, and thickness.

Ao = Dimension designed to accommodate the component width.
Bo = Dimension designed to accommodate the component length.
Ko = Dimension designed to accommodate the component thickness.
W = Overall width of the carrier tape.
P = Pitch between successive cavity centers.



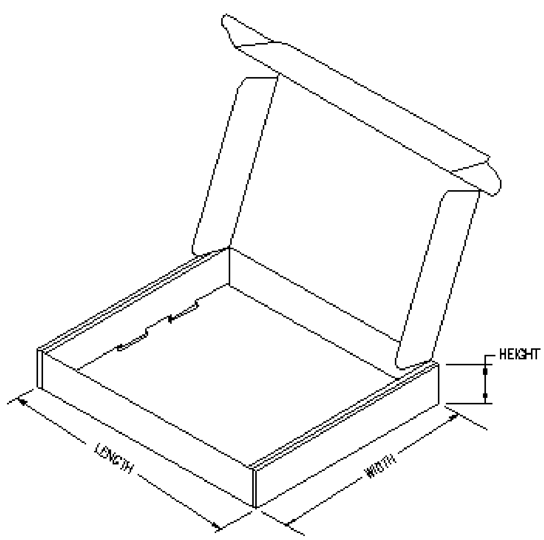
TAPE AND REEL INFORMATION

Device	Package	Pins	Site	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMDS141RHAR	RHA	40	MLA	330	16	6.3	6.3	1.5	12	16	PKGORN T2TR-MS P

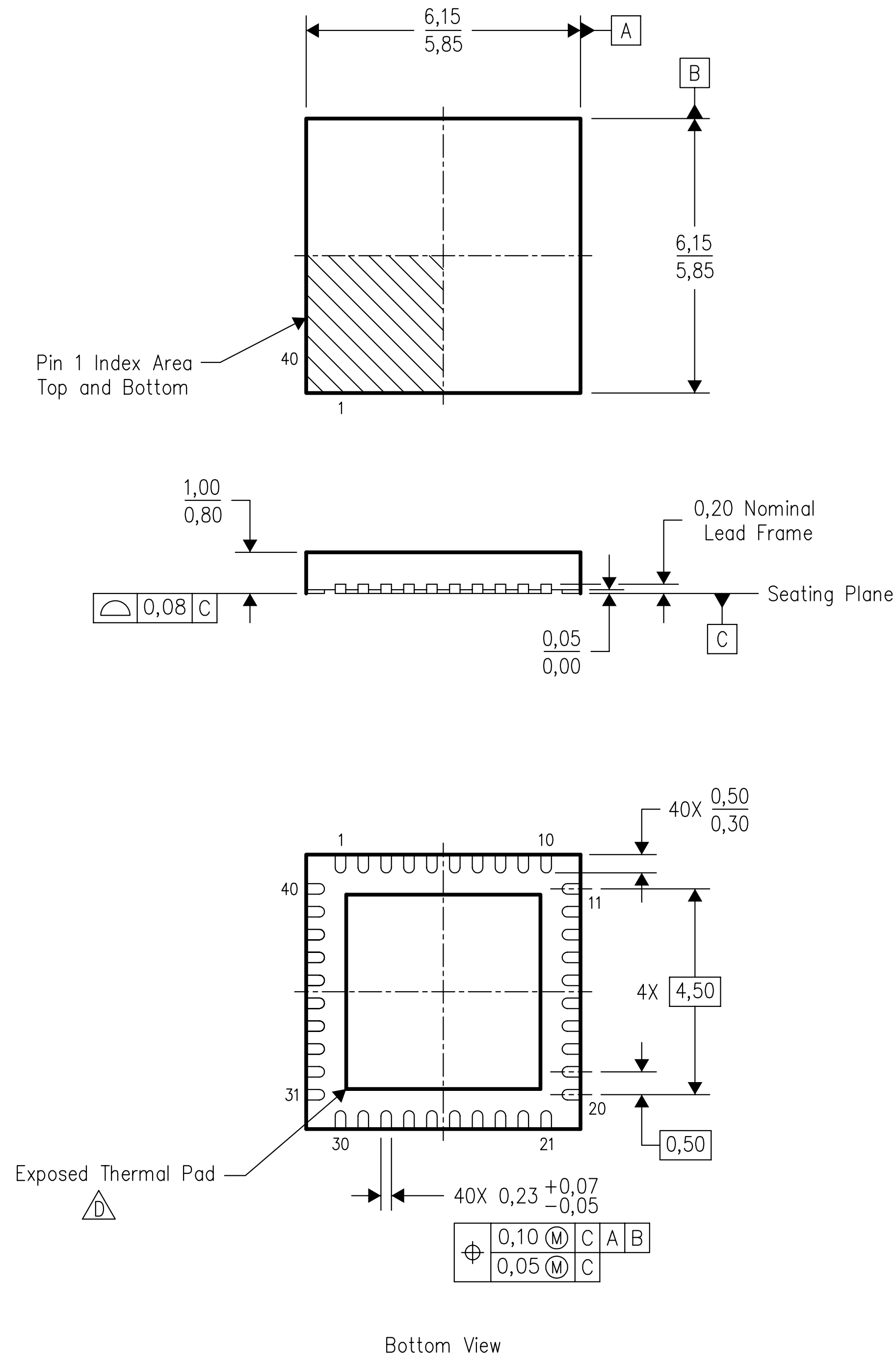


TAPE AND REEL BOX INFORMATION

Device	Package	Pins	Site	Length (mm)	Width (mm)	Height (mm)
TMDS141RHAR	RHA	40	MLA	346.0	346.0	33.0



RHA (S-PQFP-N40) PLASTIC QUAD FLATPACK



4204276/C 12/2004

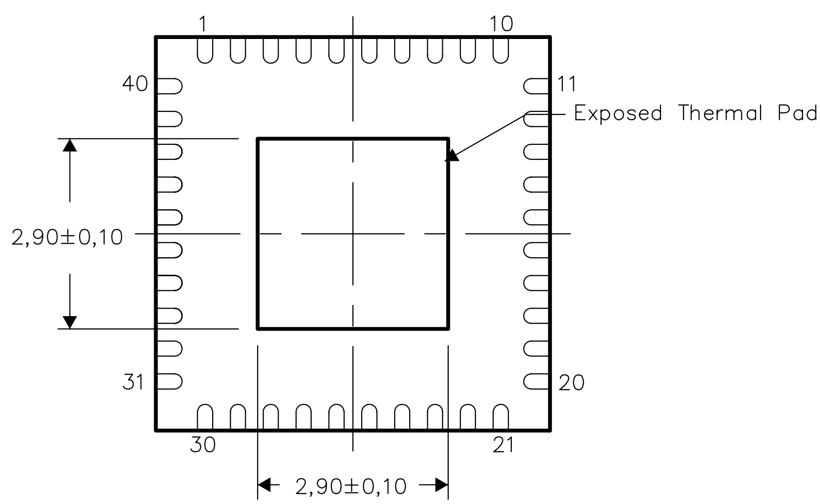
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M−1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No−Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Package complies to JEDEC MO−220 variation VJJD−2.

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to a ground or power plane (whichever is applicable), or alternatively, a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No–Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

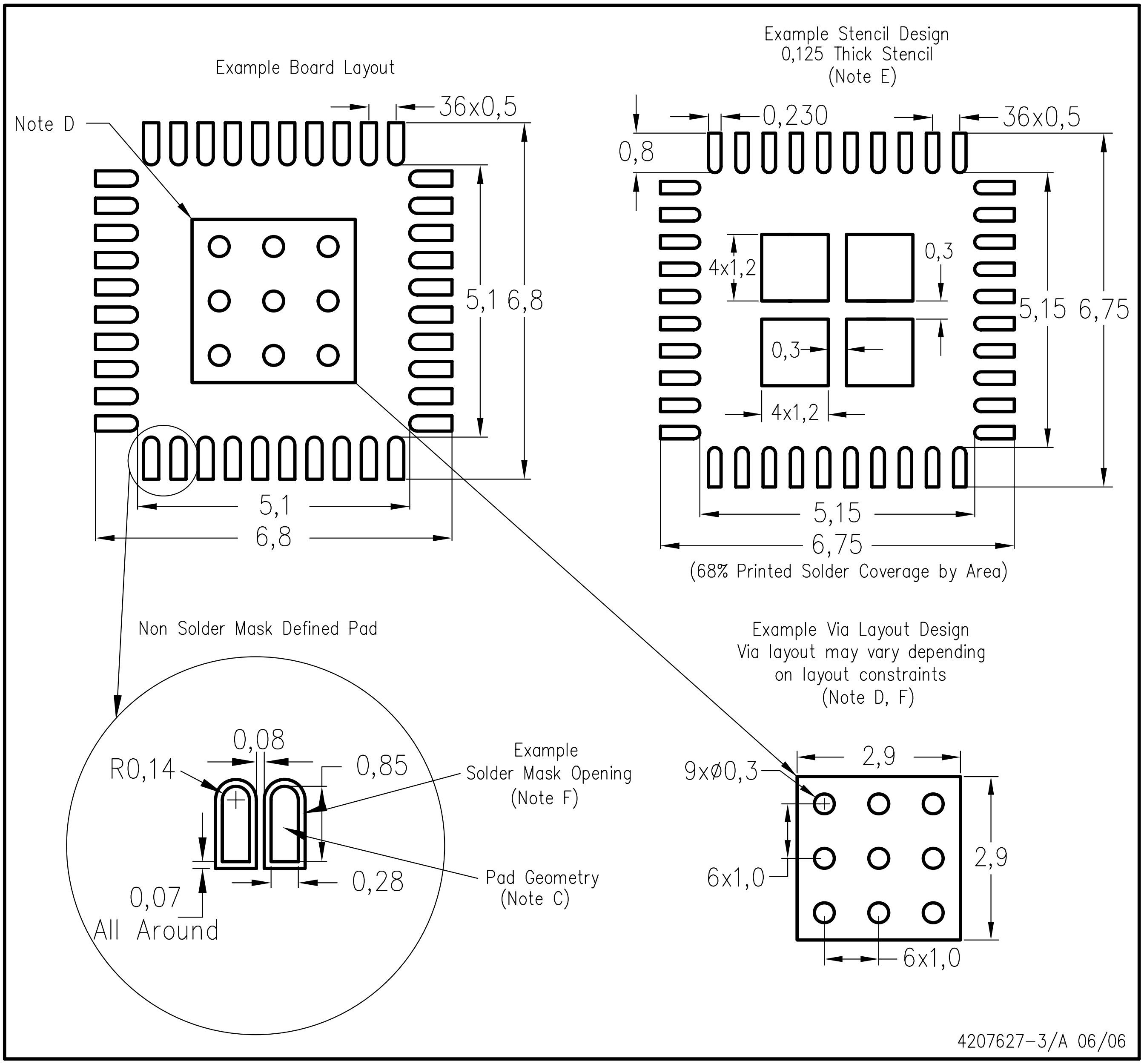


Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

RHA (S–PQFP–N40)



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.