3.5W/CH STEREO CLASS-D AUDIO POWER AMPLIFIER

GENERAL DESCRIPTION

The TMPA218DS is a stereo class-D audio power amplifier IC with digital volume control. With BTL (Bridge-Tied-Load) configuration, it delivers up to 3.5W/ch (7W in all) into a 2 ohm load. Up and down volume control signals provide -60dB attenuation form maximum voltage gain. No external heat-sink is required.

For multiple-input applications, independent gain control and corner frequency can be implemented by summing the input sources through resistor ratio and input capacitor values. Automatic output power control makes the best use of battery.

Analog input signal is converted into digital output which drives directly to the speaker. High power efficiency is achieved due to digital output at the load. The audio information is embedded in PWM（Pulse Width Modulation）.

APPLICATIONS

Multimedia application includes Cellular Phones, PDAs, DVD/CD players, TFT LCD TVs/Monitors, 2.1 channel audio systems, USB audio. It is also ideal for other portable devices like Wireless Radios.

FEATURES

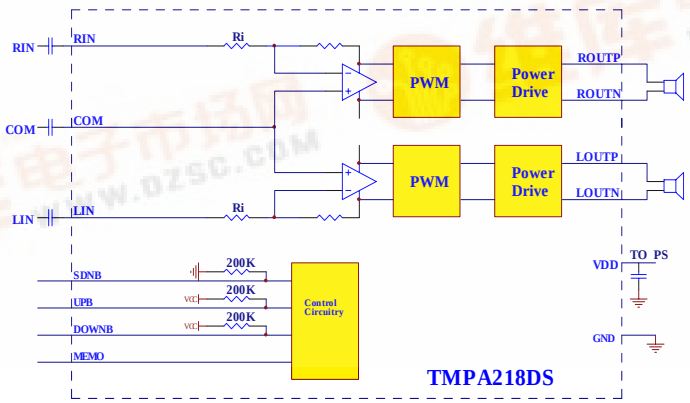
- 2.5V to 6V Single Supply
- Up to 3.5W / Ch at 5.5V, 2 ohms
- Up to 88% Power Efficiency
- Automatic output power control (APC)
- Memory of voltage gain at shutdown
- 0dB to -60dB attenuation from max. voltage gain
- 2.2mA / Ch Quiescent Current at 5V
- Less Than 0.2uA / Ch Shutdown Current
- Pop-less Power-Up, Shutdown and Recovery
- Differential 250 KHz PWM Allows Bridge-Tied Load to increase Output Power and Eliminates LC Output Filter
- Thermal Shutoff and Automatic Recovery
- Compatible with earphone application
- Output Pin Short-Circuit Protection (Short to Other Outputs, Short to VCC, Short to Ground)
- Differential Signal Processing Improves CMRR

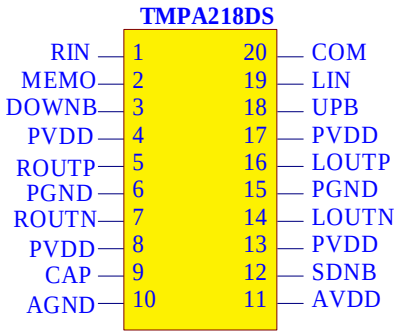
Package

TSSOP20 Available, pb free【RoHS】

For best performance, please refer to
http://www.taimec.com.tw/English/EVM.htm
http://www.class-d.com.tw/English/EVM.htm
for PCB layout.

REFERENCE CIRCUIT（Please refer to TMPA002.APP for application）

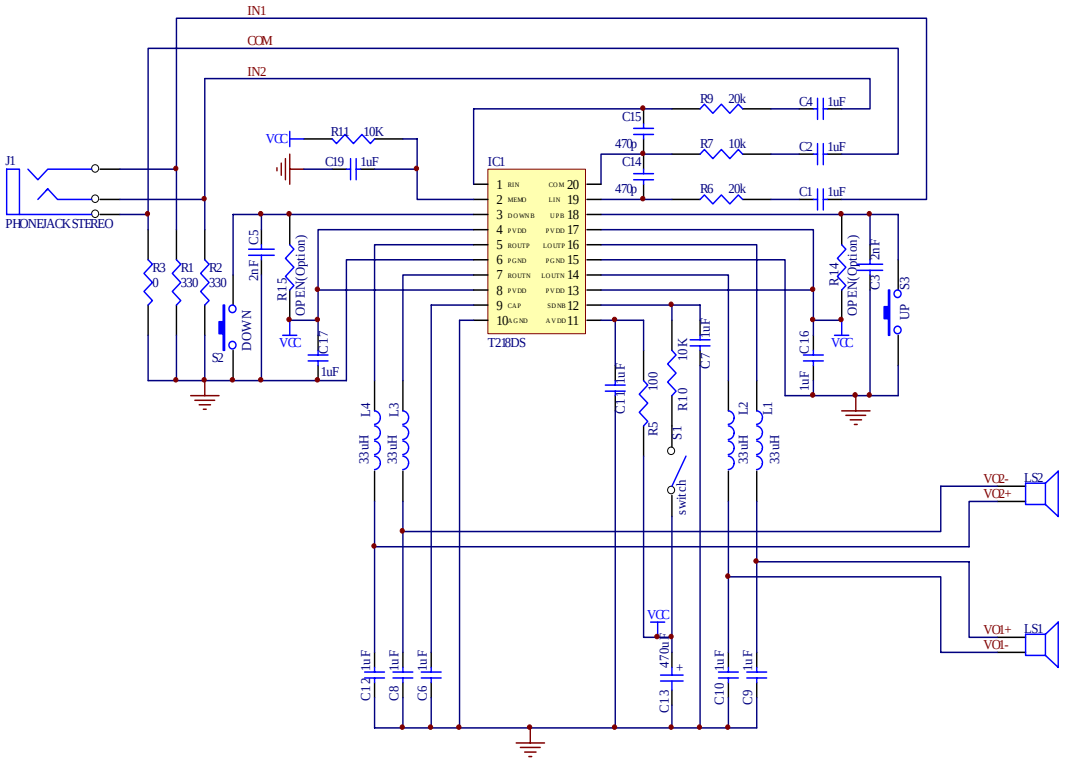




（Please email david@taimec.com.tw for complete datasheet.）

Note that the external components or PCB layout should be designed not to generate abnormal voltages to the chip to prevent from latch up which may cause damage to the device.

Typical Application



ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature range unless otherwise noted(1)

Supply voltage, V_{DD}, AV_{DD}	In normal mode	-0.3V to 6V	V
	In shutdown mode	-0.3V to 7V	V
Input voltage, V_I		-0.3V to V_{DD}+0.3V	V
Continuous total power dissipation		See package dissipation ratings	
Operating free-air temperature, T_A		-20 to 85	°C
Operating junction temperature, T_J		-20 to 150	°C
Storage temperature, T_{stg}		-40 to 150	°C

(1) Stresses beyond those listed under"absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions "is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITONS

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
Supply voltage	V_{DD}, AV_{DD}		2.5		6	V
High-level input voltage, $V_{IH}1$	VIH for SDNB	V_{DD}= AV_{DD} = 5V	2		V_{DD}	
Low-level input voltage, $V_{IL}1$	VIL for SDNB		0		0.8	
High-level input voltage, $V_{IH}2$	VIH for MEMO		70%xV_{DD}		V_{DD}	
Low-level input voltage, $V_{IL}2$	VIL for MEMO		0		30%xV_{DD}	
High-level input voltage, $V_{IH}3$	VIH for UPB, DOWNB		70%xV_{DD}		V_{DD}	
Low-level input voltage, $V_{IL}3$	VIL for UPB, DOWNB		0		30%xV_{DD}	
Operating free-air temperature, T_A			-20		85	°C

PACKAGE DISSIPATION RATINGS

PACKAGE	DERATING FACTOR	$T_A \leq 25$ °C POWER RATING	T_A = 70 °C POWER RATING	T_A = 85 °C POWER RATING
TSSOP20	8.73 mW/ °C	1.09W	698mW	567mW

ELECTRICAL CHARACTERISTICS

T_A=25 °C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\lvert V_{OS} \rvert$	Output offset voltage (measured differentially)	V_I=0V,A_V=2, V_{DD}=AV_{DD}=2.5V to 5.5V		25		mV
PSRR	Power supply rejection ratio	V_{DD}=AV_{DD}=2.5V to 5.5V		-75	-55	dB
CMRR	Common mode rejection ratio	V_{DD}=AV_{DD}=2.5V to 5.5V, V_{IC}=1Vpp, RL=8Ω		-55	-50	dB
$\lvert I_{IH1} \rvert$	High-level input current	V_{DD}=AV_{DD}=5.5V, V_I=5.8V (SDNB)		30		μA
$\lvert I_{IL1} \rvert$	Low-level input current	V_{DD}=AV_{DD}=5.5V, V_I=-0.3V (SDNB)			1	μA
$\lvert I_{IH2} \rvert$	High-level input current	V_{DD}=AV_{DD}=5.5V, V_I=5.8V (MEMO)			1	μA
$\lvert I_{IL2} \rvert$	Low-level input current	V_{DD}=AV_{DD}=5.5V, V_I=-0.3V (MEMO)			1	μA

$\|I_{IH3}\|$	High-level input current	V_{DD}=AV_{DD}=5.5V, V_I=5.8V (UPB, DOWNB)			1	μA
$\|I_{IL3}\|$	Low-level input current	V_{DD}=AV_{DD}=5.5V, V_I=-0.3V (UPB, DOWNB)		30		μA
I_Q (SD)	Shutdown current / Ch	V($\overline{SDN}$)=0.8V, V_{DD}=AV_{DD}=2.5V to 5.5V		0.2	0.5	μA
$r_{DS(on)}$	Static output resistance	V_{DD}=AV_{DD}=5.5V		790		mΩ
f(sw)	Switching frequency	V_{DD}=AV_{DD}=2.5V to 5.5V	200	250	300	kHz
Avmax	Max. BTL Gain	V_{DD}=AV_{DD}=2.5V to 5.5V, RL=8Ω	21		25	db
R_{SDN}	Resistance from SDNB to GND	V(SDNB)= 5V		200		kΩ
Rud	Resistance from UpB / DownB to VDD	V(UPB)= V(DOWNB)=5V		200		kΩ
Z_I	Input impedance	RIN,LIN		30		kΩ

OPERATING CHARACTERISTICS

T_A=25 °C, R_L=8Ω speaker (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN TYP MAX	UNIT
P_O	Output power / Ch THD+N=10%,f=1kHz. (Limited by thermal condition)	R_L=8Ω	V_{DD}=AV_{DD}=5V.	1.5	W
		R_L=4Ω		2.3	
		R_L=3Ω		2.7	
		R_L=2Ω	V_{DD}=AV_{DD}=5.5V.	3.5	
THD+N	Total harmonic distortion plus noise	V_{DD}=AV_{DD}=5V, P_O=1W, R_L=8Ω, f=1kHz		0.2	%
		V_{DD}=AV_{DD}=5V, P_O=1.5W, R_L=4Ω, f=1kHz		0.2	
		V_{DD}=AV_{DD}=5V, P_O=1.8W, R_L=3Ω, f=1kHz		0.25	
SNR	Signal-to-noise ratio	V_{DD}=AV_{DD}=5V, P_O=1W, R_L=8Ω		95	dB
Crosstalk	Crosstalk between outputs	V_{DD}=AV_{DD}=5V, P_O=1W R_L=8Ω		-68	dB

TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	PIN NO		
AGND	10	-	Analog ground
AV_{DD}	11	-	Analog power supply
CAP	9	I	Capacitance for power up delay and UPB/DOWNB reaction time
DOWNB	3	I	Volume down
PGND	6,15	-	Digital ground
COM	20	I	Common ground
LIN	19	I	Left channel input
LOUTN	14	O	Negative output of left channel
LOUTP	16	O	Positive output of left channel
RIN	1	I	Right channel input
MEMO	2	I	Memory
ROUTN	7	O	Negative output of right channel
ROUTP	5	O	Positive output of right channel
SDNB	12	I	Shutdown terminal (active low logic)

UPB	18	I	Volume up
PV_{DD}	4,8,13,17	-	Digital Power supply

TYPICAL CHARACTERISTICS

Note 1. Input coupling 1μF capacitors are used for all measurements.

2. Differential inputs are applied and BTL outputs are measured.

3. Balanced LC filter is used for THD+N measurement and power efficiency measurement.

4. Characteristic frequency of the LC filter is set 41 KHz unless otherwise specified.

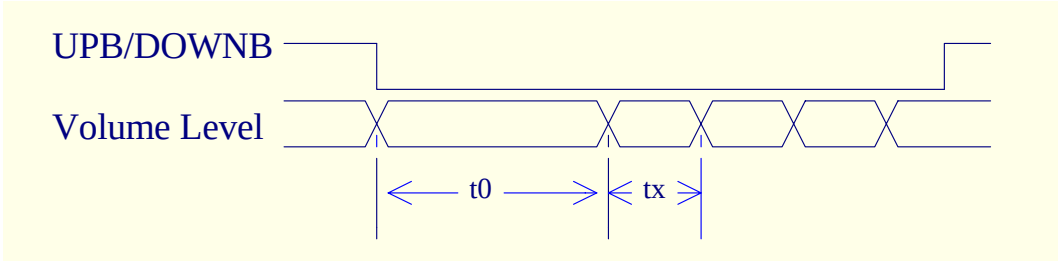
Volume Step and Attenuation at Vdd=5v

Step	Attenuation(dB)	Overall AV(dB)	Step	Attenuation(dB)	Overall AV(dB)	Step	Attenuation(dB)	Overall AV(dB)
0	0	23	11	12	11	22	36	-13
1	1	22	※ 12	14	9	23	39	-16
2	2	21	13	16	7	24	42	-19
3	3	20	14	18	5	25	45	-22
4	4	19	15	20	3	26	48	-25
5	5	18	16	22	1	27	51	-28
6	6	17	17	24	-1	28	54	-31
7	7	16	18	26	-3	29	57	-34
8	8	15	19	28	-5	30	60	-37
9	9	14	20	30	-7	31	∞	-∞
10	10	13	21	33	-10			

※ Overall gain is preset at 5db at power up.

Volume UP/DOWN Control

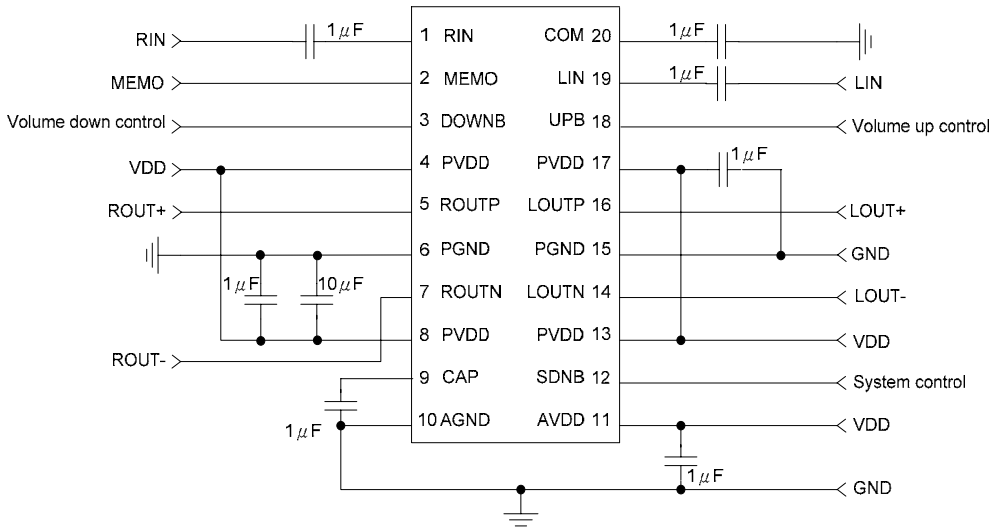
- Volume up and down control is executed by UPB and DOWNB digital input signals.
- UPB and DOWNB are “low” active.
- Continuous “low” at UPB or DOWNB will make volume to change continuously.
- A “low” at DOWNB overwrites a “low” at UPB.
- Timing diagram(capacitance at CAP pin has to be 1uF for following timing relationship)



1. First volume change is set at falling edge of UPB/DOWNB input.
2. Second volume change is set at ~0.5s(t0) after falling edge of UPB/DOWNB input.
3. Following volume changes are set at ~0.1s(tx) from previous change.

Note that the capacitance at pin CAP=1uF for t0=0.5s & t1=0.1s. The delay time t0 & t1 change linearly with capacitance at CAP pin, i.e. t0=1s & t1=0.2s if CAP=2uF.

APPLICATION INFORMATION



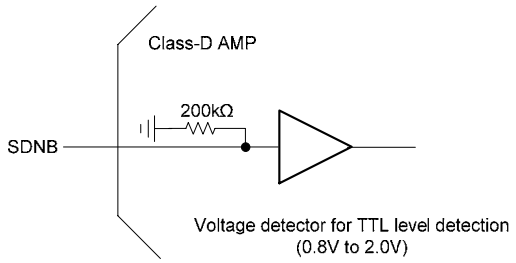
DETAILED DESCRIPTION

Efficiency

The output transistors of a class D amplifier act as switches. The power loss is mainly due to the turn on resistance of the output transistors when driving current to the load. As the turn on resistance is so small that the power loss is small and the power efficiency is high. With 8 ohm load the power efficiency can be up to 88%.

Shutdown

The shutdown mode reduces power consumption. A LOW at shutdown pin forces the device in shutdown mode and a HIGH forces the device in normal operating mode. Shutdown mode is useful for power saving when not in use. This function is useful when other devices like earphone amplifier on the same PCB are used but class D amplifier is not necessary.
Internal circuit for shutdown is shown below.



Note that shutdown pin or SDNB is also used for volume control. Please refer to Voltage Gain section for details.

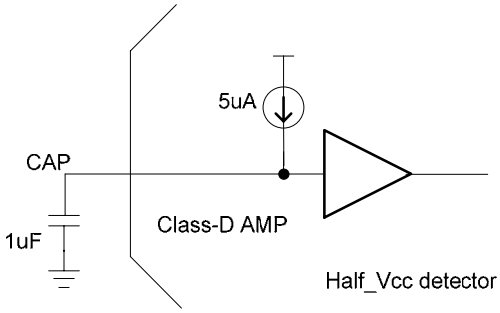
Pop-less

A soft start capacitor can be added to the CAP pin. This capacitor introduces delay for the internal circuit to be stable before driving the load. The pop or click noise when power up/down or switching in between shutdown mode can be thus eliminated. The delay time is proportional to the value of the capacitance. It is about 500ms for a capacitor of 1uF at 5v.

CAP

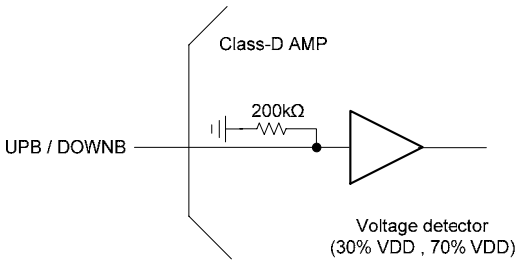
Cap provides a way of soft startup delay. A 5uA current source and a half_Vcc detector are integrated in the chip. The charged capacitor is externally hooked up. For C=1uF the half_Vcc delay is

T = CV / I = （1uF X 2.5V）/ 5uA = 0.5 seconds



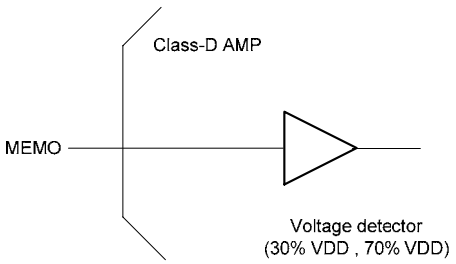
Voltage gain

The voltage gain is preset, at power up, to 5db typical with 8 ohms load. The voltage gain can be increased by applying a LOW at UPB or decreased by applying a LOW at DOWNB. The maximum gain it can reach is 23db and the minimum gain is -55db. Beyond -55db is a MUTE.



Memory of voltage gain

The voltage gain is preset to 5db at power up. The voltage gain can be changed to higher or lower value by applying a LOW at UPB or DOWNB. The changed voltage gain can be memorized during shutdown if MEMO=Vcc. In other words the voltage gain is the same before and after shutdown operation with MEMO=Vcc. Note that a RC delay is necessary between Vcc & MEMO at power up to ensure proper operation of the memory.



During shutdown mode, memory of voltage gain is still in effect even battery is removed for some time. The time period in which the voltage gain is still memorized during battery removed depends on the Vcc-GND capacitance and Vcc voltage.

Example 1. Four-battery power supply with Vcc-GND capacitance equals 1000uF.
If the voltage of each exhausted battery to be replaced is 1.0v on average then the voltage on the 1000uF capacitor is 4.0v. Since the chip can keep memory for down to 0.5v, the voltage allowed to drop is 4.0v-0.5v=3.5v. The voltage drop is caused by the small leakage of the chip, typical 0.2uA, during shutdown. So the time to survive is

CV/I =1000uF x 3.5v/ 0.2uA = 17500 sec = 4.8 hrs

Example 2. Two-battery power supply with Vcc-GND capacitance equals 1000uF.
If the voltage of each exhausted battery to be replaced is 1.0v on average then the voltage on the 1000uF capacitor is 2.0v. The voltage allowed to drop is 2.0v-0.5v=1.5v. With typical leakage current of 0.2uA the time to survive is

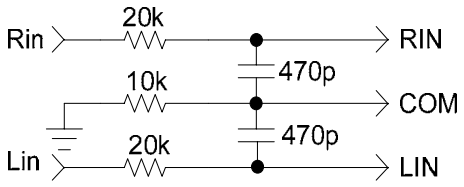
CV/I =1000uF x 1.5v / 0.2uA = 7500 sec = 2.08 hrs

Automatic output Power Control (APC)

The voltage gain is self adjusted in the chip over voltage range. This means that, regardless supply voltage change, the output power keeps about the same for a given input level from V_{DD}=5.5v to 2.5v. It allows the best use of the battery.

Input filter

Input filter is not required for most of the applications. However in some designs if it is necessary to reduce overall voltage gain, one can add an external input resistor as a voltage divider. It is advantageous to add a capacitor in between positive input and negative input to form an input filter.
An example to reduce voltage gain to 60%, as shown in the schematic on page 2, is also shown below. Note that the layout of input traces has to be symmetric.

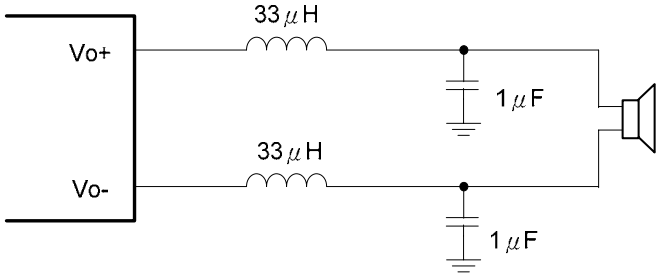


Output filter

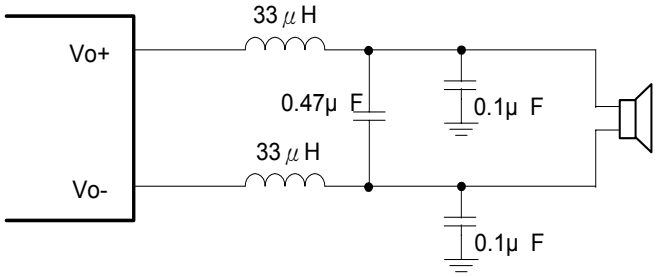
Ferrite bead filter can be used for EMI purpose. The ferrite filter reduces EMI around 1 MHz and higher（FCC and CE only test radiated emissions greater than 30 MHz）. When selecting a ferrite bead, choose one with high impedance at high frequencies, but low impedance at low frequencies.

Use an LC output filter if there are low frequency（＜1 MHz）EMI sensitive circuits and/or there are long wires from the amplifier to the speaker. EMI is also affected by PCB layout and the placement of the surrounding components.

The suggested LC values for different speaker impendence are showed in following figures for reference.



Typical LC Output Filter (1)



Typical LC Output Filter (2)

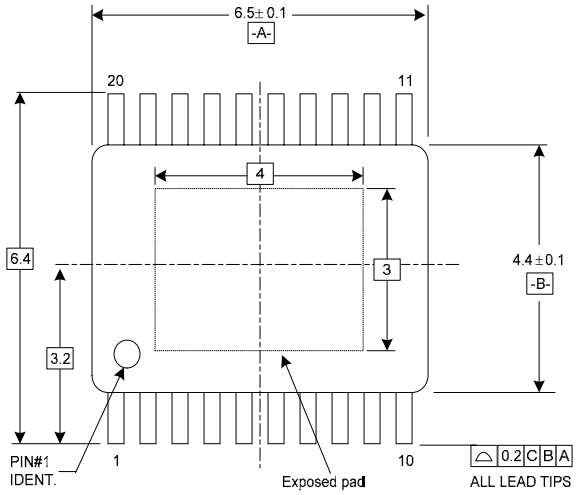
Over temperature protection

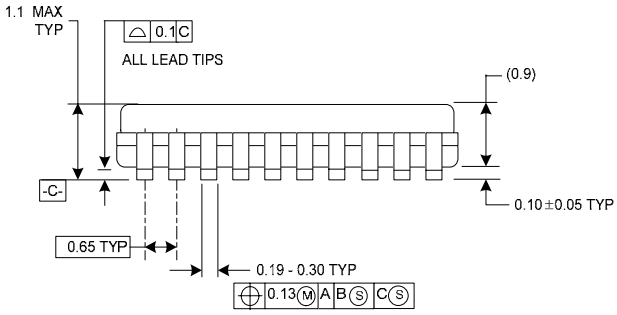
A temperature sensor is built in the device to detect the temperature inside the device. When a high temperature around 145°C and above is detected the switching output signals are disabled to protect the device from over temperature. Automatic recovery circuit enables the device to come back to normal operation when the internal temperature of the device is below around 120 °C.

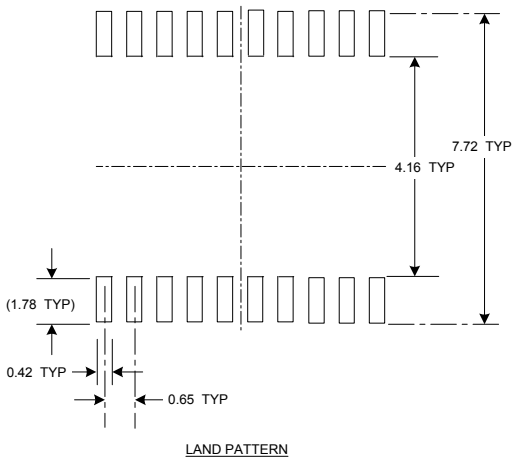
Over current protection

A current detection circuit is built in the device to detect the switching current of the output stages of the device. It disables the device when the current is beyond about 3.5amps. It protects the device when there is an accident short between outputs or between output and power/gnd pins. It also protects the device when an abnormal low impedance is tied to the output. High current beyond the specification may potentially causes electron migration and permanently damage the device. Shutdown or power down is necessary to resolve the protection situation. There is no automatic recovery from over current protection.

Physical Dimensions (IN MILLIMETERS)







TSSOP20

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