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TMPR28051 STS-1/AU-3 (STM-0) Mapper Device Advisory for Version 5 of the Device

Register Architecture (RA) Map

RA-1. Reset Bit

The software reset bit (bit 0) of register 0x00 is not functional.

RA-2. Transmit Path AIS Insert Bit

The TXPAISINS bit (bit 5) of register 0x01 produces both AIS-P and AIS-L.

RA-3. STS-1 Loss of Pointer Mask Bit

The STS1LOPMSK bit (bit 2) of register 0x04 masks both STS1LOP and STS1LOF.

RA-4. STS-1 Loss of Frame Mask Bit

The STS1LOFMSK bit (bit 1) of register 0x04 is not functional.

RA-5. VTLABCOM and VTRFIRDICOM Interrupt Bits

Occasionally, it might require multiple reads to clear the composite interrupt bits VTLABCOM (bit 2 of register 0x05) and VTRFIRDICOM (bit 4 of register 0x05).

Error Insertion (EI)

EI-1. DS1/E1 Alarm Indication Signal

The device does not insert DS1/E1 AIS towards the STS-1 if there is an LOC condition in the incoming DS1/E1 signal.

EI-2. LOC Condition in E1 Loopback Mode

In the absence of an input clock, the device detects an LOC condition and generates TU-AIS upstream, even if the loopback path is selected (the loopback signal is overwritten by TU-AIS).

Error Insertion (EI) (continued)

EI-3. False S-BIP, L-BIP, and P-BIP Error Insertion

The device transmits S-BIP, L-BIP, and P-BIP errors when configured for automatic insertion of REI, and certain STS-1 error conditions such as LOS, LOF, LOP-P, S-BIP, L-BIP, and P-BIP are inserted.

VT Alarms (VT)

VT-1. VT Path Payload Label Mismatch

The device reports PLM-V when it detects three consecutive consistent new values for the VT label. This is in compliance with G.783 Section 2.2.2.7 and T1.231 Section 8.1.3.5.2.4.2 specifications, but is not compliant with GR-253 Section 6.2.1.1.8.C.

VT-2. Failure in the Detection of VT Loss of Pointer Defects

The device also apparently fails to detect an LOP-V defect when it continuously receives a VT pointer word of 6C68 (i.e., a value indicating a VT1.5 with an offset of 104 bytes, versus a maximum valid offset of 103 bytes). In this case, the device inserts the required DS1 AIS downstream, but does not subsequently declare an LOP-V failure (nonconformance to GR 253, R6-71).

VT-3. Inappropriate Termination of VT Loss of Pointer Defect Condition

After the device has detected an LOP-V defect, it inappropriately terminates that defect upon receiving two pointer words containing the same value as the previous valid pointer. According to GR 253, an LOP-V defect must not be terminated unless a valid pointer is received in three consecutive VT superframes (nonconformance to GR 253, R6-75).

VT-4. Inappropriate Termination of VT Alarm Indication Signal Defect Condition

After the device has detected an AIS-V defect, it inappropriately terminates that defect upon receiving two pointer words containing the same value as the previous valid pointer and without a set NDF (e.g., with the N bits set to 0110). According to GR 253, an AIS-V defect must not be terminated unless a normal valid pointer is received in three consecutive VT superframes, or a valid pointer with a set NDF is received in one VT superframe (nonconformance to GR 253, R6-183).

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TMPR28051 STS-1/AU-3 (STM-0) Mapper
Device Advisory for Version 2 of the Device

Register Architecture (RA) Map

RA-1. Reset Bit

The software reset bit (bit 0) of register 0x00 is not functional.

RA-2. Transmit Path AIS Insert Bit

The TXPAISINS bit (bit 5) of register 0x01 produces both AIS-P and AIS-L.

RA-3. STS-1 Loss of Pointer Mask Bit

The STS1LOPMSK bit (bit 2) of register 0x04 masks both STS1LOP and STS1LOF.

RA-4. STS-1 Loss of Frame Mask Bit

The STS1LOFMSK bit (bit 1) of register 0x04 is not functional.

RA-5. VTLABCOM and VTRFIRDICOM Interrupt Bits

Occasionally, it might require multiple reads to clear the composite interrupt bits VTLABCOM (bit 2 of register 0x05) and VTRFIRDICOM (bit 4 of register 0x05).

Error Insertion (EI)

EI-1. DS1/E1 Alarm Indication Signal

The device does not insert DS1/E1 AIS towards the STS-1 if there is an LOC condition in the incoming DS1/E1 signal.

EI-2. LOC Condition in E1 Loopback Mode

In the absence of an input clock, the device detects an LOC condition and generates TU-AIS upstream, even if the loopback is selected (the loopback signal is overwritten by TU-AIS).

Error Insertion (EI) (continued)

EI-3. False S-BIP, L-BIP, and P-BIP Error Insertion

The device transmits S-BIP, L-BIP, and P-BIP errors when configured for automatic insertion of REI, and certain STS-1 error conditions such as LOS, LOF, LOP-P, S-BIP, L-BIP, and P-BIP are inserted.

EI-4. Forcing AIS Condition

In order to force AIS using the VTDROP bits, a value of 0x1D must be programmed for DS1 AIS, and a value of 0x1E must be programmed for E1 AIS.

VT Mapping (VT)

VT-1. VT Path Payload Label Mismatch

The device reports PLM-V when it detects three consecutive consistent new values for the VT label. This is in compliance with G.783 Section 2.2.2.7 and T1.231 Section 8.1.3.5.2.4.2 specifications, but is not compliant with GR-253 Section 6.2.1.1.8.C.

VT-2. Failure in the Detection of VT Loss of Pointer Defects

■ The device fails to detect an LOP-V defect or insert the required DS1/E1 AIS downstream when it receives VT pointer words with the N bits continuously set to 1001 (i.e., with a continuously set NDF).

■ The device also apparently fails to detect an LOP-V defect when it continuously receives a VT pointer word of 6C68 (i.e., a value indicating a VT1.5 with an offset of 104 bytes, versus a maximum valid offset of 103 bytes). In this case, the device inserts the required DS1 AIS downstream, but does not subsequently declare an LOP-V failure (nonconformance to GR 253, R6-71).

VT-3. Inappropriate Termination of VT Loss of Pointer Defect Condition

After the device has detected an LOP-V defect, it inappropriately terminates that defect upon receiving two pointer words containing the same value as the previous valid pointer. According to GR 253, an LOP-V defect must not be terminated unless a valid pointer is received in three consecutive VT superframes (nonconformance to GR 253, R6-75).

VT-4. Inappropriate Termination of VT Alarm Indication Signal Defect Condition

After the device has detected an AIS-V defect, it inappropriately terminates that defect upon receiving two pointer words containing the same value as the previous valid pointer and without a set NDF (e.g., with the N bits set to 0110). According to GR 253, an AIS-V defect must not be terminated unless a normal valid pointer is received in three consecutive VT superframes, or a valid pointer with a set NDF is received in one VT superframe (nonconformance to GR 253, R6-183).

VT Mapping (VT) (continued)

VT-5. C-Bit Decoding

In the presence of a receive SONET/SDH bit error rate, the device may destuff the DS1 from the VT1.5 incorrectly. This is the result of an error in the VT1.5 C-bit decoding process. The C-bit decoding process should be capable of correcting single errors to the C bits. Because of this error, an error in the first or second C bit for position 2 will be incorrectly decoded if the first C-bit position is calling for a stuff and the second C-bit position is not. The end result of this error is that both positions will call for a stuff, resulting in a bit being removed from the DS1 data stream. This will force downstream equipment to experience a reframe.

The minimum time to false decode severity is as shown in Table VT-5 (in terms of seconds to false decode).

Table VT-5. Minimum Time (in Seconds) to
False Decode Severity of the C Bit

BER	Theoretical	Actual
10^{-3}	125	0.25
10^{-4}	12500	2.5
10^{-5}	1250000	25
10^{-6}	1.25e+8	250
10^{-7}	1.25e+10	2500
10^{-8}	1.25e+12	2.5e+4
10^{-9}	1.25e+14	2.5e+5
10^{-10}	1.25e+16	2.5e+6

In the absence of an external bit error rate, the algorithm decodes these C bits correctly.

Test Pattern (TP) Generator/Monitor

TP-1. Test Pattern Insert

The transmitted test pattern comes out on the opposite edge with respect to the jitter-attenuated data.

TP-2. Test Pattern Drop

The test pattern detector always inverts the clock coming into the block before retiming the data.

Jitter Attenuation (JA)

JA-1. Jitter Attenuator

The digital jitter attenuator buffers are not functional. The DJACTL bit in register 0x01 should be set to 0 in this device. Putting the device in the jitter attenuator mode (DJACTL = 1) causes loss of transmission.

STS Path Overhead (POH)

POH-1. False H4LOMF Indication

Forcing a SONET/SDH line level decrement (H1, H2) from a value of either 348 or 347 results in false H4LOMF indications.

Loss of Data (LOD)

LOD-1. Loss of DS1/E1 Data

Simultaneously forcing VT pointer adjustments while forcing SONET/SDH decrements from values of 348 and 347 results in loss of DS1/E1 data.

AY99-026SONT-2 Replaces AY99-026SONT to Incorporate the Following Updates

Added issues RA-5 and EI-3 to the document.

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TMPR28051 STS-1/AU-3 (STM-0) Mapper
Device Advisory for Version 3 of the Device

Register Architecture (RA) Map

RA-1. Reset Bit

The software reset bit (bit 0) of register 0x00 is not functional.

RA-2. Transmit Path AIS Insert Bit

The TXPAISINS bit (bit 5) of register 0x01 produces both AIS-P and AIS-L.

RA-3. STS-1 Loss of Pointer Mask Bit

The STS1LOPMSK bit (bit 2) of register 0x04 masks both STS1LOP and STS1LOF.

RA-4. STS-1 Loss of Frame Mask Bit

The STS1LOFMSK bit (bit 1) of register 0x04 is not functional.

RA-5. VTLABCOM and VTRFIRDICOM Interrupt Bits

Occasionally, it might require multiple reads to clear the composite interrupt bits VTLABCOM (bit 2 of register 0x05) and VTRFIRDICOM (bit 4 of register 0x05).

Error Insertion (EI)

EI-1. DS1/E1 Alarm Indication Signal

The device does not insert DS1/E1 AIS towards the STS-1 if there is an LOC condition in the incoming DS1/E1 signal.

EI-2. LOC Condition in E1 Loopback Mode

In the absence of an input clock, the device detects an LOC condition and generates TU-AIS upstream, even if the loopback is selected (the loopback signal is overwritten by TU-AIS).

Error Insertion (EI) (continued)

EI-3. False S-BIP, L-BIP, and P-BIP Error Insertion

The device transmits S-BIP, L-BIP, and P-BIP errors when configured for automatic insertion of REI, and certain STS-1 error conditions such as LOS, LOF, LOP-P, S-BIP, L-BIP, and P-BIP are inserted.

EI-4. Forcing AIS Condition

In order to force AIS using the VTDROP bits, a value of 0x1D must be programmed for DS1 AIS, and a value of 0x1E must be programmed for E1 AIS.

VT Mapping (VT)

VT-1. VT Path Payload Label Mismatch

The device reports PLM-V when it detects three consecutive consistent new values for the VT label. This is in compliance with G.783 Section 2.2.2.7 and T1.231 Section 8.1.3.5.2.4.2 specifications, but is not compliant with GR-253 Section 6.2.1.1.8.C.

VT-2. Failure in the Detection of VT Loss of Pointer Defects

- The device fails to detect an LOP-V defect or insert the required DS1/E1 AIS downstream when it receives VT pointer words with the N bits continuously set to 1001 (i.e., with a continuously set NDF).

- The device also apparently fails to detect an LOP-V defect when it continuously receives a VT pointer word of 6C68 (i.e., a value indicating a VT1.5 with an offset of 104 bytes, versus a maximum valid offset of 103 bytes). In this case, the device inserts the required DS1 AIS downstream, but does not subsequently declare an LOP-V failure (nonconformance to GR 253, R6-71).

VT-3. Inappropriate Termination of VT Loss of Pointer Defect Condition

After the device has detected an LOP-V defect, it inappropriately terminates that defect upon receiving two pointer words containing the same value as the previous valid pointer. According to GR 253, an LOP-V defect must not be terminated unless a valid pointer is received in three consecutive VT superframes (nonconformance to GR 253, R6-75).

VT-4. Inappropriate Termination of VT Alarm Indication Signal Defect Condition

After the device has detected an AIS-V defect, it inappropriately terminates that defect upon receiving two pointer words containing the same value as the previous valid pointer and without a set NDF (e.g., with the N bits set to 0110). According to GR 253, an AIS-V defect must not be terminated unless a normal valid pointer is received in three consecutive VT superframes, or a valid pointer with a set NDF is received in one VT superframe (nonconformance to GR 253, R6-183).

VT Mapping (VT) (continued)

VT-5. C-Bit Decoding

In the presence of a receive SONET/SDH bit error rate, the device may destuff the DS1 from the VT1.5 incorrectly. This is the result of an error in the VT1.5 C-bit decoding process. The C-bit decoding process should be capable of correcting single errors to the C bits. Because of this error, an error in the first or second C bit for position 2 will be incorrectly decoded if the first C-bit position is calling for a stuff and the second C-bit position is not. The end result of this error is that both positions will call for a stuff, resulting in a bit being removed from the DS1 data stream. This will force downstream equipment to experience a reframe.

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In the absence of an external bit error rate, the algorithm decodes these C bits correctly.

Test Pattern (TP) Generator/Monitor

TP-1. Test Pattern Insert

The transmitted test pattern comes out on the opposite edge with respect to the jitter-attenuated data.

TP-2. Test Pattern Drop

The test pattern detector always inverts the clock coming into the block before retiming the data.

Device Version (DV)

DV-1. Device Version Report

The device version register, 0x16, reports the device version as 0x02.

AY99-027SONT-2 Replaces AY99-027SONT to Incorporate the Following Updates

Added issues RA-5 and EI-3 to the document.

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TMPR28051 STS-1/AU-3 (STM-0) Mapper Device Advisory for Version 4 of the Device

Register Architecture (RA) Map

RA-1. Reset Bit

The software reset bit (bit 0) of register 0x00 is not functional.

RA-2. Transmit Path AIS Insert Bit

The TXPAISINS bit (bit 5) of register 0x01 produces both AIS-P and AIS-L.

RA-3. STS-1 Loss of Pointer Mask Bit

The STS1LOPMSK bit (bit 2) of register 0x04 masks both STS1LOP and STS1LOF.

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Occasionally, it might require multiple reads to clear the composite interrupt bits VTLABCOM (bit 2 of register 0x05) and VTRFIRDICOM (bit 4 of register 0x05).

Error Insertion (EI)

EI-1. DS1/E1 Alarm Indication Signal

The device does not insert DS1/E1 AIS towards the STS-1 if there is an LOC condition in the incoming DS1/E1 signal.

EI-2. LOC Condition in E1 Loopback Mode

In the absence of an input clock, the device detects an LOC condition and generates TU-AIS upstream, even if the loopback is selected (the loopback signal is overwritten by TU-AIS).

Error Insertion (EI) (continued)

EI-3. False S-BIP, L-BIP, and P-BIP Error Insertion

The device transmits S-BIP, L-BIP, and P-BIP errors when configured for automatic insertion of REI, and certain STS-1 error conditions such as LOS, LOF, LOP-P, S-BIP, L-BIP, and P-BIP are inserted.

VT Mapping (VT)

VT-1. VT Path Payload Label Mismatch

The device reports PLM-V when it detects three consecutive consistent new values for the VT label. This is in compliance with G.783 Section 2.2.2.7 and T1.231 Section 8.1.3.5.2.4.2 specifications, but is not compliant with GR-253 Section 6.2.1.1.8.C.

VT-2. Failure in the Detection of VT Loss of Pointer Defects

- The device fails to detect an LOP-V defect or insert the required DS1/E1 AIS downstream when it receives VT pointer words with the N bits continuously set to 1001 (i.e., with a continuously set NDF).

- The device also apparently fails to detect an LOP-V defect when it continuously receives a VT pointer word of 6C68 (i.e., a value indicating a VT1.5 with an offset of 104 bytes, versus a maximum valid offset of 103 bytes). In this case, the device inserts the required DS1 AIS downstream, but does not subsequently declare an LOP-V failure (nonconformance to GR 253, R6-71).

VT-3. Inappropriate Termination of VT Loss of Pointer Defect Condition

After the device has detected an LOP-V defect, it inappropriately terminates that defect upon receiving two pointer words containing the same value as the previous valid pointer. According to GR 253, an LOP-V defect must not be terminated unless a valid pointer is received in three consecutive VT superframes (nonconformance to GR 253, R6-75).

VT-4. Inappropriate Termination of VT Alarm Indication Signal Defect Condition

After the device has detected an AIS-V defect, it inappropriately terminates that defect upon receiving two pointer words containing the same value as the previous valid pointer and without a set NDF (e.g., with the N bits set to 0110). According to GR 253, an AIS-V defect must not be terminated unless a normal valid pointer is received in three consecutive VT superframes, or a valid pointer with a set NDF is received in one VT superframe (nonconformance to GR 253, R6-183).

VT Mapping (VT) (continued)

VT-5. C-Bit Decoding

In the presence of a receive SONET/SDH bit error rate, the device may destuff the DS1 from the VT1.5 incorrectly. This is the result of an error in the VT1.5 C-bit decoding process. The C-bit decoding process should be capable of correcting single errors to the C bits. Because of this error, an error in the first or second C bit for position 2 will be incorrectly decoded if the first C-bit position is calling for a stuff and the second C-bit position is not. The end result of this error is that both positions will call for a stuff, resulting in a bit being removed from the DS1 data stream. This will force downstream equipment to experience a reframe.

The minimum time to false decode severity is as shown in Table VT-5 (in terms of seconds to false decode).

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10^{-8}	1.25e+12	2.5e+4
10^{-9}	1.25e+14	2.5e+5
10^{-10}	1.25e+16	2.5e+6

In the absence of an external bit error rate, the algorithm decodes these C bits correctly.

Device Version (DV)

DV-1. Device Version Report

The device version register, 0x16, reports the device version as 0x03.

AY99-028SONT-2 Replaces AY99-028SONT to Incorporate the Following Updates

Added issues RA-5 and E1-3 to the document.

August 5, 1999

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TMPR28051 STS-1/AU-3 (STM-0) Mapper

Features

- Maps signals in one of the following ways:
  — Maps up to 28 asynchronous DS1 signals to SONET STS-1 via VT Groups, or SDH AU-3 via TUG-2.
  — Maps up to 21 asynchronous E1 signals to SDH AU-3 via TUG-2, or SONET STS-1 via VT Groups.
  — Maps any valid combination of DS1/E1 signals at the VT Group/TUG-2 level.
- PLL-free receive operation using built-in digital jitter attenuators.
- High-speed microprocessor interface configurable to operate with most commercial microprocessors.
- Inserts valid B1, B2, and B3 bit interleaved parity (BIP) in the transmit direction.
- Detects and counts B1, B2, and B3 BIP-8 errors on either a bit or block basis for performance monitoring in the receive direction.
- Detects and counts V5 BIP-2 errors on either a bit or block basis for performance monitoring.
- Configurable continuous B1, B2, B3, and V5 BIP-2 error insertion.
- Configurable remote error indication (REI) insertion for B2, B3, and V5 BIP-2 errors.
- Detects and counts remote errors.
- Built-in test pattern insertion and drop for setup and maintenance.
- Configurable VT1.5/TU-11 slot selection for DS1 insertion and drop.
- Configurable VT2/TU-12 slot selection for E1 insertion and drop.
- Detects STS-1 path loss of pointer (LOP-P), loss of H4 multiframe (H4LOMF), path alarm indication signal (AIS-P), and path remote defect indication (RDI-P).
- Automatic receive monitor functions include VT/TU remote defect indication (RDI-V), VT/TU remote error indication (REI-V), BIP-2 errors, VT/TU AIS (AIS-V), and VT/TU loss of pointer (LOP-V).

- Automatic receive monitoring functions can be configured to provide an interrupt to the control system, or the device can be operated in a polled mode.
- User configurable for VT/TU label, AIS-V, RDI-V, REI-V, force BIP-2 errors, or unequipped tributary insertion.
- Typical 3.3 V operation with 5 V TTL tolerant I/O and boundary scan.
- –40 °C to +85 °C temperature range.
- 208-pin shrink quad flat pack (SQFP) package.
- Provides alarm and control features to easily implement the latest release of the following standards:

  GR253-CORE (12/97 with the exception of GR-253 section 6.2.1.1.8.C), G.707 (3/96), G.783 (1/94), G.823.393, T1.105-1995, T1.105.02-1995, T1.105.03-1994, T1.105.03A-1995, T1.105.07-1996, T1.105.09-1996, ETS300.147 (1/95), ETS300.417-1-1 (1/96).

Applications

- SONET/SDH path termination multiplexers
- SONET/SDH add/drop multiplexers
- SONET/SDH cross connects
- Digital access cross connects
- DS1/E1 broadcast
- SONET/SDH test equipment

Description

The Lucent Technologies Microelectronics Group TMPR28051 device is designed to map any valid combination of DS1 and E1 signals into a stream at a rate of 51.84 Mbits/s. This device provides all of the functions necessary to insert and drop any valid combination up to 28 asynchronous DS1 signals or 21 asynchronous E1 signals into an SPE.

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Description (continued)

On the STS-1 side, the device can be configured for either a serial bit stream or an 8-bit parallel bus. This allows the device to drive an OC-1 optical signal directly and also allows for modular growth in terminal or add/drop applications.

On the DS1/E1 side, the device is designed to interface with the Lucent T7698FL3/T7693 Quad Line Transceiver, or equivalent, using the internal digital jitter attenuator buffer for PLL-free operation.

The TMPR28051 device contains built-in test pattern insertion and drop that allows end-to-end testing for initial setup or maintenance without the need for external test equipment. Built-in loopbacks at both the STS-1 and DS1/E1 sides provide maximum flexibility for use in a number of SONET/SDH or DS1/E1 products including terminal multiplexers, add/drop multiplexers, and digital cross connects. A high-speed microprocessor interface and full user programmability for VT slot insertion and drop provide maximum flexibility for DS1/E1 I/O configuration.

Block Diagram

The block diagram is shown in Figure 1. For illustration purposes, only two of the DS1/E1 bidirectional blocks are shown.
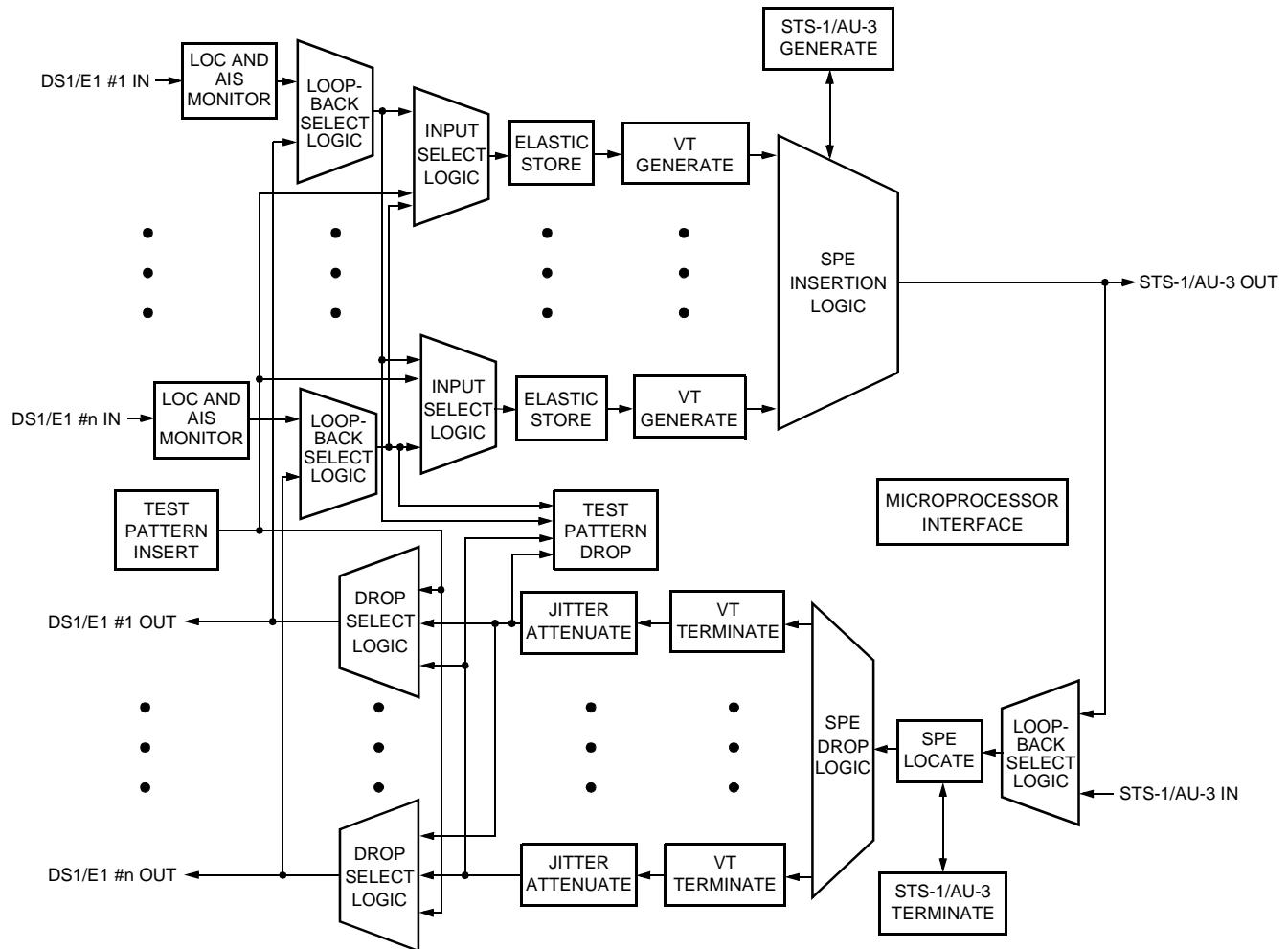
5-4875(F).ar.10

Note: "n" represents 28 or 21 for DS1 or E1, respectively.

Figure 1. Block Diagram
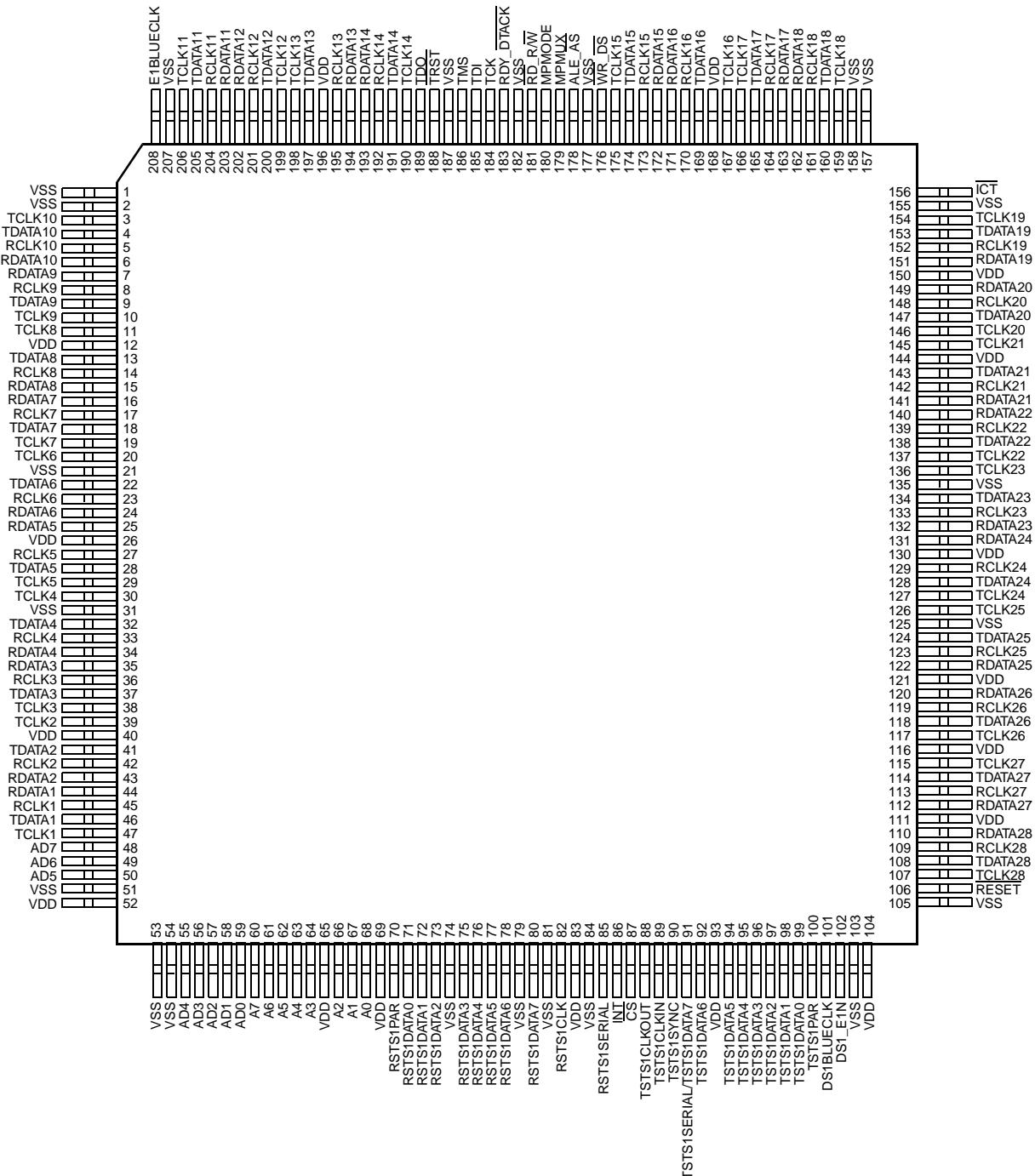
Pin Information

Figure 2. Pin Diagram of 208-Pin SQFP

5-4873(F).cr.5

Pin Information (continued)

Table 1. Pin Descriptions

Pin	Symbol	Type*	Name/Description
47, 39, 38, 30, 29, 20, 19, 11, 10, 3, 206, 199, 198, 190, 175, 167, 166, 159, 154, 146, 145, 137, 136, 127, 126, 117, 115, 107	TCLK[1:28]	O	**Transmit DS1/E1 Clock.** DS1/E1 clock output. E1 signals can only occupy TCLK[1:21].
46, 41, 37, 32, 28, 22, 18, 13, 9, 4, 205, 200, 197, 191, 174, 169, 165, 160, 153, 147, 143, 138, 134, 128, 124, 118, 114, 108	TDATA[1:28]	O	**Transmit DS1/E1 Data.** Transmit data output. E1 signals can only occupy TDATA[1:21].
45, 42, 36, 33, 27, 23, 17, 14, 8, 5, 204, 201, 195, 192, 173, 170, 164, 161, 152, 148, 142, 139, 133, 129, 123, 119, 113, 109	RCLK[1:28]	I^u	**Receive DS1/E1 Clock.** Receive clock input. These pins have an internal 20 kΩ pull-up resistor. E1 signals can only occupy RCLK[1:21].
44, 43, 35, 34, 25, 24, 16, 15, 7, 6, 203, 202, 194, 193, 172, 171, 163, 162, 151, 149, 141, 140, 132, 131, 122, 120, 112, 110	RDATA[1:28]	I^u	**Receive DS1/E1 Data.** Receive data input. These pins have an internal 20 kΩ pull-up resistor. E1 signals can only occupy RDATA[1:21].
102	DS1_E1N	I	**DS1/E1 Input Identifier.** If this pin is pulled high, the device will default to DS1 to STS-1 mode and transmit 0s in the unused overhead bytes and 00 in the SS bits of H1. If pulled low, the device will default to E1 to AU-3 mode and transmit 1s in the unused overhead bytes and 10 in the SS bits of H1. This default selection can be overridden by setting TOVERRIDE and ROVERRIDE bits in registers 0x88 (bit 0) and 0x89 (bit 0), respectively. The seven VT Groups can then be individually programmed to carry either DS1 (TVTG-1. . . 7 = 1, RVTG-1. . . 7 = 1) or E1 (TVTG-1. . . 7 = 0, RVTG-1. . . 7 = 0) signals.
101	DS1BLUECLK	I	**DS1 Blue Signal Clock.** In the event of a loss of input DS1 clock or an unprovisioned DS1 output, this clock signal is used to generate the DS1 blue signal (all 1s). This clock must be 1.544 MHz ± 32 ppm or 16 times this rate when using the digital jitter attenuator.
208	E1BLUECLK	I	**E1 Blue Signal Clock.** In the event of a loss of input E1 clock or an unprovisioned E1 output, this clock signal is used to generate the E1 blue signal (all 1s). This clock must be 2.048 MHz ± 50 ppm or 16 times this rate when using the digital jitter attenuator.

* I^u indicates an internal pull-up; I^d indicates an internal pull-down. All I/O not explicitly stated with a buffer type are 5 V TTL compatible; they will tolerate 5 V at their inputs.

Pin Information (continued)

Table 1. Pin Descriptions (continued)

Pin	Symbol	Type*	Name/Description
179	MPMUX	I	**Microprocessor Multiplex Mode.** Setting MPMUX = 1 allows the micropro-cessor interface to accept the multiplexed address and data signals. Setting MPMUX = 0 allows the microprocessor interface to accept demultiplexed (separate) address and data signals.
180	MPMODE	I	**Microprocessor Mode.** When MPMODE = 1, the device uses the address latch enable type microprocessor read/write protocol with separate read and write controls. Setting MPMODE = 0 allows the device to use the address strobe type microprocessor read/write protocol with a separate data strobe and a combined read/write control.
181	$\overline{RD}$_R/$\overline{W}$	I	**Read (Active-Low).** If MPMODE = 1, this pin is asserted low by the micropro-cessor to initiate a read cycle. **Read/Write.** If MPMODE = 0, this pin is asserted high by the microprocessor to indicate a read cycle or asserted low to indicate a write cycle.
178	ALE_$\overline{AS}$	I	**Address Latch Enable.** If MPMODE = 1, this pin becomes the address latch enable for the microprocessor. When this pin transitions from high to low, the address bus inputs are latched into the internal registers. **Address Strobe (Active-Low).** If MPMODE = 0, this pin becomes the address strobe for the microprocessor. When this pin transitions from high to low, the address bus inputs are latched into the internal registers.
87	$\overline{CS}$	I^u	**Chip Select (Active-Low).** This pin is asserted low by the microprocessor to enable the microprocessor interface (see Microprocessor Configuration Modes section on page 20). This pin has an internal 100 kΩ pull-up resistor.
86	INT	O	**Interrupt.** This pin is asserted high to indicate an interrupt produced by an alarm condition in register 3 or 5. The activation of this pin can be masked by microprocessor registers 4 and 6.
183	RDY_DTACK	O	**Ready.** If MPMODE = 1, this pin is asserted high to indicate the device has completed a read or write operation. This pin is in a high-impedance state when CS is high. **Data Transfer Acknowledge (Active-Low).** If MPMODE = 0, this pin is asserted low to indicate the device has completed a read or write operation.
48—50, 55—59	AD[7:0]	I/O	**Microprocessor Interface Address/Data Bus.** If MPMUX = 0, these pins become the bidirectional, 3-statable data bus. If MPMUX = 1, these pins become the multiplexed address/data bus.
60—64, 66—68	A[7:0]	I	**Microprocessor Interface Address.** If MPMUX = 0, these pins become the address bus for the microprocessor interface registers.
176	$\overline{WR}$_$\overline{DS}$	I	**Write (Active-Low).** If MPMODE = 1, this pin is asserted low by the micro-processor to initiate a write cycle. **Data Strobe (Active-Low).** If MPMODE = 0, this pin becomes the data strobe for the microprocessor. When R/W = 0 (write), a low applied to this pin latches the signal on the data bus into internal registers.
106	$\overline{RESET}$	I^u	**Hardware Reset (Active-Low).** If RESET is forced low, all internal states in the transceiver paths are reset and data flow through each channel will be interrupted (see Device-Level Control, Alarm, and Mask Bits (0x00—0x16) section on page 37). This pin has an internal 20 kΩ pull-up resistor.
184	TCK	I^u	**Boundary-Scan Clock.** This pin has an internal 20 kΩ pull-up resistor.

* I^u indicates an internal pull-up; I^d indicates an internal pull-down. All I/O not explicitly stated with a buffer type are 5 V TTL compatible; they will tolerate 5 V at their inputs.

Pin Information (continued)

Table 1. Pin Descriptions (continued)

Pin	Symbol	Type*	Name/Description
185	TDI	I^u	**Boundary-Scan Input Data.** This pin has an internal 20 kΩ pull-up resistor.
186	TMS	I^u	**Boundary-Scan Mode Select.** This pin has an internal 20 kΩ pull-up resistor.
188	$\overline{\text{TRST}}$	I^d	**Boundary-Scan Reset (Active-Low).** This pin has an internal 20 kΩ pull-down resistor.
189	TDO	O	**Boundary-Scan Output Data.**
89	TSTS1CLKIN	I	**Transmit STS-1 Clock.** The STS-1 clock can be 51.84 MHz for serial input data, or 19.44 MHz or 6.48 MHz for byte-wide data.
90	TSTS1SYNC	I	**Transmit STS-1 Sync.** The STS-1 sync pulse can be either J0 for 8 kHz only or a composite of J0J1V1 for 2 kHz.
92, 94—99	TSTS1DATA[6:0]	O	**Transmit STS-1 Data.** In the byte-wide output mode, this is bit 6—bit 0 of the data bus. TSTS1DATA7 is the most significant bit of the output byte.
100	TSTS1PAR	O	**Transmit STS-1 Parity.** The parity output is only defined for byte-wide data. The device can be provisioned to source either an odd or even parity.
91	TSTS1SERIAL/ TSTS1DATA7	O	**Transmit STS-1 Serial Data/Transmit STS-1 Data Bit 7 (MSB).** In serial mode, this pin provides 51.84 Mbits/s serial data. In parallel mode, this pin provides TSTS1DATA7.
88	TSTS1CLKOUT	O	**Transmit STS-1 Output Clock.**
82	RSTS1CLK	I	**Receive STS-1 Clock.** The STS-1 clock can be 51.84 MHz for serial input data, or 19.44 MHz or 6.48 MHz for byte-wide data.
80, 78—75, 73—71	RSTS1DATA[7:0]	I^u	**Receive STS-1 Data.** In the byte-wide input mode, this is the data bus with RSTS1DATA7 as the most significant bit of the input byte. This pin has an internal 100 kΩ pull-up resistor.
70	RSTS1PAR	I^u	**Receive STS-1 Parity.** The parity input is only defined for byte-wide data. The device can be provisioned to accept either an odd or even parity. This pin has an internal 100 kΩ pull-up resistor.
85	RSTS1SERIAL	I	**Receive STS-1 Serial Data.** If the device is operating in the serial mode, then RSTS1SERIAL is used as the input data pin. In the bus mode, this pin is used to synchronize byte 1 of 3 (see Figure 15, page 71).
156	$\overline{\text{ICT}}$	I^u	**In-Circuit Test Control (Active-Low).** If ICT is forced low, all output pins are placed in the high-impedance state. This pin has an internal 20 kΩ pull-up resistor.
1, 2, 21, 31, 51, 53, 54, 74, 79, 81, 84, 103, 105, 125, 135, 155, 157, 158, 177, 182, 187, 207	VSS	I	**Ground Reference for Digital Circuitry.**
12, 26, 40, 52, 65, 69, 83, 93, 104, 111, 116, 121, 130, 144, 150, 168, 196	VDD	I	**Power Supply for Digital Circuitry.**

* I^u indicates an internal pull-up; I^d indicates an internal pull-down. All I/O not explicitly stated with a buffer type are 5 V TTL compatible; they will tolerate 5 V at their inputs.

Nomenclature Assumptions

The mapping methods (VT1.5, VT2, and VT Group in ANSI nomenclature; TU-11, TU-12, and TUG-2 in ITU nomenclature) are analogous, and for the rest of this document will be referred to as VT1.5, VT2, or VT Group. STS-1 and AU-3 are also analogous with a few minor differences.

For the remainder of this document, the 51.84 Mbits/s signals are referred to as STS-1.

DS1/E1 to STS-1 Block Descriptions

In the descriptions of the block diagram of Figure 1, some of the control bits exist for each of the DS1/E1 or VT signals.

Upon start-up, the device will set all of the input data types (DS1 or E1) based on the level of the DS1_E1N pin (pin 102). DS1_E1N controls the value transmitted in the unused overhead bytes and the value of the transmitted spare bits (SS) in the H1 byte. If this pin is high, then all of the VT Groups are populated with DS1 signals. If this pin is low, then all of the VT Groups are populated with E1 signals.

This default selection can be overridden by setting TOVERRIDE and ROVERRIDE bits in registers 0x88 (bit 0) and 0x89 (bit 0), respectively. The seven VT Groups can then be individually programmed to carry either DS1 (TVTG-1 . . . 7 = 1, RVTG-1 . . . 7 = 1) or E1 (TVTG-1 . . . 7 = 0, RVTG-1 . . . 7 = 0) signals.

LOC and AIS Monitor

The incoming DS1/E1 signal is first checked for loss of clock (LOC). LOC is reported to the microprocessor via the DS1/E1LOC[1:21] and DS1LOC[22:28] bit (LOC = 1, 0 otherwise) in registers 0x17—0x32 (bit 6) and also via the AISLOCCOM composite bit in register 0x05 (bit 1). If LOC is present, the device inserts DS1/E1 AIS towards the STS-1 using the blue signal clock.

The incoming DS1/E1 data (RDATA[28:1]) is retimed immediately by the associated DS1/E1 clock (RCLK[28:1]). The edge of the clock that is used to retime the data is user-provisionable at the device level to either the rising edge (RXDS1EDGE = 1) in register 0x02 (bit 1) or falling edge (RXDS1EDGE = 0) in register 0x02 (bit 1).

After being retimed, the incoming data stream is checked for AIS. The device will declare AIS if the input data is at logic 1 for 3 ms. The device will withstand up to eight errors in the 3 ms period. AIS is reported to the microprocessor via the AISLOCCOM composite bit in register 0x05 (bit 1) and the individual DS1/E1AIS[1:21] and DS1AIS[22:28] bits in registers 0x17—0x32 (bit 7).

The blue signal clock input signal to the device can be at the exact DS1/E1 rate (1.544/2.048 MHz) or at 16 times the DS1/E1 rate (24.704/32.768 MHz), with a tolerance of 32 ppm or 50 ppm for DS1 or E1, respectively. This allows users of the Lucent Technologies T7698FL3/T7693 devices to reuse the XCLK on the board. The TMPR28051 is provisioned to accept the exact DS1 rate by default (BLUECLKSEL = 0 in bit 2 of register 0x00), but can be changed to perform the divide-by-16 function (BLUECLKSEL = 1 in bit 2 of register 0x00). The duty cycle of the clock can be 45%/55% because the data is retimed internally in the device. The duty cycle requires a much tighter tolerance when used for XCLK as described earlier.

DS1/E1 Loopback Select Logic

The first stage after retiming the signal into the device is selection of the externally received DS1/E1 (DS1/E1LB[1:21] or DS1LB[22:28] = 0) or the looped back DS1/E1 (DS1/E1LB[1:21] or DS1LB[22:28] = 1). This selection is provisionable per DS1/E1 input in registers 0x17—0x32 (bit 5).

Input Select Logic

Once the DS1/E1 data sources have been selected, the DS1/E1 for each VT tributary is selected. This selection requires 5 bits per slot to determine which DS1/E1 input to use by provisioning DS1/E1INS[4:0]_[1:21] or DS1INS[4:0]_[22:28] bits in registers 0x17—0x32 (bits 4 through 0). The range [1:28] following the _ refers to the target VT #. Refer to Table 8 on page 15 and Table 10 on page 15 for details on the VT locations within the SPE.

The numbering scheme for the five provisioned bits ranges from 00001 to 11100 where the binary value of the 5 bits corresponds to the DS1/E1 input. For instance, the value 00001 corresponds to selecting DS1/E1 #1.

The unused value of 00000 results in VT unequipped being transmitted. This is the default value for all the VT slots at powerup. VT unequipped has a valid pointer and all-zero payload.

The unused values of 11101—11110 will cause AIS-V to be inserted for that VT slot.

DS1/E1 to STS-1 Block Descriptions
(continued)

Input Select Logic (continued)

The value of 11111 will cause the internally generated test pattern to be inserted for that VT slot.

There are no restrictions on the number of VT slots that any given DS1/E1 input can supply (e.g., up to 28 VT1.5 slots can select the same DS1 input).

This block can also be used to insert the test pattern (see Test Pattern Insert section on page 19).

Elastic Store

The selected DS1/E1 clock and data signals are fed to an elastic store that is used to synchronize the incoming DS1/E1 to the local STS-1 clock. This block determines the need for positive/zero/negative (P/Z/N) stuffing for each input. Data that is transmitted from this block is synchronized to the local transmit STS-1 clock (TSTS1CLK). This block allows the device to accept DS1 signals at 1.544 Mbits/s ± 130 ppm with up to ±5 unit intervals peak jitter, or E1 signals at 2.048 Mbits/s ± 130 ppm with up to ±5 unit intervals peak jitter.

VT Generate

This block generates the VT superframe. Unless AIS-V is being forced, the superframe is built with a fixed output pointer value of decimal 78 in all the VT1.5 slots. The VT size field is set to 11 binary, and the new data flag is set to 0110 binary. This corresponds to 0x6C4E for the V1 and V2 bytes within the VT1.5 superframe.

Also, unless AIS-V is being forced, the superframe is built with a fixed output pointer value of decimal 105 in all the VT2 slots. The VT size field is set to 10 binary, and the new data flag is set to 0110 binary. This corresponds to 0x6869 for the V1 and V2 bytes within the VT2 superframe.

In this block, the DS1/E1 data is placed into the VT, and the VT overhead is generated. The format of the VT overhead byte, V5, is shown in Table 2.

Table 2. VT1.5 Overhead Byte Format (V5)

Bit #	1	2	3	4	5	6	7	8
	BIP-2		REI-V	RFI-V	Signal Label			RDI-V

Each VT can be provisioned to insert AIS-V by assigning VTAISINS[1:28] = 1 in registers 0x4F—0x6A (bit 3). AIS-V consists of overwriting the entire VT payload and overhead with ones.

RDI-V can be automatically inserted by the device (VTRFIRDIEN[1:28] = 1 in registers 0x4F—0x6A, bit 6) or written into the V5 byte under control of the microprocessor (VTRFIRDIEN[1:28] = 0 in registers 0x4F—0x6A, bit 6). In the automatic mode, the values for bit 4 (RFI-V) and bit 8 (RDI-V) are defined in Table 3. The automatic insertion mode may not meet the different standards body requirements unless the VT PTE at both ends of the path (and any intermediate NEs provisioned to perform intermediate-path PM on that path) support the protocol defined in Table 3. To meet the different standards requirements, the microprocessor mode allows programming the RDI-V and RFI-V bits in registers 0x4F—0x6A by programming VTRFIINS[1:28] (bit 5) and VTRDIINS[1:28] (bit 4), respectively.

Table 3. RFI-V, RDI-V Description

Bit 4	Bit 8	Description
0	0	No alarm
0	1	AIS-V or LOP-V
1	0	VT payload mismatch
1	1	VT unequipped

The VT label for each VT is also provisionable through the microprocessor by programming the VTLABINS[2:0]_[1:28] in registers 0x4F—0x6A, bit 2 through bit 0.

DS1/E1 to STS-1 Block Descriptions

(continued)

VT Generate (continued)

In addition to generating the superframe, this block automatically generates the BIP-2 signal. Each VT can be configured to intentionally insert continuous BIP-2 errors for troubleshooting purposes (BIP2ERINS[1:28] = 1 in bit 7 of registers 0x4F—0x6A). This BIP error insert field forces errors on both BIP-2 bits.

The resultant VT1.5 and VT2 superframes are shown in Table 4 and Table 5,

Where:

Byte[24/32:1] = information bit

O = overhead bit

R = fixed stuff bit

V1, V2, V3 = pointer and pointer action bytes

S1, S2 = stuff opportunity bits

V4 = reserved

C1, C2 = stuff indication bits

V5 = VT overhead byte

J2, Z6/N2, Z7/K4 = unused

Table 4. VT1.5 Superframe

	V1
	V5
	RRRRRRIR
	Byte 1
	:
	Byte 24
	V2
	J2
	C1C2OOOOIR
	Byte 1
	:
	Byte 24
VT1.5 Superframe	V3
	Z6/N2
	C1C2OOOOIR
	Byte 1
	:
	Byte 24
	V4
	Z7/K4
	C1C2RRRS1S2R
	Byte 1
	:
	Byte 24

Table 5. VT2 Superframe

V1	
V5	
RRRRRRRR	
Byte 1	
:	
Byte 32	
RRRRRRRR	
V2	
J2	
C1C2OOOORR	
Byte 1	
:	
Byte 32	
RRRRRRRR	
V3	VT2 Superframe
Z6/N2	
C1C2OOOORR	
Byte 1	
:	
Byte 32	
RRRRRRRR	
V4	
Z7/K4	
C1C2RRRRRS1	
S2 Byte 1[6:0]	
:	
Byte 32	
RRRRRRRR	

DS1/E1 to STS-1 Block Descriptions
(continued)

VT Generate (continued)

The device would transmit 0 in each of the O bits when the DS1_E1N pin is pulled high. If DS1_E1N is pulled low, the device will transmit 1 in each of the O bits.

The R bits are always set to 1.

The device transmits all 1s in the J2, Z6/N2, and Z7/K4 bytes.

The device can be configured such that any detected BIP-2 errors in the VT receive side result in REI-V being written into the corresponding transmit VT slot (when REI_EN = 1 in bit 7 of register 0x01).

STS-1/AU-3 Generate

The device generates an STS-1 signal based on an incoming clock (TSTS1CLK) and frame sync pulse (TSTS1SYNC). The frame sync pulse can be a single clock-period wide to indicate an 8 kHz sync, or it can contain pulses in three clock periods to indicate a composite 2 kHz sync. (See the Transmit Sync Timing section, page 70.)

The STS-1 frame is 9 rows x 90 columns that repeats at an 8 kHz rate. Each column is 1-byte wide. The STS-1 frame contains three columns of transport overhead, one column of path overhead, and 86 columns of payload.

The 36 bytes of STS-1 overhead are allocated as shown in Table 6.

Table 6. STS-1 Overhead Byte Allocation

	Col. 1	Col. 2	Col. 3	Col. 4
Row 1	A1	A2	J0	J1
Row 2	B1	E1	F1	B3
Row 3	D1	D2	D3	C2
Row 4	H1	H2	H3	G1
Row 5	B2	K1	K2	F2
Row 6	D4	D5	D6	H4
Row 7	D7	D8	D9	Z3/F3
Row 8	D10	D11	D12	Z4/K3
Row 9	S1	M0	E2	Z5/N1

The overhead bytes that are inserted by the device are described below. All of the remaining overhead bytes are given a fixed value of all 0s when DS1_E1N (bit 0 in register 0x07) is high, or all 1s when DS1_E1N is low.

The device inserts the correct frame pattern of 0xF628 into the A1 and A2 bytes.

The device inserts a fixed value of 0x01 into the J0 byte.

The device generates and inserts valid B1, B2, and B3 BIP-8 even parity bytes into the STS-1 overhead. These bytes are forced to odd parity when B[1:3]ERRINS = 1 in bit 6 through bit 4 of register 0x00.

The device will provide an STS-1 pointer with a fixed value of 522 (decimal) with 0110 in the new data flag (NDF) bits. The SS bits are determined by the level of the DS1_E1N pin. When this pin is high, the device puts 00 in the SS bits. When this pin is low, the device puts 10 in the SS bits. This pointer value indicates that the J1 path overhead byte follows immediately after the J0 line overhead byte.

The J1 byte is used for path trace. This byte repetitively transmits a 64-byte fixed length sequence to verify end-to-end connectivity. These 64 bytes are program-mable by the microprocessor by provisioning TJ1BYTE[7:0]_[64:1] in registers 0xC0—0xFF (when TJ1BYTE = 1 in register 0xBF). The method for pro-gramming these bits is described in detail in the regis-ter description of the transmit J1 path trace bytes, page 59.

The F2 byte can be provisioned by the microprocessor (F2INS-[7:0]) in register 0x10.

The device inserts a value of 0x02 into the C2 byte, indicating VT structured STS-1 SPE.

The three least significant bits of the K2 byte can be provisioned by the microprocessor (K2INS-[6:8]) in reg-ister 0x11.

The four least significant bits of the S1 byte can be pro-visioned by the microprocessor (S1INS-[3:0]) in regis-ter 0x13.

The M0 byte is used to report B2 line REI (REI-L) when REI_EN = 1 in register 0x01. This register contains the number of B2 BIP-8 errors detected in the current receive frame circuitry when REI_EN = 1 (bit 7 0f regis-ter 0x01). Valid values for these 4 bits are 0000—1000.

The G1 byte is used to convey path condition and per-formance back to the far end. The format of the G1 byte is shown in Table 7.

Table 7. G1 Path Condition/Performance Byte Format

Bit #	1	2	3	4	5	6	7	8
	REI-P				User-Provisioned RDI-P			

DS1/E1 to STS-1 Block Descriptions

(continued)

STS-1/AU-3 Generate (continued)

Path remote error indicator (REI-P) reports the number of remote errors. The four REI-P bits contain the number of B3 BIP-8 errors detected in the current frame when REI_EN = 1 (bit 7 of register 0x01). Valid values for these 4 bits are 0000—1000. The path remote defect indicator (RDI-P) bits report back such conditions as receive AIS-P, signal failure, and path trace mismatch. These bits, 5 through 8 of the G1 byte (G1INS-[5:8] in register 0x11), are user programmable by the microprocessor and are **not** inserted automatically by the device.

The H4 byte is inserted using the reduced H4 coding sequence format, where the 6 most significant bits are ones, and the 2 least significant bits take on the following values: 00-01-10-11-00, etc. The value of 00 indicates that the next STS-1 SPE contains the V1 overhead byte.

The STS-1 can be provisioned to send AIS-P (TXPAISINS = 1 in bit 5 of register 0x01). Writing AIS-P consists of writing all 1s into the H1—H3 bytes and the entire SPE.

The transmitted STS-1 can be configured to scramble the output data (STS1SCR = 1 in bit 2 of register 0x01) or transmit the data without scrambling (STS1SCR = 0 in bit 2, register 0x01). It is useful to turn off SONET scrambling if the data is going to be immediately multiplexed into a higher rate SONET signal. When STS1SCR = 1 in register 0x01, the device scrambles the outgoing STS-1 frame according to the SONET frame synchronous scrambling sequence $1 + x^6 + x^7$. The sequence is reset to 1111111 at the beginning of the byte following the C1 byte and scrambles all of the STS-1 data except the A1, A2, and C1 bytes. When this bit is 0, then the transmit data is not scrambled by the device.

SPE Insertion Logic

In addition to the one column of path overhead and 84 columns of VT payload, the STS-1 SPE also contains two columns of fixed stuff bytes. The path overhead is located in column #1, while column #30 and column #59 contain the fixed stuff bytes. The remaining columns contain the interleaved VT data as shown in Table 8.

The SPE insertion logic block acts in conjunction with the STS-1 frame generate block to place the VT information in the transmitted data stream.

The cross-referencing between the VT1.5 # listed in Table 8 and the standard format (VT Group #, VT #) listed in GR-253-CORE section 3.2.4 is shown in Table 9.

The cross-referencing between the VT2 # listed in Table 10 and the standard format (VT Group #, VT #) listed in GR-253-CORE section 3.2.4 is shown in Table 11.

DS1/E1 to STS-1 Block Descriptions (continued)

SPE Insertion Logic (continued)

Table 8. VT1.5 SPE Insertion Format

SPE Column #	1	2	3	4	5	6	7	8	9	10	11		28	29	30	31	32		57	58	59	60	61	62		81	82	83	84	85	86	87
	PATH OH	VT1.5 #1	VT1.5 #2	VT1.5 #3	VT1.5 #4	VT1.5 #5	VT1.5 #6	VT1.5 #7	VT1.5 #8	VT1.5 #9	VT1.5 #10	•••	VT1.5 #27	VT1.5 #28	FIXED	VT1.5 #1	VT1.5 #2	•••	VT1.5 #27	VT1.5 #28	FIXED	VT1.5 #1	VT1.5 #2	VT1.5 #3	•••	VT1.5 #22	VT1.5 #23	VT1.5 #24	VT1.5 #25	VT1.5 #26	VT1.5 #27	VT1.5 #28

Table 9. Mapping of VT1.5 # to (VT Group #, VT #)

VT1.5 #	(VT Group #, VT #)	VT1.5 #	(VT Group #, VT #)	VT1.5 #	(VT Group #, VT #)	VT1.5 #	(VT Group #, VT #)
1	1, 1	8	1, 2	15	1, 3	22	1, 4
2	2, 1	9	2, 2	16	2, 3	23	2, 4
3	3, 1	10	3, 2	17	3, 3	24	3, 4
4	4, 1	11	4, 2	18	4, 3	25	4, 4
5	5, 1	12	5, 2	19	5, 3	26	5, 4
6	6, 1	13	6, 2	20	6, 3	27	6, 4
7	7, 1	14	7, 2	21	7, 3	28	7, 4

Table 10. VT2 SPE Insertion Format

SPE Column #	1	2	3	4	5	6	7	8	9	10	11		28	29	30	31	32		57	58	59	60	61	62		81	82	83	84	85	86	87
	PATH OH	VT2 #1	VT2 #2	VT2 #3	VT2 #4	VT2 #5	VT2 #6	VT2 #7	VT2 #8	VT2 #9	VT2 #10	•••	VT2 #6	VT2 #7	FIXED	VT2 #8	VT2 #9	•••	VT2 #13	VT2 #14	FIXED	VT2 #15	VT2 #16	VT2 #17	•••	VT2 #15	VT2 #16	VT2 #17	VT2 #18	VT2 #19	VT2 #20	VT2 #21

Table 11. Mapping of VT2 # to (VT Group #, VT #)

VT2 #	(VT Group #, VT #)	VT2 #	(VT Group #, VT #)	VT2 #	(VT Group #, VT #)
1	1, 1	8	1, 2	15	1, 3
2	2, 1	9	2, 2	16	2, 3
3	3, 1	10	3, 2	17	3, 3
4	4, 1	11	4, 2	18	4, 3
5	5, 1	12	5, 2	19	5, 3
6	6, 1	13	6, 2	20	6, 3
7	7, 1	14	7, 2	21	7, 3

DS1/E1 to STS-1 Block Descriptions
(continued)

SPE Insertion Logic (continued)

The device can transmit the data as either a serial bit stream (TXSERIAL = 1 in register 0x02, bit 6) or as a parallel byte of data (TXSERIAL = 0 in register 0x02, bit 6). There are two parallel modes of operation: bus mode and nonbus mode. Bus mode allows multiple TMPR28051 devices to operate on a 19.44 MHz bus; in nonbus mode, the device transmits data in a point-to-point fashion at 6.48 MHz. In either parallel mode, the device sends a parity bit with the data. This parity bit is configurable to be either odd (TXPARITY = 1 in register 0x02, bit position 4) or even (TXPARITY = 0 in register 0x02, bit position 4) parity.

The bus mode of operation requires the device to select which STS-1 time slot of the three that are available to transmit data. The TBUSMODE bit (bit 2) in register 0x12 determines whether the device operates in bus mode (TBUSMODE = 1) or nonbus mode (TBUSMODE = 0). By default, the device powers up in bus mode. The TBUSPOS bits (bit 1 and bit 0) in register 0x12 determine in which of the three time slots the device transmits. By default, the device does **not** transmit (TBUSPOS-[1:0] = 00 in register 0x12), but it can be configured to transmit during any of the three STS-1 time slots on the 19.44 MHz bus.

In all three modes, the device frame sync input allows the 8 kHz STS-1 frames as well as the 2 kHz VT superframes to be aligned.

STS-1 to DS1/E1 Block Descriptions

Loopback Select Logic

The device can be configured to loop back the transmit STS-1 (STS1LB = 1 in bit 0 of register 0x01) or accept the receive STS-1 signal (STS1LB = 0 in bit 0 of register 0x01). When the receive STS-1 signal is selected, the user can configure which edge of the clock to use to retime the data (RXSTS1EDGE = 1 in bit 3 of register 0x02 uses the rising edge; RXSTS1EDGE = 0 in bit 3 of register 0x02 uses the falling edge).

SPE Locate

The device can receive data as either a serial bit stream (RXSERIAL = 1 in bit 7 of register 0x02) or as a parallel byte (RXSERIAL = 0 in bit 7 of register 0x02). In the parallel mode, the device receives a parity bit

with the data. This bit is configurable to odd (RXPARITY = 1 in bit 5 of register 0x02) or even (RXPARITY = 0 in bit 5 of register 0x02) parity. Errors in this bit are reported to the microprocessor (RXPARER in bit 6 of register 0x03).

The bus mode of operation is similar to normal operation in the DS1/E1 to STS-1 direction. The device defaults to the bus mode (RBUSMODE = 1 in bit 5 of register 0x12) of operation and listens to none of the receive channels (RBUSPOS-[1:0] = 00 in bit 4 and bit 3 of register 0x12). The sync pulse is used only to define time slot #1 of the three that are possible. Bus mode operation requires at least one sync pulse to define the time slot.

The STS-1 locate block performs the functions necessary to locate the SPE. The device will frame on the incoming STS-1 signal, and indicate when it is in the out of frame (OOF) condition (STS1OOF = 1 in bit 0 of register 0x03) or loss of frame (LOF) condition (STS1LOF = 1 in bit 1 of register 0x03). Loss of frame is defined as being in the OOF condition for 3 ms or more. Both the OOF and LOF are current state conditions; they hold their value for a minimum of 500 μs after the event. The indications reset if the condition is no longer true.

The device monitors the received data bytes for continuous ones or zeros. If the number of continuous data bytes exceeds the provisioned value (LOSDET-[7:0] in register 0x91), then loss of signal (STS1LOS = 1 in bit 0 of register 0x05) is declared. If the value in LOSDET-[7:0] in register 0x91 is 0x00, then LOS is **not** declared.

STS-1/AU-3 Terminate

The STS-1 terminate block can descramble the output data (STS1DSCR = 1 in bit 1 of register 0x01) or output the received data without descrambling (STS1DSCR = 0 in bit 1 of register 0x01). It is useful to turn off descrambling if the data is received locally from a higher-rate signal where descrambling has already taken place.

For performance monitoring purposes, there are a number of BIP and REI error counters (registers 0xC0—0xFF) in the receive section of the device. All of these internal counters are comprised of a running error counter and a hold register that presents stable results to the microprocessor. The counts in all of the running counters are latched to the hold registers when LATCH_CNT (bit 3) in register 0x00 is written from 0 to 1. This also resets all of the running counters. The results are then held until read by the microprocessor.

STS-1 to DS1/E1 Block Descriptions
(continued)

STS-1/AU-3 Terminate (continued)

All of the internal counters have the ability to store more than one second of counts. As long as the LATCH_CNT (bit 3) in register 0x00 occurs every second or faster, no counts will be lost. In case this does not happen, all of the running counters will hold their maximum value rather than roll over to zeros.

The device performs pointer interpretation on the incoming signal to locate the start of the SPE. The pointer interpretation block will indicate when the device is in the path loss of pointer (LOP-P) or path AIS (AIS-P) condition.

Loss of pointer condition is declared as the result of either of the following conditions:

1. Continuous NDF—If the device receives 1001 in the NDF field for nine consecutive frames, then LOP-P is declared.

2. Invalid pointer values—If the device receives nine frames consecutively of a pointer that is not a normal value, NDF, AIS-P, increment, or decrement, then LOP-P is declared. The SS bits do not contribute to LOP-P when DS1_E1N is high; otherwise, a non-10 value in the SS bits **will** contribute to LOP-P.

AIS-P is declared on three consecutive frames with all 1s in the H1 and H2 bytes.

AIS-P and LOP-P are mutually exclusive conditions. If neither STS1PAIS (bit 3 in register 0x03) or STS1LOP (bit 2 in register 0x03) is a logic 1, then the pointer interpreter declares a normal pointer. As part of the normal operation, the device will respond appropriately to valid NDF, increment, and decrement indications. Increment and decrement operations will be counted by the device and presented to the microprocessor via the SPTR+[7:0] and SPTR–[7:0] bits in registers 0xFE and 0xFF, respectively.

The B1, B2, and B3 BIP-8 values are recalculated and compared to the received values. Any differences are counted by the appropriate error counter (B[1:3]BIPCNT-[15:0] in registers 0xC0—0xC5 when BIP_CNTS = 1 in register 0xBF). In addition, B2 and B3 REI errors are also counted in registers 0xC2—0xC5 (B[2:3]REI-[15:0]; register 0xBF settings: REI_CNTS = 1 and BIP_CNTS = 0). The running and latched counts for both B1 and B2 counters are held at zero during OOF. The running and latched counts for B3 counters are held at zero during OOF as well as LOP-P.

The device can be provisioned to count bits in error (BIPBLKCNT = 0 in bit 1 of register 0x00) or blocks in error (BIPBLKCNT = 1 in bit 0 of register 0x00).

The J1 byte is terminated within the device. This consists of writing the receive J1 sequentially in a 64-byte register (modulo 64).

At start-up, the receive J1 byte register is all 0s. Whenever the received J1 byte value does not match the current J1 byte in the register, the path trace mismatch TRACEER bit (bit 7 in register 0x03) is set to logic 1. This allows the user to read the 64-byte register once, and then ignore it unless differences are received. TRACEER bit (bit 7 in register 0x03) is masked during AIS-P and LOP-P.

The F2 byte (F2-[7:0] in register 0x0B), the C2 byte (C2-[7:0] in register 0x0C), the 3 least significant bits of the K2 byte (K2-[6:8] in register 0x0D), the 4 least significant bits of the S1 byte (S1-[3:0] in register 0x14), and the 4 least significant bits of the G1 byte (G1-[5:8] in register 0x0D) are monitored by the microprocessor. The number of consistent, consecutive frames to update the values of all of these monitored bytes can be set by the user to anywhere between 2 and 15 frames (F2#DET-[3:0] in register 0x0E, C2#DET-[3:0] in register 0x0E, K2#DET-[3:0] in register 0x0F, G1#DET-[3:0] in register 0x0F). None of these registers will update during OOF condition.

SPE Drop Logic

The SPE drop logic uses the H4 multiframe indicator to identify the V1 byte and drop the data to the correct VT termination blocks. Loss of multiframe synchronization will be reported to the microprocessor (H4LOMF = 1 in bit 4 of register 0x03).

VT Terminate

The VT terminate block performs VT pointer interpretation on the received signal to locate the VT overhead. LOP-V (VTLOP[1:28] bit 6 in registers 0x6B—0x86) and AIS-V (VTAIS[1:28] bit 3 in registers 0x6B—0x86) are reported to the microprocessor. LOP-V is declared as a result of either of the following conditions:

1. Continuous NDF—If the device receives 1001 in the NDF field for nine consecutive superframes, then LOP-V is declared.

2. Invalid pointer values—If the device receives nine frames consecutively of a pointer that is not a normal value, NDF, AIS-V, increment, or decrement, then LOP-V is declared. The SS bits **do** contribute to LOP-V.

STS-1 to DS1/E1 Block Descriptions
(continued)

VT Terminate (continued)

AIS-V is declared on three consecutive superframes with all 1s in the V1 and V2 bytes.

AIS-V and LOP-V are mutually exclusive conditions. If neither VTAIS[1:28] (bit 3 in registers 0x6B—0x86) or VTLOP[1:28] (bit 6 in registers 0x6B—0x86) is a logic 1, then the pointer interpreter declares a normal pointer. As part of the normal operation, the device will respond appropriately to valid NDF, increment, and decrement indications. Increment and decrement operations will be counted by the device and presented to the microprocessor via bits VT[1:28]PTR+[3:0] in registers 0xC6—0xFF (BIP_CNTS = 1), and via VT[1:28]PTR–[3:0] in registers 0xC6—0xFF (REI_CNTS = 1 and BIP_CNTS = 0), respectively.

Mismatches between the expected VT size bits, bit 11 for VT1.5 and bit 10 for VT2, and the actual received SS size bits are reported to the microprocessor VTSIZEER[1:28] bit (bit 7 in registers 0x6B—0x86).

Once the V5 byte is located, the device checks for received BIP-2 errors (B2BIPCNT-[15:0] in registers 0xC0—0xC1 when BIP_CNTS bit in register 0xBF is set to 1) and received REI (B[2:3]REI-[15:0] in registers 0xC2—0xC5 when REI_CNTS and BIP_CNTS in register 0xBF are set to a 1 and 0, respectively). In addition to reporting the occurrence of BIP-2 errors and REI, the device also maintains a count of each of these on a per VT basis (VTREI[7:0]_[1:28] in registers 0xC7—0xFD: REI_CNTS = 1, BIP_CNTS = 0, and BIP2CNT[7:0]_[1:28] in registers 0xC7—0xFD: BIP_CNTS = 1). These running and latched counts for both BIP-2 and REI counters are held at zero during OOF, LOP-P, LOP-V, and AIS-V.

Additionally, the device checks for received RFI-V and RDI-V (bit 5 and bit 4, respectively, in registers 0x6B—0x86) and received VT label (VTLAB[2:0]_[1:28], bit 2 through bit 0 in registers 0x6B—0x86). Whenever the device receives three consecutive consistent values for the VT label fields that are different from the current values, it latches the new value and reports the change to the microprocessor. When a 1 is received in VTRDI0_[1:28], bit 4 in registers 0x6B—0x86 (represents bit 8 of the VT V5 overhead byte), for 10 consecutive superframes, it declares an RDI-V condition.

Jitter Attenuate

Each of the 28 VTs has a built-in digital jitter attenuator to remove the effects of mapping jitter and pointer adjustment jitter. The bits in registers 0x8A—0x8F are used to control various aspects of the digital jitter attenuator. Two programmable terms are used to set the 2nd-order loop damping factor and natural frequency of the PLL. These terms are the gain threshold, set by DJAGTHR[23:0] in registers 0x8D—0x8F, and scale value, set by DJASCALE[15:0] in registers 0x8B—0x8C. The PLL bandwidth can be set using the above registers to accommodate various system constraints.

The digital jitter attenuator block can be enabled by setting the bit DJACTL = 1 (bit 4) in register 0x01. These digital jitter attenuators require a blue signal clock that runs at 16 times the nominal output rate.

The digital jitter attenuators are designed to meet current jitter specifications as well as maximum time interval error (MTIE) requirements. The clock transmitted from this block nominally has a 50% duty cycle. The jitter attenuator block can be bypassed by setting DJACTL = 0 (bit 4) in register 0x01. If this block is bypassed, the output produces gapped clock and data.

Drop Select Logic

Once the VT has been terminated, the source VT for each DS1/E1 output is selected. This selection requires 5 bits per slot to determine which VT to use by programming VTDROP[4:0]_[1:28] bits (bits 4 through 0 in registers 0x33—0x4E). The numbering scheme for the five provisioned bits ranges from 00001 to 11100, where the binary value of the 5 bits corresponds to the VT source. For instance, the value 00001 corresponds to selecting VT Group 1, VT #1.

The unused values of 00000 and 11101—11110 will cause AIS to be inserted for that DS1 output. By default, all DS1/E1 outputs reset to a value of 00000 on powerup, which causes all of the DS1/E1s to transmit AIS (all 1s) using the blue signal clock.

The value of 11111 will insert the test pattern as described next.

Test Pattern Block Descriptions

The device contains a test pattern generator and a test pattern detector for use in maintenance and trouble-shooting.

Test Pattern Insert

The test pattern generator is capable of transmitting four different test patterns (XMT_PAT-[1:0] in bit positions 0 and 1 of register 0x08). In addition to a $2^{15} - 1$, a $2^{20} - 1$, and a $2^{23} - 1$ sequence, the device can also transmit a QRSS sequence. The QRSS pattern is a $2^{20} - 1$ pseudorandom bit sequence defined by the equation $1 + x^{17} + x^{20} = 0$, with a 14 zero limit.

As can be seen in Figure 1 on page 5, this test pattern can be inserted in the place of any of the transmitted **or** received DS1/E1 signals. The test pattern can also be provisioned to be framed (XMT_FRAME = 1 in bit 2 of register 0x08) or unframed (XMT_FRAME = 0 in bit 2 of register 0x08). The framed sequence can be either DS1 SF format (TP_DS1E1N = 1 in bit 7 of register 0x09) or E1 format (TP_DS1E1N = 0 in bit 7 of register 0x09). The test pattern can also be forced to transmit a bit error (ERROR_INS bit in register 0x08, bit position 3, is forced to make low to high transition). The test patterns are O.151 compliant, so they can be used to drive external test equipment as well as to perform internal maintenance and troubleshooting.

Test Pattern Drop

The test pattern detector can detect the same four test sequences generated by the test pattern generator (RCV_PAT-[1:0] in bit positions 4 and 5 of register 0x08). When the detector is out of synchronization, the device continuously monitors the input data signal for matches with the expected data signal. When the device detects 32 matches in a row, it declares itself in sync (TPOOS = 0 in bit 7 of register 0x0A), and the error detector is enabled. If the device detects eight consecutive bit mismatches, the test pattern detector declares itself out of sync (TPOOS = 1), and starts searching again.

The test pattern detector can be configured to look for a framed (RCV_FRAME = 1 in bit 6 of register 0x08) or unframed (RCV_FRAME = 0 in bit 6 of register 0x08) signal.

While in sync, the device counts the number of times the input data differs from the expected data in a 7-bit counter, TPERR-[6:0] (bit 0 through bit 6 in register 0x0A), that holds its count when it reaches the maximum value of 128. This counter is reset when the LATCH_TP bit (bit 7) in register 0x08 makes a 0 to 1 transition.

Microprocessor Interface Description

Overview

The device is equipped with an asynchronous microprocessor interface that allows operation with most commercially available microprocessors. Inputs MPMUX and MPMODE are used to configure this interface into one of four possible modes. The MPMUX setting selects either a multiplexed 8-bit address/data bus (AD[7:0]), or a demultiplexed 8-bit address bus (A[7:0]) and an 8-bit data bus (AD[7:0]). The MPMODE setting selects the associated set of registers within the device.

The microprocessor interface can operate at speeds up to 33 MHz in interrupt-driven or polled mode without wait-states. To conform to standards, there are a limited number of default powerup or reset states. All read/write registers must be written by the microprocessor on system start-up to guarantee proper device functionality.

Microprocessor Configuration Modes

Table 12 highlights the four microprocessor modes controlled by the MPMUX and MPMODE inputs.

Table 12. Microprocessor Configuration Modes

Mode	MPMODE	MPMUX	Address/Data Bus	Generic Control, Data, and Output Pin Names
Mode 1	0	0	DeMUXed	$\overline{CS}$, $\overline{AS}$, $\overline{DS}$, R/$\overline{W}$, A[7:0], AD[7:0], INT, $\overline{DTACK}$
Mode 2	0	1	MUXed	$\overline{CS}$, $\overline{AS}$, $\overline{DS}$, R/$\overline{W}$, AD[7:0], INT, $\overline{DTACK}$
Mode 3	1	0	DeMUXed	$\overline{CS}$, ALE, $\overline{RD}$, $\overline{WR}$, A[7:0], AD[7:0], INT, RDY
Mode 4	1	1	MUXed	$\overline{CS}$, ALE, $\overline{RD}$, $\overline{WR}$, AD[7:0], INT, RDY

Microprocessor Interface Description (continued)

Microprocessor Interface Pins

The mode [1—4] specific pin definitions are given in Table 13. Note that the microprocessor interface uses the same set of pins in all modes.

Table 13. Mode [1—4] Microprocessor Pin Definitions

Configuration	Device Pin Name	Generic Pin Name	Pin Type	Assertion Sense	Function
Mode 1	$\overline{WR}\_\overline{DS}$	$\overline{DS}$	Input	Active-Low	Data Strobe
	$\overline{RD}\_R/\overline{W}$	$R/\overline{W}$	Input	—	Read/Write R/W = 1 for Read R/W = 0 for Write
	$ALE\_\overline{AS}$	$\overline{AS}$	Input	—	Address Strobe
	$\overline{CS}$	$\overline{CS}$	Input	Active-Low	Chip Select
	INT	INT	Output	Active-High	Interrupt
	$RDY\_\overline{DTACK}$	$\overline{DTACK}$	Output	Active-Low	Data Acknowledge
	AD[7:0]	AD[7:0]	I/O	—	Data Bus
	A[7:0]	A[7:0]	Input	—	Address Bus
Mode 2	$\overline{WR}\_\overline{DS}$	$\overline{DS}$	Input	Active-Low	Data Strobe
	$\overline{RD}\_R/\overline{W}$	$R/\overline{W}$	Input	—	Read/Write R/W = 1 for Read R/W = 0 for Write
	$ALE\_\overline{AS}$	$\overline{AS}$	Input	—	Address Strobe
	$\overline{CS}$	$\overline{CS}$	Input	Active-Low	Chip Select
	INT	INT	Output	Active-High	Interrupt
	$RDY\_\overline{DTACK}$	$\overline{DTACK}$	Output	Active-Low	Data Acknowledge
	AD[7:0]	AD[7:0]	I/O	—	Address/Data Bus

Microprocessor Interface Description (continued)

Microprocessor Interface Pins (continued)

Table 13. Mode [1—4] Microprocessor Pin Definitions (continued)

Configuration	Device Pin Name	Generic Pin Name	Pin Type	Assertion Sense	Function
Mode 3	$\overline{WR}$_$\overline{DS}$	$\overline{WR}$	Input	Active-Low	Write
	$\overline{RD}$_R/$\overline{W}$	$\overline{RD}$	Input	—	Read
	ALE_$\overline{AS}$	ALE	Input	—	Address Latch Enable
	$\overline{CS}$	$\overline{CS}$	Input	Active-Low	Chip Select
	INT	INT	Output	Active-High	Interrupt
	RDY_$\overline{DTACK}$	RDY	Output	Active-Low	Ready
	AD[7:0]	AD[7:0]	I/O	—	Data Bus
	A[7:0]	A[7:0]	Input	—	Address Bus
Mode 4	$\overline{WR}$_$\overline{DS}$	$\overline{WR}$	Input	Active-Low	Write
	$\overline{RD}$_R/$\overline{W}$	$\overline{RD}$	Input	—	Read
	ALE_$\overline{AS}$	ALE	Input	—	Address Latch Enable
	$\overline{CS}$	$\overline{CS}$	Input	Active-Low	Chip Select
	INT	$\overline{INT}$	Output	Active-High	Interrupt
	RDY_$\overline{DTACK}$	RDY	Output	Active-Low	Ready
	AD[7:0]	AD[7:0]	I/O	—	Address/Data Bus

Microprocessor Interface Description (continued)

Register Architecture Map

The register bank architecture of the microprocessor interface is shown in Table 14. All addresses referred to in this section are given in hexadecimal and binary notation, where hexadecimal is the left column and binary is the right column under Address.

Note: Bits in registers 0xC0—0xFF can have one of four configurations, depending upon the setting of register 0xBF (see the Register Architecture Description section, page 57—page 59).

Table 14. Device Register Map

Address		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Control, Alarm, and Mask Bit Registers							
00	00000000	TEST_CNT	B1ERRINS	B2ERRINS	B3ERRINS	LATCH_CNT	BLUECLKSEL	BIPBLKCNT	0
01	00000001	REI_EN	AUTO_LRDI	TXPAISINS	DJACTL	0	STS1SCR	STS1DSCR	STS1LB
02	00000010	RXSERIAL	TXSERIAL	RXPARITY	TXPARITY	RXSTS1EDGE	TXSTS1EDGE	RXDS1EDGE	TXDS1EDGE
03	00000011	TRACEER	RXPARER	0	H4LOMF	STS1PAIS	STS1LOP	STS1LOF	STS1OOF
04	00000100	TRACEERMSK	RXPARERMSK	0	H4LOMFMSK	STS1PAISMSK	STS1LOPMSK	STS1LOFMSK	STS1OOFMSK
05	00000101	ESOFCOM	VTSIZECOM	VTLOPCOM	VTRFIRDICOM	VTAISCOM	VTLABCOM	AISLOCCOM	STS1LOS
06	00000110	ESOFMSK	VTSIZEMSK	VTLOPMSK	VTRFIRDIMSK	VTAISMSK	VTLABMSK	AISLOCMSK	STS1LOSMSK
07	00000111	0	0	0	0	0	0	0	DS1_E1N
08	00001000	LATCH_TP	RCV_FRAME	RCV_PAT-1	RCV_PAT-0	ERROR_INS	XMT_FRAME	XMT_PAT-1	XMT_PAT-0
09	00001001	TP_DS1E1N	TP_INVERT	TPDROPSIDE	TPDROP-4	TPDROP-3	TPDROP-2	TPDROP-1	TPDROP-0
0A	00001010	TPOOS	TPERR-6	TPERR-5	TPERR-4	TPERR-3	TPERR-2	TPERR-1	TPERR-0
0B	00001011	F2-7	F2-6	F2-5	F2-4	F2-3	F2-2	F2-1	F2-0
0C	00001100	C2-7	C2-6	C2-5	C2-4	C2-3	C2-2	C2-1	C2-0
0D	00001101	G1-5	G1-6	G1-7	G1-8	0	K2-6	K2-7	K2-8
0E	00001110	C2#DET-3	C2#DET-2	C2#DET-1	C2#DET-0	F2#DET-3	F2#DET-2	F2#DET-1	F2#DET-0
0F	00001111	G1#DET-3	G1#DET-2	G1#DET-1	G1#DET-0	K2#DET-3	K2#DET-2	K2#DET-1	K2#DET-0
10	00010000	F2INS-7	F2INS-6	F2INS-5	F2INS-4	F2INS-3	F2INS-2	F2INS-1	F2INS-0
11	00010001	G1INS-5	G1INS-6	G1INS-7	G1INS-8	0	K2INS-6	K2INS-7	K2INS-8
12	00010010	0	0	RBUSMODE	RBUSPOS-1	RBUSPOS-0	TBUSMODE	TBUSPOS-1	TBUSPOS-0
13	00010011	0	0	0	0	S1INS-3	S1INS-2	S1INS-1	S1INS-0
14	00010100	S1#DET-3	S1#DET-2	S1#DET-1	S1#DET-0	S1-3	S1-2	S1-1	S1-0
15	00010101	DEVID-7	DEVID-6	DEVID-5	DEVID-4	DEVID-3	DEVID-2	DEVID-1	DEVID-0
16	00010110	0	0	0	0	DEVVER-3	DEVVER-2	DEVVER-1	DEVVER-0

Microprocessor Interface Description (continued)

Register Architecture Map (continued)

Table 14. Device Register Map (continued)

Address		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
				DS1/E1 Insertion Selection Registers					
17	00010111	DS1/E1AIS1	DS1/E1LOC1	DS1/E1LB1	DS1/E1INS4_1	DS1/E1INS3_1	DS1/E1INS2_1	DS1/E1INS1_1	DS1/E1INS0_1
18	00011000	DS1/E1AIS2	DS1/E1LOC2	DS1/E1LB2	DS1/E1INS4_2	DS1/E1INS3_2	DS1/E1INS2_2	DS1/E1INS1_2	DS1/E1INS0_2
19	00011001	DS1/E1AIS3	DS1/E1LOC3	DS1/E1LB3	DS1/E1INS4_3	DS1/E1INS3_3	DS1/E1INS2_3	DS1/E1INS1_3	DS1/E1INS0_3
1A	00011010	DS1/E1AIS4	DS1/E1LOC4	DS1/E1LB4	DS1/E1INS4_4	DS1/E1INS3_4	DS1/E1INS2_4	DS1/E1INS1_4	DS1/E1INS0_4
1B	00011011	DS1/E1AIS5	DS1/E1LOC5	DS1/E1LB5	DS1/E1INS4_5	DS1/E1INS3_5	DS1/E1INS2_5	DS1/E1INS1_5	DS1/E1INS0_5
1C	00011100	DS1/E1AIS6	DS1/E1LOC6	DS1/E1LB6	DS1/E1INS4_6	DS1/E1INS3_6	DS1/E1INS2_6	DS1/E1INS1_6	DS1/E1INS0_6
1D	00011101	DS1/E1AIS7	DS1/E1LOC7	DS1/E1LB7	DS1/E1INS4_7	DS1/E1INS3_7	DS1/E1INS2_7	DS1/E1INS1_7	DS1/E1INS0_7
1E	00011110	DS1/E1AIS8	DS1/E1LOC8	DS1/E1LB8	DS1/E1INS4_8	DS1/E1INS3_8	DS1/E1INS2_8	DS1/E1INS1_8	DS1/E1INS0_8
1F	00011111	DS1/E1AIS9	DS1/E1LOC9	DS1/E1LB9	DS1/E1INS4_9	DS1/E1INS3_9	DS1/E1INS2_9	DS1/E1INS1_9	DS1/E1INS0_9
20	00100000	DS1/E1AIS10	DS1/E1LOC10	DS1/E1LB10	DS1/E1INS4_10	DS1/E1INS3_10	DS1/E1INS2_10	DS1/E1INS1_10	DS1/E1INS0_10
21	00100001	DS1/E1AIS11	DS1/E1LOC11	DS1/E1LB11	DS1/E1INS4_11	DS1/E1INS3_11	DS1/E1INS2_11	DS1/E1INS1_11	DS1/E1INS0_11
22	00100010	DS1/E1AIS12	DS1/E1LOC12	DS1/E1LB12	DS1/E1INS4_12	DS1/E1INS3_12	DS1/E1INS2_12	DS1/E1INS1_12	DS1/E1INS0_12
23	00100011	DS1/E1AIS13	DS1/E1LOC13	DS1/E1LB13	DS1/E1INS4_13	DS1/E1INS3_13	DS1/E1INS2_13	DS1/E1INS1_13	DS1/E1INS0_13
24	00100100	DS1/E1AIS14	DS1/E1LOC14	DS1/E1LB14	DS1/E1INS4_14	DS1/E1INS3_14	DS1/E1INS2_14	DS1/E1INS1_14	DS1/E1INS0_14
25	00100101	DS1/E1AIS15	DS1/E1LOC15	DS1/E1LB15	DS1/E1INS4_15	DS1/E1INS3_15	DS1/E1INS2_15	DS1/E1INS1_15	DS1/E1INS0_15
26	00100110	DS1/E1AIS16	DS1/E1LOC16	DS1/E1LB16	DS1/E1INS4_16	DS1/E1INS3_16	DS1/E1INS2_16	DS1/E1INS1_16	DS1/E1INS0_16
27	00100111	DS1/E1AIS17	DS1/E1LOC17	DS1/E1LB17	DS1/E1INS4_17	DS1/E1INS3_17	DS1/E1INS2_17	DS1/E1INS1_17	DS1/E1INS0_17
28	00101000	DS1/E1AIS18	DS1/E1LOC18	DS1/E1LB18	DS1/E1INS4_18	DS1/E1INS3_18	DS1/E1INS2_18	DS1/E1INS1_18	DS1/E1INS0_18
29	00101001	DS1/E1AIS19	DS1/E1LOC19	DS1/E1LB19	DS1/E1INS4_19	DS1/E1INS3_19	DS1/E1INS2_19	DS1/E1INS1_19	DS1/E1INS0_19
2A	00101010	DS1/E1AIS20	DS1/E1LOC20	DS1/E1LB20	DS1/E1INS4_20	DS1/E1INS3_20	DS1/E1INS2_20	DS1/E1INS1_20	DS1/E1INS0_20
2B	00101011	DS1/E1AIS21	DS1/E1LOC21	DS1/E1LB21	DS1/E1INS4_21	DS1/E1INS3_21	DS1/E1INS2_21	DS1/E1INS1_21	DS1/E1INS0_21
2C	00101100	DS1AIS22	DS1LOC22	DS1LB22	DS1INS4_22	DS1INS3_22	DS1INS2_22	DS1INS1_22	DS1INS0_22
2D	00101101	DS1AIS23	DS1LOC23	DS1LB23	DS1INS4_23	DS1INS3_23	DS1INS2_23	DS1INS1_23	DS1INS0_23
2E	00101110	DS1AIS24	DS1LOC24	DS1LB24	DS1INS4_24	DS1INS3_24	DS1INS2_24	DS1INS1_24	DS1INS0_24
2F	00101111	DS1AIS25	DS1LOC25	DS1LB25	DS1INS4_25	DS1INS3_25	DS1INS2_25	DS1INS1_25	DS1INS0_25
30	00110000	DS1AIS26	DS1LOC26	DS1LB26	DS1INS4_26	DS1INS3_26	DS1INS2_26	DS1INS1_26	DS1INS0_26
31	00110001	DS1AIS27	DS1LOC27	DS1LB27	DS1INS4_27	DS1INS3_27	DS1INS2_27	DS1INS1_27	DS1INS0_27
32	00110010	DS1AIS28	DS1LOC28	DS1LB28	DS1INS4_28	DS1INS3_28	DS1INS2_28	DS1INS1_28	DS1INS0_28

Microprocessor Interface Description (continued)

Register Architecture Map (continued)

Table 14. Device Register Map (continued)

Address		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
					VT Drop Selection Registers				
33	00110011	0	RXESOF1	TXESOF1	VTDROP4_1	VTDROP3_1	VTDROP2_1	VTDROP1_1	VTDROP0_1
34	00110100	0	RXESOF2	TXESOF2	VTDROP4_2	VTDROP3_2	VTDROP2_2	VTDROP1_2	VTDROP0_2
35	00110101	0	RXESOF3	TXESOF3	VTDROP4_3	VTDROP3_3	VTDROP2_3	VTDROP1_3	VTDROP0_3
36	00110110	0	RXESOF4	TXESOF4	VTDROP4_4	VTDROP3_4	VTDROP2_4	VTDROP1_4	VTDROP0_4
37	00110111	0	RXESOF5	TXESOF5	VTDROP4_5	VTDROP3_5	VTDROP2_5	VTDROP1_5	VTDROP0_5
38	00111000	0	RXESOF6	TXESOF6	VTDROP4_6	VTDROP3_6	VTDROP2_6	VTDROP1_6	VTDROP0_6
39	00111001	0	RXESOF7	TXESOF7	VTDROP4_7	VTDROP3_7	VTDROP2_7	VTDROP1_7	VTDROP0_7
3A	00111010	0	RXESOF8	TXESOF8	VTDROP4_8	VTDROP3_8	VTDROP2_8	VTDROP1_8	VTDROP0_8
3B	00111011	0	RXESOF9	TXESOF9	VTDROP4_9	VTDROP3_9	VTDROP2_9	VTDROP1_9	VTDROP0_9
3C	00111100	0	RXESOF10	TXESOF10	VTDROP4_10	VTDROP3_10	VTDROP2_10	VTDROP1_10	VTDROP0_10
3D	00111101	0	RXESOF11	TXESOF11	VTDROP4_11	VTDROP3_11	VTDROP2_11	VTDROP1_11	VTDROP0_11
3E	00111110	0	RXESOF12	TXESOF12	VTDROP4_12	VTDROP3_12	VTDROP2_12	VTDROP1_12	VTDROP0_12
3F	00111111	0	RXESOF13	TXESOF13	VTDROP4_13	VTDROP3_13	VTDROP2_13	VTDROP1_13	VTDROP0_13
40	01000000	0	RXESOF14	TXESOF14	VTDROP4_14	VTDROP3_14	VTDROP2_14	VTDROP1_14	VTDROP0_14
41	01000001	0	RXESOF15	TXESOF15	VTDROP4_15	VTDROP3_15	VTDROP2_15	VTDROP1_15	VTDROP0_15
42	01000010	0	RXESOF16	TXESOF16	VTDROP4_16	VTDROP3_16	VTDROP2_16	VTDROP1_16	VTDROP0_16
43	01000011	0	RXESOF17	TXESOF17	VTDROP4_17	VTDROP3_17	VTDROP2_17	VTDROP1_17	VTDROP0_17
44	01000100	0	RXESOF18	TXESOF18	VTDROP4_18	VTDROP3_18	VTDROP2_18	VTDROP1_18	VTDROP0_18
45	01000101	0	RXESOF19	TXESOF19	VTDROP4_19	VTDROP3_19	VTDROP2_19	VTDROP1_19	VTDROP0_19
46	01000110	0	RXESOF20	TXESOF20	VTDROP4_20	VTDROP3_20	VTDROP2_20	VTDROP1_20	VTDROP0_20
47	01000111	0	RXESOF21	TXESOF21	VTDROP4_21	VTDROP3_21	VTDROP2_21	VTDROP1_21	VTDROP0_21
48	01001000	0	RXESOF22	TXESOF22	VTDROP4_22	VTDROP3_22	VTDROP2_22	VTDROP1_22	VTDROP0_22
49	01001001	0	RXESOF23	TXESOF23	VTDROP4_23	VTDROP3_23	VTDROP2_23	VTDROP1_23	VTDROP0_23
4A	01001010	0	RXESOF24	TXESOF24	VTDROP4_24	VTDROP3_24	VTDROP2_24	VTDROP1_24	VTDROP0_24
4B	01001011	0	RXESOF25	TXESOF25	VTDROP4_25	VTDROP3_25	VTDROP2_25	VTDROP1_25	VTDROP0_25
4C	01001100	0	RXESOF26	TXESOF26	VTDROP4_26	VTDROP3_26	VTDROP2_26	VTDROP1_26	VTDROP0_26
4D	01001101	0	RXESOF27	TXESOF27	VTDROP4_27	VTDROP3_27	VTDROP2_27	VTDROP1_27	VTDROP0_27
4E	01001110	0	RXESOF28	TXESOF28	VTDROP4_28	VTDROP3_28	VTDROP2_28	VTDROP1_28	VTDROP0_28

Microprocessor Interface Description (continued)

Register Architecture Map (continued)

Table 14. Device Register Map (continued)

Address		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
					Tx VT Overhead Insertion Control Registers				
4F	01001111	BIP2ERINS1	VTRFIRDIEN1	VTRFIINS1	VTRDIINS1	VTAISINS1	VTLABINS2_1	VTLABINS1_1	VTLABINS0_1
50	01010000	BIP2ERINS2	VTRFIRDIEN2	VTRFIINS2	VTRDIINS2	VTAISINS2	VTLABINS2_2	VTLABINS1_2	VTLABINS0_2
51	01010001	BIP2ERINS3	VTRFIRDIEN3	VTRFIINS3	VTRDIINS3	VTAISINS3	VTLABINS2_3	VTLABINS1_3	VTLABINS0_3
52	01010010	BIP2ERINS4	VTRFIRDIEN4	VTRFIINS4	VTRDIINS4	VTAISINS4	VTLABINS2_4	VTLABINS1_4	VTLABINS0_4
53	01010011	BIP2ERINS5	VTRFIRDIEN5	VTRFIINS5	VTRDIINS5	VTAISINS5	VTLABINS2_5	VTLABINS1_5	VTLABINS0_5
54	01010100	BIP2ERINS6	VTRFIRDIEN6	VTRFIINS6	VTRDIINS6	VTAISINS6	VTLABINS2_6	VTLABINS1_6	VTLABINS0_6
55	01010101	BIP2ERINS7	VTRFIRDIEN7	VTRFIINS7	VTRDIINS7	VTAISINS7	VTLABINS2_7	VTLABINS1_7	VTLABINS0_7
56	01010110	BIP2ERINS8	VTRFIRDIEN8	VTRFIINS8	VTRDIINS8	VTAISINS8	VTLABINS2_8	VTLABINS1_8	VTLABINS0_8
57	01010111	BIP2ERINS9	VTRFIRDIEN9	VTRFIINS9	VTRDIINS9	VTAISINS9	VTLABINS2_9	VTLABINS1_9	VTLABINS0_9
58	01011000	BIP2ERINS10	VTRFIRDIEN10	VTRFIINS10	VTRDIINS10	VTAISINS10	VTLABINS2_10	VTLABINS1_10	VTLABINS0_10
59	01011001	BIP2ERINS11	VTRFIRDIEN11	VTRFIINS11	VTRDIINS11	VTAISINS11	VTLABINS2_11	VTLABINS1_11	VTLABINS0_11
5A	01011010	BIP2ERINS12	VTRFIRDIEN12	VTRFIINS12	VTRDIINS12	VTAISINS12	VTLABINS2_12	VTLABINS1_12	VTLABINS0_12
5B	01011011	BIP2ERINS13	VTRFIRDIEN13	VTRFIINS13	VTRDIINS13	VTAISINS13	VTLABINS2_13	VTLABINS1_13	VTLABINS0_13
5C	01011100	BIP2ERINS14	VTRFIRDIEN14	VTRFIINS14	VTRDIINS14	VTAISINS14	VTLABINS2_14	VTLABINS1_14	VTLABINS0_14
5D	01011101	BIP2ERINS15	VTRFIRDIEN15	VTRFIINS15	VTRDIINS15	VTAISINS15	VTLABINS2_15	VTLABINS1_15	VTLABINS0_15
5E	01011110	BIP2ERINS16	VTRFIRDIEN16	VTRFIINS16	VTRDIINS16	VTAISINS16	VTLABINS2_16	VTLABINS1_16	VTLABINS0_16
5F	01011111	BIP2ERINS17	VTRFIRDIEN17	VTRFIINS17	VTRDIINS17	VTAISINS17	VTLABINS2_17	VTLABINS1_17	VTLABINS0_17
60	01100000	BIP2ERINS18	VTRFIRDIEN18	VTRFIINS18	VTRDIINS18	VTAISINS18	VTLABINS2_18	VTLABINS1_18	VTLABINS0_18
61	01100001	BIP2ERINS19	VTRFIRDIEN19	VTRFIINS19	VTRDIINS19	VTAISINS19	VTLABINS2_19	VTLABINS1_19	VTLABINS0_19
62	01100010	BIP2ERINS20	VTRFIRDIEN20	VTRFIINS20	VTRDIINS20	VTAISINS20	VTLABINS2_20	VTLABINS1_20	VTLABINS0_20
63	01100011	BIP2ERINS21	VTRFIRDIEN21	VTRFIINS21	VTRDIINS21	VTAISINS21	VTLABINS2_21	VTLABINS1_21	VTLABINS0_21
64	01100100	BIP2ERINS22	VTRFIRDIEN22	VTRFIINS22	VTRDIINS22	VTAISINS22	VTLABINS2_22	VTLABINS1_22	VTLABINS0_22
65	01100101	BIP2ERINS23	VTRFIRDIEN23	VTRFIINS23	VTRDIINS23	VTAISINS23	VTLABINS2_23	VTLABINS1_23	VTLABINS0_23
66	01100110	BIP2ERINS24	VTRFIRDIEN24	VTRFIINS24	VTRDIINS24	VTAISINS24	VTLABINS2_24	VTLABINS1_24	VTLABINS0_24
67	01100111	BIP2ERINS25	VTRFIRDIEN25	VTRFIINS25	VTRDIINS25	VTAISINS25	VTLABINS2_25	VTLABINS1_25	VTLABINS0_25
68	01101000	BIP2ERINS26	VTRFIRDIEN26	VTRFIINS26	VTRDIINS26	VTAISINS26	VTLABINS2_26	VTLABINS1_26	VTLABINS0_26
69	01101001	BIP2ERINS27	VTRFIRDIEN27	VTRFIINS27	VTRDIINS27	VTAISINS27	VTLABINS2_27	VTLABINS1_27	VTLABINS0_27
6A	01101010	BIP2ERINS28	VTRFIRDIEN28	VTRFIINS28	VTRDIINS28	VTAISINS28	VTLABINS2_28	VTLABINS1_28	VTLABINS0_28

Microprocessor Interface Description (continued)

Register Architecture Map (continued)

Table 14. Device Register Map (continued)

Address		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
				Rx VT Drop Monitoring Registers					
6B	01101011	VTSIZEER1	VTLOP1	VTRDI1_1	VTRDI0_1	VTAIS1	VTLAB2_1	VTLAB1_1	VTLAB0_1
6C	01101100	VTSIZEER2	VTLOP2	VTRDI1_2	VTRDI0_2	VTAIS2	VTLAB2_2	VTLAB1_2	VTLAB0_2
6D	01101101	VTSIZEER3	VTLOP3	VTRDI1_3	VTRDI0_3	VTAIS3	VTLAB2_3	VTLAB1_3	VTLAB0_3
6E	01101110	VTSIZEER4	VTLOP4	VTRDI1_4	VTRDI0_4	VTAIS4	VTLAB2_4	VTLAB1_4	VTLAB0_4
6F	01101111	VTSIZEER5	VTLOP5	VTRDI1_5	VTRDI0_5	VTAIS5	VTLAB2_5	VTLAB1_5	VTLAB0_5
70	01110000	VTSIZEER6	VTLOP6	VTRDI1_6	VTRDI0_6	VTAIS6	VTLAB2_6	VTLAB1_6	VTLAB0_6
71	01110001	VTSIZEER7	VTLOP7	VTRDI1_7	VTRDI0_7	VTAIS7	VTLAB2_7	VTLAB1_7	VTLAB0_7
72	01110010	VTSIZEER8	VTLOP8	VTRDI1_8	VTRDI0_8	VTAIS8	VTLAB2_8	VTLAB1_8	VTLAB0_8
73	01110011	VTSIZEER9	VTLOP9	VTRDI1_9	VTRDI0_9	VTAIS9	VTLAB2_9	VTLAB1_9	VTLAB0_9
74	01110100	VTSIZEER10	VTLOP10	VTRDI1_10	VTRDI0_10	VTAIS10	VTLAB2_10	VTLAB1_10	VTLAB0_10
75	01110101	VTSIZEER11	VTLOP11	VTRDI1_11	VTRDI0_11	VTAIS11	VTLAB2_11	VTLAB1_11	VTLAB0_11
76	01110110	VTSIZEER12	VTLOP12	VTRDI1_12	VTRDI0_12	VTAIS12	VTLAB2_12	VTLAB1_12	VTLAB0_12
77	01110111	VTSIZEER13	VTLOP13	VTRDI1_13	VTRDI0_13	VTAIS13	VTLAB2_13	VTLAB1_13	VTLAB0_13
78	01111000	VTSIZEER14	VTLOP14	VTRDI1_14	VTRDI0_14	VTAIS14	VTLAB2_14	VTLAB1_14	VTLAB0_14
79	01111001	VTSIZEER15	VTLOP15	VTRDI1_15	VTRDI0_15	VTAIS15	VTLAB2_15	VTLAB1_15	VTLAB0_15
7A	01111010	VTSIZEER16	VTLOP16	VTRDI1_16	VTRDI0_16	VTAIS16	VTLAB2_16	VTLAB1_16	VTLAB0_16
7B	01111011	VTSIZEER17	VTLOP17	VTRDI1_17	VTRDI0_17	VTAIS17	VTLAB2_17	VTLAB1_17	VTLAB0_17
7C	01111100	VTSIZEER18	VTLOP18	VTRDI1_18	VTRDI0_18	VTAIS18	VTLAB2_18	VTLAB1_18	VTLAB0_18
7D	01111101	VTSIZEER19	VTLOP19	VTRDI1_19	VTRDI0_19	VTAIS19	VTLAB2_19	VTLAB1_19	VTLAB0_19
7E	01111110	VTSIZEER20	VTLOP20	VTRDI1_20	VTRDI0_20	VTAIS20	VTLAB2_20	VTLAB1_20	VTLAB0_20
7F	01111111	VTSIZEER21	VTLOP21	VTRDI1_21	VTRDI0_21	VTAIS21	VTLAB2_21	VTLAB1_21	VTLAB0_21
80	10000000	VTSIZEER22	VTLOP22	VTRDI1_22	VTRDI0_22	VTAIS22	VTLAB2_22	VTLAB1_22	VTLAB0_22
81	10000001	VTSIZEER23	VTLOP23	VTRDI1_23	VTRDI0_23	VTAIS23	VTLAB2_23	VTLAB1_23	VTLAB0_23
82	10000010	VTSIZEER24	VTLOP24	VTRDI1_24	VTRDI0_24	VTAIS24	VTLAB2_24	VTLAB1_24	VTLAB0_24
83	10001000	VTSIZEER25	VTLOP25	VTRDI1_25	VTRDI0_25	VTAIS25	VTLAB2_25	VTLAB1_25	VTLAB0_25
84	10000100	VTSIZEER26	VTLOP26	VTRDI1_26	VTRDI0_26	VTAIS26	VTLAB2_26	VTLAB1_26	VTLAB0_26
85	10000101	VTSIZEER27	VTLOP27	VTRDI1_27	VTRDI0_27	VTAIS27	VTLAB2_27	VTLAB1_27	VTLAB0_27
86	10000110	VTSIZEER28	VTLOP28	VTRDI1_28	VTRDI0_28	VTAIS28	VTLAB2_28	VTLAB1_28	VTLAB0_28
		Reserved Register							
87	10000111	0	0	0	0	0	0	0	0
		Signal Override Control Registers							
88	10001000	TVTG-7	TVTG-6	TVTG-5	TVTG-4	TVTG-3	TVTG-2	TVTG-1	TOVERRIDE
89	10001001	RVTG-7	RVTG-6	RVTG-5	RVTG-4	RVTG-3	RVTG-2	RVTG-1	ROVERRIDE
		Jitter Attenuator Control Registers							
8A	10001010	SCALETHR-7	SCALETHR-6	SCALETHR-5	SCALETHR-4	SCALETHR-3	SCALETHR-2	SCALETHR-1	SCALETHR-0
8B	10001011	DJASCALE-15	DJASCALE-14	DJASCALE-13	DJASCALE-12	DJASCALE-11	DJASCALE-10	DJASCALE-9	DJASCALE-8
8C	10001100	DJASCALE-7	DJASCALE-6	DJASCALE-5	DJASCALE-4	DJASCALE-3	DJASCALE-2	DJASCALE-1	DJASCALE-0
8D	10001101	DJAGTHR-23	DJAGTHR-22	DJAGTHR-21	DJAGTHR-20	DJAGTHR-19	DJAGTHR-18	DJAGTHR-17	DJAGTHR-16
8E	10001110	DJAGTHR-15	DJAGTHR-14	DJAGTHR-13	DJAGTHR-12	DJAGTHR-11	DJAGTHR-10	DJAGTHR-9	DJAGTHR-8
8F	10001111	DJAGTHR-7	DJAGTHR-6	DJAGTHR-5	DJAGTHR-4	DJAGTHR-3	DJAGTHR-2	DJAGTHR-1	DJAGTHR-0

Microprocessor Interface Description (continued)

Register Architecture Map (continued)

Table 14. Device Register Map (continued)

	Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
					Reserved Register				
90	10010000	0	0	0	0	0	0	0	0
				STS-1 LOS Detect/Test Pattern Edge Control Register					
91	10010001	LOSDET-7	LOSDET-6	LOSDET-5	LOSDET-4	LOSDET-3	LOSDET-2	LOSDET-1/ TP_EDGE-1	LOSDET-0/ TP_EDGE-0
					Reserved Registers				
92	10010010	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
93	10010011	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
94	10010100	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
95	10010101	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
96	10010110	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
97	10010111	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
98	10011000	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
99	10011001	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
9A	10011010	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
9B	10011011	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
9C	10011100	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
9D	10011101	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
9E	10011110	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
9F	10011111	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
A0	10100000	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
A1	10100001	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
A2	10100010	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
A3	10100011	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
A4	10100100	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
A5	10100101	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
A6	10100110	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
A7	10100111	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
A8	10101000	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
A9	10101001	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
AA	10101010	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
AB	10101011	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
AC	10101100	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
AD	10101101	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
AE	10101110	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
AF	10101111	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
B0	10110000	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
B1	10110001	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
B2	10110010	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
B3	10110011	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
B4	10110100	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED

Microprocessor Interface Description (continued)

Register Architecture Map (continued)

Table 14. Device Register Map (continued)

	Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Reserved Registers (continued)							
B5	10110101	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
B6	10110110	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
B7	10110111	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
B8	10111000	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
B9	10111001	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
BA	10111010	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
BB	10111011	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
BC	10111100	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
BD	10111101	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
BE	10111110	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
		Block Control Register							
BF	10111111	0	0	0	0	TJ1BYTE	RJ1BYTE	REI_CNTS	BIP_CNTS
		Block Registers 0xC0—0xFF: Detected BIP Errors							
		Register 0xBF Setting: BIP_CNTS = 1							
C0	11000000	B1BIPCNT-15	B1BIPCNT-14	B1BIPCNT-13	B1BIPCNT-12	B1BIPCNT-11	B1BIPCNT-10	B1BIPCNT-9	B1BIPCNT-8
C1	11000001	B1BIPCNT-7	B1BIPCNT-6	B1BIPCNT-5	B1BIPCNT-4	B1BIPCNT-3	B1BIPCNT-2	B1BIPCNT-1	B1BIPCNT-0
C2	11000010	B2BIPCNT-15	B2BIPCNT-14	B2BIPCNT-13	B2BIPCNT-12	B2BIPCNT-11	B2BIPCNT-10	B2BIPCNT-9	B2BIPCNT-8
C3	11000011	B2BIPCNT-7	B2BIPCNT-6	B2BIPCNT-5	B2BIPCNT-4	B2BIPCNT-3	B2BIPCNT-2	B2BIPCNT-1	B2BIPCNT-0
C4	11000100	B3BIPCNT-15	B3BIPCNT-14	B3BIPCNT-13	B3BIPCNT-12	B3BIPCNT-11	B3BIPCNT-10	B3BIPCNT-9	B3BIPCNT-8
C5	11000101	B3BIPCNT-7	B3BIPCNT-6	B3BIPCNT-5	B3BIPCNT-4	B3BIPCNT-3	B3BIPCNT-2	B3BIPCNT-1	B3BIPCNT-0
C6	11000110	VT1PTR+3	VT1PTR+2	VT1PTR+1	VT1PTR+0	BIP2CNT11_1	BIP2CNT10_1	BIP2CNT9_1	BIP2CNT8_1
C7	11000111	BIP2CNT7_1	BIP2CNT6_1	BIP2CNT5_1	BIP2CNT4_1	BIP2CNT3_1	BIP2CNT2_1	BIP2CNT1_1	BIP2CNT0_1
C8	11001000	VT2PTR+3	VT2PTR+2	VT2PTR+1	VT2PTR+0	BIP2CNT11_2	BIP2CNT10_2	BIP2CNT9_2	BIP2CNT8_2
C9	11001001	BIP2CNT7_2	BIP2CNT6_2	BIP2CNT5_2	BIP2CNT4_2	BIP2CNT3_2	BIP2CNT2_2	BIP2CNT1_2	BIP2CNT0_2
CA	11001010	VT3PTR+3	VT3PTR+2	VT3PTR+1	VT3PTR+0	BIP2CNT11_3	BIP2CNT10_3	BIP2CNT9_3	BIP2CNT8_3
CB	11001011	BIP2CNT7_3	BIP2CNT6_3	BIP2CNT5_3	BIP2CNT4_3	BIP2CNT3_3	BIP2CNT2_3	BIP2CNT1_3	BIP2CNT0_3
CC	11001100	VT4PTR+3	VT4PTR+2	VT4PTR+1	VT4PTR+0	BIP2CNT11_4	BIP2CNT10_4	BIP2CNT9_4	BIP2CNT8_4
CD	11001101	BIP2CNT7_4	BIP2CNT6_4	BIP2CNT5_4	BIP2CNT4_4	BIP2CNT3_4	BIP2CNT2_4	BIP2CNT1_4	BIP2CNT0_4
CE	11001110	VT5PTR+3	VT5PTR+2	VT5PTR+1	VT5PTR+0	BIP2CNT11_5	BIP2CNT10_5	BIP2CNT9_5	BIP2CNT8_5
CF	11001111	BIP2CNT7_5	BIP2CNT6_5	BIP2CNT5_5	BIP2CNT4_5	BIP2CNT3_5	BIP2CNT2_5	BIP2CNT1_5	BIP2CNT0_5
D0	11010000	VT6PTR+3	VT6PTR+2	VT6PTR+1	VT6PTR+0	BIP2CNT11_6	BIP2CNT10_6	BIP2CNT9_6	BIP2CNT8_6
D1	11010001	BIP2CNT7_6	BIP2CNT6_6	BIP2CNT5_6	BIP2CNT4_6	BIP2CNT3_6	BIP2CNT2_6	BIP2CNT1_6	BIP2CNT0_6
D2	11010010	VT7PTR+3	VT7PTR+2	VT7PTR+1	VT7PTR+0	BIP2CNT11_7	BIP2CNT10_7	BIP2CNT9_7	BIP2CNT8_7
D3	11010011	BIP2CNT7_7	BIP2CNT6_7	BIP2CNT5_7	BIP2CNT4_7	BIP2CNT3_7	BIP2CNT2_7	BIP2CNT1_7	BIP2CNT0_7
D4	11010100	VT8PTR+3	VT8PTR+2	VT8PTR+1	VT8PTR+0	BIP2CNT11_8	BIP2CNT10_8	BIP2CNT9_8	BIP2CNT8_8
D5	11010101	BIP2CNT7_8	BIP2CNT6_8	BIP2CNT5_8	BIP2CNT4_8	BIP2CNT3_8	BIP2CNT2_8	BIP2CNT1_8	BIP2CNT0_8
D6	11010110	VT9PTR+3	VT9PTR+2	VT9PTR+1	VT9PTR+0	BIP2CNT11_9	BIP2CNT10_9	BIP2CNT9_9	BIP2CNT8_9
D7	11010111	BIP2CNT7_9	BIP2CNT6_9	BIP2CNT5_9	BIP2CNT4_9	BIP2CNT3_9	BIP2CNT2_9	BIP2CNT1_9	BIP2CNT0_9
D8	11011000	VT10PTR+3	VT10PTR+2	VT10PTR+1	VT10PTR+0	BIP2CNT11_10	BIP2CNT10_10	BIP2CNT9_10	BIP2CNT8_10
D9	11011001	BIP2CNT7_10	BIP2CNT6_10	BIP2CNT5_10	BIP2CNT4_10	BIP2CNT3_10	BIP2CNT2_10	BIP2CNT1_10	BIP2CNT0_10

Microprocessor Interface Description (continued)

Register Architecture Map (continued)

Table 14. Device Register Map (continued)

Address		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Block Registers 0xC0—0xFF: Detected BIP Errors (continued)									
DA	11011010	VT11PTR+3	VT11PTR+2	VT11PTR+1	VT11PTR+0	BIP2CNT11_11	BIP2CNT10_11	BIP2CNT9_11	BIP2CNT8_11
DB	11011011	BIP2CNT7_11	BIP2CNT6_11	BIP2CNT5_11	BIP2CNT4_11	BIP2CNT3_11	BIP2CNT2_11	BIP2CNT1_11	BIP2CNT0_11
DC	11011100	VT12PTR+3	VT12PTR+2	VT12PTR+1	VT12PTR+0	BIP2CNT11_12	BIP2CNT10_12	BIP2CNT9_12	BIP2CNT8_12
DD	11011101	BIP2CNT7_12	BIP2CNT6_12	BIP2CNT5_12	BIP2CNT4_12	BIP2CNT3_12	BIP2CNT2_12	BIP2CNT1_12	BIP2CNT0_12
DE	11011110	VT13PTR+3	VT13PTR+2	VT13PTR+1	VT13PTR+0	BIP2CNT11_13	BIP2CNT10_13	BIP2CNT9_13	BIP2CNT8_13
DF	11011111	BIP2CNT7_13	BIP2CNT6_13	BIP2CNT5_13	BIP2CNT4_13	BIP2CNT3_13	BIP2CNT2_13	BIP2CNT1_13	BIP2CNT0_13
E0	11100000	VT14PTR+3	VT14PTR+2	VT14PTR+1	VT14PTR+0	BIP2CNT11_14	BIP2CNT10_14	BIP2CNT9_14	BIP2CNT8_14
E1	11100001	BIP2CNT7_14	BIP2CNT6_14	BIP2CNT5_14	BIP2CNT4_14	BIP2CNT3_14	BIP2CNT2_14	BIP2CNT1_14	BIP2CNT0_14
E2	11100010	VT15PTR+3	VT15PTR+2	VT15PTR+1	VT15PTR+0	BIP2CNT11_15	BIP2CNT10_15	BIP2CNT9_15	BIP2CNT8_15
E3	11100011	BIP2CNT7_15	BIP2CNT6_15	BIP2CNT5_15	BIP2CNT4_15	BIP2CNT3_15	BIP2CNT2_15	BIP2CNT1_15	BIP2CNT0_15
E4	11100100	VT16PTR+3	VT16PTR+2	VT16PTR+1	VT16PTR+0	BIP2CNT11_16	BIP2CNT10_16	BIP2CNT9_16	BIP2CNT8_16
E5	11100101	BIP2CNT7_16	BIP2CNT6_16	BIP2CNT5_16	BIP2CNT4_16	BIP2CNT3_16	BIP2CNT2_16	BIP2CNT1_16	BIP2CNT0_16
E6	11100110	VT17PTR+3	VT17PTR+2	VT17PTR+1	VT17PTR+0	BIP2CNT11_17	BIP2CNT10_17	BIP2CNT9_17	BIP2CNT8_17
E7	11100111	BIP2CNT7_17	BIP2CNT6_17	BIP2CNT5_17	BIP2CNT4_17	BIP2CNT3_17	BIP2CNT2_17	BIP2CNT1_17	BIP2CNT0_17
E8	11101000	VT18PTR+3	VT18PTR+2	VT18PTR+1	VT18PTR+0	BIP2CNT11_18	BIP2CNT10_18	BIP2CNT9_18	BIP2CNT8_18
E9	11101001	BIP2CNT7_18	BIP2CNT6_18	BIP2CNT5_18	BIP2CNT4_18	BIP2CNT3_18	BIP2CNT2_18	BIP2CNT1_18	BIP2CNT0_18
EA	11101010	VT19PTR+3	VT19PTR+2	VT19PTR+1	VT19PTR+0	BIP2CNT11_19	BIP2CNT10_19	BIP2CNT9_19	BIP2CNT8_19
EB	11101011	BIP2CNT7_19	BIP2CNT6_19	BIP2CNT5_19	BIP2CNT4_19	BIP2CNT3_19	BIP2CNT2_19	BIP2CNT1_19	BIP2CNT0_19
EC	11101100	VT20PTR+3	VT20PTR+2	VT20PTR+1	VT20PTR+0	BIP2CNT11_20	BIP2CNT10_20	BIP2CNT9_20	BIP2CNT8_20
ED	11101101	BIP2CNT7_20	BIP2CNT6_20	BIP2CNT5_20	BIP2CNT4_20	BIP2CNT3_20	BIP2CNT2_20	BIP2CNT1_20	BIP2CNT0_20
EE	11101110	VT21PTR+3	VT21PTR+2	VT21PTR+1	VT21PTR+0	BIP2CNT11_21	BIP2CNT10_21	BIP2CNT9_21	BIP2CNT8_21
EF	11101111	BIP2CNT7_21	BIP2CNT6_21	BIP2CNT5_21	BIP2CNT4_21	BIP2CNT3_21	BIP2CNT2_21	BIP2CNT1_21	BIP2CNT0_21
F0	11110000	VT22PTR+3	VT22PTR+2	VT22PTR+1	VT22PTR+0	BIP2CNT11_22	BIP2CNT10_22	BIP2CNT9_22	BIP2CNT8_22
F1	11110001	BIP2CNT7_22	BIP2CNT6_22	BIP2CNT5_22	BIP2CNT4_22	BIP2CNT3_22	BIP2CNT2_22	BIP2CNT1_22	BIP2CNT0_22
F2	11110010	VT23PTR+3	VT23PTR+2	VT23PTR+1	VT23PTR+0	BIP2CNT11_23	BIP2CNT10_23	BIP2CNT9_23	BIP2CNT8_23
F3	11110011	BIP2CNT7_23	BIP2CNT6_23	BIP2CNT5_23	BIP2CNT4_23	BIP2CNT3_23	BIP2CNT2_23	BIP2CNT1_23	BIP2CNT0_23
F4	11110100	VT24PTR+3	VT24PTR+2	VT24PTR+1	VT24PTR+0	BIP2CNT11_24	BIP2CNT10_24	BIP2CNT9_24	BIP2CNT8_24
F5	11110101	BIP2CNT7_24	BIP2CNT6_24	BIP2CNT5_24	BIP2CNT4_24	BIP2CNT3_24	BIP2CNT2_24	BIP2CNT1_24	BIP2CNT0_24
F6	11110110	VT25PTR+3	VT25PTR+2	VT25PTR+1	VT25PTR+0	BIP2CNT11_25	BIP2CNT10_25	BIP2CNT9_25	BIP2CNT8_25
F7	11110111	BIP2CNT7_25	BIP2CNT6_25	BIP2CNT5_25	BIP2CNT4_25	BIP2CNT3_25	BIP2CNT2_25	BIP2CNT1_25	BIP2CNT0_25
F8	11111000	VT26PTR+3	VT26PTR+2	VT26PTR+1	VT26PTR+0	BIP2CNT11_26	BIP2CNT10_26	BIP2CNT9_26	BIP2CNT8_26
F9	11111001	BIP2CNT7_26	BIP2CNT6_26	BIP2CNT5_26	BIP2CNT4_26	BIP2CNT3_26	BIP2CNT2_26	BIP2CNT1_26	BIP2CNT0_26
FA	11111010	VT27PTR+3	VT27PTR+2	VT27PTR+1	VT27PTR+0	BIP2CNT11_27	BIP2CNT10_27	BIP2CNT9_27	BIP2CNT8_27
FB	11111011	BIP2CNT7_27	BIP2CNT6_27	BIP2CNT5_27	BIP2CNT4_27	BIP2CNT3_27	BIP2CNT2_27	BIP2CNT1_27	BIP2CNT0_27
FC	11111100	VT28PTR+3	VT28PTR+2	VT28PTR+1	VT28PTR+0	BIP2CNT11_28	BIP2CNT10_28	BIP2CNT9_28	BIP2CNT8_28
FD	11111101	BIP2CNT7_28	BIP2CNT6_28	BIP2CNT5_28	BIP2CNT4_28	BIP2CNT3_28	BIP2CNT2_28	BIP2CNT1_28	BIP2CNT0_28
Received SONET/SDH Pointer Value Registers									
Register 0xBF Setting: BIP_CNTS = 1									
FE	11111110	SPTR+7	SPTR+6	SPTR+5	SPTR+4	SPTR+3	SPTR+2	SPTR+1	SPTR+0
FF	11111111	SPTR–7	SPTR–6	SPTR–5	SPTR–4	SPTR–3	SPTR–2	SPTR–1	SPTR–0

Microprocessor Interface Description (continued)

Register Architecture Map (continued)

Table 14. Device Register Map (continued)

Address		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Block Registers 0xC0—0xFF: Detected REI Errors							
		Register 0xBF Settings: REI_CNTS = 1, BIP_CNTS = 0							
C0	11000000	0	0	0	0	0	0	0	0
C1	11000001	0	0	0	0	0	0	0	0
C2	11000010	B2REI-15	B2REI-14	B2REI-13	B2REI-12	B2REI-11	B2REI-10	B2REI-9	B2REI-8
C3	11000011	B2REI-7	B2REI-6	B2REI-5	B2REI-4	B2REI-3	B2REI-2	B2REI-1	B2REI-0
C4	11000100	B3REI-15	B3REI-14	B3REI-13	B3REI-12	B3REI-11	B3REI-10	B3REI-9	B3REI-8
C5	11000101	B3REI-7	B3REI-6	B3REI-5	B3REI-4	B3REI-3	B3REI-2	B3REI-1	B3REI-0
C6	11000110	VT1PTR–3	VT1PTR–2	VT1PTR–1	VT1PTR–0	0	VTREI10_1	VTREI9_1	VTREI8_1
C7	11000111	VTREI7_1	VTREI6_1	VTREI5_1	VTREI4_1	VTREI3_1	VTREI2_1	VTREI1_1	VTREI0_1
C8	11001000	VT2PTR–3	VT2PTR–2	VT2PTR–1	VT2PTR–0	0	VTREI10_2	VTREI9_2	VTREI8_2
C9	11001001	VTREI7_2	VTREI6_2	VTREI5_2	VTREI4_2	VTREI3_2	VTREI2_2	VTREI1_2	VTREI0_2
CA	11001010	VT3PTR–3	VT3PTR–2	VT3PTR–1	VT3PTR–0	0	VTREI10_3	VTREI9_3	VTREI8_3
CB	11001011	VTREI7_3	VTREI6_3	VTREI5_3	VTREI4_3	VTREI3_3	VTREI2_3	VTREI1_3	VTREI0_3
CC	11001100	VT4PTR–3	VT4PTR–2	VT4PTR–1	VT4PTR–0	0	VTREI10_4	VTREI9_4	VTREI8_4
CD	11001101	VTREI7_4	VTREI6_4	VTREI5_4	VTREI4_4	VTREI3_4	VTREI2_4	VTREI1_4	VTREI0_4
CE	11001110	VT5PTR–3	VT5PTR–2	VT5PTR–1	VT5PTR–0	0	VTREI10_5	VTREI9_5	VTREI8_5
CF	11001111	VTREI7_5	VTREI6_5	VTREI5_5	VTREI4_5	VTREI3_5	VTREI2_5	VTREI1_5	VTREI0_5
D0	11010000	VT6PTR–3	VT6PTR–2	VT6PTR–1	VT6PTR–0	0	VTREI10_6	VTREI9_6	VTREI8_6
D1	11010001	VTREI7_6	VTREI6_6	VTREI5_6	VTREI4_6	VTREI3_6	VTREI2_6	VTREI1_6	VTREI0_6
D2	11010010	VT7PTR–3	VT7PTR–2	VT7PTR–1	VT7PTR–0	0	VTREI10_7	VTREI9_7	VTREI8_7
D3	11010011	VTREI7_7	VTREI6_7	VTREI5_7	VTREI4_7	VTREI3_7	VTREI2_7	VTREI1_7	VTREI0_7
D4	11010100	VT8PTR–3	VT8PTR–2	VT8PTR–1	VT8PTR–0	0	VTREI10_8	VTREI9_8	VTREI8_8
D5	11010101	VTREI7_8	VTREI6_8	VTREI5_8	VTREI4_8	VTREI3_8	VTREI2_8	VTREI1_8	VTREI0_8
D6	11010110	VT9PTR–3	VT9PTR–2	VT9PTR–1	VT9PTR–0	0	VTREI10_9	VTREI9_9	VTREI8_9
D7	11010111	VTREI7_9	VTREI6_9	VTREI5_9	VTREI4_9	VTREI3_9	VTREI2_9	VTREI1_9	VTREI0_9
D8	11011000	VT10PTR–3	VT10PTR–2	VT10PTR–1	VT10PTR–0	0	VTREI10_10	VTREI9_10	VTREI8_10
D9	11011001	VTREI7_10	VTREI6_10	VTREI5_10	VTREI4_10	VTREI3_10	VTREI2_10	VTREI1_10	VTREI0_10
DA	11011010	VT11PTR–3	VT11PTR–2	VT11PTR–1	VT11PTR–0	0	VTREI10_11	VTREI9_11	VTREI8_11
DB	11011011	VTREI7_11	VTREI6_11	VTREI5_11	VTREI4_11	VTREI3_11	VTREI2_11	VTREI1_11	VTREI0_11
DC	11011100	VT12PTR–3	VT12PTR–2	VT12PTR–1	VT12PTR–0	0	VTREI10_12	VTREI9_12	VTREI8_12
DD	11011101	VTREI7_12	VTREI6_12	VTREI5_12	VTREI4_12	VTREI3_12	VTREI2_12	VTREI1_12	VTREI0_12
DE	11011110	VT13PTR–3	VT13PTR–2	VT13PTR–1	VT13PTR–0	0	VTREI10_13	VTREI9_13	VTREI8_13
DF	11011111	VTREI7_13	VTREI6_13	VTREI5_13	VTREI4_13	VTREI3_13	VTREI2_13	VTREI1_13	VTREI0_13
E0	11100000	VT14PTR–3	VT14PTR–2	VT14PTR–1	VT14PTR–0	0	VTREI10_14	VTREI9_14	VTREI8_14
E1	11100001	VTREI7_14	VTREI6_14	VTREI5_14	VTREI4_14	VTREI3_14	VTREI2_14	VTREI1_14	VTREI0_14
E2	11100010	VT15PTR–3	VT15PTR–2	VT15PTR–1	VT15PTR–0	0	VTREI10_15	VTREI9_15	VTREI8_15
E3	11100011	VTREI7_15	VTREI6_15	VTREI5_15	VTREI4_15	VTREI3_15	VTREI2_15	VTREI1_15	VTREI0_15
E4	11100100	VT16PTR–3	VT16PTR–2	VT16PTR–1	VT16PTR–0	0	VTREI10_16	VTREI9_16	VTREI8_16
E5	11100101	VTREI7_16	VTREI6_16	VTREI5_16	VTREI4_16	VTREI3_16	VTREI2_16	VTREI1_16	VTREI0_16
E6	11100110	VT17PTR–3	VT17PTR–2	VT17PTR–1	VT17PTR–0	0	VTREI10_17	VTREI9_17	VTREI8_17
E7	11100111	VTREI7_17	VTREI6_17	VTREI5_17	VTREI4_17	VTREI3_17	VTREI2_17	VTREI1_17	VTREI0_17
E8	11101000	VT18PTR–3	VT18PTR–2	VT18PTR–1	VT18PTR–0	0	VTREI10_18	VTREI9_18	VTREI8_18
E9	11101001	VTREI7_18	VTREI6_18	VTREI5_18	VTREI4_18	VTREI3_18	VTREI2_18	VTREI1_18	VTREI0_18
EA	11101010	VT19PTR–3	VT19PTR–2	VT19PTR–1	VT19PTR–0	0	VTREI10_19	VTREI9_19	VTREI8_19

Microprocessor Interface Description (continued)

Register Architecture Map (continued)

Table 14. Device Register Map (continued)

Address		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Block Registers 0xC0—0xFF: Detected REI Errors (continued)							
EB	11101011	VTREI7_19	VTREI6_19	VTREI5_19	VTREI4_19	VTREI3_19	VTREI2_19	VTREI1_19	VTREI0_19
EC	11101100	VT20PTR–3	VT20PTR–2	VT20PTR–1	VT20PTR–0	0	VTREI10_20	VTREI9_20	VTREI8_20
ED	11101101	VTREI7_20	VTREI6_20	VTREI5_20	VTREI4_20	VTREI3_20	VTREI2_20	VTREI1_20	VTREI0_20
EE	11101110	VT21PTR–3	VT21PTR–2	VT21PTR–1	VT21PTR–0	0	VTREI10_21	VTREI9_21	VTREI8_21
EF	11101111	VTREI7_21	VTREI6_21	VTREI5_21	VTREI4_21	VTREI3_21	VTREI2_21	VTREI1_21	VTREI0_21
F0	11110000	VT22PTR–3	VT22PTR–2	VT22PTR–1	VT22PTR–0	0	VTREI10_22	VTREI9_22	VTREI8_22
F1	11110001	VTREI7_22	VTREI6_22	VTREI5_22	VTREI4_22	VTREI3_22	VTREI2_22	VTREI1_22	VTREI0_22
F2	11110010	VT23PTR–3	VT23PTR–2	VT23PTR–1	VT23PTR–0	0	VTREI10_23	VTREI9_23	VTREI8_23
F3	11110011	VTREI7_23	VTREI6_23	VTREI5_23	VTREI4_23	VTREI3_23	VTREI2_23	VTREI1_23	VTREI0_23
F4	11110100	VT24PTR–3	VT24PTR–2	VT24PTR–1	VT24PTR–0	0	VTREI10_24	VTREI9_24	VTREI8_24
F5	11110101	VTREI7_24	VTREI6_24	VTREI5_24	VTREI4_24	VTREI3_24	VTREI2_24	VTREI1_24	VTREI0_24
F6	11110110	VT25PTR–3	VT25PTR–2	VT25PTR–1	VT25PTR–0	0	VTREI10_25	VTREI9_25	VTREI8_25
F7	11110111	VTREI7_25	VTREI6_25	VTREI5_25	VTREI4_25	VTREI3_25	VTREI2_25	VTREI1_25	VTREI0_25
F8	11111000	VT26PTR–3	VT26PTR–2	VT26PTR–1	VT26PTR–0	0	VTREI10_26	VTREI9_26	VTREI8_26
F9	11111001	VTREI7_26	VTREI6_26	VTREI5_26	VTREI4_26	VTREI3_26	VTREI2_26	VTREI1_26	VTREI0_26
FA	11111010	VT27PTR–3	VT27PTR–2	VT27PTR–1	VT27PTR–0	0	VTREI10_27	VTREI9_27	VTREI8_27
FB	11111011	VTREI7_27	VTREI6_27	VTREI5_27	VTREI4_27	VTREI3_27	VTREI2_27	VTREI1_27	VTREI0_27
FC	11111100	VT28PTR–3	VT28PTR–2	VT28PTR–1	VT28PTR–0	0	VTREI10_28	VTREI9_28	VTREI8_28
FD	11111101	VTREI7_28	VTREI6_28	VTREI5_28	VTREI4_28	VTREI3_28	VTREI2_28	VTREI1_28	VTREI0_28
FE	11111110	0	0	0	0	0	0	0	0
FF	11111111	0	0	0	0	0	0	0	0

Microprocessor Interface Description (continued)

Register Architecture Map (continued)

Table 14. Device Register Map (continued)

	Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
			**Block Registers 0xC0—0xFF: Receive J1 Path Trace Bytes**						
			Register 0xBF Settings: RJ1BYTE = 1, BIP_CNTS = 0, REI_CNTS = 0						
C0	11000000	RJ1BYTE7_64	RJ1BYTE6_64	RJ1BYTE5_64	RJ1BYTE4_64	RJ1BYTE3_64	RJ1BYTE2_64	RJ1BYTE1_64	RJ1BYTE0_64
C1	11000001	RJ1BYTE7_63	RJ1BYTE6_63	RJ1BYTE5_63	RJ1BYTE4_63	RJ1BYTE3_63	RJ1BYTE2_63	RJ1BYTE1_63	RJ1BYTE0_63
C2	11000010	RJ1BYTE7_62	RJ1BYTE6_62	RJ1BYTE5_62	RJ1BYTE4_62	RJ1BYTE3_62	RJ1BYTE2_62	RJ1BYTE1_62	RJ1BYTE0_62
C3	11000011	RJ1BYTE7_61	RJ1BYTE6_61	RJ1BYTE5_61	RJ1BYTE4_61	RJ1BYTE3_61	RJ1BYTE2_61	RJ1BYTE1_61	RJ1BYTE0_61
C4	11000100	RJ1BYTE7_60	RJ1BYTE6_60	RJ1BYTE5_60	RJ1BYTE4_60	RJ1BYTE3_60	RJ1BYTE2_60	RJ1BYTE1_60	RJ1BYTE0_60
C5	11000101	RJ1BYTE7_59	RJ1BYTE6_59	RJ1BYTE5_59	RJ1BYTE4_59	RJ1BYTE3_59	RJ1BYTE2_59	RJ1BYTE1_59	RJ1BYTE0_59
C6	11000110	RJ1BYTE7_58	RJ1BYTE6_58	RJ1BYTE5_58	RJ1BYTE4_58	RJ1BYTE3_58	RJ1BYTE2_58	RJ1BYTE1_58	RJ1BYTE0_58
C7	11000111	RJ1BYTE7_57	RJ1BYTE6_57	RJ1BYTE5_57	RJ1BYTE4_57	RJ1BYTE3_57	RJ1BYTE2_57	RJ1BYTE1_57	RJ1BYTE0_57
C8	11001000	RJ1BYTE7_56	RJ1BYTE6_56	RJ1BYTE5_56	RJ1BYTE4_56	RJ1BYTE3_56	RJ1BYTE2_56	RJ1BYTE1_56	RJ1BYTE0_56
C9	11001001	RJ1BYTE7_55	RJ1BYTE6_55	RJ1BYTE5_55	RJ1BYTE4_55	RJ1BYTE3_55	RJ1BYTE2_55	RJ1BYTE1_55	RJ1BYTE0_55
CA	11001010	RJ1BYTE7_54	RJ1BYTE6_54	RJ1BYTE5_54	RJ1BYTE4_54	RJ1BYTE3_54	RJ1BYTE2_54	RJ1BYTE1_54	RJ1BYTE0_54
CB	11001011	RJ1BYTE7_53	RJ1BYTE6_53	RJ1BYTE5_53	RJ1BYTE4_53	RJ1BYTE3_53	RJ1BYTE2_53	RJ1BYTE1_53	RJ1BYTE0_53
CC	11001100	RJ1BYTE7_52	RJ1BYTE6_52	RJ1BYTE5_52	RJ1BYTE4_52	RJ1BYTE3_52	RJ1BYTE2_52	RJ1BYTE1_52	RJ1BYTE0_52
CD	11001101	RJ1BYTE7_51	RJ1BYTE6_51	RJ1BYTE5_51	RJ1BYTE4_51	RJ1BYTE3_51	RJ1BYTE2_51	RJ1BYTE1_51	RJ1BYTE0_51
CE	11001110	RJ1BYTE7_50	RJ1BYTE6_50	RJ1BYTE5_50	RJ1BYTE4_50	RJ1BYTE3_50	RJ1BYTE2_50	RJ1BYTE1_50	RJ1BYTE0_50
CF	11001111	RJ1BYTE7_49	RJ1BYTE6_49	RJ1BYTE5_49	RJ1BYTE4_49	RJ1BYTE3_49	RJ1BYTE2_49	RJ1BYTE1_49	RJ1BYTE0_49
D0	11010000	RJ1BYTE7_48	RJ1BYTE6_48	RJ1BYTE5_48	RJ1BYTE4_48	RJ1BYTE3_48	RJ1BYTE2_48	RJ1BYTE1_48	RJ1BYTE0_48
D1	11010001	RJ1BYTE7_47	RJ1BYTE6_47	RJ1BYTE5_47	RJ1BYTE4_47	RJ1BYTE3_47	RJ1BYTE2_47	RJ1BYTE1_47	RJ1BYTE0_47
D2	11010010	RJ1BYTE7_46	RJ1BYTE6_46	RJ1BYTE5_46	RJ1BYTE4_46	RJ1BYTE3_46	RJ1BYTE2_46	RJ1BYTE1_46	RJ1BYTE0_46
D3	11010011	RJ1BYTE7_45	RJ1BYTE6_45	RJ1BYTE5_45	RJ1BYTE4_45	RJ1BYTE3_45	RJ1BYTE2_45	RJ1BYTE1_45	RJ1BYTE0_45
D4	11010100	RJ1BYTE7_44	RJ1BYTE6_44	RJ1BYTE5_44	RJ1BYTE4_44	RJ1BYTE3_44	RJ1BYTE2_44	RJ1BYTE1_44	RJ1BYTE0_44
D5	11010101	RJ1BYTE7_43	RJ1BYTE6_43	RJ1BYTE5_43	RJ1BYTE4_43	RJ1BYTE3_43	RJ1BYTE2_43	RJ1BYTE1_43	RJ1BYTE0_43
D6	11010110	RJ1BYTE7_42	RJ1BYTE6_42	RJ1BYTE5_42	RJ1BYTE4_42	RJ1BYTE3_42	RJ1BYTE2_42	RJ1BYTE1_42	RJ1BYTE0_42
D7	11010111	RJ1BYTE7_41	RJ1BYTE6_41	RJ1BYTE5_41	RJ1BYTE4_41	RJ1BYTE3_41	RJ1BYTE2_41	RJ1BYTE1_41	RJ1BYTE0_41
D8	11011000	RJ1BYTE7_40	RJ1BYTE6_40	RJ1BYTE5_40	RJ1BYTE4_40	RJ1BYTE3_40	RJ1BYTE2_40	RJ1BYTE1_40	RJ1BYTE0_40
D9	11011001	RJ1BYTE7_39	RJ1BYTE6_39	RJ1BYTE5_39	RJ1BYTE4_39	RJ1BYTE3_39	RJ1BYTE2_39	RJ1BYTE1_39	RJ1BYTE0_39
DA	11011010	RJ1BYTE7_38	RJ1BYTE6_38	RJ1BYTE5_38	RJ1BYTE4_38	RJ1BYTE3_38	RJ1BYTE2_38	RJ1BYTE1_38	RJ1BYTE0_38
DB	11011011	RJ1BYTE7_37	RJ1BYTE6_37	RJ1BYTE5_37	RJ1BYTE4_37	RJ1BYTE3_37	RJ1BYTE2_37	RJ1BYTE1_37	RJ1BYTE0_37
DC	11011100	RJ1BYTE7_36	RJ1BYTE6_36	RJ1BYTE5_36	RJ1BYTE4_36	RJ1BYTE3_36	RJ1BYTE2_36	RJ1BYTE1_36	RJ1BYTE0_36
DD	11011101	RJ1BYTE7_35	RJ1BYTE6_35	RJ1BYTE5_35	RJ1BYTE4_35	RJ1BYTE3_35	RJ1BYTE2_35	RJ1BYTE1_35	RJ1BYTE0_35
DE	11011110	RJ1BYTE7_34	RJ1BYTE6_34	RJ1BYTE5_34	RJ1BYTE4_34	RJ1BYTE3_34	RJ1BYTE2_34	RJ1BYTE1_34	RJ1BYTE0_34
DF	11011111	RJ1BYTE7_33	RJ1BYTE6_33	RJ1BYTE5_33	RJ1BYTE4_33	RJ1BYTE3_33	RJ1BYTE2_33	RJ1BYTE1_33	RJ1BYTE0_33
E0	11100000	RJ1BYTE7_32	RJ1BYTE6_32	RJ1BYTE5_32	RJ1BYTE4_32	RJ1BYTE3_32	RJ1BYTE2_32	RJ1BYTE1_32	RJ1BYTE0_32
E1	11100001	RJ1BYTE7_31	RJ1BYTE6_31	RJ1BYTE5_31	RJ1BYTE4_31	RJ1BYTE3_31	RJ1BYTE2_31	RJ1BYTE1_31	RJ1BYTE0_31
E2	11100010	RJ1BYTE7_30	RJ1BYTE6_30	RJ1BYTE5_30	RJ1BYTE4_30	RJ1BYTE3_30	RJ1BYTE2_30	RJ1BYTE1_30	RJ1BYTE0_30
E3	11100011	RJ1BYTE7_29	RJ1BYTE6_29	RJ1BYTE5_29	RJ1BYTE4_29	RJ1BYTE3_29	RJ1BYTE2_29	RJ1BYTE1_29	RJ1BYTE0_29
E4	11100100	RJ1BYTE7_28	RJ1BYTE6_28	RJ1BYTE5_28	RJ1BYTE4_28	RJ1BYTE3_28	RJ1BYTE2_28	RJ1BYTE1_28	RJ1BYTE0_28
E5	11100101	RJ1BYTE7_27	RJ1BYTE6_27	RJ1BYTE5_27	RJ1BYTE4_27	RJ1BYTE3_27	RJ1BYTE2_27	RJ1BYTE1_27	RJ1BYTE0_27
E6	11100110	RJ1BYTE7_26	RJ1BYTE6_26	RJ1BYTE5_26	RJ1BYTE4_26	RJ1BYTE3_26	RJ1BYTE2_26	RJ1BYTE1_26	RJ1BYTE0_64
E7	11100111	RJ1BYTE7_25	RJ1BYTE6_25	RJ1BYTE5_25	RJ1BYTE4_25	RJ1BYTE3_25	RJ1BYTE2_25	RJ1BYTE1_25	RJ1BYTE0_25

Microprocessor Interface Description (continued)

Register Architecture Map (continued)

Table 14. Device Register Map (continued)

Address		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Block Registers 0xC0—0xFF: Receive J1 Path Trace Bytes (continued)									
E8	11101000	RJ1BYTE7_24	RJ1BYTE6_24	RJ1BYTE5_24	RJ1BYTE4_24	RJ1BYTE3_24	RJ1BYTE2_24	RJ1BYTE1_24	RJ1BYTE0_24
E9	11101001	RJ1BYTE7_23	RJ1BYTE6_23	RJ1BYTE5_23	RJ1BYTE4_23	RJ1BYTE3_23	RJ1BYTE2_23	RJ1BYTE1_23	RJ1BYTE0_23
EA	11101010	RJ1BYTE7_22	RJ1BYTE6_22	RJ1BYTE5_22	RJ1BYTE4_22	RJ1BYTE3_22	RJ1BYTE2_22	RJ1BYTE1_22	RJ1BYTE0_22
EB	11101011	RJ1BYTE7_21	RJ1BYTE6_21	RJ1BYTE5_21	RJ1BYTE4_21	RJ1BYTE3_21	RJ1BYTE2_21	RJ1BYTE1_21	RJ1BYTE0_21
EC	11101100	RJ1BYTE7_20	RJ1BYTE6_20	RJ1BYTE5_20	RJ1BYTE4_20	RJ1BYTE3_20	RJ1BYTE2_20	RJ1BYTE1_20	RJ1BYTE0_20
ED	11101101	RJ1BYTE7_19	RJ1BYTE6_19	RJ1BYTE5_19	RJ1BYTE4_19	RJ1BYTE3_19	RJ1BYTE2_19	RJ1BYTE1_19	RJ1BYTE0_19
EE	11101110	RJ1BYTE7_18	RJ1BYTE6_18	RJ1BYTE5_18	RJ1BYTE4_18	RJ1BYTE3_18	RJ1BYTE2_18	RJ1BYTE1_18	RJ1BYTE0_18
EF	11101111	RJ1BYTE7_17	RJ1BYTE6_17	RJ1BYTE5_17	RJ1BYTE4_17	RJ1BYTE3_17	RJ1BYTE2_17	RJ1BYTE1_17	RJ1BYTE0_17
F0	11110000	RJ1BYTE7_16	RJ1BYTE6_16	RJ1BYTE5_16	RJ1BYTE4_16	RJ1BYTE3_16	RJ1BYTE2_16	RJ1BYTE1_16	RJ1BYTE0_16
F1	11110001	RJ1BYTE7_15	RJ1BYTE6_15	RJ1BYTE5_15	RJ1BYTE4_15	RJ1BYTE3_15	RJ1BYTE2_15	RJ1BYTE1_15	RJ1BYTE0_15
F2	11110010	RJ1BYTE7_14	RJ1BYTE6_14	RJ1BYTE5_14	RJ1BYTE4_14	RJ1BYTE3_14	RJ1BYTE2_14	RJ1BYTE1_14	RJ1BYTE0_14
F3	11110011	RJ1BYTE7_13	RJ1BYTE6_13	RJ1BYTE5_13	RJ1BYTE4_13	RJ1BYTE3_13	RJ1BYTE2_13	RJ1BYTE1_13	RJ1BYTE0_13
F4	11110100	RJ1BYTE7_12	RJ1BYTE6_12	RJ1BYTE5_12	RJ1BYTE4_12	RJ1BYTE3_12	RJ1BYTE2_12	RJ1BYTE1_12	RJ1BYTE0_12
F5	11110101	RJ1BYTE7_11	RJ1BYTE6_11	RJ1BYTE5_11	RJ1BYTE4_11	RJ1BYTE3_11	RJ1BYTE2_11	RJ1BYTE1_11	RJ1BYTE0_11
F6	11110110	RJ1BYTE7_10	RJ1BYTE6_10	RJ1BYTE5_10	RJ1BYTE4_10	RJ1BYTE3_10	RJ1BYTE2_10	RJ1BYTE1_10	RJ1BYTE0_10
F7	11110111	RJ1BYTE7_9	RJ1BYTE6_9	RJ1BYTE5_9	RJ1BYTE4_9	RJ1BYTE3_9	RJ1BYTE2_9	RJ1BYTE1_9	RJ1BYTE0_9
F8	11111000	RJ1BYTE7_8	RJ1BYTE6_8	RJ1BYTE5_8	RJ1BYTE4_8	RJ1BYTE3_8	RJ1BYTE2_8	RJ1BYTE1_8	RJ1BYTE0_8
F9	11111001	RJ1BYTE7_7	RJ1BYTE6_7	RJ1BYTE5_7	RJ1BYTE4_7	RJ1BYTE3_7	RJ1BYTE2_7	RJ1BYTE1_7	RJ1BYTE0_7
FA	11111010	RJ1BYTE7_6	RJ1BYTE6_6	RJ1BYTE5_6	RJ1BYTE4_6	RJ1BYTE3_6	RJ1BYTE2_6	RJ1BYTE1_6	RJ1BYTE0_6
FB	11111011	RJ1BYTE7_5	RJ1BYTE6_5	RJ1BYTE5_5	RJ1BYTE4_5	RJ1BYTE3_5	RJ1BYTE2_5	RJ1BYTE1_5	RJ1BYTE0_5
FC	11111100	RJ1BYTE7_4	RJ1BYTE6_4	RJ1BYTE5_4	RJ1BYTE4_4	RJ1BYTE3_4	RJ1BYTE2_4	RJ1BYTE1_4	RJ1BYTE0_4
FD	11111101	RJ1BYTE7_3	RJ1BYTE6_3	RJ1BYTE5_3	RJ1BYTE4_3	RJ1BYTE3_3	RJ1BYTE2_3	RJ1BYTE1_3	RJ1BYTE0_3
FE	11111110	RJ1BYTE7_2	RJ1BYTE6_2	RJ1BYTE5_2	RJ1BYTE4_2	RJ1BYTE3_2	RJ1BYTE2_2	RJ1BYTE1_2	RJ1BYTE0_2
FF	11111111	RJ1BYTE7_1	RJ1BYTE6_1	RJ1BYTE5_1	RJ1BYTE4_1	RJ1BYTE3_1	RJ1BYTE2_1	RJ1BYTE1_1	RJ1BYTE0_1

Microprocessor Interface Description (continued)

Register Architecture Map (continued)

Table 14. Device Register Map (continued)

Address		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
**Block Registers 0xC0—0xFF: Transmit J1 Path Trace Bytes**									
Register 0xBF Settings: TJ1BYTE_RD = 1, BIP_CNTS = 0, REI_CNTS = 0, RJ1BYTE = 0									
C0	11000000	TJ1BYTE7_64	TJ1BYTE6_64	TJ1BYTE5_64	TJ1BYTE4_64	TJ1BYTE3_64	TJ1BYTE2_64	TJ1BYTE1_64	TJ1BYTE0_64
C1	11000001	TJ1BYTE7_63	TJ1BYTE6_63	TJ1BYTE5_63	TJ1BYTE4_63	TJ1BYTE3_63	TJ1BYTE2_63	TJ1BYTE1_63	TJ1BYTE0_63
C2	11000010	TJ1BYTE7_62	TJ1BYTE6_62	TJ1BYTE5_62	TJ1BYTE4_62	TJ1BYTE3_62	TJ1BYTE2_62	TJ1BYTE1_62	TJ1BYTE0_62
C3	11000011	TJ1BYTE7_61	TJ1BYTE6_61	TJ1BYTE5_61	TJ1BYTE4_61	TJ1BYTE3_61	TJ1BYTE2_61	TJ1BYTE1_61	TJ1BYTE0_61
C4	11000100	TJ1BYTE7_60	TJ1BYTE6_60	TJ1BYTE5_60	TJ1BYTE4_60	TJ1BYTE3_60	TJ1BYTE2_60	TJ1BYTE1_60	TJ1BYTE0_60
C5	11000101	TJ1BYTE7_59	TJ1BYTE6_59	TJ1BYTE5_59	TJ1BYTE4_59	TJ1BYTE3_59	TJ1BYTE2_59	TJ1BYTE1_59	TJ1BYTE0_59
C6	11000110	TJ1BYTE7_58	TJ1BYTE6_58	TJ1BYTE5_58	TJ1BYTE4_58	TJ1BYTE3_58	TJ1BYTE2_58	TJ1BYTE1_58	TJ1BYTE0_58
C7	11000111	TJ1BYTE7_57	TJ1BYTE6_57	TJ1BYTE5_57	TJ1BYTE4_57	TJ1BYTE3_57	TJ1BYTE2_57	TJ1BYTE1_57	TJ1BYTE0_57
C8	11001000	TJ1BYTE7_56	TJ1BYTE6_56	TJ1BYTE5_56	TJ1BYTE4_56	TJ1BYTE3_56	TJ1BYTE2_56	TJ1BYTE1_56	TJ1BYTE0_56
C9	11001001	TJ1BYTE7_55	TJ1BYTE6_55	TJ1BYTE5_55	TJ1BYTE4_55	TJ1BYTE3_55	TJ1BYTE2_55	TJ1BYTE1_55	TJ1BYTE0_55
CA	11001010	TJ1BYTE7_54	TJ1BYTE6_54	TJ1BYTE5_54	TJ1BYTE4_54	TJ1BYTE3_54	TJ1BYTE2_54	TJ1BYTE1_54	TJ1BYTE0_54
CB	11001011	TJ1BYTE7_53	TJ1BYTE6_53	TJ1BYTE5_53	TJ1BYTE4_53	TJ1BYTE3_53	TJ1BYTE2_53	TJ1BYTE1_53	TJ1BYTE0_53
CC	11001100	TJ1BYTE7_52	TJ1BYTE6_52	TJ1BYTE5_52	TJ1BYTE4_52	TJ1BYTE3_52	TJ1BYTE2_52	TJ1BYTE1_52	TJ1BYTE0_52
CD	11001101	TJ1BYTE7_51	TJ1BYTE6_51	TJ1BYTE5_51	TJ1BYTE4_51	TJ1BYTE3_51	TJ1BYTE2_51	TJ1BYTE1_51	TJ1BYTE0_51
CE	11001110	TJ1BYTE7_50	TJ1BYTE6_50	TJ1BYTE5_50	TJ1BYTE4_50	TJ1BYTE3_50	TJ1BYTE2_50	TJ1BYTE1_50	TJ1BYTE0_50
CF	11001111	TJ1BYTE7_49	TJ1BYTE6_49	TJ1BYTE5_49	TJ1BYTE4_49	TJ1BYTE3_49	TJ1BYTE2_49	TJ1BYTE1_49	TJ1BYTE0_49
D0	11010000	TJ1BYTE7_48	TJ1BYTE6_48	TJ1BYTE5_48	TJ1BYTE4_48	TJ1BYTE3_48	TJ1BYTE2_48	TJ1BYTE1_48	TJ1BYTE0_48
D1	11010001	TJ1BYTE7_47	TJ1BYTE6_47	TJ1BYTE5_47	TJ1BYTE4_47	TJ1BYTE3_47	TJ1BYTE2_47	TJ1BYTE1_47	TJ1BYTE0_47
D2	11010010	TJ1BYTE7_46	TJ1BYTE6_46	TJ1BYTE5_46	TJ1BYTE4_46	TJ1BYTE3_46	TJ1BYTE2_46	TJ1BYTE1_46	TJ1BYTE0_46
D3	11010011	TJ1BYTE7_45	TJ1BYTE6_45	TJ1BYTE5_45	TJ1BYTE4_45	TJ1BYTE3_45	TJ1BYTE2_45	TJ1BYTE1_45	TJ1BYTE0_45
D4	11010100	TJ1BYTE7_44	TJ1BYTE6_44	TJ1BYTE5_44	TJ1BYTE4_44	TJ1BYTE3_44	TJ1BYTE2_44	TJ1BYTE1_44	TJ1BYTE0_44
D5	11010101	TJ1BYTE7_43	TJ1BYTE6_43	TJ1BYTE5_43	TJ1BYTE4_43	TJ1BYTE3_43	TJ1BYTE2_43	TJ1BYTE1_43	TJ1BYTE0_43
D6	11010110	TJ1BYTE7_42	TJ1BYTE6_42	TJ1BYTE5_42	TJ1BYTE4_42	TJ1BYTE3_42	TJ1BYTE2_42	TJ1BYTE1_42	TJ1BYTE0_42
D7	11010111	TJ1BYTE7_41	TJ1BYTE6_41	TJ1BYTE5_41	TJ1BYTE4_41	TJ1BYTE3_41	TJ1BYTE2_41	TJ1BYTE1_41	TJ1BYTE0_41
D8	11011000	TJ1BYTE7_40	TJ1BYTE6_40	TJ1BYTE5_40	TJ1BYTE4_40	TJ1BYTE3_40	TJ1BYTE2_40	TJ1BYTE1_40	TJ1BYTE0_40
D9	11011001	TJ1BYTE7_39	TJ1BYTE6_39	TJ1BYTE5_39	TJ1BYTE4_39	TJ1BYTE3_39	TJ1BYTE2_39	TJ1BYTE1_39	TJ1BYTE0_39
DA	11011010	TJ1BYTE7_38	TJ1BYTE6_38	TJ1BYTE5_38	TJ1BYTE4_38	TJ1BYTE3_38	TJ1BYTE2_38	TJ1BYTE1_38	TJ1BYTE0_38
DB	11011011	TJ1BYTE7_37	TJ1BYTE6_37	TJ1BYTE5_37	TJ1BYTE4_37	TJ1BYTE3_37	TJ1BYTE2_37	TJ1BYTE1_37	TJ1BYTE0_37
DC	11011100	TJ1BYTE7_36	TJ1BYTE6_36	TJ1BYTE5_36	TJ1BYTE4_36	TJ1BYTE3_36	TJ1BYTE2_36	TJ1BYTE1_36	TJ1BYTE0_36
DD	11011101	TJ1BYTE7_35	TJ1BYTE6_35	TJ1BYTE5_35	TJ1BYTE4_35	TJ1BYTE3_35	TJ1BYTE2_35	TJ1BYTE1_35	TJ1BYTE0_35
DE	11011110	TJ1BYTE7_34	TJ1BYTE6_34	TJ1BYTE5_34	TJ1BYTE4_34	TJ1BYTE3_34	TJ1BYTE2_34	TJ1BYTE1_34	TJ1BYTE0_34
DF	11011111	TJ1BYTE7_33	TJ1BYTE6_33	TJ1BYTE5_33	TJ1BYTE4_33	TJ1BYTE3_33	TJ1BYTE2_33	TJ1BYTE1_33	TJ1BYTE0_33
E0	11100000	TJ1BYTE7_32	TJ1BYTE6_32	TJ1BYTE5_32	TJ1BYTE4_32	TJ1BYTE3_32	TJ1BYTE2_32	TJ1BYTE1_32	TJ1BYTE0_32
E1	11100001	TJ1BYTE7_31	TJ1BYTE6_31	TJ1BYTE5_31	TJ1BYTE4_31	TJ1BYTE3_31	TJ1BYTE2_31	TJ1BYTE1_31	TJ1BYTE0_31
E2	11100010	TJ1BYTE7_30	TJ1BYTE6_30	TJ1BYTE5_30	TJ1BYTE4_30	TJ1BYTE3_30	TJ1BYTE2_30	TJ1BYTE1_30	TJ1BYTE0_30
E3	11100011	TJ1BYTE7_29	TJ1BYTE6_29	TJ1BYTE5_29	TJ1BYTE4_29	TJ1BYTE3_29	TJ1BYTE2_29	TJ1BYTE1_29	TJ1BYTE0_29
E4	11100100	TJ1BYTE7_28	TJ1BYTE6_28	TJ1BYTE5_28	TJ1BYTE4_28	TJ1BYTE3_28	TJ1BYTE2_28	TJ1BYTE1_28	TJ1BYTE0_28
E5	11100101	TJ1BYTE7_27	TJ1BYTE6_27	TJ1BYTE5_27	TJ1BYTE4_27	TJ1BYTE3_27	TJ1BYTE2_27	TJ1BYTE1_27	TJ1BYTE0_27
E6	11100110	TJ1BYTE7_26	TJ1BYTE6_26	TJ1BYTE5_26	TJ1BYTE4_26	TJ1BYTE3_26	TJ1BYTE2_26	TJ1BYTE1_26	TJ1BYTE0_26

Microprocessor Interface Description (continued)

Register Architecture Map (continued)

Table 14. Device Register Map (continued)

Address		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Block Registers 0xC0—0xFF: Transmit J1 Path Trace Bytes (continued)									
E7	11100111	TJ1BYTE7_25	TJ1BYTE6_25	TJ1BYTE5_25	TJ1BYTE4_25	TJ1BYTE3_25	TJ1BYTE2_25	TJ1BYTE1_25	TJ1BYTE0_25
E8	11101000	TJ1BYTE7_24	TJ1BYTE6_24	TJ1BYTE5_24	TJ1BYTE4_24	TJ1BYTE3_24	TJ1BYTE2_24	TJ1BYTE1_24	TJ1BYTE0_24
E9	11101001	TJ1BYTE7_23	TJ1BYTE6_23	TJ1BYTE5_23	TJ1BYTE4_23	TJ1BYTE3_23	TJ1BYTE2_23	TJ1BYTE1_23	TJ1BYTE0_23
EA	11101010	TJ1BYTE7_22	TJ1BYTE6_22	TJ1BYTE5_22	TJ1BYTE4_22	TJ1BYTE3_22	TJ1BYTE2_22	TJ1BYTE1_22	TJ1BYTE0_22
EB	11101011	TJ1BYTE7_21	TJ1BYTE6_21	TJ1BYTE5_21	TJ1BYTE4_21	TJ1BYTE3_21	TJ1BYTE2_21	TJ1BYTE1_21	TJ1BYTE0_21
EC	11101100	TJ1BYTE7_20	TJ1BYTE6_20	TJ1BYTE5_20	TJ1BYTE4_20	TJ1BYTE3_20	TJ1BYTE2_20	TJ1BYTE1_20	TJ1BYTE0_20
ED	11101101	TJ1BYTE7_19	TJ1BYTE6_19	TJ1BYTE5_19	TJ1BYTE4_19	TJ1BYTE3_19	TJ1BYTE2_19	TJ1BYTE1_19	TJ1BYTE0_19
EE	11101110	TJ1BYTE7_18	TJ1BYTE6_18	TJ1BYTE5_18	TJ1BYTE4_18	TJ1BYTE3_18	TJ1BYTE2_18	TJ1BYTE1_18	TJ1BYTE0_18
EF	11101111	TJ1BYTE7_17	TJ1BYTE6_17	TJ1BYTE5_17	TJ1BYTE4_17	TJ1BYTE3_17	TJ1BYTE2_17	TJ1BYTE1_17	TJ1BYTE0_17
F0	11110000	TJ1BYTE7_16	TJ1BYTE6_16	TJ1BYTE5_16	TJ1BYTE4_16	TJ1BYTE3_16	TJ1BYTE2_16	TJ1BYTE1_16	TJ1BYTE0_16
F1	11110001	TJ1BYTE7_15	TJ1BYTE6_15	TJ1BYTE5_15	TJ1BYTE4_15	TJ1BYTE3_15	TJ1BYTE2_15	TJ1BYTE1_15	TJ1BYTE0_15
F2	11110010	TJ1BYTE7_14	TJ1BYTE6_14	TJ1BYTE5_14	TJ1BYTE4_14	TJ1BYTE3_14	TJ1BYTE2_14	TJ1BYTE1_14	TJ1BYTE0_14
F3	11110011	TJ1BYTE7_13	TJ1BYTE6_13	TJ1BYTE5_13	TJ1BYTE4_13	TJ1BYTE3_13	TJ1BYTE2_13	TJ1BYTE1_13	TJ1BYTE0_13
F4	11110100	TJ1BYTE7_12	TJ1BYTE6_12	TJ1BYTE5_12	TJ1BYTE4_12	TJ1BYTE3_12	TJ1BYTE2_12	TJ1BYTE1_12	TJ1BYTE0_12
F5	11110101	TJ1BYTE7_11	TJ1BYTE6_11	TJ1BYTE5_11	TJ1BYTE4_11	TJ1BYTE3_11	TJ1BYTE2_11	TJ1BYTE1_11	TJ1BYTE0_11
F6	11110110	TJ1BYTE7_10	TJ1BYTE6_10	TJ1BYTE5_10	TJ1BYTE4_10	TJ1BYTE3_10	TJ1BYTE2_10	TJ1BYTE1_10	TJ1BYTE0_10
F7	11110111	TJ1BYTE7_9	TJ1BYTE6_9	TJ1BYTE5_9	TJ1BYTE4_9	TJ1BYTE3_9	TJ1BYTE2_9	TJ1BYTE1_9	TJ1BYTE0_9
F8	11111000	TJ1BYTE7_8	TJ1BYTE6_8	TJ1BYTE5_8	TJ1BYTE4_8	TJ1BYTE3_8	TJ1BYTE2_8	TJ1BYTE1_8	TJ1BYTE0_8
F9	11111001	TJ1BYTE7_7	TJ1BYTE6_7	TJ1BYTE5_7	TJ1BYTE4_7	TJ1BYTE3_7	TJ1BYTE2_7	TJ1BYTE1_7	TJ1BYTE0_7
FA	11111010	TJ1BYTE7_6	TJ1BYTE6_6	TJ1BYTE5_6	TJ1BYTE4_6	TJ1BYTE3_6	TJ1BYTE2_6	TJ1BYTE1_6	TJ1BYTE0_6
FB	11111011	TJ1BYTE7_5	TJ1BYTE6_5	TJ1BYTE5_5	TJ1BYTE4_5	TJ1BYTE3_5	TJ1BYTE2_5	TJ1BYTE1_5	TJ1BYTE0_5
FC	11111100	TJ1BYTE7_4	TJ1BYTE6_4	TJ1BYTE5_4	TJ1BYTE4_4	TJ1BYTE3_4	TJ1BYTE2_4	TJ1BYTE1_4	TJ1BYTE0_4
FD	11111101	TJ1BYTE7_3	TJ1BYTE6_3	TJ1BYTE5_3	TJ1BYTE4_3	TJ1BYTE3_3	TJ1BYTE2_3	TJ1BYTE1_3	TJ1BYTE0_3
FE	11111110	TJ1BYTE7_2	TJ1BYTE6_2	TJ1BYTE5_2	TJ1BYTE4_2	TJ1BYTE3_2	TJ1BYTE2_2	TJ1BYTE1_2	TJ1BYTE0_2
FF	11111111	TJ1BYTE7_1	TJ1BYTE6_1	TJ1BYTE5_1	TJ1BYTE4_1	TJ1BYTE3_1	TJ1BYTE2_1	TJ1BYTE1_1	TJ1BYTE0_1

Microprocessor Interface Description (continued)

Register Architecture Description

Hexadecimal notation is used in both the Address and the Reset Default columns in all the register description tables in this section.

Device-Level Control, Alarm, and Mask Bits (0x00—0x16)

Table 15. Registers 0x00—0x16: Device-Level Control, Alarm, and Mask Bits

Address (Hex)	Bit #	Name	Function	Reset Default (Hex)
0x00	—	—	The bits in the register 0x00 are used for device-level control and error reporting.	0x00
	7	TEST_CNT	Factory Test Mode. TEST_CNT = 1 forces all internal counters to test mode and is intended for factory use only. This bit should always be set to 0.	
	6	B1ERRINS	B1ERRINS, B2ERRINS, and B3ERRINS. B1ERRINS, B2ERRINS, and B3ERRINS all cause continuous BIP-8 errors to be transmitted in their respective BIP-8 values.	
	5	B2ERRINS		
	4	B3ERRINS		
	3	LATCH_CNT	Latch Count. The device has a number of BIP, REI, and pointer adjustment counters that are all updated when the LATCH_CNT bit is written from 0 to 1. Nothing happens when the bit is written from 1 to 0. The only internal counter that is not updated by this bit is the test pattern counter.	
	2	BLUECLKSEL	The device can accept a blue signal clock at either the exact DS1 rate (BLUECLKSEL = 0), or at 16 times the DS1 rate (BLUECLKSEL = 1).	
	1	BIPBLKCNT	BIP Error Counter or BIP Block Counter. The BIPBLKCNT bit is used to determine whether the BIP counters count the number of BIP errors (BIPBLKCNT = 0) or the number of BIP blocks that contain errors (BIPBLKCNT = 1).	
	0	—	Reserved.	

Microprocessor Interface Description (continued)

Register Architecture Description (continued)

Table 15. **Registers 0x00—0x16: Device-Level Control, Alarm, and Mask Bits** (continued)

Address (Hex)	Bit #	Name	Function	Reset Default (Hex)
0x01	—	—	The bits in register 0x01 are used to provision device-level control bits. The functions of these bits are described below.	0x00
	7	REI_EN	REI_Enable. When REI_EN = 1, the device will automatically insert the appropriate REI into the transmitted Z2, G1, V5 overhead bytes whenever it receives BIP errors. If REI_EN = 0, then the automatic insertion of REI is disabled.	
	6	AUTO_LRDI	When AUTO_LRDI = 1, the device will automatically insert line RDI.	
	5	TXPAISINS	When TXPAISINS = 1, the device will write all 1s into the pointer bytes (H1—H3) and all of the synchronous payload envelope (SPE).	
	4	DJACTL	The DJACTL is used to enable the use of the built-in digital jitter attenuators. When DJACTL = 0, the gapped DS1/E1 clock and data are transmitted by the device; otherwise, the smoothed clock and data are transmitted.	
	3	—	Reserved.	
	2	STS1SCR	STS-1_Scramble. When STS1SCR = 1, the device scrambles the outgoing STS-1 frame according to the SONET frame synchronous scrambling sequence $1 + x^6 + x^7$. The sequence is reset to 1111111 at the beginning of the byte following the C1 byte and scrambles all of the STS-1 data except the A1, A2, and C1 bytes. When this bit is 0, then the transmit data is not scrambled.	
	1	STS1DSCR	STS-1_Descramble. When STS1DSCR = 1, the device descrambles the incoming STS-1 frame according to the SONET frame synchronous descrambling sequence $1 + x^6 + x^7$. The sequence is reset to 1111111 at the beginning of the byte following the C1 byte and descrambles all of the STS-1 data except the A1, A2, and C1 bytes. When this bit is 0, then the received data is not descrambled.	
	0	STS1LB	STS-1_Loopback. When STS1LB = 1, the transmitted data is looped back to the receive side. When this bit is 0, the device uses the received data.	

Microprocessor Interface Description (continued)

Register Architecture Description (continued)

Table 15. **Registers 0x00—0x16: Device-Level Control, Alarm, and Mask Bits** (continued)

Address (Hex)	Bit #	Name	Function	Reset Default (Hex)
0x02	—	—	The bits in register 0x02 are used to set the edges that retime data into and out of the device.	0x00
	7	RXSERIAL	Receive Serial Data, Transmit Serial Data. Both the RXSERIAL and TXSERIAL bits are used to set the type of STS-1 data. When either serial bit is written to 1, the STS-1 rail runs in serial mode; otherwise, the STS-1 rail runs in parallel mode.	
	6	TXSERIAL		
	5	RXPARITY	Both the RXPARITY and TXPARITY bits determine the type of parity for data buses. When these bits are written with 1, odd parity is used; otherwise, even parity is used.	
	4	TXPARITY		
	3	RXSTS1EDGE	When the edge register bits are set to 1, the data is retimed (either in or out) by the rising clock edge; when set to a logic 0, the data is retimed by the falling clock edge. Note that the TSTS1SERIAL data always comes out on the rising edge of the TSTS1CLKOUT.	
	2	TXSTS1EDGE		
	1	RXDS1EDGE		
	0	TXDS1EDGE	**Note:** The TXSTS1EDGE (bit 2) should always be set to 0 to avoid potential race condition inside the device.	

Microprocessor Interface Description (continued)

Register Architecture Description (continued)

Table 15. **Registers 0x00—0x16: Device-Level Control, Alarm, and Mask Bits** (continued)

Address (Hex)	Bit #	Name	Function	Reset Default (Hex)
0x03	—	—	The bits in register 0x03 are used to report problems at the receive STS-1 level.	0x00
	7	TRACEER	The device monitors the received J1 byte for path trace mismatches. When the received J1 byte pattern does not match the previously received pattern, then TRACEER = 1. This is an event bit and is held until read.	
	6	RXPARER	RXPARER = 1 reports a parity violation on the receive STS-1 data bus when in parallel mode. This is an event bit and is held until read.	
	5	—	Reserved.	
	4	H4LOMF	The device monitors the incoming H4 byte for loss of multi-frame indication (H4LOMF = 1). This is an event bit and is held until read.	
	3	STS1PAIS	STS1PAIS = 1 reports path AIS as detected by the receive pointer interpreter. This is a current state bit with a minimum persistence of 375 µs. The indications reset if the condition is no longer true.	
	2	STS1LOP	STS1LOP = 1 reports a loss of STS-1 pointer. This is a current state bit with a minimum persistence of 125 µs. The indications reset if the condition is no longer true.	
	1	STS1LOF	STS1LOF = 1 reports an out of frame condition that persists for more than 3 ms. This is a current state bit with a minimum persistence of 3 ms. The indications reset if the condition is no longer true.	
	0	STS1OOF	STS1OOF = 1 reports an out of frame condition on the receive STS-1 signal. This is a current state bit with a minimum persistence of 500 µs. The indications reset if the condition is no longer true.	
0x04	7	TRACEERMSK	The bits in register 0x04 are used to mask the contributions of the bits in register 0x03 to the microprocessor interrupt output, INT. When any of these bits are at a logic 1 level, the corresponding bit in register 0x03 is masked from contributing to the output interrupt. The reset default for this register masks all of the bits in register 0x03. Bit 5 is reserved.	0xFF
	6	RXPARERMSK		
	5	—		
	4	H4LOMFMSK		
	3	STS1PAISMSK		
	2	STS1LOPMSK		
	1	STS1LOFMSK		
	0	STS1OOFMSK		

Microprocessor Interface Description (continued)

Register Architecture Description (continued)

Table 15. **Registers 0x00—0x16: Device-Level Control, Alarm, and Mask Bits** (continued)

Address (Hex)	Bit #	Name	Function	Reset Default (Hex)
0x05	—	—	The bits in register 0x05 are used to report problems at the receive DS1/E1 and VT level. The bits in this register are composite bits. The bits that report the problems at the VT level are located in 28 separate registers (one for each VT) as described below. These composite bits are placed in the register map to determine which type of error was detected. When any one of the 28 VT bits indicates an error, the corresponding composite bit indicates an error.	0x00
	7	ESOFCOM	ESOFCOM = 1 reports that the device has experienced either a receive or a transmit elastic store overflow. This is an event bit and is held until read.	
	6	VTSIZECOM	VTSIZECOM = 1 reports incorrect VT size bits. The valid VT size bits are 11 for VT1.5 and 10 for VT2.	
	5	VTLOPCOM	VTLOPCOM = 1 reports LOP-V.	
	4	VTRFIRDICOM	VTRFIRDICOM = 1 reports the fact that the VT RFI/RDI bits have been received as a new consistent value for three consecutive superframes. This is an event bit and is held until read.	
	3	VTAISCOM	VTAISCOM = 1 reports the fact that the V1 and V2 pointer bytes are all 1s for three consecutive superframes.	
	2	VTLABCOM	VTLABCOM = 1 reports change of state of the VT label. In order for this bit to be set, the device must detect three consecutive consistent new values for the VT label. This is an event bit and is held until read.	
	1	AISLOCCOM	AISLOCCOM = 1 reports an AIS or LOC condition on DS1/E1. This is a current state bit with a minimum persistence of 2 ms. The indications reset if the condition is no longer true.	
	0	STS1LOS	STS1LOS = 1 reports an STS-1 loss of signal. The bits in register 0x91 are used to set the number of 6.48 MHz clock periods required to declare received STS-1 loss of signal. If this value is 0x00, then STS1LOS is not declared. This is a current state bit with a minimum persistence of 250 μs. The indications reset if the condition is no longer true.	

Microprocessor Interface Description (continued)

Register Architecture Description (continued)

Table 15. **Registers 0x00—0x16: Device-Level Control, Alarm, and Mask Bits** (continued)

Address (Hex)	Bit #	Name	Function	Reset Default (Hex)
0x06	7	ESOFMSK	The bits in register 0x06 are used to mask the contributions of the bits in register 0x05 to the microprocessor interrupt output, INT. When any of these bits is 1, the corresponding bit in register 0x05 is masked from contributing to the output interrupt. The reset default for this register masks all of the bits in register 0x05.	0xFF
	6	VTSIZEMSK		
	5	VTLOPMSK		
	4	VTRFIRDIMSK		
	3	VTAISMSK		
	2	VTLABMSK		
	1	AISLOCMSK		
	0	STS1LOSMSK		
0x07			This register reports the hardware selected device mode.	0x01
	7—1	—	Reserved. These bits are set to 0 at reset.	
	0	DS1_E1N	This bit reports the DS1_E1N value from the device input pin.	
0x08			The bits in register 0x08 are used to configure the test pattern generator and detector.	0x00
	7	LATCH_TP	A 0 to 1 transition on LATCH_TP causes the running error count to be latched and presented to the microprocessor.	
	6	RCV_FRAME	RCV_FRAME = 1 causes a framed test pattern to be expected; a 0 causes an unframed test pattern to be expected.	
	5	RCV_PAT-1	RCV_PAT[1:0] determines the receive test pattern sequence where 00 = QRSS, 01 = $2^{23} - 1$, $10 = 2^{20} - 1$, $11 = 2^{15} - 1$.	
	4	RCV_PAT-0		
	3	ERROR_INS	ERROR_INS causes a single error to be inserted in the data (not frame) bits after a 0 to 1 transition.	
	2	XMT_FRAME	XMT_FRAME = 1 causes a framed test pattern to be generated; a 0 causes an unframed test pattern to be generated.	
	1	XMT_PAT-1	XMTPAT-[1:0] determines the transmit test pattern sequence where 00 = QRSS, 01 = $2^{23} - 1$, $10 = 2^{20} - 1$, $11 = 2^{15} - 1$.	
	0	XMT_PAT-0		

Microprocessor Interface Description (continued)

Register Architecture Description (continued)

Table 15. **Registers 0x00—0x16: Device-Level Control, Alarm, and Mask Bits** (continued)

Address (Hex)	Bit #	Name	Function	Reset Default (Hex)
0x09	—	—	The bits in register 0x09 are used to set up the test pattern.	0x00
	7	TP_DS1E1N	TP_DS1E1N = 1 sets the frame sequence to DS1; TP_DS1E1N = 0 sets the frame sequence to E1.	
	6	TP_INVERT	TP_INVERT = 1 forces the test pattern sequence to be inverted.	
	5	TPDROPSIDE	When TPDROPSIDE = 1, the test pattern is dropped from the SPE drop logic. The DS1/E1 output that is dropped is described in the Microprocessor Interface Description (continued) section on page 50. When TPDROPSIDE = 0, the DS1/E1 that is dropped is the same as described in the DS1/E1 Insertion Selection section on page 47.	
	4	TPDROP-4	The TPDROP[4:0] bits are used to select the VT that needs to be dropped.	
	3	TPDROP-3		
	2	TPDROP-2		
	1	TPDROP-1		
	0	TPDROP-0		
0x0A	—	—	The bits in register 0x0A indicate the condition of the test pattern detector.	0x80
	7	TPOOS	If the test pattern detector has been able to synchronize on the dropped signal, then TPOOS = 0.	
	6	TPERR-6	When TPOOS = 0, then the TPERR-[6:0] bits are used to keep count of the number of bit errors the test pattern detector has seen. This error count is cleared when the register is read by the microprocessor.	
	5	TPERR-5		
	4	TPERR-4		
	3	TPERR-3		
	2	TPERR-2		
	1	TPERR-1		
	0	TPERR-0		
0x0B	7—0	F2-[7:0]	The F2-[7:0] bits in register 0x0B are used to report the F2 receive byte in the path overhead.	0x00
0x0C	7—0	C2-[7:0]	The C2-[7:0] bits in register 0x0C are used to report the received C2 label byte in the path overhead. The default value for this register indicates path unequipped.	0x00

Microprocessor Interface Description (continued)

Register Architecture Description (continued)

Table 15. **Registers 0x00—0x16: Device-Level Control, Alarm, and Mask Bits** (continued)

Address (Hex)	Bit #	Name	Function	Reset Default (Hex)
0x0D	—	—	The bits in register 0x0D are used to report path and section overhead.	0x00
	7	G1-5	The G1-[5:8] are used to report the four least significant bits of the G1 path overhead byte.	
	6	G1-6		
	5	G1-7		
	4	G1-8		
	3	—	Reserved.	
	2	K2-6	The K2-[6:8] bits are used to report the three least significant bits of the K2 section overhead byte.	
	1	K2-7		
	0	K2-8		
0x0E	—	—	The bits in register 0x0E are used to set the number of consecutive, consistent values required by registers 0x0B and 0x0C before updating their values.	0x33
	7	C2#DET-3	The C2#DET-[3:0] bits are used to set the number of consecutive and consistent values required before updating C2-[7:0] bits in register 0x0C.	
	6	C2#DET-2		
	5	C2#DET-1		
	4	C2#DET-0		
	3	F2#DET-3	The F2#DET-[3:0] bits are used to set the number of consecutive and consistent values required before updating F2-[7:0] bits in register 0x0B. Valid values for this register range from 3 to 15. Any value less than 3 defaults to 2 inside the device.	
	2	F2#DET-2		
	1	F2#DET-1		
	0	F2#DET-0		
0x0F	—	—	The bits in register 0x0F are used to set the number of consecutive, consistent values required by register 0x0D before updating their values.	0x33
	7	G1#DET-3	The G1#DET-[3:0] bits are used to set the number of consecutive and consistent values required before updating G1-[5:8] bits in register 0x0D.	
	6	G1#DET-2		
	5	G1#DET-1		
	4	G1#DET-0		
	3	K2#DET-3	The K2#DET-[3:0] bits are used to set the number of consecutive and consistent values required before updating K2-[6:8] bits in register 0x0D. Valid values for this register range from 3 to 15. Any value less than 3 defaults to 2 inside the device.	
	2	K2#DET-2		
	1	K2#DET-1		
	0	K2#DET-0		
0x10	7—0	F2INS-[7:0]	The F2INS-[7:0] bits in register 0x10 are used to set the values to be transmitted in the F2 byte.	0x00

Microprocessor Interface Description (continued)

Register Architecture Description (continued)

Table 15. **Registers 0x00—0x16: Device-Level Control, Alarm, and Mask Bits** (continued)

Address (Hex)	Bit #	Name	Function	Reset Default (Hex)
0x11	—	—	The bits in register 0x11 are used to set the values to be transmitted in the G1 and K2 bytes.	0x00
	7	G1INS-5	The G1INS-[5:8] bits are used to set values to be transmitted in the four least significant bits of the G1 byte. The G1 byte is written by the microprocessor.	
	6	G1INS-6		
	5	G1INS-7		
	4	G1INS-8		
	3	—	Reserved.	
	2	K2INS-6	The K2INS-[6:8] bits are used to set the values to be transmitted in the three least significant bits of the K2 byte. AUTO_LRDI bit (bit 6 of register 0x01) should be set to 0 for K2INS-[6:8] insertion (i.e., K2 insertion) through the microprocessor interface.	
	1	K2INS-7		
	0	K2INS-8		
0x12	—	—	The bits in register 0x12 are used to set the bus mode of operation for both the transmit and receive sides.	0x24
	7—6	—	Reserved.	
	5	RBUSMODE	The RBUSMODE bit sets the STS-1 receive side of the device to the bus mode of operation when a 1; otherwise, the device is set to nonbus mode.	
	4	RBUSPOS-1	The RBUSPOS-[1:0] sets the time slot for the receive side. 00 causes the receive side not to listen. Otherwise, the time slots are determined by the binary value of these bits as follows: 01 = time slot 1 10 = time slot 2 11 = time slot 3	
	3	RBUSPOS-0		
	2	TBUSMODE	The TBUSMODE bit sets the STS-1 transmit side of the device to the bus mode of operation when a 1; otherwise, the device is set to nonbus mode.	
	1	TBUSPOS-1	The TBUSPOS-[1:0] sets the time slot for the transmit sides. 00 causes the transmit side not to transmit. Otherwise, the time slots are determined by the binary value of these bits as follows: 01 = time slot 1 10 = time slot 2 11 = time slot 3	
	0	TBUSPOS-0		

Microprocessor Interface Description (continued)

Register Architecture Description (continued)

Table 15. **Registers 0x00—0x16: Device-Level Control, Alarm, and Mask Bits** (continued)

Address (Hex)	Bit #	Name	Function	Reset Default (Hex)
0x13	7—4	—	Reserved.	0x00
	3	S1INS-3	The S1INS-[3:0] bits in register 0x13 are used to set the four least significant bits of the S1 path overhead byte.	
	2	S1INS-2		
	1	S1INS-1		
	0	S1INS-0		
0x14			The bits in register 0x14 are for the S1 path overhead byte.	0x30
	7	S1#DET-3	The S1#DET-[3:0] bits are used to set the number of consecutive, consistent values required by the receive S1 byte before updating the value. Valid values for these registers range from 3 to 15. Any value less than 3 defaults to 2 inside the device.	
	6	S1#DET-2		
	5	S1#DET-1		
	4	S1#DET-0		
	3	S1-3	The S1-[3:0] bits are used to report the four least significant bits of the S1 path overhead byte.	
	2	S1-2		
	1	S1-1		
	0	S1-0		
0x15	7—0	DEVID-[7:0]	DEVID-[7:0] bits in register 0x15 are used to report the device ID.	0x51
0x16	—	—	The DEVVER-[3:0] bits in register 0x16 are used to report the device version. Anytime there are silicon changes that modify the operation of this device, this register will be incremented by 1.	—
	7—4	—		
	3	DEVVER-3		
	2	DEVVER-2		
	1	DEVVER-1	**Notes:**	
	0	DEVVER-0	The reset default value is the device version. Bits 7—4 are reserved.	

Microprocessor Interface Description (continued)

Register Architecture Description (continued)

DS1/E1 Insertion Selection

Table 16. Registers 0x17—0x32: DS1/E1 Insertion Selection

Address (Hex)	Bit #	Name	Function	Reset Default (Hex)
0x17—0x2B	—	—	Registers 0x17—0x2B report DS1 or E1 conditions.	Value is 0.
	7	DS1/E1AIS[1:21]	The DS1/E1AIS[1:21] bits report the received DS1/E1 AIS condition. When any of these bits is 1, the corresponding DS1/E1 input has an AIS condition. This value represents the current received state. The AIS condition is not latched by these bits. The indication is reset when the condition is no longer true.	
	6	DS1/E1LOC[1:21]	The DS1/E1LOC[1:21] bits in bit 6 report the received DS1/E1 loss of clock condition. When any of these bits is 1, the corresponding DS1/E1 input has a received loss of clock condition. This value represents the current received state. The loss of clock condition is not latched by these bits. The indication is reset when the condition is no longer true.	
	5	DS1/E1LB[1:21]	The DS1/E1LB[1:21] bits in bit 5 are used to force DS1/E1 loopback from output to input. When any of these bits is 1, the corresponding DS1/E1 input is overwritten by the outgoing DS1/E1 signal for that location.	
	4	DS1/E1INS4_[1:21]	The DS1/E1INS[4:0]_[1:21] bits in registers 0x17—0x2B are used to select the DS1/E1 input for the transmit VT1.5 slots. The DS1/E1 selected corresponds to the decimal value of the programmed 5 bits. If these bits contain 00000, the device will insert unequipped into the corresponding VT1.5 slot. If these bits contain 11101—11110, the device will insert AIS-V into the corresponding VT1.5 slot. Since the device defaults all 28 of these registers to the value 00000, all of the 28 VT1.5 slots begin transmitting unequipped following reset. The value 11111 inserts the test pattern. Addresses 0x17—0x32 correspond to VT1.5s as shown in Table 17, page 49.	
	3	DS1/E1INS3_[1:21]		
	2	DS1/E1INS2_[1:21]		
	1	DS1/E1INS1_[1:21]		
	0	DS1/E1INS0_[1:21]		

Microprocessor Interface Description (continued)

Register Architecture Description (continued)

Table 16. Registers 0x17—0x32: DS1/E1 Insertion Selection (continued)

Address (Hex)	Bit #	Name	Function	Reset Default (Hex)
0x2C—0x32	—	—	Registers 0x17—0x32 report DS1 conditions.	Value is 0.
	7	DS1AIS[22:28]	The DS1/E1AIS[1:21] and DS1AIS[22:28] bits report the received DS1 AIS condition. When any of these bits is 1, the corresponding DS1 input has an AIS condition. This value represents the current received state. The AIS condition is not latched by these bits. The indication is reset when the condition is no longer true.	
	6	DS1LOC[22:28]	The DS1/E1LOC[1:21] and DS1LOC[22:28] bits in bit 6 report the received DS1 loss of clock condition. When any of these bits is 1, the corresponding DS1 input has a received loss of clock condition. This value represents the current received state. The loss of clock condition is not latched by these bits. The indication is reset when the condition is no longer true.	
	5	DS1LB[22:28]	The DS1/E1LB[1:21] and DS1LB[22:28] bits in bit 5 are used to force DS1 loopback from output to input. When any of these bits is 1, the corresponding DS1 input is overwritten by the outgoing DS1 signal for that location.	
	4	DS1INS4_[22:28]	The DS1/E1INS[4:0]_[1:21] and DS1INS[4:0]_[22:28] bits in registers 0x17—0x32 are used to select the DS1 input for the transmit VT1.5 slots. The DS1 selected corresponds to the decimal value of the programmed 5 bits. If these bits contain 00000, the device will insert unequipped into the corresponding VT1.5 slot. If these bits contain 11101—11110, the device will insert AIS-V into the corresponding VT1.5 slot. Since the device defaults all 28 of these registers to the value 00000, all of the 28 VT1.5 slots begin transmitting unequipped following reset. The value 11111 inserts the test pattern. Addresses 0x17—0x32 correspond to VT1.5s as shown in Table 17, page 49.	
	3	DS1INS3_[22:28]		
	2	DS1INS2_[22:28]		
	1	DS1INS1_[22:28]		
	0	DS1INS0_[22:28]		

Microprocessor Interface Description (continued)

Register Architecture Description (continued)

Table 17. DS1/E1 Insertion Selection Format

				5 Programmed DS1/E1INS[4:0]_x Bits				
VT1.5 #	**VT Group #**	**VT #**	**Address**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
1	1	1	17	0	0	0	0	1
2	2	1	18	0	0	0	1	0
3	3	1	19	0	0	0	1	1
•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•
26	5	4	30	1	1	0	1	0
27	6	4	31	1	1	0	1	1
28	7	4	32	1	1	1	0	0

VT Drop Selection (0x33—0x4E)

Table 18. Registers 0x33—0x4E: VT Drop Selection

Address (Hex)	Bit #	Name	Function	Reset Default (Hex)
0x33—0x4E	7	—	Reserved.	Value is 0.
	6	RXESOF[1:28]	The RXESOF[1:28] bits (see VT Drop Selection Registers, Table 14, page 25) report the receive elastic store overflow condition. When any of these bits is 1, the corresponding DS1/E1 output has experienced an elastic store overflow. This value is latched by these bits until read by the microprocessor.	
	5	TXESOF[1:28]	The TXESOF[1:28] bits (see Control, Alarm, and Mask Bit Registers, Table 14, page 23) report the transmit elastic store overflow condition. When any of these bits is 1, the corresponding DS1/E1 input has experienced an elastic store overflow. This value is latched by these bits until read by the microprocessor.	
	4	VTDROP4_[1:28]	These bits in registers 0x33—0x4E are used to select the VT1.5 slot for the DS1/E1 outputs. The VT1.5 selected in Table 17 corresponds to the decimal value of these programmed 5 bits. If these bits contain 00000, or 11101—11111, then the device inserts the following: 00000 = device does not transmit any clock or data 11101 = device inserts a DS1 AIS into the corresponding DS1/E1 slot 11110 = device inserts a E1 AIS into the corresponding DS1/E1 slot 11111= device inserts the test pattern Since the device defaults these bits in all 28 of these registers to 00000, there will be no clock or data in any of the 28 DS1 or 21 E1 slots after reset. VTDROP[4:0]_[1:28], bits 00001—11100, correspond to the specific VT1.5 streams as shown in Table , page 50. Address 0x33—0x4E correspond to VTs as shown in Table 20, also on page 50.	
	3	VTDROP3_[1:28]		
	2	VTDROP2_[1:28]		
	1	VTDROP1_[1:28]		
	0	VTDROP0_[1:28]		

Microprocessor Interface Description (continued)

Register Architecture Description (continued)

Table 19. VT Drop Selection Format

VT1.5 Drop #	VT Group #	VT #	5 Programmed DS1/E1INS[4:0]_x or VT Drop Data Bits				
			Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	1	1	0	0	0	0	1
2	2	1	0	0	0	1	0
3	3	1	0	0	0	1	1
•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•
26	5	4	1	1	0	1	0
27	6	4	1	1	0	1	1
28	7	4	1	1	1	0	0

Table 20. VT to Address Mapping

VT #	Address
1	33
2	34
3	35
•	•
•	•
26	4C
27	4D
28	4E

Microprocessor Interface Description (continued)

Register Architecture Description (continued)

Tx VT Overhead Insertion Control (0x4F—0x6A)

Table 21. Registers 0x4F—0x6A: Tx VT Overhead Insertion Control

Address (Hex)	Bit #	Name	Function	Reset Default (Hex)
0x4F—0x6A	—	—	The bits in these registers provision the transmitted VT overhead byte, V5.	Value is 0.
	7	BIP2ERINS[1:28]	Each BIP2ERINS[1:28] bit = 1 forces the selected VT to transmit inverted BIP-2 bits which causes the downstream receiver to declare continuous BIP-2 errors.	
	6	VTRFIRDIEN[1:28]	The VTRFIRDIEN[1:28] bits control whether RDI-V bits are inserted automatically by the device (VTRFIRDIEN[1:28] = 1) or manually by the microprocessor (VTRFIRDIEN[1:28] = 0).	
	5	VTRFIINS[1:28]	The VTRFIINS[1:28] bits directly program the transmitted RFI-V bits when the corresponding VTRFIRDIEN[1:28] bits = 1.	
	4	VTRDIINS[1:28]	The VTRDIINS[1:28] bits directly program the transmitted RDI-V bits when the corresponding VTRFIRDIEN[1:28] bits = 1.	
	3	VTAISINS[1:28]	Each VTAISINS[1:28] bit = 1 forces AIS-V to be written into the corresponding VT slot. This consists of writing all 1s into the selected VT slot.	
	2	VTLABINS2_[1:28]	The VTLABINS[2:0]_[1:28] bits directly program the transmitted VT label bits. These bits are used to carry unequipped information (VTLABINS[2:0]_[1:28] = 000) as well as specific payload mappings and AIS-V.	
	1	VTLABINS1_[1:28]		
	0	VTLABINS0_[1:28]		

Microprocessor Interface Description (continued)

Register Architecture Description (continued)

Rx VT Drop Monitoring (0x6B—0x86)

Table 22. Registers 0x6B—0x86: Rx VT Drop Monitoring

Address (Hex)	Bit #	Name	Function	Reset Default (Hex)
0x6B—0x86	—	—	The bits in register 0x6B—0x86 are used to report the VT slot status.	Value is 0.
	7	VTSIZEER[1:28]	The VTSIZEER[1:28] bits report incorrect VT size bits when the value is 1. M = 1 reports an AIS or LOC condition on DS1/E1. These are current state bits with a minimum persistence of 500 µs. The indications reset if the condition is no longer true.	
	6	VTLOP[1:28]	The VTLOP[1:28] bits report VT loss of pointer when the value is 1. These are current state bits with a minimum persistence of 500 µs. The indications reset if the condition is no longer true.	
	5	VTRDI1_[1:28]	The VTRDI[1:0]_[1:28] bits report VT RDI. These are current state bits with a minimum persistence of 500 µs. The indications reset if the condition is no longer true.	
	4	VTRDI0_[1:28]		
	3	VTAIS[1:28]	Each VTAIS[1:28] bit = 1 reports that the V1 and V2 pointer bytes are all 1s for three consecutive superframes. These are current state bits with a minimum persistence of 1500 µs. The indications reset if the condition is no longer true.	
	2	VTLAB2_[1:28]	The VTLAB[2:0]_[1:28] bits report the received VT labels. These bits have a minimum persistence of 500 µs.	
	1	VTLAB1_[1:28]		
	0	VTLAB0_[1:28]		
0x87	7—0	—	Reserved.	0x00

Microprocessor Interface Description (continued)

Register Architecture Description (continued)

Table 23. Registers 0x88—0x89: Signal Override Control

Address (Hex)	Bit #	Name	Function	Reset Default (Hex)
0x88	—	—	The bits in register 0x88 are used to override the DS1_E1N signal pin. These bits represent the seven VT Groups and can be individually programmed as follows.	0x00
	7	TVTG-7	If TVTG-1 . . . 7 = 1, the signal will be DS1; otherwise, the signal will be E1.	
	6	TVTG-6		
	5	TVTG-5		
	4	TVTG-4		
	3	TVTG-3		
	2	TVTG-2		
	1	TVTG-1		
	0	TOVERRIDE	If TOVERRIDE = 1, then the type of signal in each VT Group is determined by the 7 TVTG bits.	
0x89	—	—	The bits in register 0x89 are used to override the DS1_E1N signal pin. These bits represent the seven VT Groups and can be individually programmed as follows.	0x00
	7	RVTG-7	If RVTG-1 . . . 7 = 1, the signal will be DS1; otherwise, the signal will be E1.	
	6	RVTG-6		
	5	RVTG-5		
	4	RVTG-4		
	3	RVTG-3		
	2	RVTG-2		
	1	RVTG-1		
	0	ROVERRIDE	If ROVERRIDE = 1, then the type of signal in each VT Group is determined by the 7 RVTG bits.	

Microprocessor Interface Description (continued)

Register Architecture Description (continued)

Digital Jitter Attenuator Controls (0x8A—0x8F)

Table 24. Registers 0x8A—0x8F: Digital Jitter Attenuator Controls

Address (Hex)	Bit #	Name	Function	Reset Default (Hex)
0x8A—0x8F	—	—	The bits in registers 0x8A—0x8F are used to control various aspects of the digital jitter attenuator. Two programmable terms are used to set the 2nd order loop damping factor and natural frequency of the PLL. These terms are the gain threshold, set by DJAGTHR-[23:0] in registers 0x8D—0x8F, and scale value, set by DJASCALE-[15:0] in registers 0x8B—0x8C. The PLL bandwidth can be set, using the above registers, to accommodate various system constraints.	See below.
0x8A	7—0	SCALETHR-[7:0]	Scale Threshold.	0xFF
0x8B	7—0	DJASCALE-[15:8]	Scale Value.	0x0F
0x8C	7—0	DJASCALE-[7:0]		0xCA
0x8D	7—0	DJAGTHR-[23:16]	Gain Threshold.	0x00
0x8E	7—0	DJAGTHR-[15:8]		0xFE
0x8F	7—0	DJAGTHR-[7:0]		0x50

Microprocessor Interface Description (continued)

Register Architecture Description (continued)

Table 25. Register 0x91: STS-1 LOS Detect/Test Pattern Edge Control

Address (Hex)	Bit #	Name	Function	Reset Default (Hex)
0x91	—	—	The bits in register 0x91 are used to set the number of 6.48 MHz clock periods required to declare received STS-1 loss of signal. The two least significant bits have a dual purpose and can also be used to program the edge on which the QRSS pattern generator and detector data is clocked. If this value is 0x00, then LOS is not declared; otherwise, the device looks for an all-zeros or all-ones input signal for the binary equivalent of this value in clock periods to declare LOS.	0x00
	7	LOSDET-7	These bits are used to set the number of 6.48 MHz clock periods required to declare received STS-1 loss of signal.	
	6	LOSDET-6		
	5	LOSDET-5		
	4	LOSDET-4		
	3	LOSDET-3		
	2	LOSDET-2		
	1	LOSDET-1/ TP_EDGE-1	This bit has a dual purpose. It can either contribute to the above count or can be programmed to set the edge on which the test pattern detector data is clocked in. When set to 0, the detector uses the rising edge of the selected input clock to retime the data, or uses the falling edge otherwise.	
	0	LOSDET-0/ TP_EDGE-0	This bit has a dual purpose. It can either contribute to the above count or can be programmed to set the edge on which the test pattern generator data is clocked out. When set to 0, the generator uses the rising edge of the blue signal clock to retime the data, or uses the falling edge otherwise.	
0x92—0xBE	7—0	—	Reserved.	Value is 0.

Microprocessor Interface Description (continued)

Register Architecture Description (continued)

Block Control (0xBF)

Table 26. Register 0xBF: Block Control

Address (Hex)	Bit #	Name	Function	Reset Default (Hex)
0xBF	—	—	The bits in register 0xBF control the information presented to the microprocessor from the registers 0xC0—0xFF. These last 64 bytes will display different results depending on the value programmed into this byte. A hierarchy of evaluation of these bytes occurs in the following three ways presented in the description of bits 2, 1, 0.	0x00
	7—4	—	Reserved. These bits are set to 0.	
	3	TJ1BYTE	If TJ1BYTE = 1, the transmitted J1 byte values are presented. These registers are read/write. Any values written into these registers will change the J1 byte values that are transmitted.	
	2	RJ1BYTE	If RJ1BYTE = 1, the received J1 bytes are presented (read only).	
	1	REI_CNTS	If REI_CNTS = 1, REI error information is presented (read only).	
	0	BIP_CNTS	If BIP_CNTS = 1, BIP error information is presented, regardless of the values of the other bits in this register (read only).	

Microprocessor Interface Description (continued)

Register Architecture Description (continued)

Detected BIP Errors (0xC0—0xFD)

Table 27. Registers 0xC0—0xFD: Detected BIP Errors

Note: Bits in registers 0xC0—0xFF can have one of four configurations, depending upon the setting of register 0xBF. When register 0xBF is set for BIP_CNTS = 1, the bytes in registers 0xC0—0xFD are used to count the number of BIP errors detected by the device.

Address (Hex)	Bit #	Name	Function	Reset Default (Hex)
0xC0	7—0	B1BIPCNT-[15:8]	Registers 0xC0—0xC5. The first six registers in the block, 0xC0—0xC5, are the BIP errors detected by B1, B2, and B3.	Value is 0.
0xC1	7—0	B1BIPCNT-[7:0]		
0xC2	7—0	B2BIPCNT-[15:8]		
0xC3	7—0	B2BIPCNT-[7:0]		
0xC4	7—0	B3BIPCNT-[15:8]		
0xC5	7—0	B3BIPCNT-[7:0]		
0xC6—0xFC*	7	VT[1:28]PTR+3	Registers 0xC6—0xFD. The remaining registers in the block indicate the errors seen by the BIP-2 error detectors in the individual VT1.5 slots. Since the BIP-2 errors only require 12 bits, the VT pointer increment counts are also presented in these registers. The values in all of these counters are latched by the LATCH_CNT bit in register 0x00. (See the STS-1/AU-3 Terminate section, page 16 and page 17.)	Value is 0.
	6	VT[1:28]PTR+2		
	5	VT[1:28]PTR+1		
	4	VT[1:28]PTR+0		
	3	BIP2CNT11_[1:28]		
	2	BIP2CNT10_[1:28]		
	1	BIP2CNT9_[1:28]		
	0	BIP2CNT8_[1:28]		
0xC7—0xFD†	7	BIP2CNT7_[1:28]		
	6	BIP2CNT6_[1:28]		
	5	BIP2CNT5_[1:28]		
	4	BIP2CNT4_[1:28]		
	3	BIP2CNT3_[1:28]		
	2	BIP2CNT2_[1:28]		
	1	BIP2CNT1_[1:28]		
	0	BIP2CNT0_[1:28]		

* These registers are not contiguous, i.e., every other register in this group is shown (0xC6, 0xC8, 0xCA, . . . 0xFC) per the register map, page 29 and page 30.
† These registers are not contiguous, i.e., every other register in this group is shown (0xC7, 0xC9, 0xCB, . . . 0xFD) per the register map, page 29 and page 30.

Table 28. Registers 0xFE, 0xFF: Received SONET/SDH Pointer Value

When register 0xBF is set for BIP_CNTS = 1, the bytes in registers 0xFE—0xFF are used to report the received SONET/SDH pointer value.

Address (Hex)	Bit #	Name	Function	Reset Default (Hex)
0xFE	7—0	SPTR+[7:0]	Register 0xFE. The SPTR+[7:0] bits report the SONET pointer increment value.	0x00
0xFF	7—0	SPTR–[7:0]	Register 0xFF. The SPTR–[7:0] bits report the SONET pointer decrement value.	0x00

Microprocessor Interface Description (continued)

Register Architecture Description (continued)

Detected REI Errors (0xC0—0xFD)

Table 29. Registers 0xC0—0xFD: Detected REI Errors

Note: Bits in registers 0xC0—0xFF can have one of four configurations, depending upon the setting of register 0xBF. When register 0xBF is set for BIP_CNTS = 0 **and** REI_CNTS = 1, the bytes in registers 0xC0—0xFD are used to count the number of REI errors detected by the device.

Address (Hex)	Bit #	Name	Function	Reset Default (Hex)
0xC0	7—0	—	Reserved. These bits are set to 0.	Value is 0.
0xC1	7—0			
0xC2	7—0	B2REI-[15:8]	Registers 0xC2—0xC5. The registers, 0xC2—0xC5, are the REI errors detected by B2 and B3 (see the STS-1/AU-3 Terminate section, page 16 and page 17).	
0xC3	7—0	B2REI-[7:0]		
0xC4	7—0	B3REI-[15:8]		
0xC5	7—0	B3REI-[7:0]		
0xC6— 0xFC*	7	VT[1:28]PTR–3	Registers 0xC6—0xFD. The remaining registers in the block indicate the errors seen by the REI error detectors in the individual VT1.5 slots. Since the VT REI errors only require 11 bits, the VT pointer decrement counts are also presented in these registers. The values in all of these counters is latched by the LATCH_CNT bit (bit 3) in register 0x00. (See the STS-1/AU-3 Terminate section, page 16 and page 17.) **Note:** In registers 0xC6—0xFC, bit 3 is reserved.	
	6	VT[1:28]PTR–2		
	5	VT[1:28]PTR–1		
	4	VT[1:28]PTR–0		
	3	—		
	2	VTREI10_[1:28]		
	1	VTREI9_[1:28]		
	0	VTREI8_[1:28]		
0xC7— 0xFD†	7	VTREI7_[1:28]		
	6	VTREI6_[1:28]		
	5	VTREI5_[1:28]		
	4	VTREI4_[1:28]		
	3	VTREI3_[1:28]		
	2	VTREI2_[1:28]		
	1	VTREI1_[1:28]		
	0	VTREI0_[1:28]		

* These registers are not contiguous, i.e., every other register in this group is shown (0xC6, 0xC8, 0xCA, . . . 0xFC) per the register map, page 31 and page 32.

† These registers are not contiguous, i.e., every other register in this group is shown (0xC7, 0xC9, 0xCB, . . . 0xFD) per the register map, page 31 and page 32.

Table 30. Registers 0xFE—0xFF: Reserved

When register 0xBF is set for BIP_CNTS = 0 **and** REI_CNTS = 1, the bytes in registers 0xFE—0xFF are reserved.

Address (Hex)	Bit #	Name	Function	Reset Default (Hex)
0xFE	7—0	—	Reserved. These bits are set to 0.	0x00
0xFF	7—0			0x00

Microprocessor Interface Description (continued)

Register Architecture Description (continued)

Receive J1 Path Trace Bytes (0xC0—0xFF)

Table 31. Registers 0xC0—0xFF: Receive J1 Path Trace Bytes

Note: Bits in registers 0xC0—0xFF can have one of four configurations, depending upon the setting of register 0xBF. When register 0xBF is set for BIP_CNTS = 0 **and** REI_CNTS = 0 **and** RJ1BYTE = 1, the bytes in registers 0xC0—0xFF are used to read the received 64 path trace bytes.

Address (Hex)	Bit #	Name	Function	Reset Default (Hex)
0xC0—0xFF	7	RJ1BYTE7_[64:1]	The receive J1 path trace byte RJ1BYTE[7:0]_64 corresponds to the first byte in the 64-byte sequence, while the J1 path trace byte RJ1BYTE[7:0]_1 corresponds to the last byte in the 64-byte sequence. These specified receive J1 byte values are continuously written, modulo 64, into the 0xC0—0xFF registers. If any received byte does not match the previously received byte for its location, then TRACEER bit (bit 7) in register 0x03 is set to 1.	Value is 0.
	6	RJ1BYTE6_[64:1]		
	5	RJ1BYTE5_[64:1]		
	4	RJ1BYTE4_[64:1]		
	3	RJ1BYTE3_[64:1]		
	2	RJ1BYTE2_[64:1]		
	1	RJ1BYTE1_[64:1]		
	0	RJ1BYTE0_[64:1]		

Transmit J1 Path Trace Bytes (0xC0—0xFF)

Table 32. Registers 0xC0—0xFF: Transmit J1 Path Trace Bytes

Note: Bits in registers 0xC0—0xFF can have one of four configurations, depending upon the setting of register 0xBF. When register 0xBF is set for BIP_CNTS = 0 **and** RJ1BYTE = 1 **and** TJ1BYTE = 1, the bytes in registers 0xC0—0xFF are used to provision the transmit 64 path trace bytes.

Address (Hex)	Bit #	Name	Function	Reset Default (Hex)
0xC0—0xFF	7	TJ1BYTE7_[64:1]	The transmit J1 path trace byte TJ1BYTE[7:0]_64 corresponds to the first byte in the 64-byte sequence, while the J1 path trace byte TJ1BYTE[7:0]_1 corresponds to the last byte in the 64-byte sequence. These registers can be written by the microprocessor.	Value is 0.
	6	TJ1BYTE6_[64:1]		
	5	TJ1BYTE5_[64:1]		
	4	TJ1BYTE4_[64:1]		
	3	TJ1BYTE3_[64:1]		
	2	TJ1BYTE2_[64:1]		
	1	TJ1BYTE1_[64:1]		
	0	TJ1BYTE0_[64:1]		

Microprocessor Interface Description (continued)

I/O Timing

The I/O timing specifications for the microprocessor interface are given in Table 33. The microprocessor interface pins use CMOS I/O levels (see pages 20—22 for pin listings). All outputs, except the address/data bus AD[7:0], are rated for a capacitive load of 50 pF. The AD[7:0] outputs are rated for a 100 pF load. The minimum read and write cycle time is 200 ns for all device configurations.

Table 33. Microprocessor Interface I/O Timing Specifications

Symbol	Configuration	Parameter	Setup (ns) (Min)	Hold (ns) (Min)	Delay (ns) (Max)
t1	Modes 1 & 2	Address Valid to $\overline{AS}$ Asserted (Read, Write)	5	—	—
t2		$\overline{AS}$ Asserted to Address Invalid (Read, Write)	—	10	—
t3		$\overline{AS}$ Asserted to $\overline{DS}$ Asserted	0	—	—
t4		R/$\overline{W}$ High (Read) to $\overline{DS}$ Asserted	25	—	—
t5		$\overline{DS}$ Asserted (Read, Write) to $\overline{DTACK}$ Asserted	—	—	20
t6		$\overline{DTACK}$ Asserted to Data Valid (Read)	—	—	24
t7		$\overline{DS}$ Asserted (Read) to Data Valid	—	—	44
t8		$\overline{DS}$ Negated (Read, Write) to $\overline{AS}$ Negated	—	—	—
t9		$\overline{DS}$ Negated (Read) to Data Invalid	—	—	15
t10		$\overline{DS}$ Negated (Read) to $\overline{DTACK}$ Negated	—	—	15
t11		$\overline{AS}$ (Read, Write) Asserted Width	—	75	—
t12		$\overline{DS}$ (Read) Asserted Width	—	35	—
t13		$\overline{AS}$ Asserted to R/$\overline{W}$ Low (Write)	7	—	—
t14		R/$\overline{W}$ Low (Write) to $\overline{DS}$ Asserted	20	—	—
t15		Data Valid to $\overline{DS}$ Asserted (Write)	7.5	—	—
t16		$\overline{DS}$ Negated to $\overline{DTACK}$ Negated (Write)	—	—	20
t17		$\overline{DS}$ Negated to Data Invalid (Write)	—	7.5	—
t18		$\overline{DS}$ (Write) Asserted Width	—	35	—
t19	Modes 3 & 4	Address Valid to ALE Asserted Low (Read, Write)	15	—	—
t20		ALE Asserted Low (Read, Write) to Address Invalid	—	10	—
t21		ALE Asserted Low to $\overline{RD}$ Asserted (Read)	30	—	—
t22		$\overline{RD}$ Asserted (Read) to Data Valid	—	—	90
t23		$\overline{RD}$ Asserted (Read) to RDY Asserted	—	—	75
t24		$\overline{RD}$ Negated to Data Invalid (Read)	—	—	25
t25		$\overline{RD}$ Negated to RDY Negated (Read)	—	—	25
t26		ALE Asserted Low to $\overline{WR}$ Asserted (Write)	35	—	—
t27		$\overline{CS}$ Asserted to RDY Asserted Low	—	—	16
t28		Data Valid to $\overline{WR}$ Asserted (Write)	25	—	—
t29		$\overline{WR}$ Asserted (Write) to RDY Asserted	—	—	73
t30		$\overline{WR}$ Negated to RDY Negated (Write)	—	—	22
t31		$\overline{WR}$ Negated to Data Invalid	—	25	—
t32		ALE Asserted (Read, Write) Width	—	150	—
t33		$\overline{RD}$ Asserted (Read) Width	—	100	—
t34		$\overline{WR}$ Asserted (Write) Width	—	100	—

The read and write timing diagrams for all four microprocessor interface modes are shown in Figures 3—10.

Microprocessor Interface Description (continued)

I/O Timing (continued)
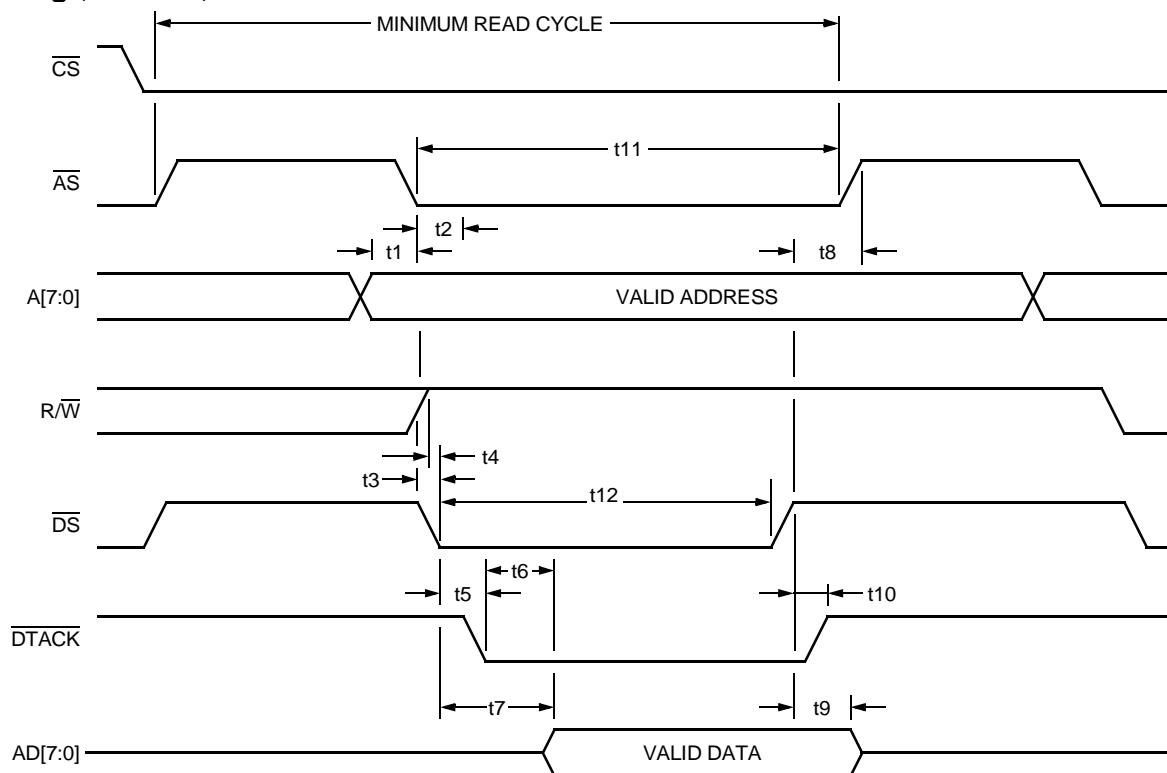
**Figure 3. Mode 1—Read Cycle Timing (MPMODE = 0, MPMUX = 0)**

5-3685(F).br.4
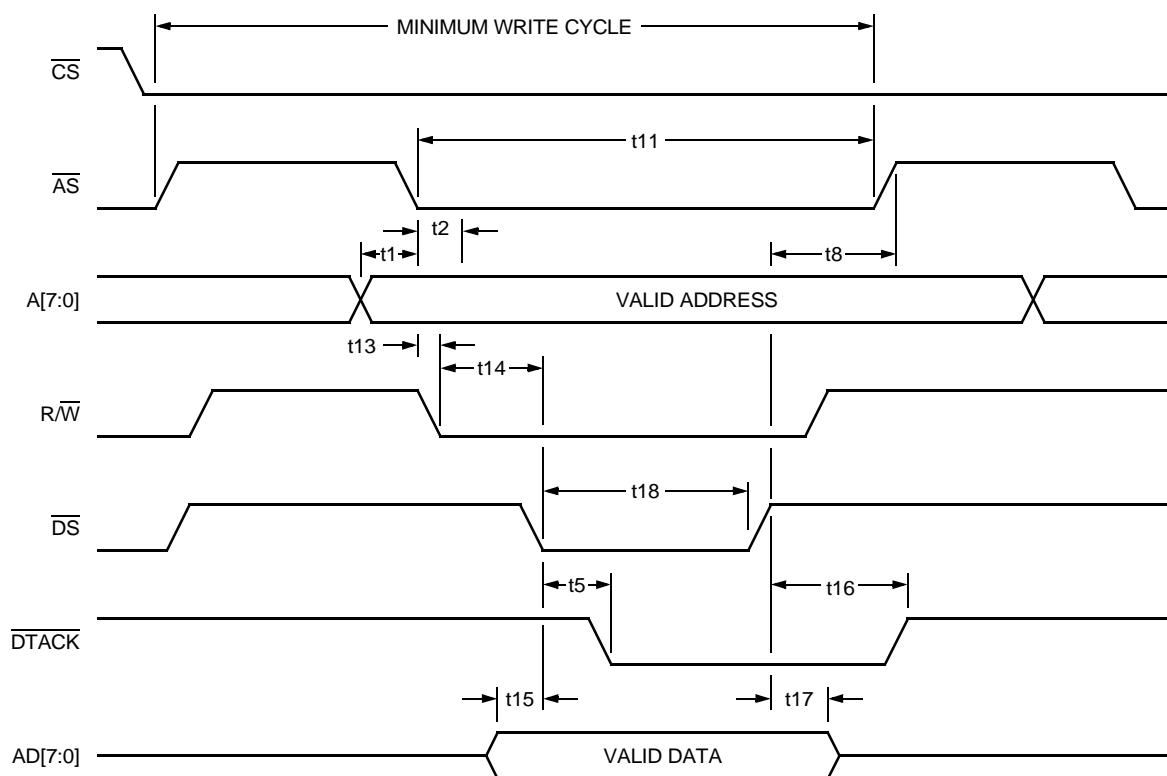
Figure 4. Mode 1—Write Cycle Timing (MPMODE = 0, MPMUX = 0)

5-3686(F).br.5

Microprocessor Interface Description (continued)

I/O Timing (continued)
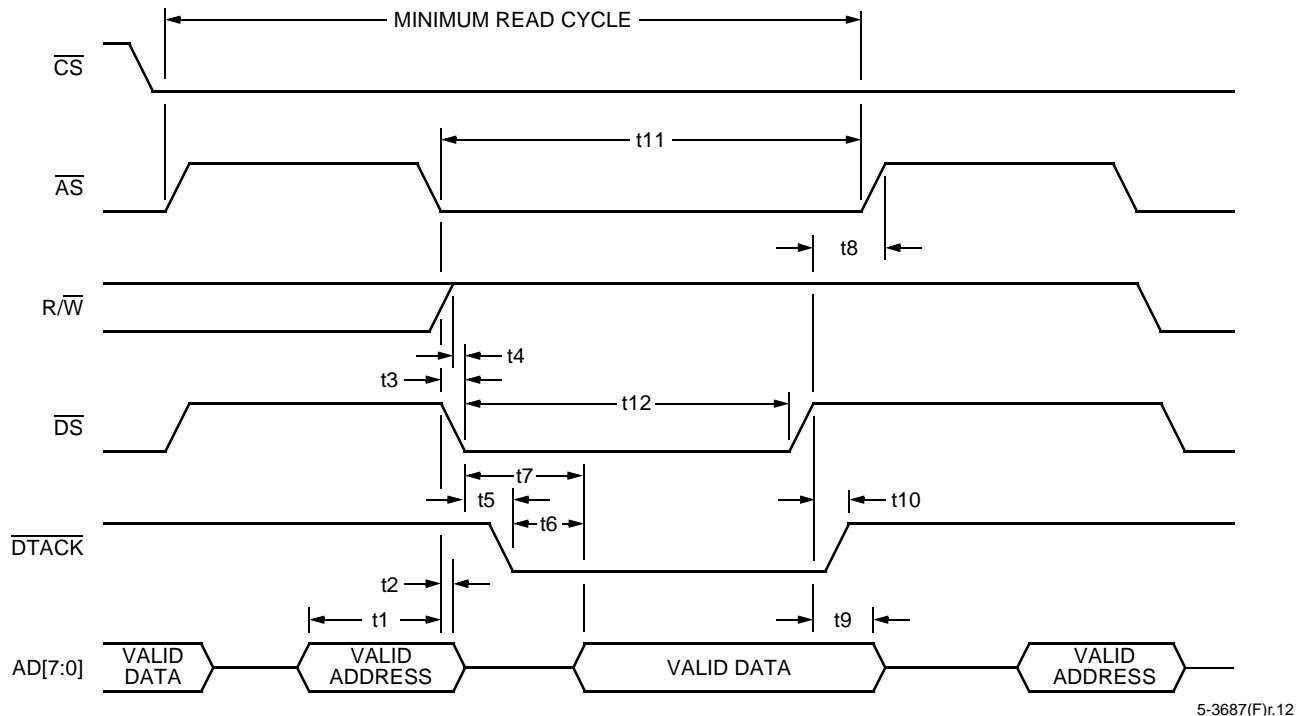
Figure 5. Mode 2—Read Cycle Timing (MPMODE = 0, MPMUX = 1)
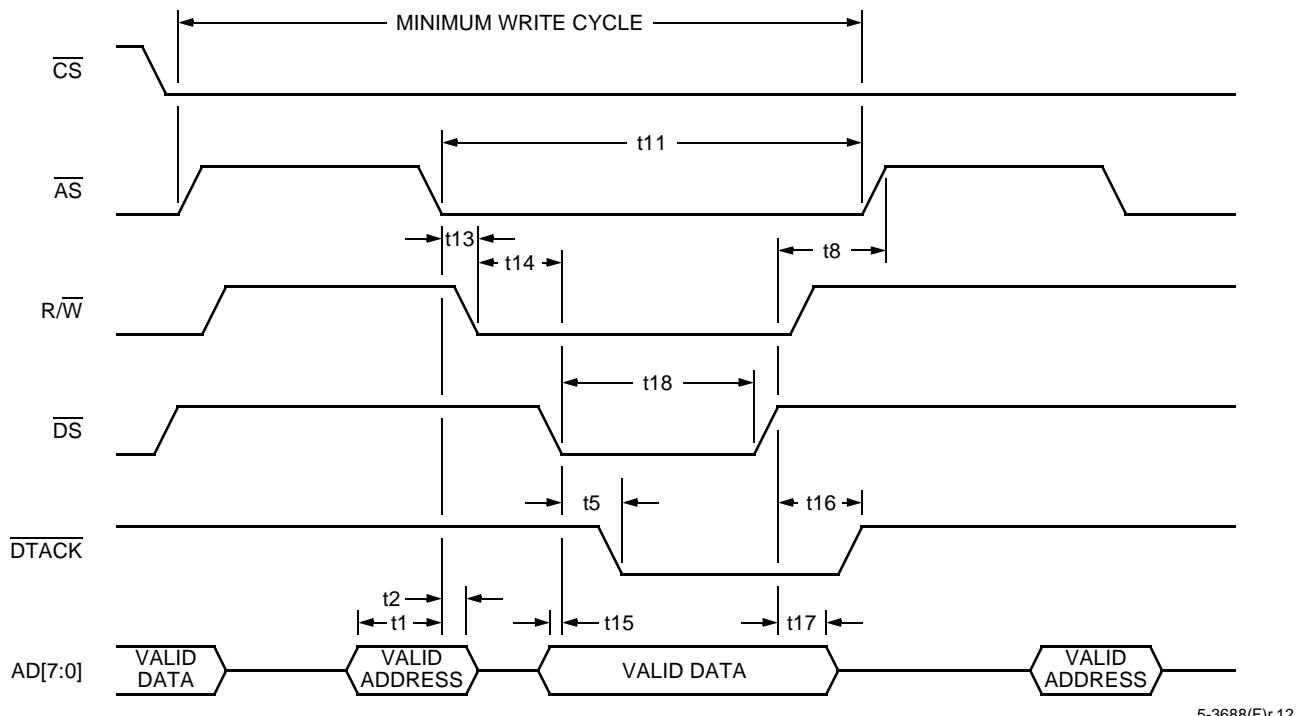
Figure 6. Mode 2—Write Cycle Timing (MPMODE = 0, MPMUX = 1)

Microprocessor Interface Description (continued)

I/O Timing (continued)
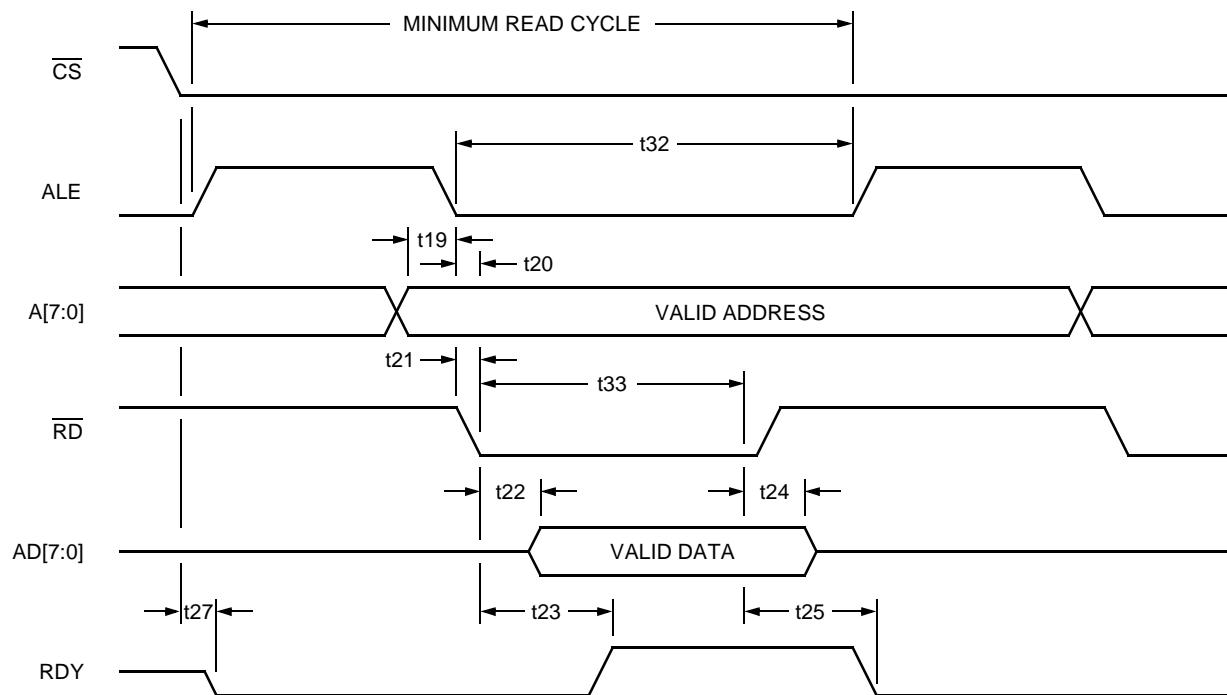
5-3689(F).br.4

Figure 7. Mode 3—Read Cycle Timing (MPMODE = 1, MPMUX = 0)
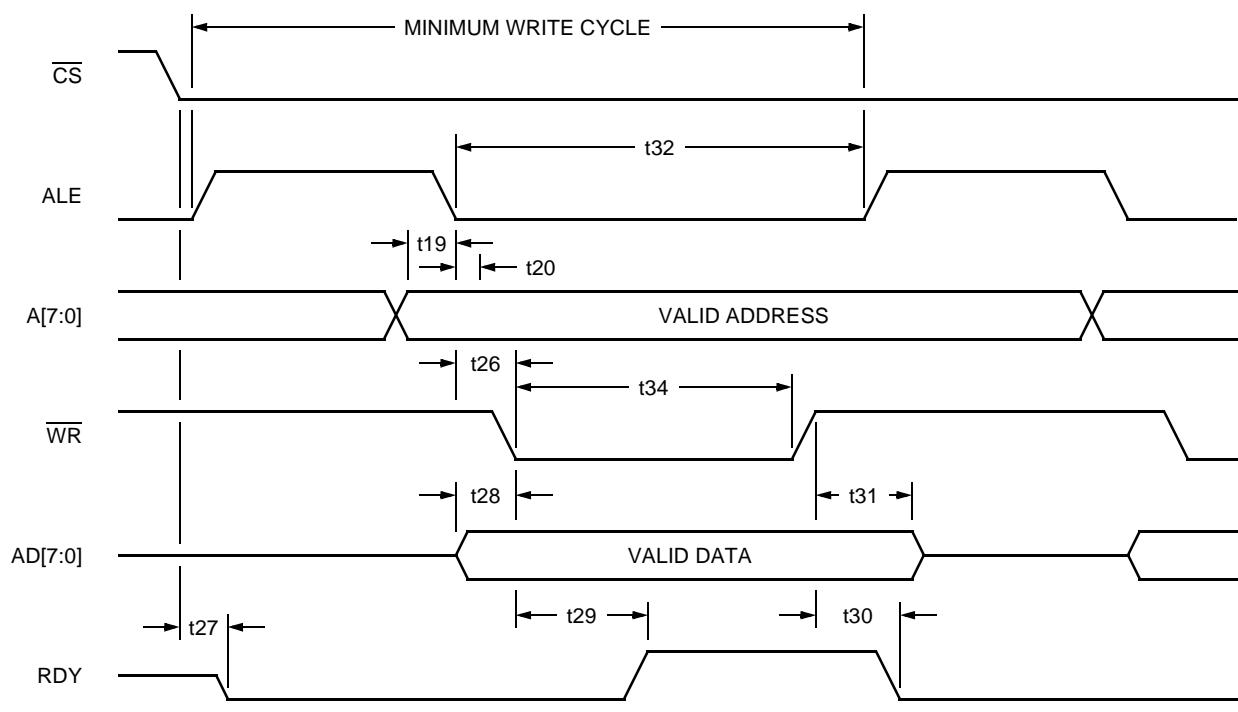
5-3690(F).br.3

Figure 8. Mode 3—Write Cycle Timing (MPMODE = 1, MPMUX = 0)

Microprocessor Interface Description (continued)

I/O Timing (continued)

5-3691(F)r.12
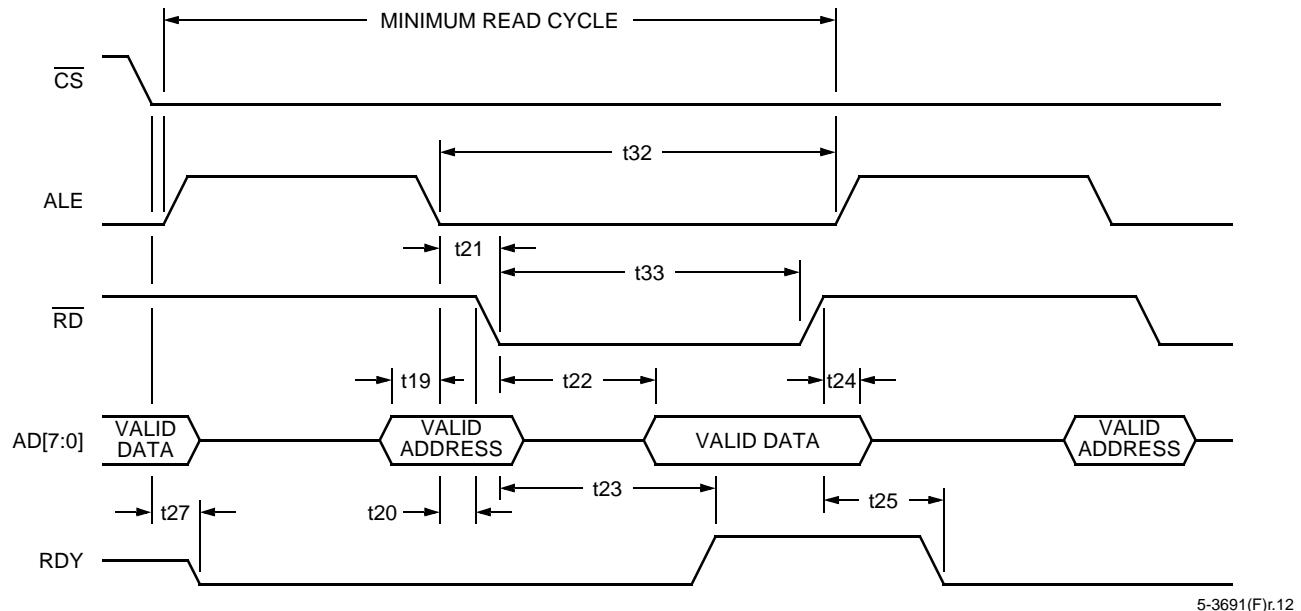
Figure 9. Mode 4—Read Cycle Timing (MPMODE = 1, MPMUX = 1)

5-3692(F)r.13
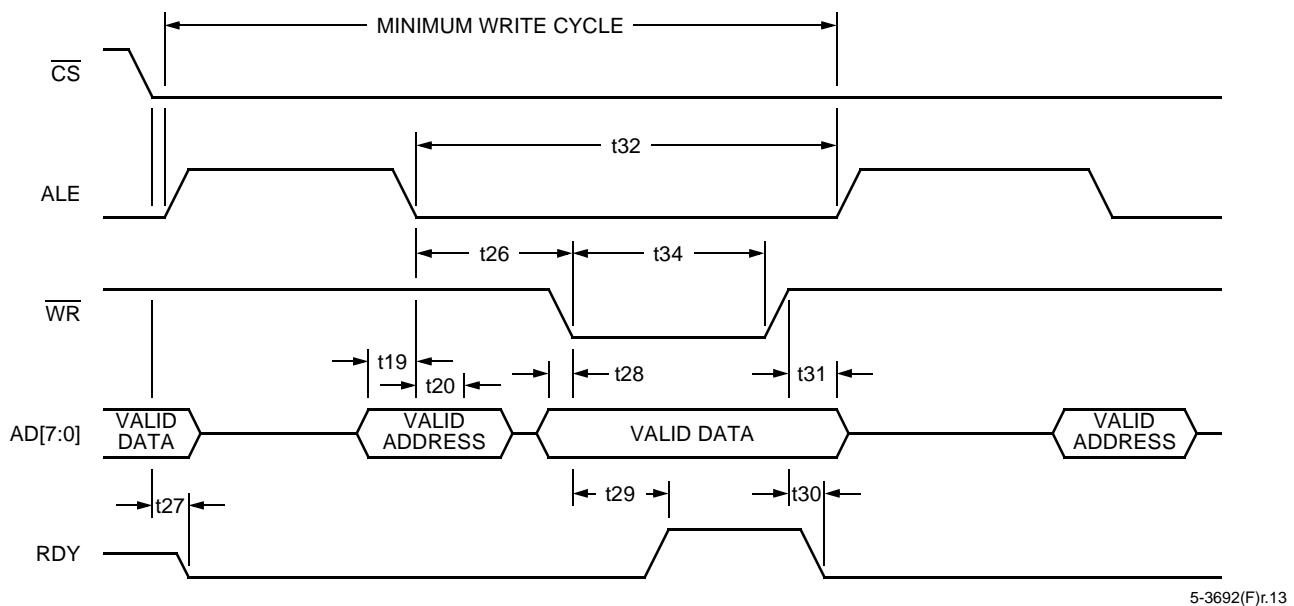
Figure 10. Mode 4—Write Cycle Timing (MPMODE = 1, MPMUX = 1)

Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause permanent or latent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of this device specification. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.

Table 34. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Power Supply (dc Voltage)	V_{DD}	−0.5	4.6	V
Input Voltage	V_I	−0.3	5.5	V
Output Voltage	V_O	—	3.63	V
Storage Temperature	T_{stg}	−65	125	°C
Ambient Operating Temperature Range	T_A	−40	85	°C

Handling Precautions

Although protection circuitry has been designed into this device, proper precautions should be taken to avoid exposure to electrostatic discharge (ESD) during handling and mounting. Lucent employs a human-body model (HBM) and charged-device model (CDM) for ESD-susceptibility testing and protection design evaluation. ESD voltage thresholds are dependent on the circuit parameters used in the defined model. No industry-wide standard has been adopted for the CDM. However, a standard HBM (resistance = 1500 Ω, capacitance = 100 pF) is widely used and, therefore, can be used for comparison purposes. The HBM ESD threshold presented here was obtained by using these circuit parameters.

Table 35. ESD Threshold Voltage

Model	Voltage (volts)
HBM	2000
CDM (all pins except corner pins)	500
CDM (all corner pins)	1000

Operating Conditions

Table 36. Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Power Supply (dc Voltage)	V_{DD}	3.14	3.3	3.46	V
Ground	V_{SS}	—	0.0	—	V
Input Voltage, High	V_{IH}	—	$V_{DD} - 1.0$	5.25	V
Input Voltage, Low	V_{IL}	—	V_{SS}	1.0	V
Ambient Temperature	T_A	−40	—	85	°C
Power Dissipation, DS1 (T_A = 23 °C, V_{DD} = 3.3 V):	P_D				
Full Loopback		—	380	—	mW
Broadcast		—	380	—	mW
Standby		—	360	—	mW
Power Dissipation, E1 (T_A = 23 °C, V_{DD} = 3.3 V):					
Full Loopback		—	450	—	mW
Broadcast		—	450	—	mW
Standby		—	430	—	mW

Electrical Characteristics

Table 37. Logic Interface Characteristics

An internal 100 kΩ pull-up is provided on the $\overline{ICT}$, $\overline{RESET}$, $\overline{CS}$, TCK, TDI, TMS, $\overline{TRST}$, RSTS1DATA[7:0], RSTS1PAR, E1BLUECLK, RCLK[28:1], and RDATA[28:1] pins. This requires these input pins to sink no more than 20 µA. All buffers use CMOS levels.

Parameter	Symbol	Test Conditions	Min	Max	Unit
Input Voltage:		—			
Low	V_{IL}		GND	1.0	V
High	V_{IH}		$V_{DD} - 1.0$	V_{DD}	V
Input Leakage	I_L	—	—	1.0	µA
Output Voltage:					
Low	V_{OL}	−5.0 mA	GND	0.5	V
High	V_{OH}	5.0 mA	$V_{DD} - 1.0$	V_{DD}	V
Input Capacitance	C_I	—	—	3.0	pF
Load Capacitance*	C_L	—	—	25	pF

* 100 pF allowed for AD[7:0] (pins 48 to 50 and 55 to 59).

Timing Characteristics

Operational Timing

The operational timing parameters can be grouped separately for clocks, inputs, and outputs. Table 38 lists the transmit and receive input clock specifications for this device. (For definitions of the signal names, see the pin descriptions in Table 1, pages 7—9.)

Table 38. Input Clock Specifications

Signal Name	Parameter	Min	Max	Unit
Input Clock Signals				
TSTS1CLKIN	Frequency	51.839	51.841	MHz
	Clock Pulse High Time	40	60	%
	Peak-to-Peak Jitter	—	1	%
	Frequency	19.439	19.441	MHz
	Clock Pulse High Time	40	60	%
	Peak-to-Peak Jitter	—	1	%
	Frequency	6.479	6.481	MHz
	Clock Pulse High Time	40	60	%
	Peak-to-Peak Jitter	—	1	%
RCLK[1:28] (DS1 Mode)	Frequency	1.5437	1.5443	MHz
	Clock Pulse High Time	40	60	%
	Peak-to-Peak Jitter	—	1	%
RCLK[1:21] (E1 Mode)	Frequency	2.0484	2.0476	MHz
	Clock Pulse High Time	40	60	%
	Peak-to-Peak Jitter	—	1	%
RSTS1CLK	Frequency	51.839	51.841	MHz
	Clock Pulse High Time	40	60	%
	Peak-to-Peak Jitter	—	1	%
JTAG Signal				
TCK	Frequency	0.5	12	MHz
	Clock Pulse High Time	40	60	%
	Peak-to-Peak Jitter	—	1	%
	Rise/Fall Time	—	15	ns

Timing Characteristics (continued)

Operational Timing (continued)

Table 39 lists the setup time (t_{SU}) and hold time (t_H) specifications for the receive input and JTAG signals. The digital system interface timing is shown in Figure 11.

Table 39. Input Timing Specifications

Input Name	Reference CLK*	Setup Time (t_{SU})		Hold Time (t_H)		Unit
		Min	Max	Min	Max	
Receive Signals						
TSTS1SYNC	TSTS1CLKIN	5	—	2	—	ns
RDATA[1:28]	RCLK[1:28] ↑↓	50	—	40	—	ns
RSTS1DATA[7:0]	RSTS1CLK ↑↓	15	—	2	—	ns
RSTS1PAR	RSTS1CLK ↑↓	15	—	2	—	ns
RSTS1SERIAL	RSTS1CLK ↑↓	5	—	2	—	ns
JTAG Signal						
TDI	TCK ↑	50	—	50	—	ns

* These clock edges are programmable through the microprocessor interface.

Notes:
↑ represents a low-to-high transition.

↓ represents a high-to-low transition.
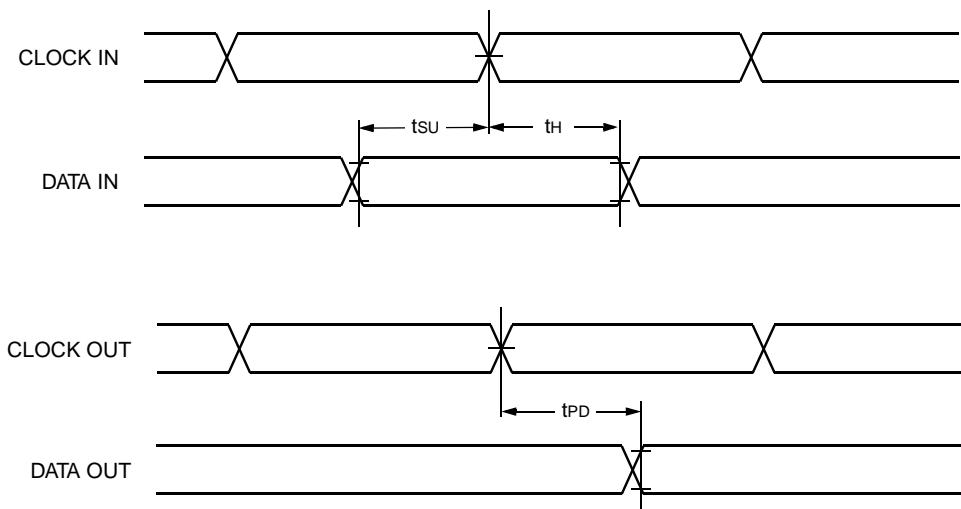
5-5342(F)r.5

Figure 11. Interface Data Timing

Timing Characteristics (continued)

Operational Timing (continued)

The output clock specifications are shown in Table 40.

Table 40. Output Clock Specifications

Signal Name	Frequency	Test Conditions	Rise Time		Fall Time		Unit
			t_R		t_F		
			Min	Max	Min	Max	
TCLK[1:28] (DS1 Mode)	1.544 MHz ± 5%	C_L = 50 pF	—	30	—	30	ns
TCLK[1:28] (E1 Mode)	2.048 MHz ± 5%	C_L = 50 pF	—	30	—	30	ns
TSTS1CLKOUT*	51.84 MHz ± 5%	C_L = 15 pF	—	3	—	3	ns
	19.44 MHz ± 5%	C_L = 15 pF	—	3	—	3	ns
	6.48 MHz ± 5%	C_L = 15 pF	—	3	—	3	ns

* The duty-cycle distortion added to the TSTS1CLKOUT signal is ≤2% worst case when measured from 1.5 V in to 1.5 V out with a 2 ns rise time input.

Table 41 lists the propagation delay (t_{PD}) specifications for the output signals. The digital system interface timing is shown in Figure 11, page 68.

Table 41. Output Timing Specifications

Output Name	Reference CLK	Test Conditions	Propagation Delay *		Unit
			t_{PD}		
			Min	Max	
Transmit Signals					
TDATA[28:1]	TCLK[1:28] ↑↓	C_L = 25 pF	40	190	ns
TSTS1DATA[7:0]	TSTS1CLKIN ↑	C_L = 15 pF	2	12	ns
TSTS1PAR	TSTS1CLKIN ↑	C_L = 15 pF	2	12	ns
TSTS1DATA7	TSTS1CLKIN ↑	C_L = 15 pF	0	3.5	ns
JTAG Signal					
TDO	TCK ↓	C_L = 50 pF	1.5	17	ns

* Propagation delay skew, t_{PLH}—t_{PHL}, is ±200 ps.

Notes:
↑ represents a low-to-high transition.

↓ represents a high-to-low transition.

Timing Characteristics (continued)

Transmit Sync Timing

In all transmit modes, the first bit/byte of the J0, J1, and V1 bytes are coincident with the sync pulse. The second and third pulses in this composite signal are only needed to force V1 superframe alignment. If there are three sync pulses as shown below, then V1 **will** be forced. The serial mode transmit sync timing is shown below in Figure 12.

TSTS1CLK

TSTS1SYNC

TSTS1DATA — J0-7 | J0-6 | J0-5 | J0-4 | J0-3 | J0-2 | J0-1 | J0-0 | J1-7 | J1-6 | J1-5 | J1-4 | J1-3 | J1-2 | J1-1 | J1-0 | V1-7 | V1-6 | V1-5 | V1-4 | V1-3 | V1-2 | V1-1 | V1-0

5-6347(F)r.1
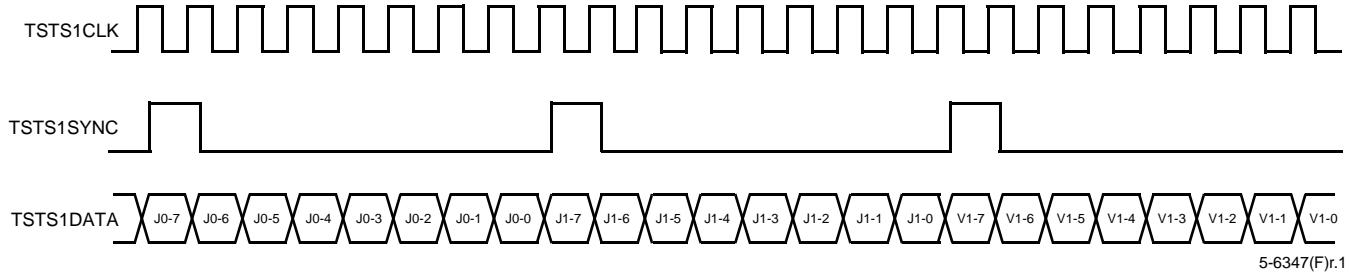
Note: The - symbol followed by a number represents the bit number in the byte.

Figure 12. Serial Mode Transmit Sync Timing

The bus mode transmit sync timing is shown below in Figure 13.

TSTS1CLK

TSTS1SYNC

TSTS1DATA — J0#1 | J0#2 | J0#3 | J1#1 | J1#2 | J1#3 | V1#1 | V1#2 | V1#3

5-6347(F).a
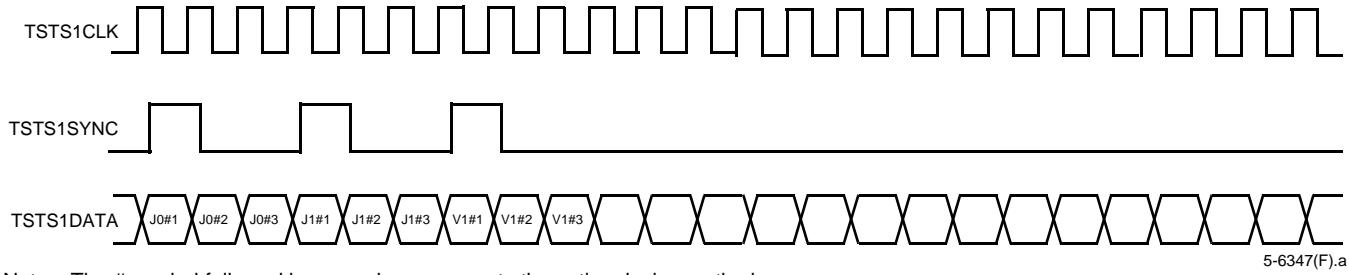
Note: The # symbol followed by a number represents the active device on the bus.

Figure 13. Bus Mode Transmit Sync Timing

Timing Characteristics (continued)

Transmit Sync Timing (continued)

The nonbus parallel mode transmit sync timing is shown below in Figure 14.

TSTS1CLK

TSTS1SYNC

TSTS1DATA   J0   J1   V1

5-6347(F).b
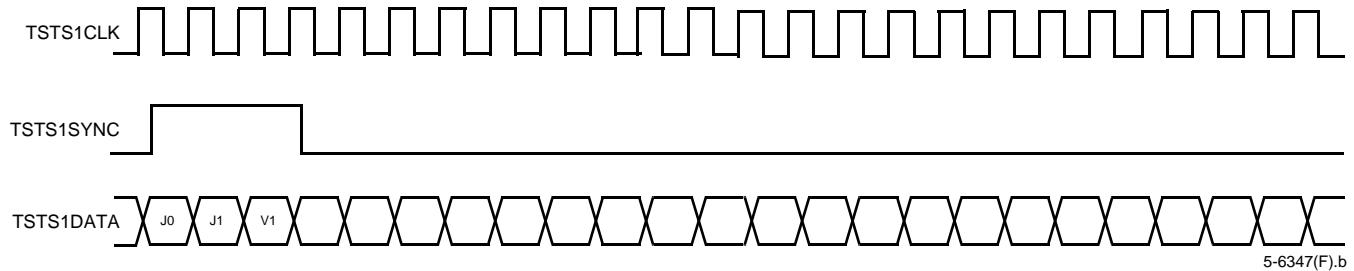
Figure 14. Nonbus Parallel Mode Transmit Sync Timing

Receive Sync Timing

The only receive mode that requires a sync pulse is the bus mode. The sync pulse is required to align the device to time slot #1. The bus parallel mode receive sync timing is shown below in Figure 15.

RSTS1CLK

RSTS1SERIAL

RSTS1DATA   J0#1   J0#2   J0#3   J1#1   J1#2   J1#3   V1#1   V1#2   V1#3

5-6347(F).cr.1
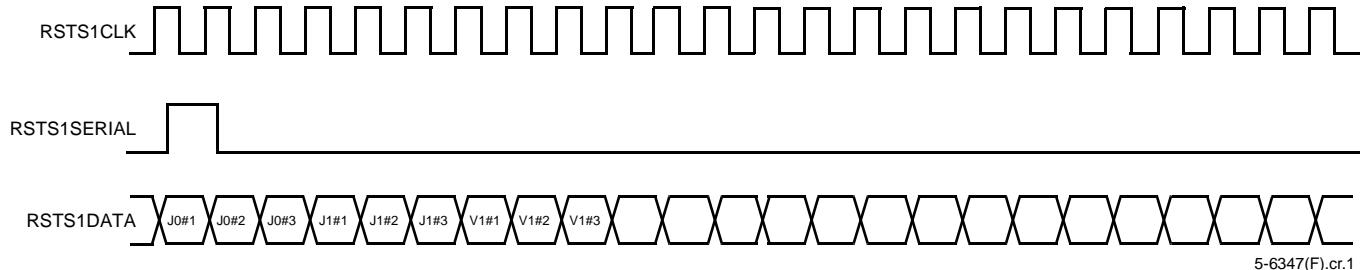
Note: The # symbol followed by a number represents the active device on the bus.

Figure 15. Bus Parallel Mode Receive Sync Timing

Typical Uses

Path Termination Multiplex

Using the device without internal loopbacks results in an SDH/SONET path terminating multiplex, as shown in Figure 16.

Note: n represents 28 or 21 for DS1 or E1, respectively.

5-4876(F)r.9
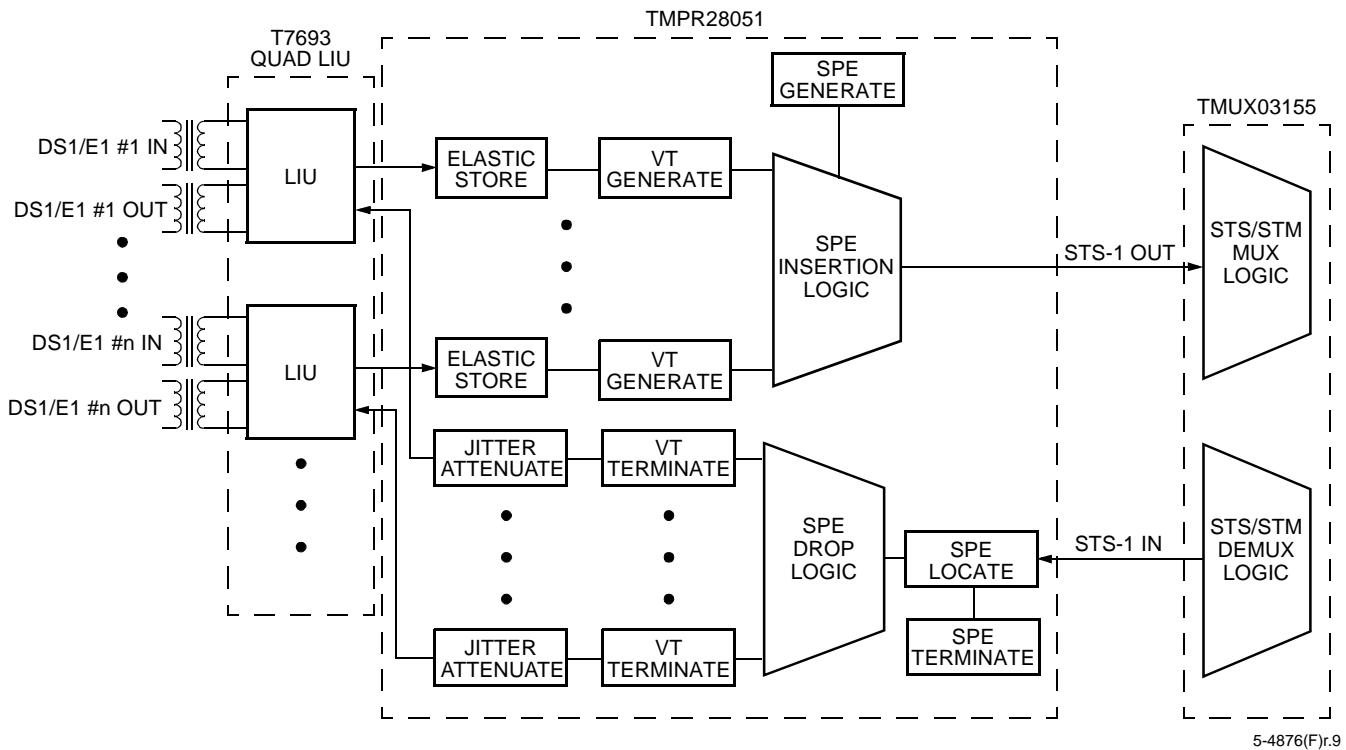
Figure 16. SDH/SONET Path Termination Multiplex Application

Digital Cross Connect

Using the device with STS-1 internal loopbacks results in a digital cross connect, as shown in Figure 17.

Note: n represents 28 or 21 for DS1 or E1, respectively.

5-4878(F)r.8
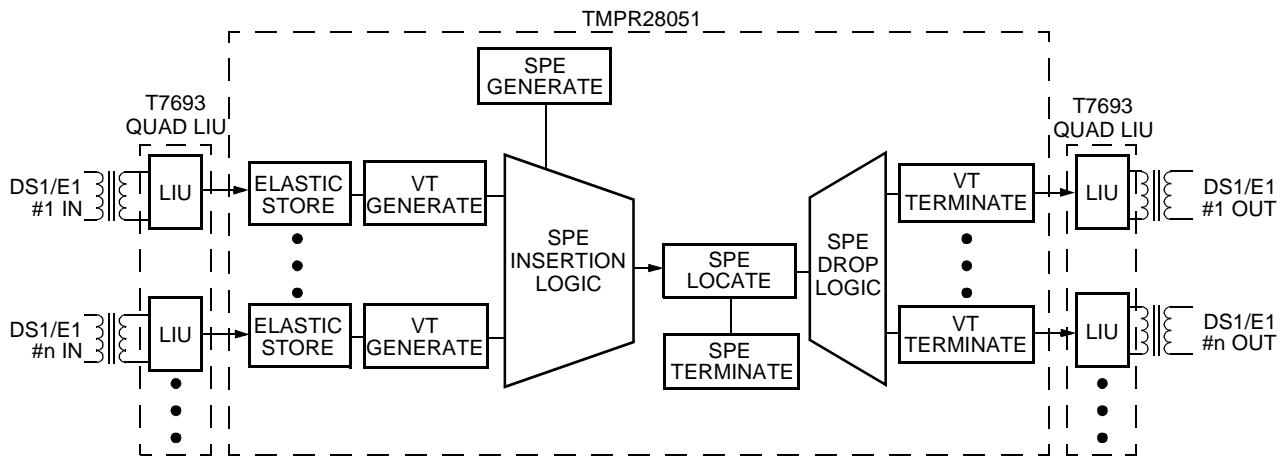
Figure 17. Digital Cross Connect Application

Typical Uses (continued)

Test Pattern Use—Complete System

The internal test pattern generator can be used in conjunction with DS1 or E1 LIU devices that have built-in loop-backs (such as the Lucent T7698FL3/T7693) to do a complete system test, as shown in Figure 18.

5-4879(F)r.7
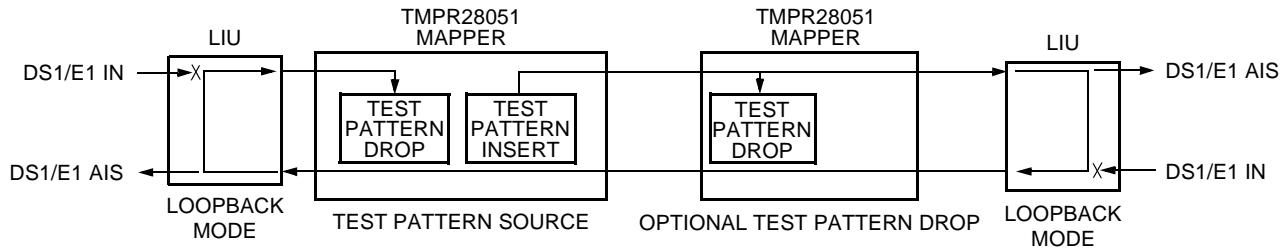
Figure 18. Test Pattern Usage for Complete System

Test Pattern Use—End to End

The internal test pattern generator can be used to test connectivity within a link by setting up a test pattern insertion at one end and a drop at the other, as shown in Figure 19.

5-4880(F)r.7
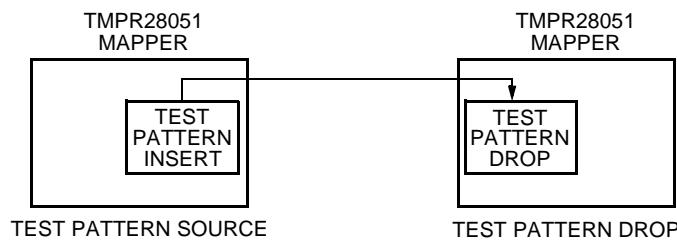
Figure 19. Test Pattern Usage for End-to-End Operation

Outline Diagram

208-Pin SQFP

Dimensions are in millimeters.

30.60 ± 0.20

28.00 ± 0.20

PIN #1 IDENTIFIER ZONE

208

157

1

156

28.00
± 0.20

30.60
± 0.20

52

105

53

104

DETAIL A

DETAIL B

3.40 ± 0.20

4.10 MAX

SEATING PLANE

0.08

0.50 TYP

0.25 MIN

1.30 REF

0.25

GAGE PLANE

SEATING PLANE

0.50/0.75

0.090/0.200

0.17/0.27

0.10 Ⓜ

DETAIL A

DETAIL B

5-2196(F)r.14
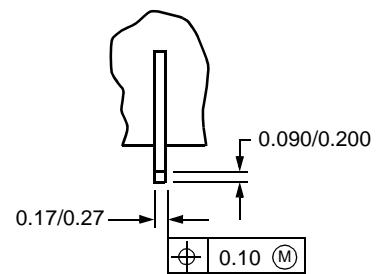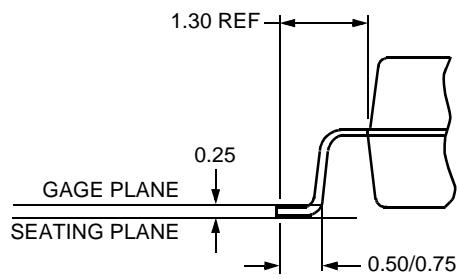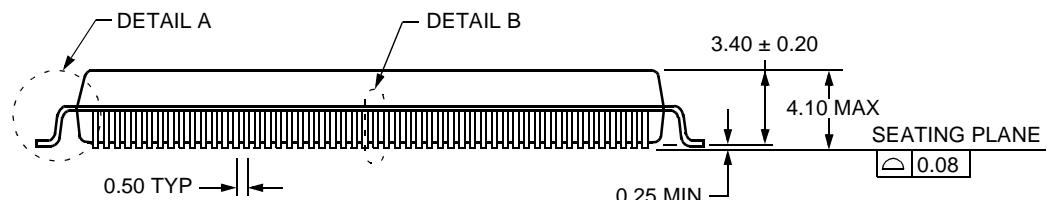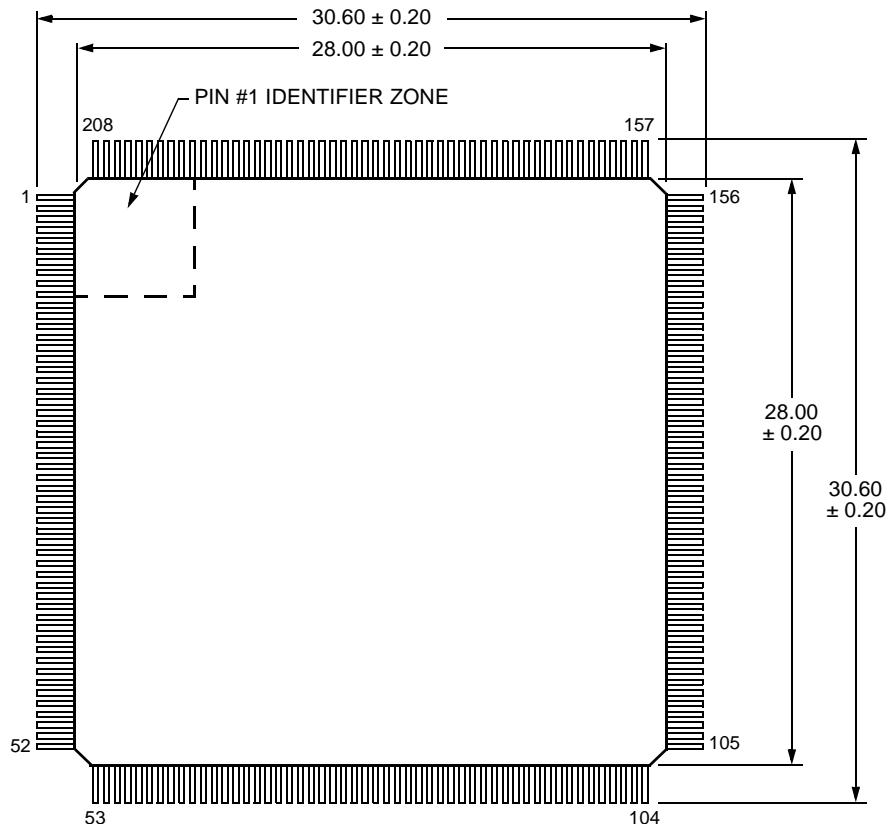
Ordering Information

Device Code	Package	Temperature	Comcode (Ordering Number)
TMPR28051-3-SL5	208-Pin SQFP	–40 °C to +85 °C	108421678

DS99-068SONT Replaces DS98-100TIC to Incorporate the Following Updates

1. Page 1, added bulleted items concerning 3.3 V operation, and alarm and control standards.

2. Page 5, Description (continued) section, replaced the Lucent T7690/T7693 Quad Line Transceiver interfacing device with the Lucent T7698FL3/T7693 Quad Line Transceiver.

3. Page 5, Figure 1, Block Diagram, clarified block flow.

4. Page 6, changed pin 184 and all corresponding references to TCK.

5. Page 7, clarified Pin 102.

6. Page 10, organized Nomenclature Assumptions section from the text at the beginning of the Description section.

7. Page 10—page 19, clarified block descriptions.

8. Page 14, 2nd paragraph, corrected the explanation of the reduced H4 coding sequence format from "alternate between" to "take on the following values."

9. Page 23—page 36, updated register map.

10. Page 37—page 59, updated register description text and placed text in tables.

11. Page 42, Table , Registers 0x00—0x16: Device-Level Control, Alarm, and Mask Bits, corrected the test pattern sequence for register XMT_PAT-0, bits 01 and 11 combinations.

12. Page 49, Table 18, Registers 0x33—0x4E: VT Drop Selection, corrected VTxDROP, bits 4 through 0, to VT_DROP[4:0]_[1:28].

13. Page 54, Table 24, Registers 0x8A—0x8F: Digital Jitter Attenuator Controls, added the register default values.

14. Page 65, Table 34, Absolute Maximum Ratings, updated table, including input and output voltages.

15. Page 65, Table 35, ESD Threshold Voltage, added parameters and values.

16. Page 66, Table 36, Recommended Operating Conditions, updated to list 3.3 V power dissipation for DS1 and E1.

17. Page 67, Table 38, Input Clock Specifications, added to the document.

18. Page 69, Table 40, Output Clock Specifications, added to the document.

19. Page 70, Transmit Sync Timing section, expanded and corrected.

20. Page 71, Figure 15, Bus Parallel Mode Receive Sync Timing, corrected pin name.

21. Page 75, updated device code.

22. *TMPR28051 STS-1/AU-3 (STM-0) Mapper Device Advisory for Version 2 of the Device*, *TMPR28051 STS-1/AU-3 (STM-0) Mapper Device Advisory for Version 3 of the Device*, *TMPR28051 STS-1/AU-3 (STM-0) Mapper Device Advisory for Version 4 of the Device*, *TMPR28051 STS-1/AU-3 (STM-0)* Data Addendum, included all printed advisories and an addendum through version 4, each published in April 1999, (AY99-026SONT, AY99-027SONT, AY99-028SONT, DA99-009SONT). An advisory was not issued for version 1 of the device.

microelectronics group

August 1999

Lucent Technologies