TOSHIBA RISC PROCESSOR

TMPR4925XB

(64-bit RISC MICROPROCESSOR)

1. GENERAL DESCRIPTION

The TMPR4925XB, to be referred as TX4925 MIPS RISC micro-controller is a highly integrated ASSP solution based on Toshiba's TX49/H2 processor core, a 64-bit MIPS I,II,III ISA Instruction Set Architecture (ISA) compatible with additional instructions. The TX4925 is a highly integrated device with integrated peripherals such as SDRAM memory controller, NAND Flash memory controller, PCI controller, AC-Link controller, PIO, SIO, SPI, CHI, PCMCIA I/F and Timer. This class of product is targeted for applications that require a high performance and cost-effective solution such as networking, digital consumer and Internet appliance.

2. FEATURES

- TX49/H2 core with an integrated IEEE 754-compliant FPU for single- and double-precision operations
- 4-channel SDRAM Controller (32bit/80MHz) and support SyncFlash® memory
- NAND Flash memory Controller
- 6-channel External Bus Controller
- 32-bit PCI Controller (33 MHz)
- 4-channel Direct Memory Access (DMA) Controller
- 2-channel Serial I/O Port
- Parallel I/O Port (up to 32-bit)
- AC-Link Controller (AC97 Interface)
- PCMCIA Interface (2-slot)
- SPI (Serial Peripheral Interface)
- CHI (high-speed serial Concentration Highway Interface)
- Interrupt Controller
- 3-channel Timer/Counter and 44-bit up-counter RTC
- Low power dissipation

  The TX4925 operates with the 1.5V core and the 3.3V I/O, while supporting a low-power (Halt) mode.
- CPU maximum operating frequency: 200 MHz
- IEEE1149.1 (JTAG) support: Debug Support Unit (Enhanced JTAG)
- 256-pin PBGA package

2.1 Internal Block Diagram

Figure 1 shows the TX4925 internal block diagram.

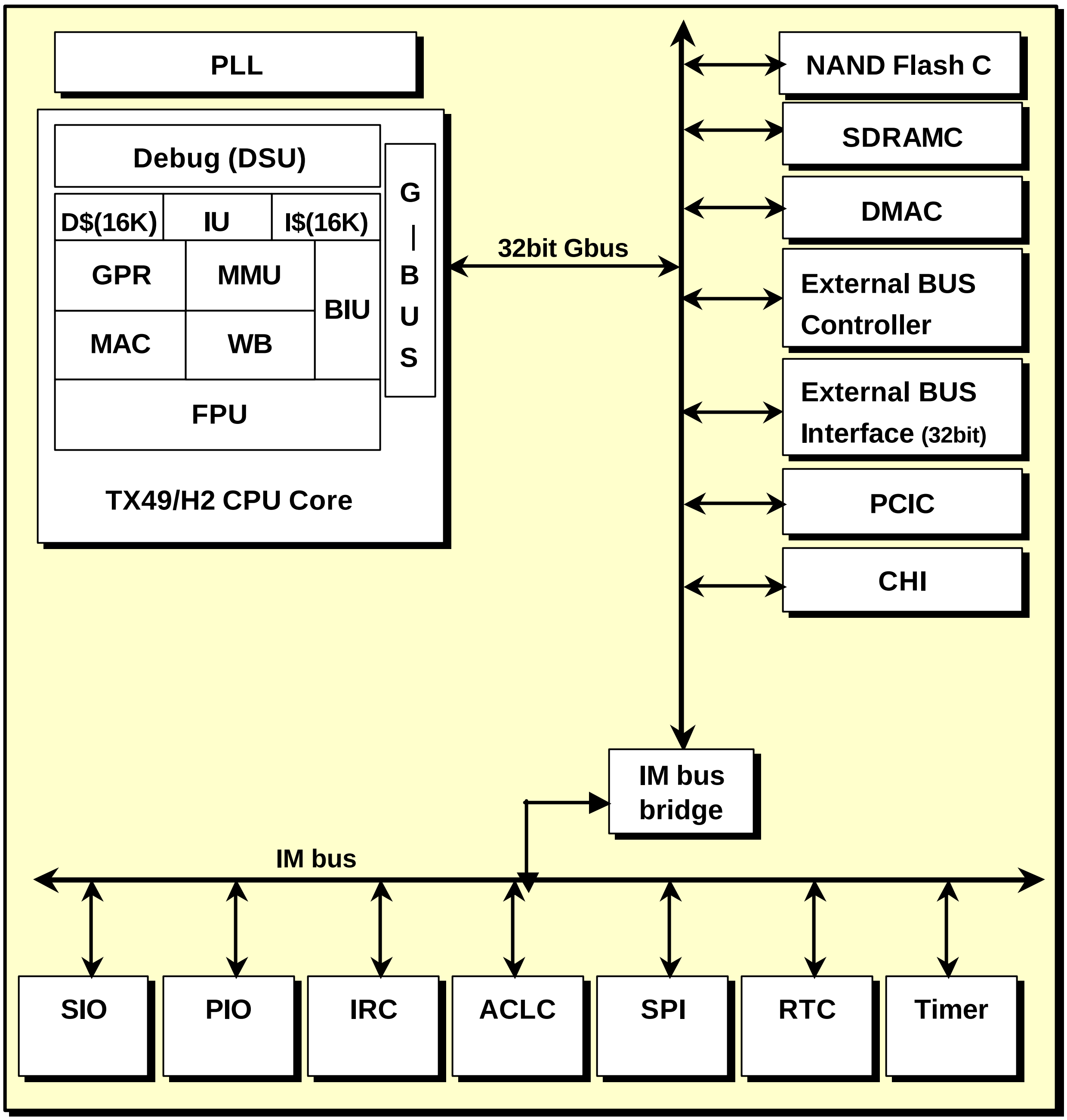

Figure 2.1 TX4925 Internal Block Diagram

2.2 System Block Diagram

Figure 2.2 shows the system block diagram with TX4925.

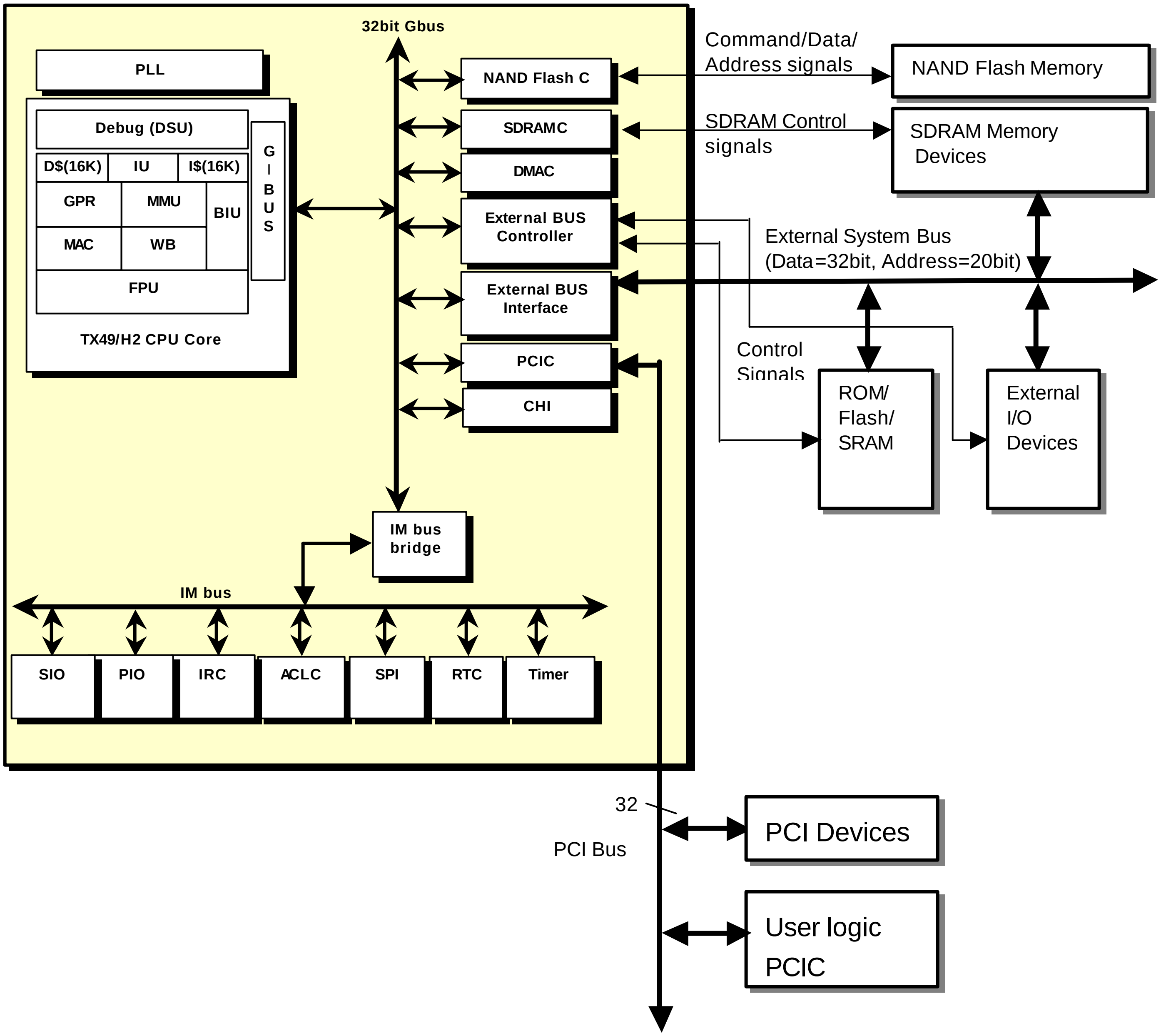

Figure 2.2 Typical TX4925 System Block Diagram

2.3 TX49/H2 Core Block Diagram

Figure 3 shows the internal block diagram of the TX49/H2 core

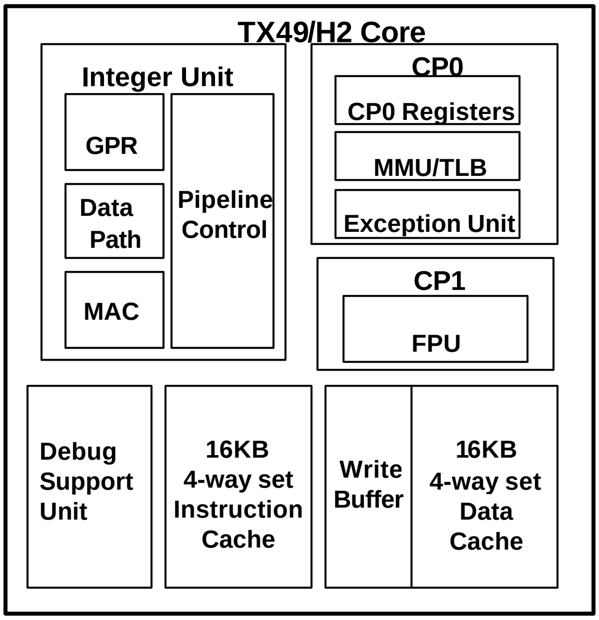

Figure 2.3 TX49/H2 Core Block Diagram

2.4 TX49/H2 CORE FEATURES

The TX49/H2 Core is high performance and low-power 64-bit RISC processor core developed by Toshiba.

- 64-bit operation
- 32, 64-bit integer general purpose registers
- 32-bit physical address space and 64-bit virtual address space
- Optimized 5-stage pipeline
- Instruction Set
  MIPS I, II , III compatible ISA
  PREF (Prefetch) and MAC (Multiply/Accumulate) instructions.
- 16k Byte Instruction Cache, and 16k Byte Data Cache
  4-way set associative with lock function
- MMU (Memory Management Unit): 48-entry fully associative JTLB
- The on-chip FPU supports both single- and double-precision arithmetic, as specified in IEEE Std 754.
- On-chip 4-deep write buffer
- Enhanced JTAG debug feature
  Built-in Debug Support Unit (DSU)

2.5 TX4925 Peripheral Circuit FEATURES

■ **External Bus Controller (EBUSC)**

The External Bus Controller generates necessary signals to control external memory and I/O devices.

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- 6 channels of chip select signals, enabling control of up to six devices (shared chip select signals of 2 channels)
- Supports access to ROM (including mask ROM, page mode ROM, EPROM and EEPROM), SRAM, flash ROM, and I/O devices
- Supports 32-bit, 16-bit and 8-bit data bus sizing on a per channel basis
- Supports selection among full speed (up to 80MHz), 1/2 speed (up to 40MHz), 1/3 speed (up tp 27MHz) and 1/4 speed (up to 20MHz) on a per channel basis
- Support specification of timing on a per channel basis
- The user can specify setup and hold times for address, chip enable, write enable, and output enable signals
- Supports memory sizes of 1M byte to 1G byte for devices with 32-bit data bus, 1M byte to 512M bytes for devices with 16-bit data bus, and 1M byte to 256M bytes for devices with 8-bit data bus

■ **DMA Controller (DMAC)**

The TX4925 contains a 4-channel DMA controller that executes DMA transfer to memory and I/O devices.

- 4-channel independently handling internal / external DMA requests (Usable only 2 channels by external DMA requests)
- Supports DMA transfer with built-in serial I/O controller and AC-link controller based on internal DMA requests
- Supports signal address (fly-by DMA) and dual address transfers in external I/O DMA transfer mode using external DMA requests
- Supports transfer between memory and external I/O devices having 32 / 16 / 8-bit data bus
- Supports memory-to-memory copy mode, with no address boundary restrictions
- Supports burst transfer of up to 8 double words for a single read / write
- Supports memory fill mode, writing double-word data to specified memory area
- Supports chained DMA transfer

SDRAM Controller (SDRAMC)

The SDRAM Controller generates necessary control signals for the SDRAM interface. It has four channels and can handle up to 2G bytes (512 MB/channel) of memory by supporting a variety of memory configurations.

- Memory clock frequency : 80MHz (divided by 2.5)
- 4 sets of independent memory channels
- Supports 16M / 64M / 128M / 256M / 512M-bit SDRAM with 2/4 bank size availability
- Supports Single Data Rate (SDR) SDRAM and SyncFlash® memory
- Supports use of Registered DIMM
- Supports 32 / 16-bit data bus sizing on a per channel basis
- Supports specification of SDRAM timing on a per channel basis
- Supports critical word first access of TX49/H2 core
- Low power mode : selectable between self-refreshing and pre-charge power-down

PCI Controller (PCIC)

The TX4925 contains a PCI Controller that complies with PCI Local Bus Specification Revision 2.2.

- Compliance with PCI Local Bus Specification Revision 2.2
  (Partly supports power management as optional function)
- 32-bit PCI interface featuring maximum PCI bus clock frequency of 33MHz
- Supports both target and initiator functions
- Supports change of address mapping between internal bus and PCI bus
- PCI bus arbiter enables connection of up 4 external bus masters
- Supports booting of TX4925 from memory on PCI bus
- 1 channel of DMA controller dedicated to PCI controller (PDMAC)

Serial I/O Controller (SIO)

The TX4925 contains a 2-channels asynchronous serial I/O interface (full duplex UART).

- 2-channel full duplex UART
- Built-in baud rate generator
- FIFOs
- 8-bit x 8 transmitter FIFO
- 13-bit (8 data bits and 5 status bits) x 16 receiver FIFO
- Supports DMA tranfer

Timers / Counters Controller (TMR)

The TX4925 contains 3-channel timer / counters.

- 3-channel 32-bit up-counter
- Supports three modes : interval timer mode, pulse generator mode, and watchdog timer mode
- 2 timer output pins
- 1 count clock input pin

Parallel I/O Ports (PIO)

The TX4925 contains 32-bit parallel I/O ports

- Independent selection of direction of pins and output port type (totem-pole or open-drain outputs) on a per bit basis.
  (PIO[4,2,0] are input-only pins.)

AC-link controller (ACLC)

The TX4925 contains an AC-link controller, which can be operated using any audio and / or modem CODECs described in Audio CODEC'97 Revision 2.1 (AC'97).

- Supports up to two CODECs
- Supports recording and playback for right and left 16-bit PCM channels
- Supports playback for 16-bit surround, center, and LFE channels
- Supports audio recording and layback at variable rate
- Supports Line1 and GPIO slots for modem CODEC
- Supports AC-link low power mode, wakeup, and warm reset
- Supports input / output of sample data by DMA transfer

Interrupt Controller (IRC)

The TX4925 contains an interrupt controller, which receives interrupt requests sent by both the TX4925's built-in peripherals and external devices and issues interrupt requests to the TX49/H2 core. It has a 32-bit flag register to generate interrupt requests to external devices or the TX49/H2 core.

- Supports 21 internal interrupt sources from built-in peripherals and 8 external interrupt signal inputs
- 8 interrupt priority levels for each interrupt source
- Supports selection between edge- and level-triggered interrupt detection for each external interrupt
- 32-bit read / write flag register for interrupt requests, making it possible to issue interrupt request to external devices and to the TX49/H2 core (IRC interrupts)

high-speed serial Concentration Highway Interface (CHI)

The TX4925 has a high-speed serial Concentration Highway Interface.

- Contents logic for interfacing to external full-duplex serial time-division-multiplexed (TDM) communication peripherals
- Supports ISDN line interface chips and other PCM/TDM serial devices
- Programmable CHI Interface (numbers of channels, frame rate, bit rate, etc.)
- supports data rates up to 4.096Mbps

Serial Peripheral Interface (SPI)

The TX4925 has a Serial Peripheral Interface.

- full-duplex, synchronous serial data transfers (data in/out, and clock signals)
- 8-bit or 16-bit data word lengths
- Programmable SPI baud rate

NAND Flash memory Controller (NDFMC)

The TX4925 has a NAND Flash memory Controller.

- Controlled NAND Flash I/F by Setting Register
- Supports ECC (Error Correct Circuit) control flow

PCMCIA Interface (PCMCIA I/F)

The TX4925 has a 2 identical full PCMCIA ports.

- Provide the control signals and accepts the status signals which conform to the PCMCIA version 2.1 standard
- Appropriate connector keying and level-shifting buffers required for 3.3V versus 5V PCMCIA interface implementations

Real Time Clock (RTC)

The TX4925 has a Real Time Clock.

- 44-bit up-counter
- Interrupts on alarm, timer, and prior to RTC roll-over
- Date managed by software

Power-down mode

The TX4925 contains support for implementation of power-down mode.

- HALT mode (stopping CPU core clock) for TX49/H2 core block
- Power-down mode (stopping input clock) for individual internal peripheral modules
- RF(Reduced Frequency) Function (1/1,1/2,1/4,1/8)

Extended EJTAG Interface

The TX4925 contains an Extended Enhanced Joint Test Action Group (Extended EJTAG) interface, which provides two functions : JTAG boundary scan test that complies with IEEE1149.1 and real-time debugging using a debug support unit (DSU) built into the TX49/H2 core.

- IEEE 1149.1 JTAG Boundary Scan
- Real-time debugging functions using special emulation probe : execution control (execution, break, step, and register / memory access) and PC trace

3. Pins

3.1 Pin designations

A1	PCICLKIO	B11	SDCS [3]*	D1	GNT [2]*	F3	PCIAD[30]	K1	PCIAD[19]
A2	TMS	B12	CKE	D2	REQ [1]*	F4	VDDS	K2	PCIAD[20]
A3	TDI*	B13	ADDR[19]	D3	GNT [1]*	F17	Vss	K3	PCIAD[21]
A4	PIO[26]	B14	ADDR[14]	D4	Vss	F18	DATA[14]	K4	VDDS
A5	PIO[24]	B15	ADDR[12]	D5	VDDC	F19	DATA[30]	K17	Vss
A6	PIO[27]	B16	ADDR[9]	D6	PIO[30]	F20	DATA[15]	K18	VDDC
A7	PIO[22]	B17	ADDR[7]	D7	Vss	G1	PCIAD[26]	K19	DATA[10]
A8	PIO[19]	B18	ADDR[5]	D8	VDDS	G2	PCIAD[27]	K20	DATA[26]
A9	SDCLKIN*	B19	DQM[3]*	D9	PON*	G3	VDDC	L1	PCIAD[17]
A10	SDCLK[1]	B20	SDCS [0]*	D10	Vss	G4	Vss	L2	PCIAD[18]
A11	SDCLK[0]	C1	PCICLK[2]	D11	VDDS	G17	Vss	L3	VDDC
A12	SDCS [2]*	C2	REQ [0]*	D12	Vss	G18	VDDC	L4	Vss
A13	ADDR[18]	C3	VDDS	D13	VDDS	G19	DATA[13]	L17	VDDS
A14	SADDR10	C4	VDDC	D14	Vss	G20	DATA[29]	L18	DATA[24]
A15	ADDR[13]	C5	PIO[25]	D15	Vss	H1	C BE[3]	L19	DATA[9]
A16	ADDR[10]	C6	PIO[28]	D16	VDDS	H2	PCIAD[24]	L20	DATA[25]
A17	ADDR[8]	C7	VDDC	D17	Vss	H3	PCIAD[25]	M1	FRAME*
A18	ADDR[6]	C8	PIO[23]	D18	WE*	H4	VDDS	M2	C BE[2]
A19	SDCS [1]*	C9	TRST	D19	CAS*	H17	Vss	M3	PCIAD[16]
A20	RAS*	C10	VDDC	D20	DQM[0]*	H18	VDDS	M4	VDDS
B1	PCICLK[1]	C11	SCANENB	E1	PCIAD[31]	H19	DATA[12]	M17	Vss
B2	GNT [0]*	C12	ADDR[17]	E2	REQ [3]*	H20	DATA[28]	M18	DATA[7]
B3	TCK	C13	ADDR[16]	E3	GNT [3]*	J1	PCIAD[22]	M19	DATA[23]
B4	TDO	C14	VDDC	E4	REQ [2]*	J2	PCIAD[23]	M20	DATA[8]
B5	PIO[31]	C15	ADDR[11]	E17	Vss	J3	IDSEL	N1	STOP*
B6	PIO[29]	C16	VDDC	E18	VDDS	J4	Vss	N2	DEVSEL*
B7	PIO[21]	C17	Vss	E19	DATA[31]	J17	Vss	N3	TRDY*
B8	PIO[18]	C18	VDDS	E20	RP*	J18	VDDC	N4	IRDY*
B9	PIO[20]	C19	DQM[2]*	F1	PCIAD[28]	J19	DATA[11]	N17	Vss

B10	RESET*	C20	DQM[1]*	F2	PCIAD[29]	J20	DATA[27]	N18	VDDS

N19	DATA[6]	T17	VDDS	U19	DATA[1]	W1	PCIAD[4]	Y3	PCIAD[2]
N20	DATA[22]	T18	DATA[2]	U20	DATA[17]	W2	PCIAD[5]	Y4	PCIAD[3]
P1	SERR*	T19	DATA[18]	V1	C BE[0]	W3	PCIAD[6]	Y5	SYSCLK*
P2	PERR*	T20	DATA[3]	V2	PCIAD[8]	W4	PCIAD[7]	Y6	SWE*
P3	VDDC	U1	PCIAD[9]	V3	VDDS	W5	BWE [1]*	Y7	ADDR[1]
P4	Vss	U2	PCIAD[10]	V4	VDDC	W6	UAE	Y8	ADDR[4]
P17	Vss	U3	PCIAD[11]	V5	BWE [0]*	W7	ADDR[0]	Y9	OE*
P18	VDDC	U4	Vss	V6	BWE [3]*	W8	ADDR[3]	Y10	ROMCE [0]
P19	DATA[5]	U5	VDDS	V7	VDDC	W9	ADDR[15]	Y11	BUSSPRT*
P20	DATA[21]	U6	BWE [2]*	V8	ADDR[2]	W10	ROMCE [1]	Y12	ACK*
R1	PCIAD[15]	U7	Vss	V9	ROMCE [2]	W11	PIO[4]	Y13	PIO[11]
R2	C BE[1]	U8	VDDS	V10	PIO[2]	W12	PIO[3]	Y14	PIO[8]
R3	PAR	U9	ROMCE [3]	V11	VDDC	W13	PIO[10]	Y15	PIO[12]
R4	VDDC	U10	PIO[0]	V12	PIO[1]	W14	PIO[9]	Y16	PIO[14]
R17	Vss	U11	Vss	V13	PIO[5]	W15	PIO[17]	Y17	BC32K
R18	DATA[19]	U12	VDDS	V14	VDDC	W16	PIO[15]	Y18	C32KIN
R19	DATA[4]	U13	PIO[6]	V15	PIO[13]	W17	NMI*	Y19	PLLVSS
R20	DATA[20]	U14	Vss	V16	PIO[16]	W18	C32KOUT	Y20	Vss
T1	PCIAD[12]	U15	PIO[7]	V17	TEST*	W19	PLLVDD		
T2	PCIAD[13]	U16	Vss	V18	VDDS	W20	MSTRCLK		
T3	PCIAD[14]	U17	Vss	V19	DATA[0]	Y1	PCIAD[0]		
T4	VDDS	U18	DATA[16]	V20	Vss	Y2	PCIAD[1]		

3.2 Pin layout

	A	B	C	D	E	F	G	H	J	K
20	RAS*	SDCS [0]*	DQM[1]*	DQM[0]*	RP*	DATA[15]	DATA[29]	DATA[28]	DATA[27]	DATA[26]
19	SDCS [1]*	DQM[3]*	DQM[2]*	CAS*	DATA[31]	DATA[30]	DATA[13]	DATA[12]	DATA[11]	DATA[10]
18	ADDR[6]	ADDR[5]	VDDS	WE*	VDDS	DATA[14]	VDDC	VDDS	VDDC	VDDC
17	ADDR[8]	ADDR[7]	Vss	Vss	Vss	Vss	Vss	Vss	Vss	Vss
16	ADDR[10]	ADDR[9]	VDDC	VDDS						
15	ADDR[13]	ADDR[12]	ADDR[11]	Vss						
14	SADDR10	ADDR[14]	VDDC	Vss						
13	ADDR[18]	ADDR[19]	ADDR[16]	VDDS						
12	SDCS [2]*	CKE	ADDR[17]	Vss						
11	SDCLK[0]	SDCS [3]*	SCANENB	VDDS						
10	SDCLK[1]	RESET*	VDDC	Vss						
9	SDCLKIN*	PIO[20]	TRST	PON*						
8	PIO[19]	PIO[18]	PIO[23]	VDDS						
7	PIO[22]	PIO[21]	VDDC	Vss						
6	PIO[27]	PIO[29]	PIO[28]	PIO[30]						
5	PIO[24]	PIO[31]	PIO[25]	VDDC	TOP View					
4	PIO[26]	TDO	VDDC	Vss	REQ [2]*	VDDS	Vss	VDDS	Vss	VDDS
3	TDI*	TCK	VDDS	GNT [1]*	GNT [3]*	PCIAD[30]	VDDC	PCIAD[25]	IDSEL	PCIAD[21]
2	TMS	GNT [0]*	REQ [0]*	REQ [1]*	REQ [3]*	PCIAD[29]	PCIAD[27]	PCIAD[24]	PCIAD[23]	PCIAD[20]
1	PCICLKIO	PCICLK[1]	PCICLK[2]	GNT [2]*	PCIAD[31]	PCIAD[28]	PCIAD[26]	C BE[3]	PCIAD[22]	PCIAD[19]

L	M	N	P	R	T	U	V	W	Y	
DATA[25]	DATA[8]	DATA[22]	DATA[21]	DATA[20]	DATA[3]	DATA[17]	Vss	MSTRCLK	Vss	20
DATA[9]	DATA[23]	DATA[6]	DATA[5]	DATA[4]	DATA[18]	DATA[1]	DATA[0]	PLLVDD	PLLVSS	19
DATA[24]	DATA[7]	VDDS	VDDC	DATA[19]	DATA[2]	DATA[16]	VDDS	C32KOUT	C32KIN	18
VDDS	Vss	Vss	Vss	Vss	VDDS	Vss	TEST*	NMI*	BC32K	17
						Vss	PIO[16]	PIO[15]	PIO[14]	16
						PIO[7]	PIO[13]	PIO[17]	PIO[12]	15
						Vss	VDDC	PIO[9]	PIO[8]	14
						PIO[6]	PIO[5]	PIO[10]	PIO[11]	13
						VDDS	PIO[1]	PIO[3]	ACK*	12
						Vss	VDDC	PIO[4]	BUSSPRT*	11
						PIO[0]	PIO[2]	ROMCE [1]	ROMCE [0]	10
						ROMCE [3]	ROMCE [2]	ADDR[15]	OE*	9
						VDDS	ADDR[2]	ADDR[3]	ADDR[4]	8
						Vss	VDDC	ADDR[0]	ADDR[1]	7
						BWE [2]*	BWE [3]*	UAE	SWE*	6
					TOP View	VDDS	BWE [0]*	BWE [1]*	SYSCLK*	5
Vss	VDDS	IRDY*	Vss	VDDC	VDDS	Vss	VDDC	PCIAD[7]	PCIAD[3]	4
VDDC	PCIAD[16]	TRDY*	VDDC	PAR	PCIAD[14]	PCIAD[11]	VDDS	PCIAD[6]	PCIAD[2]	3
PCIAD[18]	C BE[2]	DEVSEL*	PERR*	C BE[1]	PCIAD[13]	PCIAD[10]	PCIAD[8]	PCIAD[5]	PCIAD[1]	2
PCIAD[17]	FRAME*	STOP*	SERR*	PCIAD[15]	PCIAD[12]	PCIAD[9]	C BE[0]	PCIAD[4]	PCIAD[0]	1

3.3 Pin signal description

Note: In the I/O columns, “PU” indicates an I/O pin with a pull-up resistor, and the term “PD” indicates an I/O pin with a pull-down resistor. * denotes an active-low signal when used as a suffix to a signal name.

Common Memory Interface

Signal Name	Type	Function	Initial State
ADDR[19:0]	Input/output PU	Address Address signals. For SDRAM, ADDR[19:16 , 14:5] and SADDR10 are used. When the external bus controller uses these pins, the meaning of each bit varies with the data bus width. The ADDR signals are also used as boot configuration signals (input) during a reset. For details of configuration signals. The ADDR signals are input signals only when the RESET* signal is asserted and become output signals after the RESET* signal is deasserted.	Input
SADDR10	Input/output PU	Address10 for SDRAM. Address single for SDRAM. This signal is also used as a boot configuration input signal for testing. Because this signal is used for testing, ensure that it will not pulled Low during a reset sequence. For details of configuration signals. This signal is used as an input signal while the RESET* signal is asserted. It becomes an output signal once the RESET* signal has been deasserted.	Input
DATA[31:0]	Input/output PU	Data 32-bit data bus	Input
BUSSPRT*	Output	Bus Separate Controls the connection and separation of devices controlled by the external bus controller to or from a high-speed device, such as SDRAM. H: Separate devices other than SDRAM from the data bus. L: Connect devices other than SDRAM to the data bus. Separation and connection are performed using external bidirectional bus buffers (such as the 74xx245). This signal can control either the QuickSwitch or 74xx245. These devices differ in that the signal is also pulled Low during a write cycle with the QuickSwitch. Boot configuration signal ADDR[19] determines which device is used. For details of configuration signals.	High

SDRAM / SyncFlash Memory Interface

Signal Name	Type	Function	Initial State
SDCLK[1:0]	Output	SDRAM Controller Clock Clock signals used by SDRAM/SyncFlash. The clock frequency is the same as the G-Bus clock (GBUSCLK) frequency. When these clock signals are not used, the pins can be set to L using the SDCLK Enable field of the pin configuration register (PCFG.SDCLKEN[1:0]).	All High
SDCLKIN	Input/output	SDRAM Feedback Clock input Feedback clock signal for SDRAM controller input signals.	Input
CKE	Output	Clock Enable CKE signal for SDRAM/SyncFlash.	High
SDCS[3:0]*	Output	Synchronous Memory Device Chip Select Chip select signals for SDRAM/SyncFlash.	All High
RAS*	Output	Row Address Strobe RAS signal for SDRAM/SyncFlash.	High
CAS*	Output	Column Address Strobe CAS signal for SDRAM/SyncFlash.	High
WE*	Output	Write Enable WR signal for SDRAM/SyncFlash.	High
DQM[3:0]	Output	Data Mask During a write cycle, the DQM signals function as a data mask. During a read cycle, they control the SDRAM output buffers. The bits correspond to the following data bus signals: DQM[3]:DATA[31:24], DQM[2]:DATA[23:16] DQM[1]:DATA[15:8], DQM[0]:DATA[7:0]	All High
RP*	Output	Initialize/Power Down RP* signal for SyncFlash.	Low

External Bus Interface

Signal Name	Type	Function	Initial State
SYSCLK	Output	System Clock Clock for external I/O devices. Outputs a clock in full speed mode (at the same frequency as the G-Bus clock (GBUSCLK) frequency), half speed mode (at one half the GBUSCLK frequency), third speed mode (at one third the GBUSCLK frequency), or quarter speed mode (at one quarter the GBUSCLK frequency). The boot configuration signals on the ADDR[4:3] pins select which speed mode will be used. When this clock signal is not used, the pin can be set to L using the SYSCLK Enable bit of the configuration register (PCFG.SYSCLKEN).	High
UAE	Output PU	Upper Address Enable Latch enable signal for the high-order address bits of ADDR. The enable polarity can be selected. This signal is also used as a boot configuration input signal for testing. Because this signal is used for testing, ensure that it will not pulled Low during a reset sequence. For details of configuration signals. This signal is used as an input signal while the RESET* signal is asserted. It becomes an output signal once the RESET* signal has been deasserted.	Input
CE[5:4]*	Output PU	Chip Enable Chip select signals for ROM, SRAM, and I/O devices. The pins are shared with other functions.	All High
CE[3:0]*	Output	Chip Enable Chip select signals for ROM, SRAM, and I/O devices.	All High
OE*	Output	Output Enable Output enable signal for ROM, SRAM, and I/O devices.	High
SWE*	Output	Write Enable Write enable signal for SRAM and I/O devices.	High
BWE[3:0]* /BE[3:0]*	Output	Byte Enable/Byte Write Enable BE[3:0]* indicate a valid data position on the data bus DATA[31:0] during read and write bus operation. In 16-bit bus mode, only BE[1:0]* are used. In 8-bit bus mode, only BE[0]* is used. BWE[3:0]* indicate a valid data position on the data bus DATA[31:0] during write bus operation. In 16-bit bus mode, only BWE[1:0]* are used. In 8-bit bus mode, only BWE[0]* is used. The following shows the correspondence between BE[3:0]*/BWE[3:0]* and the data bus signals. BE[3]*/BWE[3]*: DATA[31:24] BE[2]*/BWE[2]*: DATA[23:16] BE[1]*/BWE[1]*: DATA[15:8] BE[0]*/BWE[0]*: DATA[7:0] The boot configuration signal on the ADDR[11] pin and the EBCCRn.BC bit of the external bus controller determine whether the signals are used as BE[3:0]* or BWE[3:0]*.	All High
ACK*/ READY	Input/output PU	Data Acknowledge/Ready Flow control signal.	Input

Signal Name	Type	Function	Initial State
CARD1CSH* CARD1CSL*	Output PU	PCMCIA card slot 1 chip select Chip select signals for PCMCIA card slot 1. The pins are shared with other functions.	PIO input
CARD2CSH* CARD2CSL*	Output PU	PCMCIA card slot 2 chip select Chip select signals for PCMCIA card slot 2. The pins are shared with other functions.	PIO input
CARDREG*	Output PU	PCMCIA card register REG* signal for a PCMCIA card. The pin is shared with other functions.	PIO input
CARDIORD*	Output PU	PCMCIA card I/O read IORD* signal for a PCMCIA card. The pin is shared with other functions.	PIO input
CARDIOWR*	Output PU	PCMCIA card I/O write IOWR* signal for a PCMCIA card. The pin is shared with other functions.	PIO input
CARDDIR*	Output PU	PCMCIA card directory Controls the direction of the bidirectional buffer used for a PCMCIA slot. This signal is asserted during a read transaction when any of CARD2CSH*, CARD2CSL*, CARD1CSH* and CARD1CSL* are asserted. The pin is shared with other functions.	PIO input
CARD1WAIT*	Input PU	PCMCIA card slot 1 wait Card wait signal from PCMCIA card slot 1. The pin is shared with other functions.	PIO input
CARD2WAIT*	Input PU	PCMCIA card slot 2 wait Card wait signal from PCMCIA card slot 2. The pin is shared with other functions.	PIO input

DMA Interface

Signal Name	Type	Function	Initial State
DMAREQ [1:0]	Input PU	DMA Request DMA transfer request signals from an external I/O device. The pins are shared with other functions.	PIO input
DMAACK [1:0]	Output	DMA Acknowledge DMA transfer acknowledge signals to an external I/O device. The pins are shared with other functions.	PIO input
DMADONE*	Input/output PU	DMA Done DMADONE* is either used as an output signal that reports the termination of DMA transfer or as an input signal that causes DMA transfer to terminate. The pin is shared with other functions.	PIO input

PCI Interface

Signal Name	Type	Function	Initial State
PCICLK [2:1]	Output	PCI Clock PCI bus clock signals. A boot configuration signal (ADDR[18]) can determine whether the clock internally generated in the TX4925 is used as PCICLK. If the TX4925 internal clock is selected, the clock signals are output from these pins. When these clock signals are not used, the pins can be set to Hi-Z using the PCICLK Enable field of the pin configuration register (PCFG.PCICLKEN[2:1]).	Selected by ADDR[18] H: High L: L
PCICLKIO	Input/output	PCI Feedback Clock PCI feedback clock input. A boot configuration signal (ADDR[18]) can determine whether the clock internally generated in the TX4925 is used as PCICLK. If the TX4925 internal clock is selected, the clock signals are output and simultaneously fed back to the internal PCI block. When using the PCI block, therefore, do not set the PCICLK Enable field of the pin configuration register (PCFG.PCICLKIOEN) to 0.	Selected by ADDR[18] H: High L: Input
PCIAD [31:0]	Input/output	PCI Address and Data Multiplexed address and data bus.	Input
C_BE [3:0]	Input/output	Command and Byte Enable Command and byte enable signals.	Input
PAR	Input/output	Parity Even parity signal for PCIAD[31:0] and C_BE[3:0]*.	Input
FRAME*	Input/output	Cycle Frame Indicates that bus operation is in progress.	Input
IRDY*	Input/output	Initiator Ready Indicates that the initiator is ready to complete data transfer.	Input
TRDY*	Input/output	Target Ready Indicates that the target is ready to complete data transfer.	Input
STOP*	Input/output	Stop The target sends this signal to the initiator to request termination of data transfer.	Input

Signal Name	Type	Function	Initial State
ID_SEL	Input	Initialization Device Select Chip select signal used for configuration access.	Input
DEVSEL*	Input/output	Device Select The target asserts this signal in response to access from the initiator.	Input
REQ [3:2] *	Input	Request Signals used by the master to request bus mastership. The boot configuration signal on the ADDR[1] pin determines whether the built-in PCI bus arbiter is used. In internal arbiter mode, REQ[3:2]* are PCI bus request input signals. In external arbiter mode, REQ[3:2]* are not used. Because the pins are still placed in the input state, they must be pulled up externally.	Input
REQ [1] *	Input/output/OD	Request Signal used by the master to request bus mastership. The boot configuration signal on the ADDR[1] pin determines whether the built-in PCI bus arbiter is used. In internal arbiter mode, this signal is a PCI bus request input signal. In external arbiter mode, this signal is an external interrupt output signal (INTOUT).	Selected by ADDR[1] H: Input L: Hi-Z
REQ [0] *	Input/output	Request Signal used by the master to request bus mastership. The boot configuration signal on the ADDR[1] pin determines whether the built-in PCI bus arbiter is used. In internal arbiter mode, this signal is a PCI bus request input signal. In external arbiter mode, this signal is a PCI bus request output signal.	Selected by ADDR[1] H: Input L: High
GNT [3:0] *	Input/output	Grant Indicates that bus mastership has been granted to the PCI bus master. The boot configuration signal on the ADDR[1] pin determines whether the built-in PCI bus arbiter is used. In internal arbiter mode, all of GNT[3:0]* are PCI bus grant output signals. In external arbiter mode, GNT[0]* is a PCI bus grant input signal. Because GNT[3:1]* also become input signals, they must be pulled up externally.	Selected by ADDR[1] H: All High L: Input
PERR*	Input/output	Data Parity Error Indicates a data parity error in a bus cycle other than special cycles.	Input
SERR*	Input/OD	System Error Indicates an address parity error, a data parity error in a special cycle, or a fatal error. In host mode, SERR* is an input signal. In satellite mode, SERR* is an open-drain output signal. The mode is determined by the boot configuration signal on the ADDR[19] pin.	Input

SIO Interface

Signal Name	Type	Function	Initial State
CTS [1:0]*	Input PU*1	SIO Clear to Send CTS* signals. The pins are shared with other functions.	PIO input
RTS [1:0]*	Output PU*1	SIO Request to Send RTS* signals. The pins are shared with other functions.	PIO input
RXD[1:0]	Input PU*1	SIO Receive Data Serial data input signals. The pins are shared with other functions.	PIO input
TXD[1:0]	3-state Output PU*1	SIO Transmit Data Serial data output signals. The pins are shared with other functions.	PIO input
SCLK	Input PU	External Serial Clock SIO clock input signal. SIO0 and SIO1 share this signal. The pin is shared with other functions.	PIO input

*1: These signals are pulled up for channel 0 only. No pull-up resistor is provided for channel 1.

Timer Interface

Signal Name	Type	Function	Initial State
TIMER[1:0]	Output PU	Timer Output Timer output signals. The pins are shared with other functions.	PIO input
TCLK	Input PU	External Timer Clock Timer input clock signal. TMR0, TMR1, and TMR2 share this signal. The pin is shared with other functions.	PIO input

PIO Interface

Signal Name	Type	Function	Initial State
PIO[31:20]	Input/output PU	PIO Ports[31:20] Parallel I/O signals. The pins are shared with other functions, including PC trace. The boot configuration signal on the TDO pin determines whether the signals are used for PC trace.	Selected by TDO H: PIO input L: Output (PC trace function)
PIO[19:0]	Input/output PU*1	PIO Ports[19:0] Parallel I/O signals. The pins are shared with other functions.	Input

*1: PIO[17:12] do not have pull-up resistors.

AC Link Interface

Signal Name	Type	Function	Initial State
ACRESET*	Output	AC '97 Master H/W Reset The pin is shared with other functions.	PIO input
SYNC	Output	48 kHz Fixed Rate Sample Sync The pin is shared with other functions.	PIO input
SDOUT	Output	Serial, Time Division Multiplexed, AC '97 Output Stream The pin is shared with other functions.	PIO input
SDIN]1]	Input	Serial, Time Division Multiplexed, AC '97 Input Stream The pin is shared with other functions.	PIO input
SDIN[0]	Input	Serial, Time Division Multiplexed, AC '97 Input Stream The pin is shared with other functions.	PIO input
BITCLK	Input	12.288 MHz Serial Data Clock The pin is shared with other functions.	PIO input

Interrupt Signals

Signal Name	Type	Function	Initial State
NMI*	Input PU	Non-Maskable Interrupt Non-maskable interrupt signal.	Input
INT[7:0]*	Input PU	External Interrupt Requests External interrupt request signals. The pins are shared with other functions.	PIO input

CHI Interface

Signal Name	Type	Function	Initial State
CHIFS	Input/output PU	CHI Frame synchronization CHI frame synchronization signal. This pin can be used in either output or input mode. In output mode, the pin allows the TX4925 to become the master CHI synchronization source. In input mode, the pin allows the external peripheral device to become the master CHI synchronization source. In that case, the TX4925 CHI module becomes a slave for external synchronization. The pin is shared with other functions.	PIO input
CHICLK	Input/output PU	CHI Clock CHI clock signal. This pin can be used in either output or input mode. In output mode, the pin allows the TX4925 to become the master CHI clock source. In input mode, the pin allows the external peripheral device to become the master CHI clock source. In that case, the TX4925 CHI module becomes a slave for the external clock. The pin is shared with other functions.	PIO input
CHIDOUT	Output PU	CHI Data Output CHI serial data output signal. The pin is shared with other functions.	PIO input
CHIDIN	Input PU	CHI Data Input CHI serial data input signal. The pin is shared with other functions.	PIO input

SPI Interface

Signal Name	Type	Function	Initial State
SPICLK	Output PU	SPI Clock This pin is used for a data clock to or from an SPI slave device. The pin is shared with other functions.	PIO input
SPIOUT	Output PU	SPI Data Output This signal contains data to be shifted to an SPI slave device. The pin is shared with other functions.	PIO input
SPIIN	Input PU	SPI Data Input This signal contains data to be shifted from an SPI slave device. The pin is shared with other functions.	PIO input

NAND Flash Memory Interface

Signal Name	Type	Function	Initial State
ND_ALE	Output	NAND Flash Address Latch Enable ALE signal for NAND flash memory. The pin is shared with other functions.	PIO input
ND_CLE	Output	NAND Flash Command Latch Enable CLE signal for NAND flash memory. The pin is shared with other functions.	PIO input
ND_CE*	Output	NAND Flash Chip Enable CE signal for NAND flash memory. The pin is shared with other functions.	PIO input
ND_RE*	Output	NAND Flash Read Enable RE signal for NAND flash memory. The pin is shared with other functions.	PIO input
ND_WE*	Output	NAND Flash Write Enable WE signal for NAND flash memory. The pin is shared with other functions.	PIO input
ND_R/B*	Input	NAND Flash Ready/Busy Ready/Busy signal for NAND flash memory. The pin is shared with other functions.	PIO input

EJTAG Interface

Signal Name	Type	Function	Initial State
TCK	Input PU	JTAG Test Clock Input Clock input signal for JTAG. TCK is used to execute JTAG instructions and input/output data.	Input
TDI/DINT*	Input PU	JTAG Test Data Input/Debug Interrupt When PC trace mode is not selected, this signal is a JTAG data input signal. It is used to input serial data to JTAG data/instruction registers. When PC trace mode is selected, this signal is an interrupt input signal used to cancel PC trace mode for the debug unit.	Input
TDO/TPC[0]	Output	JTAG Test Data Output/PC Trace Output When PC trace mode is not selected, this signal is a JTAG data output signal. Data is output by means of serial scan. When PC trace mode is selected, this signal outputs the value of the noncontiguous program counter in sync with the debug clock (DCLK).	Input
TPC[3:1]	Output	PC Trace Output TPC[3:1] output the value of the noncontiguous program counter in sync with DCLK. The pins are shared with other functions.	Selected by TDO H: PIO input L: All High
TMS	Input PU	JTAG Test Mode Select Input TMS mainly controls state transition in the TAP controller state machine.	Input
TRST*	Input	Test Reset Input Asynchronous reset input for the TAP controller and debug support unit (DSU). When an EJTAG probe is not connected, this pin must be fixed to low. When connecting an EJTAG probe, prevent floating, for example, by connecting a pull-up resistor. When this signal is deasserted, G-Bus timeout detection is disabled.	Input
DCLK	Output	Debug Clock Clock output signal for the real-time debugging system. When PC trace mode is selected, the TPC[3:1] and PCST signals are output synchronously. This clock is the TX49/H2 core operating clock (CPUCLK) divided by 3. The pin is shared with other functions.	Selected by TDO H: PIO input L: Low
PCST[8:0]	Output	PC Trace Status Information Outputs PC trace status and other information. The pins are shared with other functions.	Selected by TDO H: PIO input (PCST[8:1]) BC32K(PCST[0]) L: All Low

Clock signals

Signal Name	Type	Function	Initial State
MASTERCLK	Input	Master Clock Input pin for the TX4925 operating clock. A crystal resonator cannot be connected to this pin because the pin does not contain an oscillator.	Input
C32KIN	Input	32 KHz Crystal Input Connect this pin and C32KOUT to a 32.768 kHz crystal.	Input
C32KOUT	Output	32 KHz Crystal output Connect this pin and C32KIN to a 32.768 kHz crystal.	Output
BC32K	Output PU	Buffer output of 32 KHz Crystal Buffer output for a 32.768 kHz clock.	Selected by TDO H: Output (BC32K) L: Low

Reset signals

Signal Name	Type	Function	Initial State
RESET*	Input SMT	Reset Reset signal.	Input
PON*	Input SMT	Power On Reset Initializes the CG. For timing.	Input

Test Signals

Signal Name	Type	Function	Initial State
TEST*	Input	Test Mode Setting Test pin. This pin must be fixed to High.	Input
SCANENB*	Input	Scan Mode Test Control Test pin. This pin must be fixed to High.	Input

Power Supply Pins

Signal Name	Type	Function	Initial State
PLL1VDD_A	-	PLL Power Pins PLL analog power supply pins. PLL1VDD_A = 1.5 V	-
PLL1VSS_A	-	PLL Ground Pins PLL analog ground pins. PLL1VSS_A = 0 V	-
VccInt	-	Internal Power Pins Digital power supply pins for internal logic. VccInt = 1.5 V.	-
VccIO	-	I/O Power Pins Digital power supply pins for input/output pins. VccIO = 3.3 V.	-
Vss	-	Ground Pins Digital ground pins. Vss = 0 V.	-

4. Pin Multiplexing

A total of 33 pins of the TX4925 have multiplexed functions. Table 4.1 shows the multiplexed pins. The function of a given pin is selected in various ways, depending on the pin(s) involved.

Table 4.1 Pin Multiplexing

Pin num	Signal name	Multiplexed Function
	PIO[31]	PIO[31] / CADDIR* / BCLK / TPC[2]
	PIO[30]	PIO[30] / CARDREG* / PCST[8]
	PIO[29]	PIO[29] / CARD2CSH* / CE5* / INT[7] [*2] / PCST[6]
	PIO[28]	PIO[28] / CARD2CSL* / CE4* / INT[6] [*2] / PCST[7]
	PIO[27]	PIO[27] / CARD2WAIT* [*3] / CHIOUT / PCST[5]
	PIO[26]	PIO[26] / CARD1CSH* / DCLK
	PIO[25]	PIO[25] / CARD1CSL* / TPC[3]
	PIO[24]	PIO[24] / CARD1WAIT* [*3] / TPC[1]
	PIO[23]	PIO[23] / SPICLK / PCST[2]
	PIO[22]	PIO[22] / SPIIN / PCST[3]
	PIO[21]	PIO[21] / SPIOUT / PCST[4]
	PIO[20]	PIO[20] / TIMER[0] / CHIFS / PCST[1]
	PIO[19]	PIO[19] / TIMER[1] / CHICLK
	PIO[18]	PIO[18] / TCLK [*4] / CHIDIN
	PIO[17]	PIO[17] / AC_SDIN[0] / ND_WE* / TXD[1]
	PIO[16]	PIO[16] / AC_SDOUT / ND_RB* / RXD[1]
	PIO[15]	PIO[15] / AC_BITCLK / ND_CLE / RTS[1] / INT[5] [*2]
	PIO[14]	PIO[14] / AC_SYNC / ND_RE* / CTS[1] / INT[4] [*2]
	PIO[13]	PIO[13] / AC_SDIN[1] / ND_ALE
	PIO[12]	PIO[12] / AC_RST* / ND_CE*
	PIO[11]	PIO[11] / TXD[0]
	PIO[10]	PIO[10] / RXD[0]
	PIO[9]	PIO[9] / RTS [0] * / INT[3] [*2]
	PIO[8]	PIO[8] / CTS [0] * / INT[2] [*2]
	PIO[7]	PIO[7] / INT[1] [*2]
	PIO[6]	PIO[6] / INT[0] [*2]
	PIO[5]	PIO[5] / SCLK [*5]
	PIO[4]	PIO[4] [*1] / DMAACK[1]
	PIO[3]	PIO[3] / DMAREQ[1]
	PIO[2]	PIO[2] [*1] / DMAACK[0]
	PIO[1]	PIO[1] / DMAREQ[0]
	PIO[0]	PIO[0] [*1] / DMADONE
	BC32K	PCST[0]
	BE[3]*/BWE[3]* [*6]	CARDIOWR* [*6]
	BE[2]*/BWE[2]* [*6]	CARDIORD* [*6]

Note 1 : PIO[4], PIO[2], and PIO[0] are only input ports.

Note 2 : Not enable the interrupt in IRC if these signals are used other function because INT[7:0] are directly connected to IRC.

Note 3 : CARD1WAIT* and CARD2WAIT* are directly connected to PCMCIA controller. So PCFG register has not the control bit that be enable CADRWAIT* and CARD2WAIT* function.

Note 4 : TCLK are directly connected to Timer ch0, ch1 and ch2. Thus, Timer should not enable the use of external clock unless that is the desired function of this pin.

Note 5 : SCLK are directly connected to SIO ch0 and ch1. Thus, SIO should not enable the use of external clock unless that is the desired function of this pin.

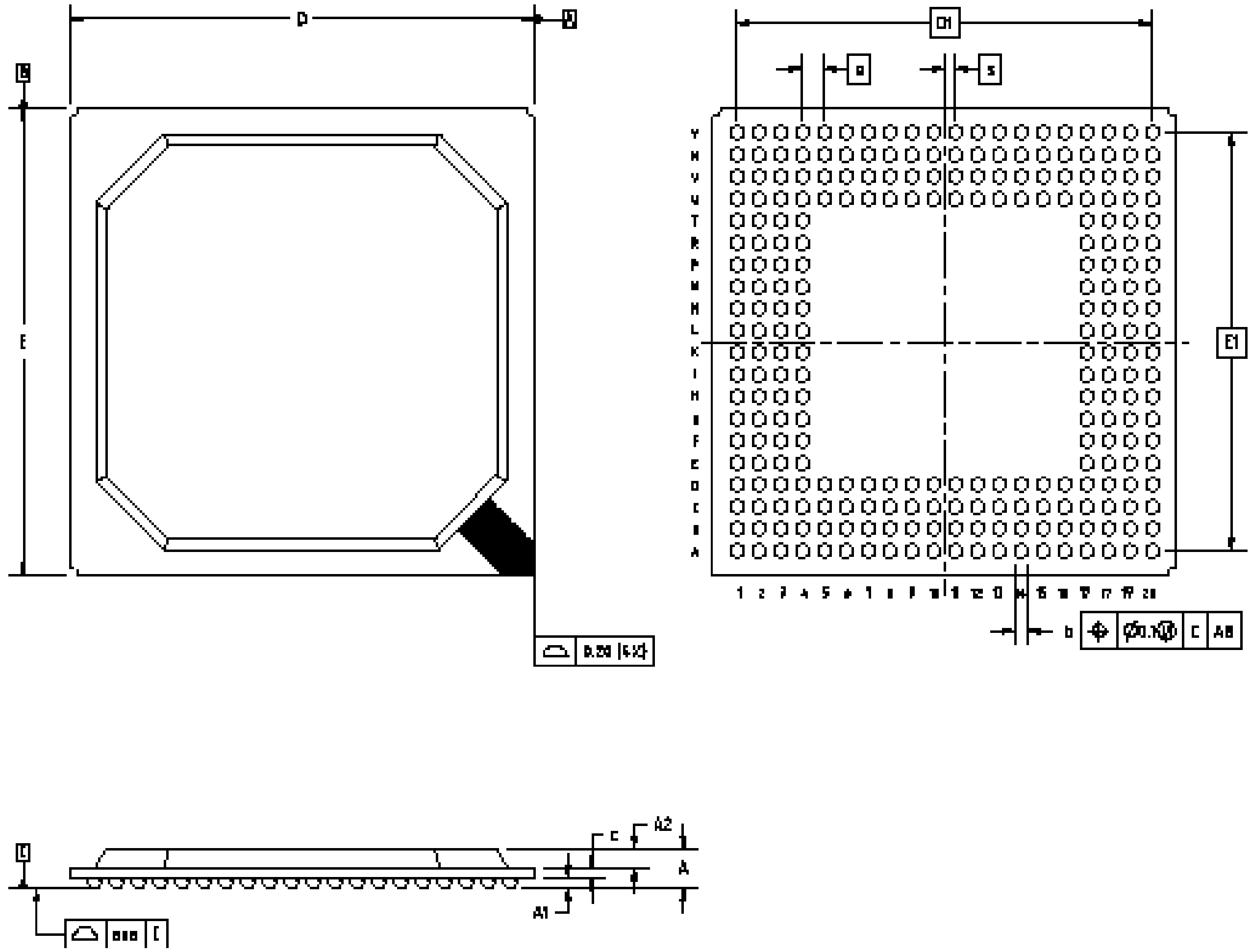
Note 6 : BE[3]*/BWE[3]* operates as CARDIOWR* when TX4925 access to PCMCIA device, and as BE[3]*/BWE[3]* when it access to any other devices. BE[2]*/BWE[2]* operates as CARDIORD* when TX4925 access to PCMCIA device, and as BE[2]*/BWE[2]* when it access to any other devices, too.

5. ELECTRICAL CHARACTERISTICS

T.B.D

6. Package

Package type (Package code) : 256-pin PBGA / PBGA[4L] (P-BGA256-2727-1.27A4)



Reference symbol	min.	typ.	max.
A	2.20	2.33	2.46
A1	0.5	0.6	0.7
A2		1.17	
b	0.60	0.75	0.90
c		0.56	
D	26.8	27.0	27.2
D1		24.13	
E	26.8	27.0	27.2
E1		24.13	
e		1.27	
s		0.635	
aaa		0.15	

7. HISTORY

-19/Feb/01	The first edition
-10/Apl/01	Modify the description for all
-18/Apl/01	Add the Clock Signals in 3.1 Pin signal description
-21/May/01	Add the export regulation on first page
-29/Aug/01	Add the 3.1 Pin designations and 3.2 Pin layout
-26/Dec/01 (Rev 0.1)	Modify the description for all