MOS LSI

TMS 3000 LR-DUAL 25-BIT STATIC SHIFT REGISTER
TMS 3001 LR-DUAL 32-BIT STATIC SHIFT REGISTER

FEBRUARY 1971

features

- Static logic
- DC to 1 MHz operation
- Low power dissipation
- Push-pull output buffers
- TTL compatible

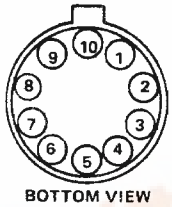
description

The TMS 3000 LR and TMS 3001 LR are dual static shift registers. Each device contains two dc-to-1-MHz shift registers with independent input and output terminals and common clocks and power. MOS thick-oxide technology is used to fabricate cross-coupled flip-flops for each register bit so that data can be stored indefinitely. Transistors in the device are P-channel enhancement-mode type. All input leads have zener network protection and all outputs contain low-output-impedance, non-inverting push-pull output buffers.

Two power supply levels and two clocks are required for operation with a third clock generated internally. Data is transferred into the register when the ϕ_1 clock is pulsed to logic 1. Data is shifted when the ϕ_1 clock is returned to logic 0 and the ϕ_2 clock is pulsed to logic 1. Output data appears on the logic 0 to logic 1 transition of the ϕ_2 clock. For long term storage, the ϕ_1 clock must be held at logic 0 and the ϕ_2 clock at logic 1.

mechanical data and pin configuration

The TMS 3000 LR and TMS 3001 LR are mounted in TO-100 packages. (See MOS/LSI packaging section.)



BOTTOM VIEW

PIN NO.	FUNCTION	PIN NO.	FUNCTION
1	Input 1	6	Clock ϕ_2
2	Output 1	7	V_{GG}
3	V_{DD}	8	Output 2
4	Clock ϕ_1	9	Input 2
5	GND (V_{SS})	10	No connection

logic definition

Negative logic is assumed

a) Logic 1 = most negative voltage

b) Logic 0 = most positive voltage.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{DD} range (See Note 1)	−30 V to 0.3 V
Supply voltage V_{GG} range (See Note 1)	−30 V to 0.3 V
Phase one clock input voltage $V_{\phi 1}$ range (See Note 1)	−30 V to 0.3 V
Phase two clock input voltage $V_{\phi 2}$ range (See Note 1)	−30 V to 0.3 V
Data input voltage V_I range (See Note 1)	−30 V to 0.3 V
Power dissipation	450 mW
Operating free-air temperature range	−55°C to 85°C
Storage temperature range	−55°C to 150°C

NOTE 1: These voltage values are with respect to network ground terminal, V_{SS}.

14

PRELIMINARY DATA SHEET
Supplementary data will be published at a later date.

recommended operating conditions

CHARACTERISTICS	MIN	NOM	MAX	UNITS
Supply voltage V_{DD}	−12	−14	−15	V
Supply voltage V_{GG}	−24	−28	−29	V
Logic 0 data input voltage $V_{i(0)}$ (See Note 2)	0.3	0	−2	V
Logic 1 data input voltage $V_{i(1)}$ (See Note 2)	−9.5	−14	−29	V
Width of data pulse, $t_{p(data)}$ (See voltage waveforms)	0.4†			μs
Data setup time, t_{setup} (See voltage waveforms and Note 3)	100			ns
Data hold time, t_{hold} (See voltage waveforms and Note 4)	20			ns
Logic 0 clock input voltage $V_{\phi 0(clock)}$ (See Notes 2 and 5)	0.3	0	−2	V
Logic 1 clock input voltage $V_{\phi 1(clock)}$ (See Notes 2 and 5)	−24	−28	−29	V
Rise time of clock pulse, $t_{r(clock)}$ (See voltage waveforms)	0		5	μs
Fall time of clock pulse, $t_{f(clock)}$ (See voltage waveforms)			5	μs
ϕ_1 clock pulse width, $t_{p(\phi 1)}$ (See voltage waveforms)	0.3†		10†	μs
ϕ_2 clock pulse width, $t_{p(\phi 2)}$ (See voltage waveforms)	0.4†		∞†	μs
Time interval from ϕ_1 clock to ϕ_2 clock input pulse, $t_{\phi 12}$ (See waveforms and Note 5)	0.01		10	μs
Time interval from ϕ_2 clock to ϕ_1 clock input pulse, $t_{\phi 21}$ (See waveforms and Note 5)	0.01		10	μs
Clock repetition rate	0		1	MHz

NOTES: 2. These voltage values are with respect to network ground terminal, V_{SS}.

3. Setup time is the interval immediately preceeding the positive-going edge of the phase 1 clock during which period the data to be recognized must be maintained at the input to ensure its recognition.

4. Hold time is the interval immediately following the positive-going edge of the phase 1 clock during which period the data to be recognized must be maintained at the input to ensure its recognition.

5. The two clock pulses must never be simultaneously more than 3 volts more negative than V_{SS}.

† These values are at $V_{DD} = -14$ V, $V_{GG} = -28$ V, and $T_A = 25°C$.

electrical characteristics over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNITS
I_{IL}	Logic 1 input current into data input	$V_I = -20$ V,	$T° = 25°C$			0.5	μA
$I_{IL(\phi)}$	Logic 1 input current into either clock input	$V_I = -28$ V, $T° = 25°C$	$V_{GG} = 0$ V,			50	μA
V_{OH}	Logic 0 output voltage	$I_O = 0$ mA,	$C_L = 20$ pF		0.3	−1	V
		$I_O = 2$ mA,	$C_L = 20$ pF		−2.6	−5	V
		$I_O = 0$ mA, $V_{gg} = -24$ V	$V_{dd} = -12$ V,		−0.5	−1	V
V_{OL}	Logic 1 output voltage	$I_O = 0$,	$C_L = 20$ pF	−12	−13.5	−14	V
		$I_O = 0.5$ mA		−10.5	−12.5	−14	V
		$I_O = 0$ mA, $V_{gg} = -24$ V, $C_L = 20$ pF, $V_{in(0)} = -2$ V	$V_{dd} = -12$ V, $V_\phi, V_{\phi L} = -24$ V, $V_{in(1)} = -8.5$ V,	−8.8	−10.5	−12	V
R_{OH}	Output resistance, logic 0	$I_O = -2.0$ mA			1.5	2.5	kΩ
R_{OL}	Output resistance, logic 1	$I_O = 0.5$ mA			1.5	7	kΩ
I_{DD}	Supply current from V_{DD} terminal*	TMS 3000 LR,	$T° = 25°C$		−14	−20	mA
		TMS 3001 LR,	$T° = 25°C$		−16	−24	mA
I_{GG}	Supply current from V_{GG} terminal*	TMS 3000 LR,	$T° = 25°C$		−2	−3.5	mA
		TMS 3001 LR,	$T° = 25°C$		−2	−3.5	mA
f_{max}	Maximum clock frequency			1			MHz

† Unless otherwise noted, voltages are as shown in the nominal column of the recommended operating conditions (nominal operating voltages).

‡ All typical values are at $T_A = 25°C$.

* Current into a terminal is a positive value.

14

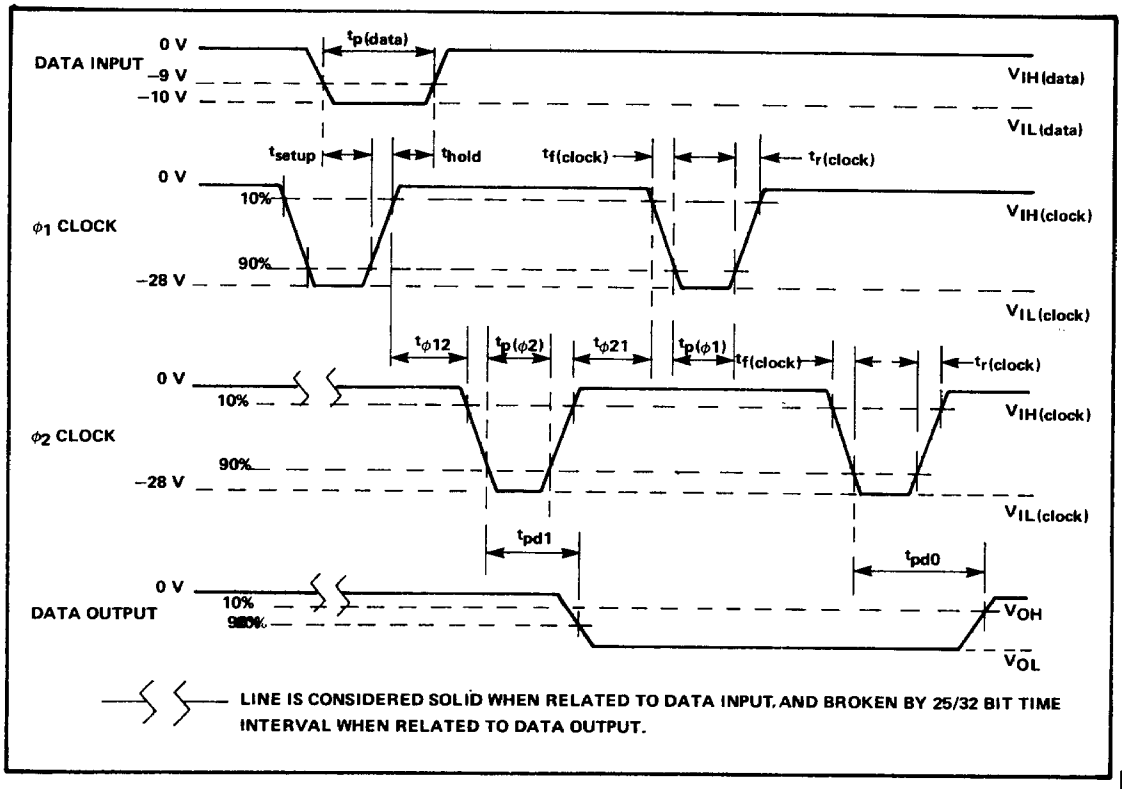
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

switching characteristics, V_{DD} = −14 V, V_{GG} = −28 V, R_L = 10 mΩ, C_L = 20 pF, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNITS
t_{pd0}	Propagation delay time to high level from ϕ_2 clock to data output	See voltage waveforms			325	475	ns
t_{pd1}	Propagation delay time to low level from ϕ_2 clock to data output	See voltage waveforms			325	475	ns
$C_{in(\phi1)}$	Capacitance of ϕ_1 clock input	V_I = 0 V, $V_{I(\phi2)}$ = 0 V, f = 1 MHz	TMS 3000 LR		8	12	pF
			TMS 3001 LR		11	15	pF
$C_{in(\phi2)}$	Capacitance of ϕ_2 clock input*	V_I = 0 V, $V_{I(\phi1)}$ = 0 V, f = 1 MHz	TMS 3000 LR		15	20	pF
			TMS 3001 LR		20	30	pF
C_{in}	Capacitance of data input	V_I = 0,	f = 1 MHz		5	7	pF

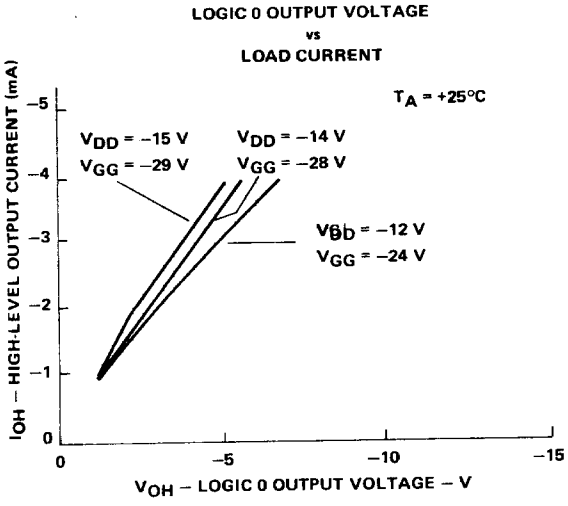
* $C_{in(\phi2)}$ includes the capacitance of the internal ϕ_2' clock.

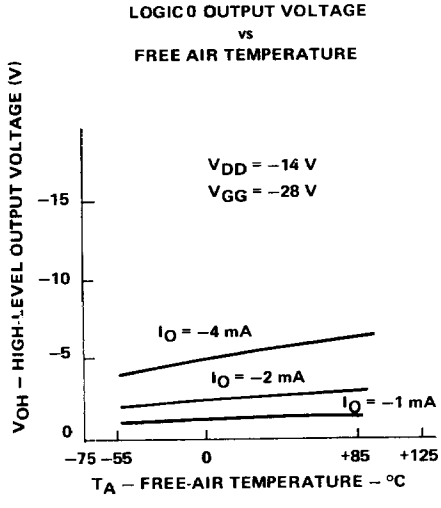
voltage waveforms

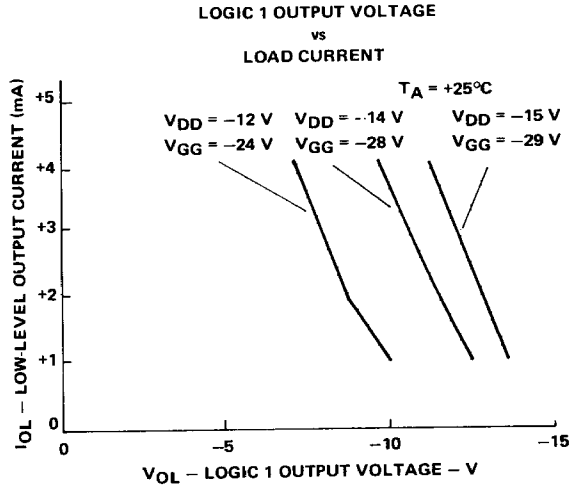


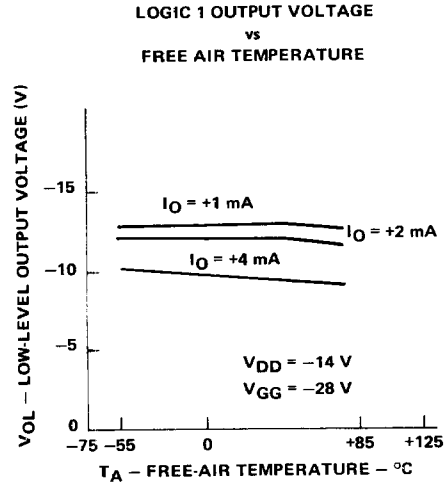
14

typical characteristics









typical application data

1) MOS/TTL interface

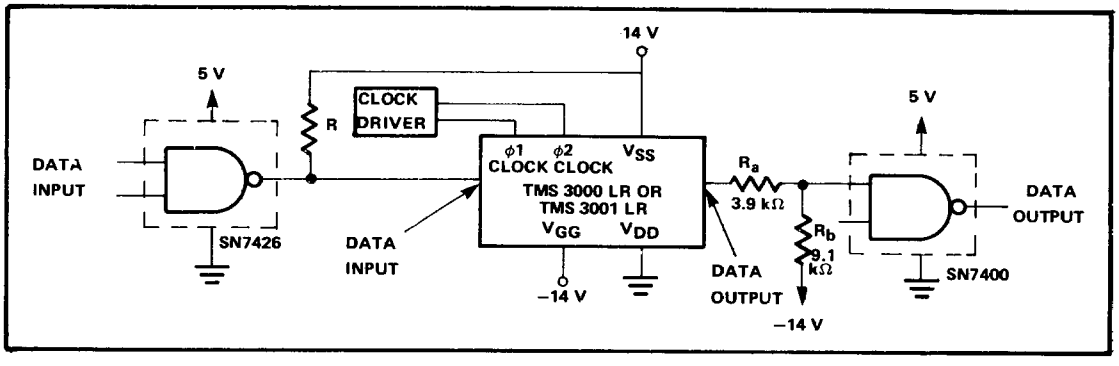
With proper supply voltages, interfacing can be achieved with only three resistors. A typical MOS/TTL interface is shown below.

An input pull-up resistor is required to provide the necessary input voltage swing. The value of this resistor (R) depends on the actual circuit requirements – values as low as 1 kΩ can be used for high-speed operation, while values as high as 15 kΩ can be used when low power consumption is important rather than high-speed.

14

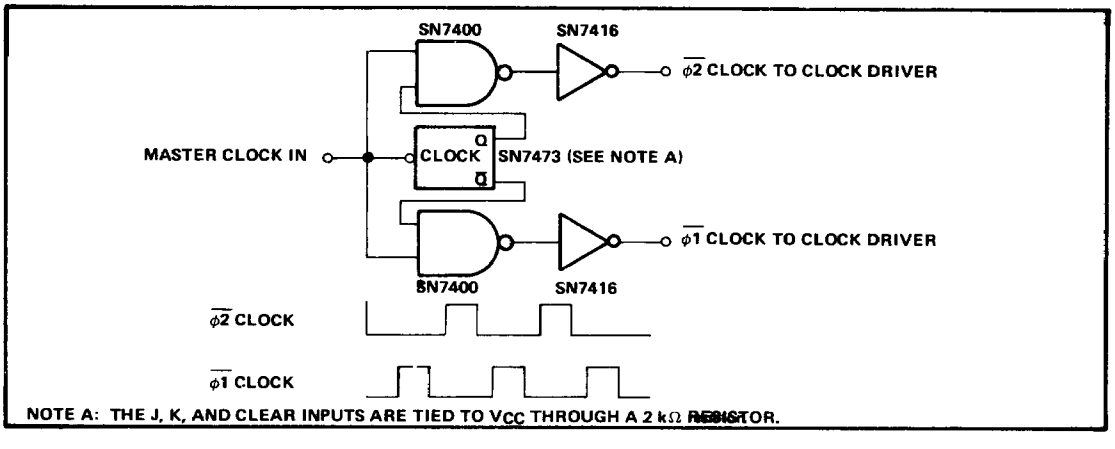
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

typical application data (continued)



At the output interface, the 9.1-kΩ resistor sinks the 1.6 mA of TTL gate current when 0 volts is required on the TTL input. When 3 volts is required on the TTL input, the MOS output device supplies current from 14 volts, through the 3.9-kΩ resistor and the 9.1-kΩ resistor, to −14 volts. The 3.9-kΩ resistor limits the voltage at the TTL gate input to 5 volts maximum.

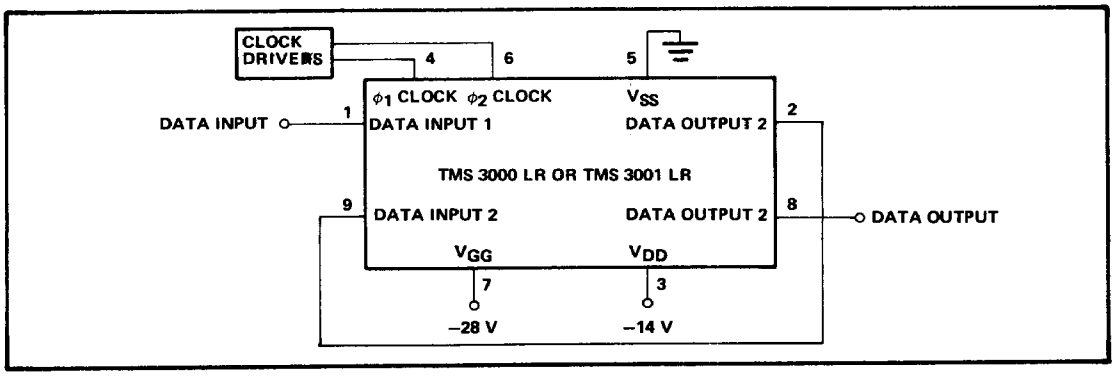
2) Two-phase clock generator



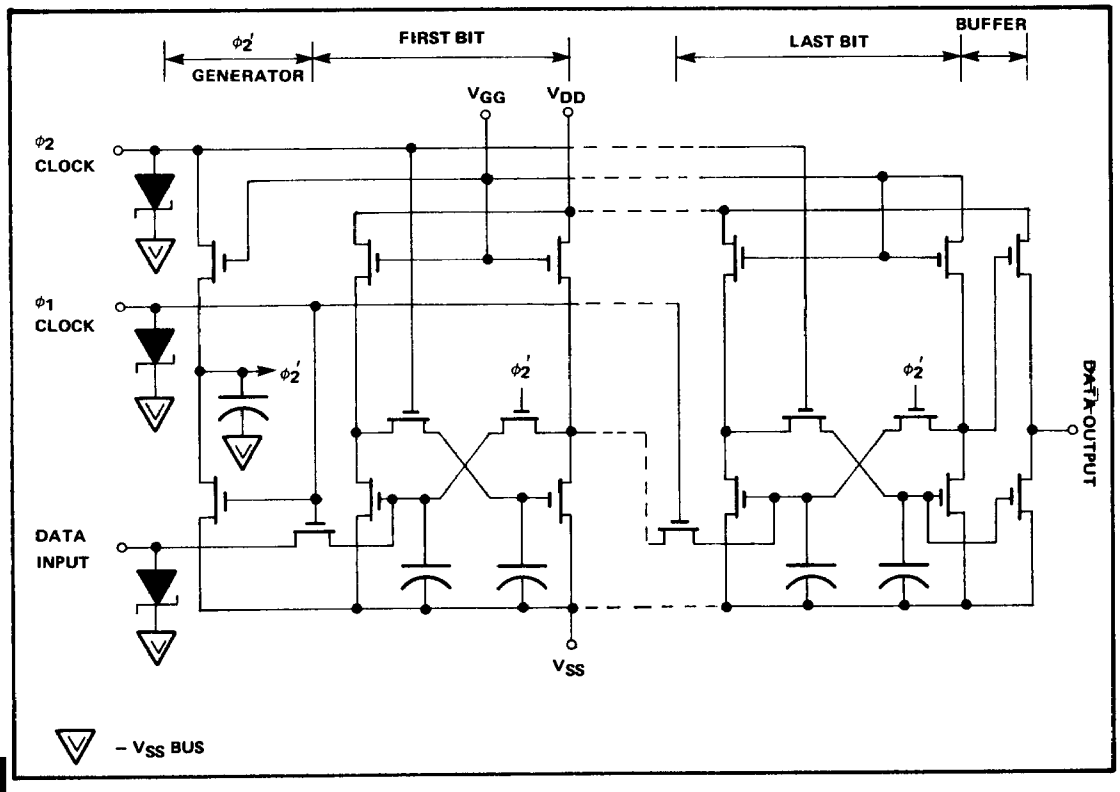
NOTE A: THE J, K, AND CLEAR INPUTS ARE TIED TO V_{CC} THROUGH A 2 kΩ RESISTOR.

14

expansion to single 50- or 64-bit register



schematic (each register)



TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222