MOS LSI

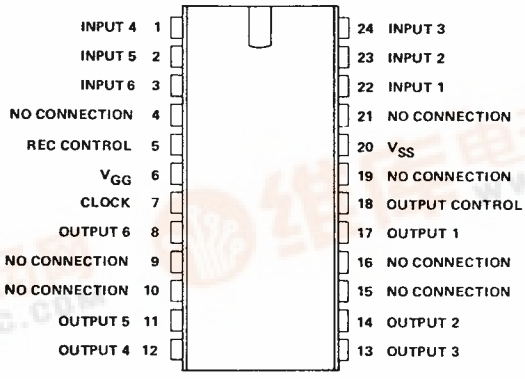
TMS 3112 JC, NC; TMS 3122 JC, NC; TMS 3123 JC, NC
HEX 32-BIT STATIC SHIFT REGISTERS

BULLETIN NO. DL-S 7512261, MAY 1975

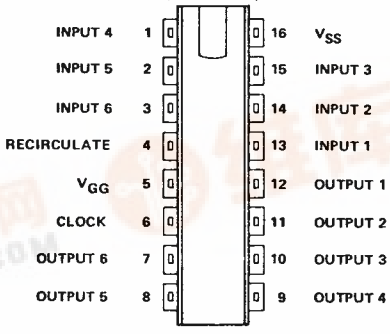
- DC to 2-MHz Operation
- Static Configuration
- Single TTL-Compatible Clock
- Inputs and Outputs are Fully TTL-Compatible
- Single-Ended (Open-Drain) Buffers
- On-Chip Recirculate Logic
- Gated-Output Control (TMS 3112, TMS 3123)
- Power Supplies . . . 5 V, −12 V
- MOS Low-Threshold P-Channel Technology

CERAMIC AND PLASTIC DUAL-IN-LINE PACKAGES

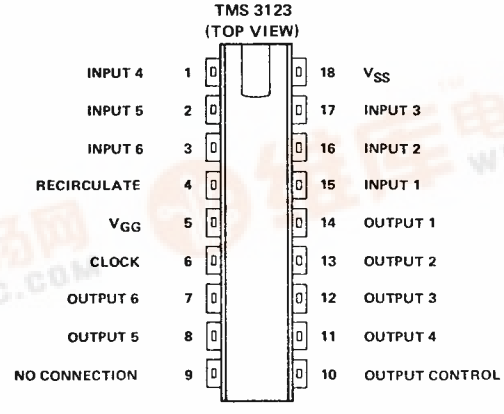
TMS 3112
(TOP VIEW)



TMS 3122
(TOP VIEW)



TMS 3123
(TOP VIEW)



NOTE: The TMS 3122 and TMS 3123 are compatible pin for pin except for output gate control, which necessitates one extra pin.

description

The TMS 3112, TMS 3122, and TMS 3123 JC, NC are 6-channel by 32-bit shift registers on a single monolithic chip with separate inputs and outputs and a common recirculate control. The TMS 3112 and TMS 3123 feature a common output gating control. The clock and all inputs can be driven directly from Series 74 TTL circuits and all outputs are capable of driving one Series 74 TTL circuit.

Cross-coupled inverters (flip-flops) are employed to implement each bit storage location. This static design allows input data rates from dc to 2 MHz and long-term data storage.

P-channel enhancement-type low-threshold processing has been employed to reduce power dissipation and provide simple interfaces with bipolar circuits.

The TMS 3122 and TMS 3123 are offered in 16-pin and 18-pin dual-in-line packages, respectively. The TMS 3112 is offered in a 24-pin dual-in-line package. All three devices are available in ceramic (JC suffix) or plastic (NC suffix) packages. The 16- and 18-pin packages are designed for insertion in mounting-hole rows on 300-mil centers. These devices are characterized for operation from −25°C to 85°C.

applications

The TMS 3112, TMS 3122 and TMS 3123 can be used in printers, terminals, and peripheral (IBM System 3) applications where 32, 64, or 96 bits of serial storage are needed.

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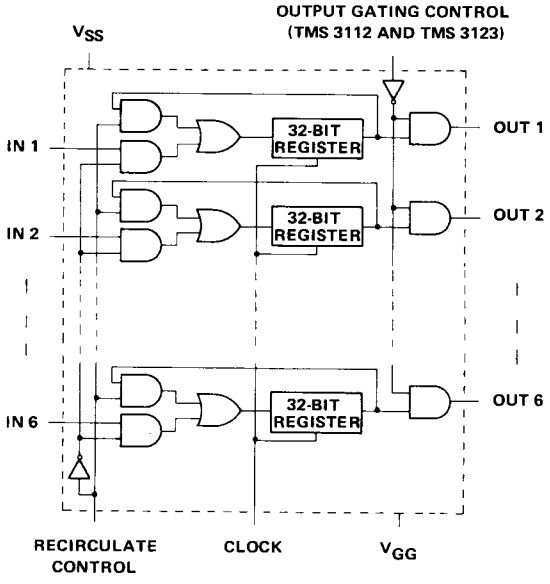
operation

Transfer of data into and out of the shift register occurs on the low-to-high transition of the clock. Input data must be set up a minimum time before the low-to-high transition and must be held for a minimum time after that transition. For long-term data storage, the clock must be maintained high, and in this mode the recirculate and data input levels may change without affecting the data output levels.

Recirculate occurs on the low-to-high clock transition with the recirculate control high. The recirculate control level must be set up a minimum time before this transition and held a minimum time after the transition. Data is entered with the recirculate control low. During recirculation, data is continuously available at the outputs when the output gate control is low. A high level on the output gate control forces all outputs low. Data inputs are inhibited during recirculation.

functional block diagram



FUNCTION TABLE

RECIRCULATE	INPUT	FUNCTION
H	L	Recirculate
H	H	Recirculate
L	L	L is written
L	H	H is written

H = high level
L = low level

NOTE: TMS 3122 does not have output gating.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)*

Supply voltage, V_{GG} (see Note 1)	−20 V to 0.3 V
Clock input voltage (see Note 1)	−20 V to 0.3 V
Data input voltage (see Note 1)	−20 V to 0.3 V
Operating free-air temperature range	−25°C to 85°C
Storage temperature range	−55°C to 150°C

NOTE 1: Under absolute maximum ratings, voltage values are with respect to the normally most-positive supply, V_{SS} (substrate). Throughout the remainder of this data sheet voltage values are with respect to a floating ground.

*Comment: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

PARAMETER	MIN	NOM	MAX	UNIT
Supply voltage, V_{GG}	−11	−12	−13	V
Supply voltage, V_{SS}	4.75	5	5.25	V
High-level input voltage, V_{IH}	V_{SS} −1.3		V_{SS}	V
High-level clock voltage, $V_{IH(\phi)}$	V_{SS} −1.3		V_{SS}	V
Low-level input voltage, V_{IL}			V_{SS} −4	V
Low-level clock voltage, $V_{IL(\phi)}$			V_{SS} −4	V
Clock pulse transition time, low-to-high-level, $t_{TLH(\phi)}$			5000	ns
Clock pulse transition time, high-to-low-level, $t_{THL(\phi)}$			5000	ns
Pulse width, clock high, $t_{w(\phi H)}$	300		∞	ns
Pulse width, clock low, $t_{w(\phi L)}$	150		50000	ns
Recirculate pulse width, $t_{w(rec)}$	250			ns
Data setup time, $t_{su(da)}$	60			ns
Recirculate setup time, $t_{su(rec)}$	120			ns
Data hold time, $t_{h(da)}$	60			ns
Recirculate hold time, $t_{h(rec)}$	100			ns
Clock frequency, f_{ϕ}	0		2	MHz
Operating free-air temperature, T_A	−25		85	°C

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electrical characteristics under nominal operating conditions, T_A = −25°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	R_L = 7.5 kΩ to V_{GG}	V_{SS} −1			V
V_{OL}	Low-level output voltage	R_L = 7.5 kΩ to V_{GG}, $I_{OL} \approx$ −1.6 mA			0.6	V
I_I	Input current (all inputs)	V_I = 0 V			−500	nA
I_{GG}	Supply current from V_{GG}	Load = 1 TTL gate (see Note 2), f = 1 MHz, T_A = 25°C		−15	−25	mA
I_{SS}	Supply current from V_{SS}	Load = 1 TTL gate (see Note 2), f = 1 MHz, T_A = 25°C		25	30	mA
P_D	Power dissipation	Load = 1 TTL gate (see Note 2), f = 1 MHz, T_A = 25°C		425	500	mW
C_i	Input capacitance, all inputs except clock	V_I = V_{SS}, f = 1 MHz		5	7	pF
$C_{i(\phi)}$	Clock input capacitance	$V_{I(\phi)}$ = V_{SS}, f = 1 MHz		6	7	pF

†All typical values are at T_A = 25°C.

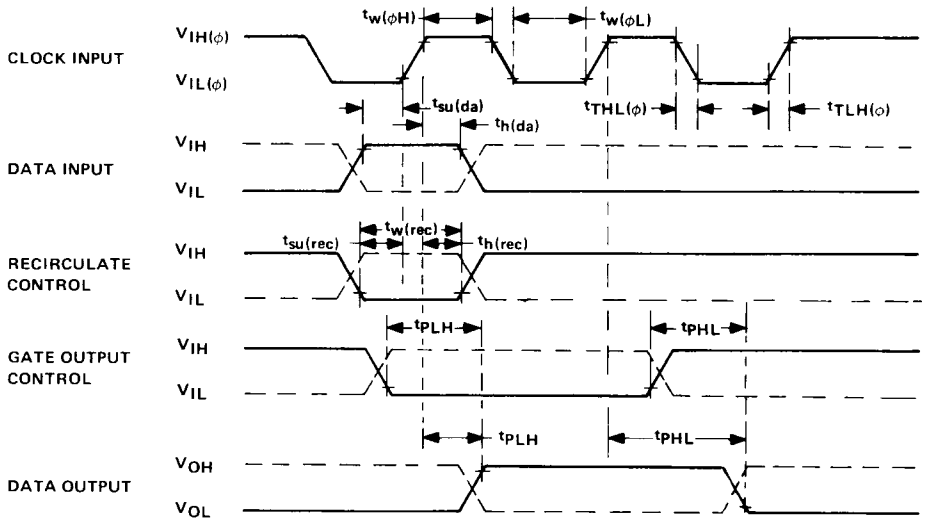
NOTE 2: For final test purposes, a worst-case TTL load is simulated by a load of 2.7 kΩ and a capacitance of 10 pF.

switching characteristics under nominal operating conditions, T_A = −25°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output from clock	R_L = 7.5 kΩ to V_{GG}, C_L = 70 pF		350	440	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock			350	440	ns
t_{PLH}	Propagation delay time, low-to-high-level output from output control	R_L = 7.5 kΩ to V_{GG}, C_L = 70 pF		180	250	ns
t_{PHL}	Propagation delay time, high-to-low-level output from output control			180	250	ns

†All typical values are at T_A = 25°C.

voltage waveforms



NOTE: Measurements are made at 90% (high) and 10% (low) timing points.

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