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TMS320C31, TMS320LC31 DIGITAL SIGNAL PROCESSORS

SPRS035B – MARCH 1996 – REVISED JANUARY 1999

- **High-Performance Floating-Point Digital Signal Processor (DSP):**
  - **TMS320C31-80 (5 V)**
    25-ns Instruction Cycle Time
    440 MOPS, 80 MFLOPS, 40 MIPS
  - **TMS320C31-60 (5 V)**
    33-ns Instruction Cycle Time
    330 MOPS, 60 MFLOPS, 30 MIPS
  - **TMS320C31-50 (5 V)**
    40-ns Instruction Cycle Time
    275 MOPS, 50 MFLOPS, 25 MIPS
  - **TMS320C31-40 (5 V)**
    50-ns Instruction Cycle Time
    220 MOPS, 40 MFLOPS, 20 MIPS
  - **TMS320LC31-40 (3.3 V)**
    50-ns Instruction Cycle Time
    220 MOPS, 40 MFLOPS, 20 MIPS
  - **TMS320LC31-33 (3.3 V)**
    60-ns Instruction Cycle Time
    183.7 MOPS, 33.3 MFLOPS, 16.7 MIPS
- **32-Bit High-Performance CPU**
- **16-/32-Bit Integer and 32-/40-Bit Floating-Point Operations**
- **32-Bit Instruction Word, 24-Bit Addresses**
- **Two 1K × 32-Bit Single-Cycle Dual-Access On-Chip RAM Blocks**
- **Boot-Program Loader**
- **On-Chip Memory-Mapped Peripherals:**
  - **One Serial Port**
  - **Two 32-Bit Timers**
  - **One-Channel Direct Memory Access (DMA) Coprocessor for Concurrent I/O and CPU Operation**
- **Fabricated Using 0.6 µm Enhanced Performance Implanted CMOS (EPIC™) Technology by Texas Instruments (TI™)**
- **132-Pin Plastic Quad Flat Package (PQ Suffix)**
- **Eight Extended-Precision Registers**
- **Two Address Generators With Eight Auxiliary Registers and Two Auxiliary Register Arithmetic Units (ARAUs)**
- **Two Low-Power Modes**
- **Two- and Three-Operand Instructions**
- **Parallel Arithmetic/Logic Unit (ALU) and Multiplier Execution in a Single Cycle**
- **Block-Repeat Capability**
- **Zero-Overhead Loops With Single-Cycle Branches**
- **Conditional Calls and Returns**
- **Interlocked Instructions for Multiprocessing Support**
- **Bus-Control Registers Configure Strobe-Control Wait-State Generation**

description

The TMS320C31 and TMS320LC31 DSPs are 32-bit, floating-point processors manufactured in 0.6 µm triple-level-metal CMOS technology. The TMS320C31 and TMS320LC31 are part of the TMS320C3x generation of DSPs from Texas Instruments.

The TMS320C3x's internal busing and special digital-signal-processing instruction set have the speed and flexibility to execute up to 80 million floating-point operations per second (MFLOPS). The TMS320C3x optimizes speed by implementing functions in hardware that other processors implement through software or microcode. This hardware-intensive approach provides performance previously unavailable on a single chip.

The TMS320C3x can perform parallel multiply and ALU operations on integer or floating-point data in a single cycle. Each processor also possesses a general-purpose register file, a program cache, dedicated ARAUs, internal dual-access memories, one DMA channel supporting concurrent I/O, and a short machine-cycle time. High performance and ease of use are results of these features.

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description (continued)

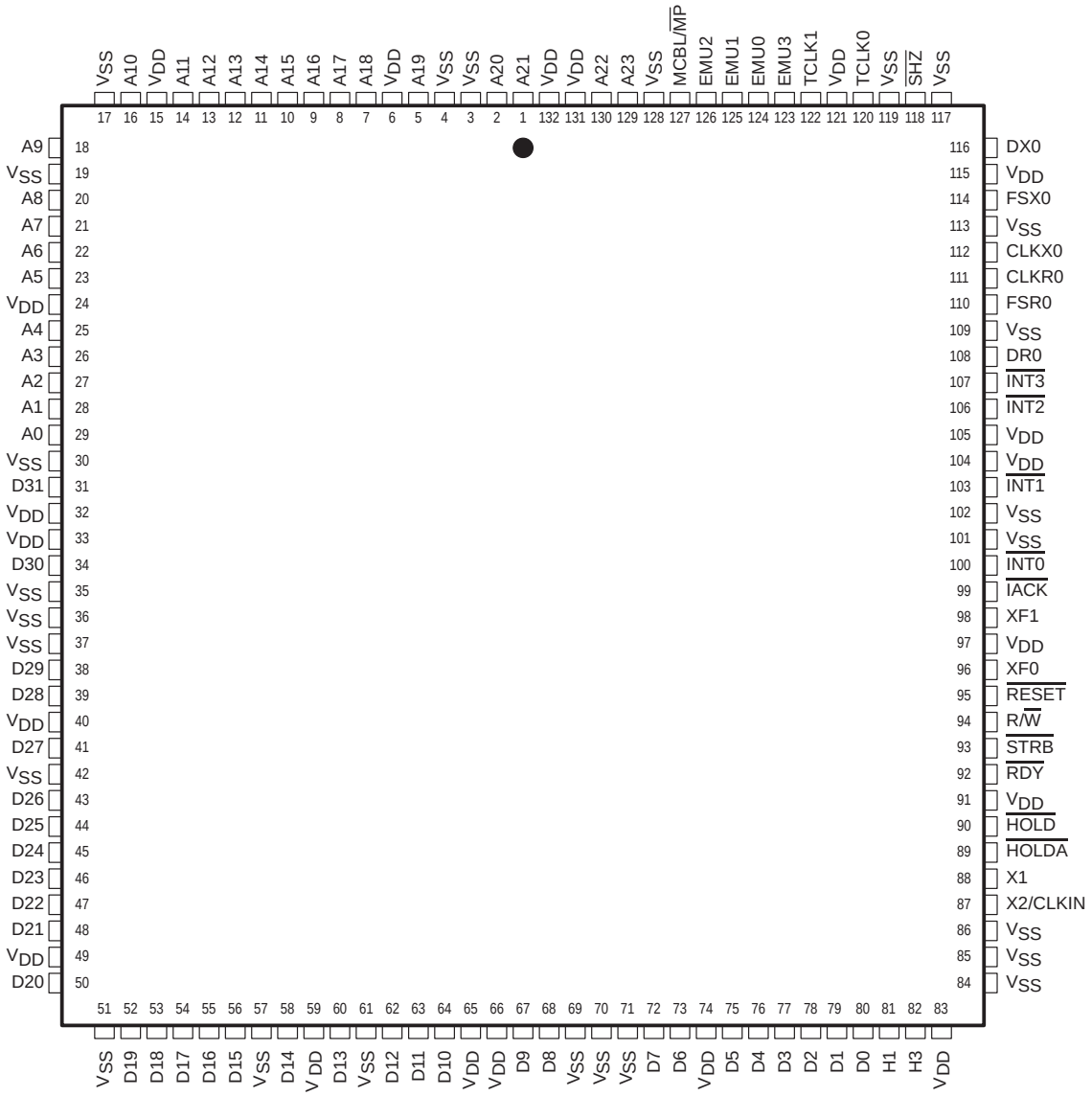
General-purpose applications are greatly enhanced by the large address space, multiprocessor interface, internally and externally generated wait states, one external interface port, two timers, one serial port, and multiple-interrupt structure. The TMS320C3x supports a wide variety of system applications from host processor to dedicated coprocessor.

High-level-language support is easily implemented through a register-based architecture, large address space, powerful addressing modes, flexible instruction set, and well-supported floating-point arithmetic.

TMS320C31 and TMS320LC31 pinout (top view)

The TMS320C31 and TMS320LC31 devices are packaged in 132-pin plastic quad flatpacks (PQ Suffix).

PQ PACKAGE
(TOP VIEW)



TMS320C31 and TMS320LC31 Terminal Assignments (Alphabetical)†

TERMINAL NAME	TERMINAL NO.	TERMINAL NAME	TERMINAL NO.	TERMINAL NAME	TERMINAL NO.	TERMINAL NAME	TERMINAL NO.	TERMINAL NAME	TERMINAL NO.
A0	29	D4	76	EMU0	124	V_{DD}	40	V_{SS}	84
A1	28	D5	75	EMU1	125	V_{DD}	49	V_{SS}	85
A2	27	D6	73	EMU2	126	V_{DD}	59	V_{SS}	86
A3	26	D7	72	EMU3	123	V_{DD}	65	V_{SS}	101
A4	25	D8	68	FSR0	110	V_{DD}	66	V_{SS}	102
A5	23	D9	67	FSX0	114	V_{DD}	74	V_{SS}	109
A6	22	D10	64	H1	81	V_{DD}	83	V_{SS}	113
A7	21	D11	63	H3	82	V_{DD}	91	V_{SS}	117
A8	20	D12	62	$\overline{HOLD}$	90	V_{DD}	97	V_{SS}	119
A9	18	D13	60	$\overline{HOLDA}$	89	V_{DD}	104	V_{SS}	128
A10	16	D14	58	$\overline{IACK}$	99	V_{DD}	105	X1	88
A11	14	D15	56	$\overline{INT0}$	100	V_{DD}	115	X2/CLKIN	87
A12	13	D16	55	$\overline{INT1}$	103	V_{DD}	121	XF0	96
A13	12	D17	54	$\overline{INT2}$	106	V_{DD}	131	XF1	98
A14	11	D18	53	$\overline{INT3}$	107	V_{DD}	132		
A15	10	D19	52	MCBL/$\overline{MP}$	127	V_{SS}	3		
A16	9	D20	50	$\overline{RDY}$	92	V_{SS}	4		
A17	8	D21	48	$\overline{RESET}$	95	V_{SS}	17		
A18	7	D22	47	R/$\overline{W}$	94	V_{SS}	19		
A19	5	D23	46	$\overline{SHZ}$	118	V_{SS}	30		
A20	2	D24	45	$\overline{STRB}$	93	V_{SS}	35		
A21	1	D25	44	TCLK0	120	V_{SS}	36		
A22	130	D26	43	TCLK1	122	V_{SS}	37		
A23	129	D27	41			V_{SS}	42		
CLKR0	111	D28	39			V_{SS}	51		
CLKX0	112	D29	38	V_{DD}	6	V_{SS}	57		
D0	80	D30	34	V_{DD}	15	V_{SS}	61		
D1	79	D31	31	V_{DD}	24	V_{SS}	69		
D2	78	DR0	108	V_{DD}	32	V_{SS}	70		
D3	77	DX0	116	V_{DD}	33	V_{SS}	71		

† V_{DD} and V_{SS} pins are on a common plane internal to the device.

TMS320C31 and TMS320LC31 Terminal Assignments (Numerical)†

TERMINAL NO.	TERMINAL NAME	TERMINAL NO.	TERMINAL NAME	TERMINAL NO.	TERMINAL NAME	TERMINAL NO.	TERMINAL NAME	TERMINAL NO.	TERMINAL NAME
1	A21	31	D31	61	V_{SS}	91	V_{DD}	121	V_{DD}
2	A20	32	V_{DD}	62	D12	92	$\overline{RDY}$	122	TCLK1
3	V_{SS}	33	V_{DD}	63	D11	93	$\overline{STRB}$	123	EMU3
4	V_{SS}	34	D30	64	D10	94	R/$\overline{W}$	124	EMU0
5	A19	35	V_{SS}	65	V_{DD}	95	$\overline{RESET}$	125	EMU1
6	V_{DD}	36	V_{SS}	66	V_{DD}	96	XF0	126	EMU2
7	A18	37	V_{SS}	67	D9	97	V_{DD}	127	MCBL/$\overline{MP}$
8	A17	38	D29	68	D8	98	XF1	128	V_{SS}
9	A16	39	D28	69	V_{SS}	99	$\overline{IACK}$	129	A23
10	A15	40	V_{DD}	70	V_{SS}	100	$\overline{INT0}$	130	A22
11	A14	41	D27	71	V_{SS}	101	V_{SS}	131	V_{DD}
12	A13	42	V_{SS}	72	D7	102	V_{SS}	132	V_{DD}
13	A12	43	D26	73	D6	103	$\overline{INT1}$		
14	A11	44	D25	74	V_{DD}	104	V_{DD}		
15	V_{DD}	45	D24	75	D5	105	V_{DD}		
16	A10	46	D23	76	D4	106	$\overline{INT2}$		
17	V_{SS}	47	D22	77	D3	107	$\overline{INT3}$		
18	A9	48	D21	78	D2	108	DR0		
19	V_{SS}	49	V_{DD}	79	D1	109	V_{SS}		
20	A8	50	D20	80	D0	110	FSR0		
21	A7	51	V_{SS}	81	H1	111	CLKR0		
22	A6	52	D19	82	H3	112	CLKX0		
23	A5	53	D18	83	V_{DD}	113	V_{SS}		
24	V_{DD}	54	D17	84	V_{SS}	114	FSX0		
25	A4	55	D16	85	V_{SS}	115	V_{DD}		
26	A3	56	D15	86	V_{SS}	116	DX0		
27	A2	57	V_{SS}	87	X2/CLKIN	117	V_{SS}		
28	A1	58	D14	88	X1	118	$\overline{SHZ}$		
29	A0	59	V_{DD}	89	$\overline{HOLDA}$	119	V_{SS}		
30	V_{SS}	60	D13	90	$\overline{HOLD}$	120	TCLK0		

† V_{DD} and V_{SS} pins are on a common plane internal to the device.

TMS320C31 and TMS320LC31 Terminal Functions

TERMINAL NAME	TERMINAL QTY	TYPE†	DESCRIPTION	CONDITIONS WHEN SIGNAL IS Z TYPE‡		
PRIMARY-BUS INTERFACE						
D31–D0	32	I/O/Z	32-bit data port	S	H	R
A23–A0	24	O/Z	24-bit address port	S	H	R
R/$\overline{W}$	1	O/Z	Read/write. R/$\overline{W}$ is high when a read is performed and low when a write is performed over the parallel interface.	S	H	R
$\overline{STRB}$	1	O/Z	External-access strobe	S	H	
$\overline{RDY}$	1	I	Ready. $\overline{RDY}$ indicates that the external device is prepared for a transaction completion.			
$\overline{HOLD}$	1	I	Hold. When $\overline{HOLD}$ is a logic low, any ongoing transaction is completed. A23–A0, D31–D0, $\overline{STRB}$, and R/$\overline{W}$ are placed in the high-impedance state and all transactions over the primary-bus interface are held until $\overline{HOLD}$ becomes a logic high or until the NOHOLD bit of the primary-bus-control register is set.			
$\overline{HOLDA}$	1	O/Z	Hold acknowledge. $\overline{HOLDA}$ is generated in response to a logic low on $\overline{HOLD}$. $\overline{HOLDA}$ indicates that A23–A0, D31–D0, $\overline{STRB}$, and R/$\overline{W}$ are in the high-impedance state and that all transactions over the bus are held. $\overline{HOLDA}$ is high in response to a logic high of $\overline{HOLD}$ or the NOHOLD bit of the primary-bus-control register is set.	S		
CONTROL SIGNALS						
$\overline{RESET}$	1	I	Reset. When $\overline{RESET}$ is a logic low, the device is in the reset condition. When $\overline{RESET}$ becomes a logic high, execution begins from the location specified by the reset vector.			
$\overline{INT3}$–$\overline{INT0}$	4	I	External interrupts			
$\overline{IACK}$	1	O/Z	Interrupt acknowledge. $\overline{IACK}$ is generated by the IACK instruction. $\overline{IACK}$ can be used to indicate the beginning or the end of an interrupt-service routine.	S		
MCBL/$\overline{MP}$	1	I	Microcomputer boot-loader/microprocessor mode-select			
$\overline{SHZ}$	1	I	Shutdown high impedance. When active, $\overline{SHZ}$ shuts down the device and places all pins in the high-impedance state. $\overline{SHZ}$ is used for board-level testing to ensure that no dual-drive conditions occur. **CAUTION:** A low on $\overline{SHZ}$ corrupts the device memory and register contents. Reset the device with $\overline{SHZ}$ high to restore it to a known operating condition.			
XF1, XF0	2	I/O/Z	External flags. XF1 and XF0 are used as general-purpose I/Os or to support interlocked processor instruction.	S		R
SERIAL PORT 0 SIGNALS						
CLKR0	1	I/O/Z	Serial port 0 receive clock. CLKR0 is the serial shift clock for the serial port 0 receiver.	S		R
CLKX0	1	I/O/Z	Serial port 0 transmit clock. CLKX0 is the serial shift clock for the serial port 0 transmitter.	S		R
DR0	1	I/O/Z	Data-receive. Serial port 0 receives serial data on DR0.	S		R
DX0	1	I/O/Z	Data-transmit output. Serial port 0 transmits serial data on DX0.	S		R
FSR0	1	I/O/Z	Frame-synchronization pulse for receive. The FSR0 pulse initiates the data-receive process using DR0.	S		R
FSX0	1	I/O/Z	Frame-synchronization pulse for transmit. The FSX0 pulse initiates the data-transmit process using DX0.	S		R
TIMER SIGNALS						
TCLK0	1	I/O/Z	Timer clock 0. As an input, TCLK0 is used by timer 0 to count external pulses. As an output, TCLK0 outputs pulses generated by timer 0.	S		R
TCLK1	1	I/O/Z	Timer clock 1. As an input, TCLK0 is used by timer 1 to count external pulses. As an output, TCLK1 outputs pulses generated by timer 1.	S		R

† I = input, O = output, Z = high-impedance state
‡ S = $\overline{SHZ}$ active, H = $\overline{HOLD}$ active, R = $\overline{RESET}$ active

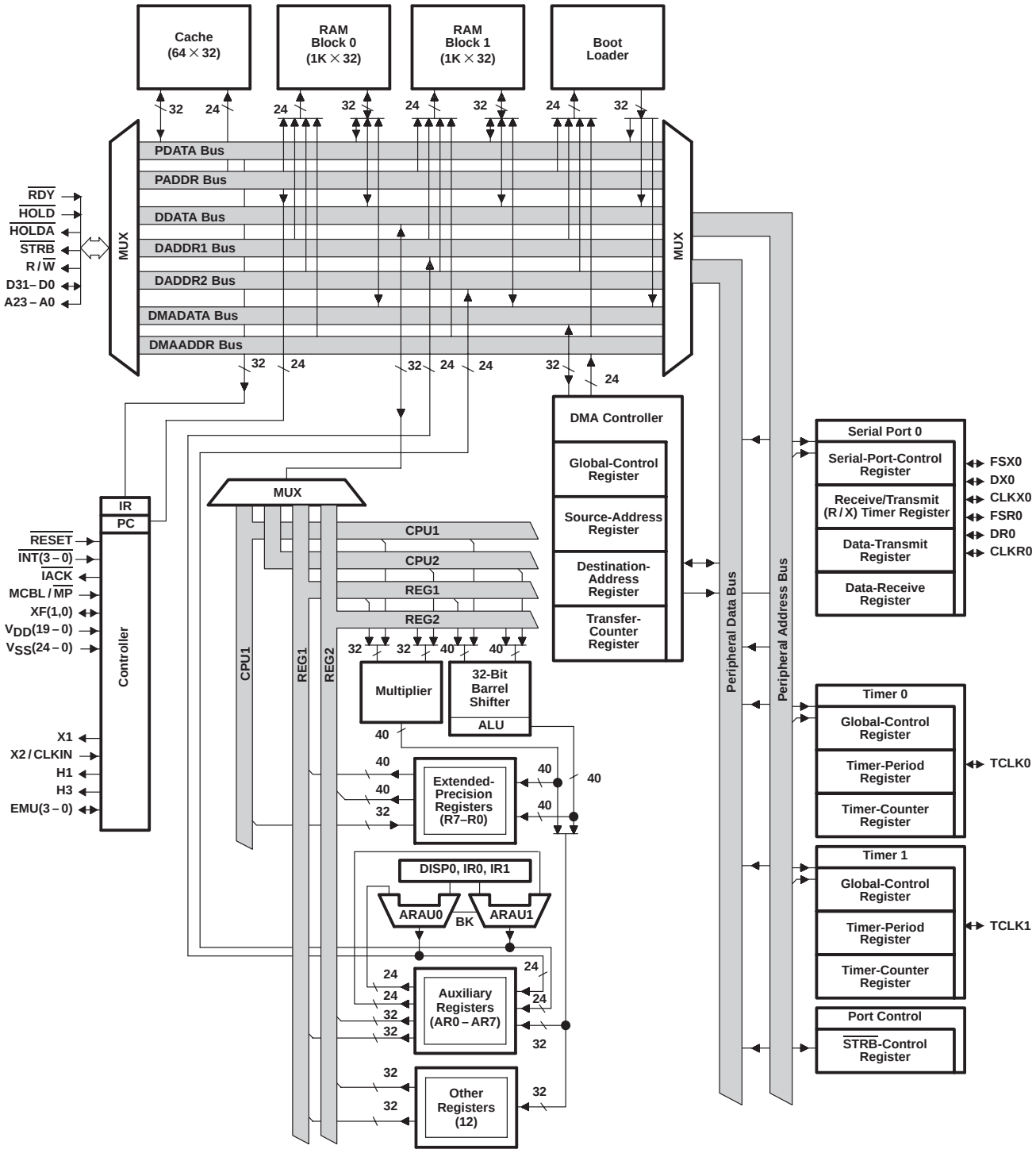
TMS320C31 and TMS320LC31 Terminal Functions (Continued)

TERMINAL NAME	TERMINAL QTY	TYPE†	DESCRIPTION	CONDITIONS WHEN SIGNAL IS Z TYPE‡
SUPPLY AND OSCILLATOR SIGNALS				
H1	1	O/Z	External H1 clock. H1 has a period equal to twice CLKIN.	S
H3	1	O/Z	External H3 clock. H3 has a period equal to twice CLKIN.	S
V_{DD}	20	I	5-V supply for ’C31 devices and 3.3-V supply for ’LC31 devices. All must be connected to a common supply plane.§	
V_{SS}	25	I	Ground. All grounds must be connected to a common ground plane.	
X1	1	O	Output from the internal-crystal oscillator. If a crystal is not used, X1 should be left unconnected.	
X2/CLKIN	1	I	Internal-oscillator input from a crystal or a clock	
RESERVED¶				
EMU2–EMU0	3	I	Reserved for emulation. Use pullup resistors to V_{DD}	
EMU3	1	O/Z	Reserved for emulation	S

† I = input, O = output, Z = high-impedance state
‡ S = $\overline{SHZ}$ active, H = $\overline{HOLD}$ active, R = $\overline{RESET}$ active
§ Recommended decoupling capacitor value is 0.1 μF.
¶ Follow the connections specified for the reserved pins. Use 18-kΩ–22-kΩ pullup resistors for best results. All V_{DD} supply pins must be connected to a common supply plane, and all ground pins must be connected to a common ground plane.

NOTES:
1. A test mode for measuring leakage currents in the TMS320C31 is implemented. This test mode powers down the clock oscillator circuit resulting in currents below 10 μA. The test mode is entered by asserting SHZ low, which tri–states all output pins and then holds both H1 and H3 at logic high. The test mode is not intended for application use because it does not preserve the processor state.
2. Since SHZ is a synchronized input and the clock is disabled, exiting the test mode occurs only when at least one of the H1/H3 pins is pulled low. Reset cannot be used to wake up in test mode since the SHZ pin is sampled and the clocks are not running.
3. On power up, the processor can be in an indeterminate state. If the state is SHZ mode and H1 and H3 are both held logic high by pull–ups, then shutdown will occur. Normally, if H1 and H3 do not have pull–ups, the rise time lag due to capacitive loading on a tri–state pin is enough to ensure a clean start. However, a slowly rising supply and board leakages to V_{CC} may be enough to cause a bad start. Therefore, a pulldown resistor on either H1 or H3 is recommended for proper wakeup.

functional block diagram



memory map

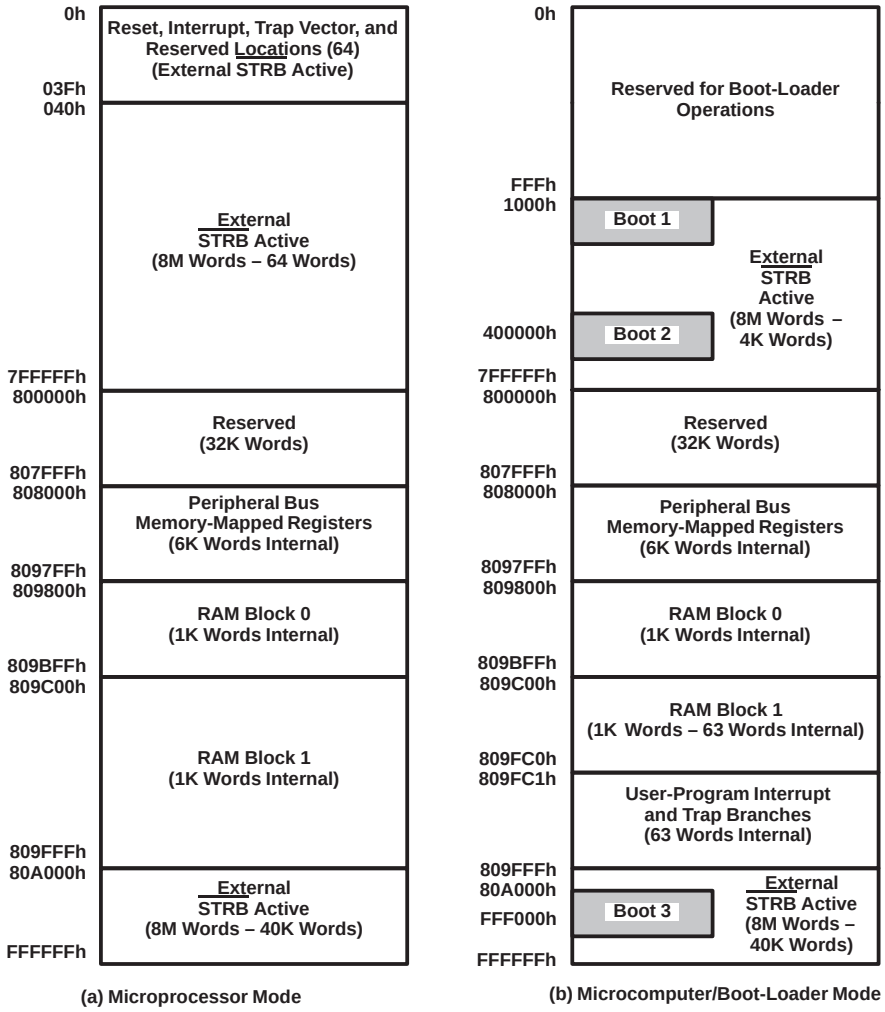


Figure 1. TMS320C31 Memory Maps

memory map (continued)

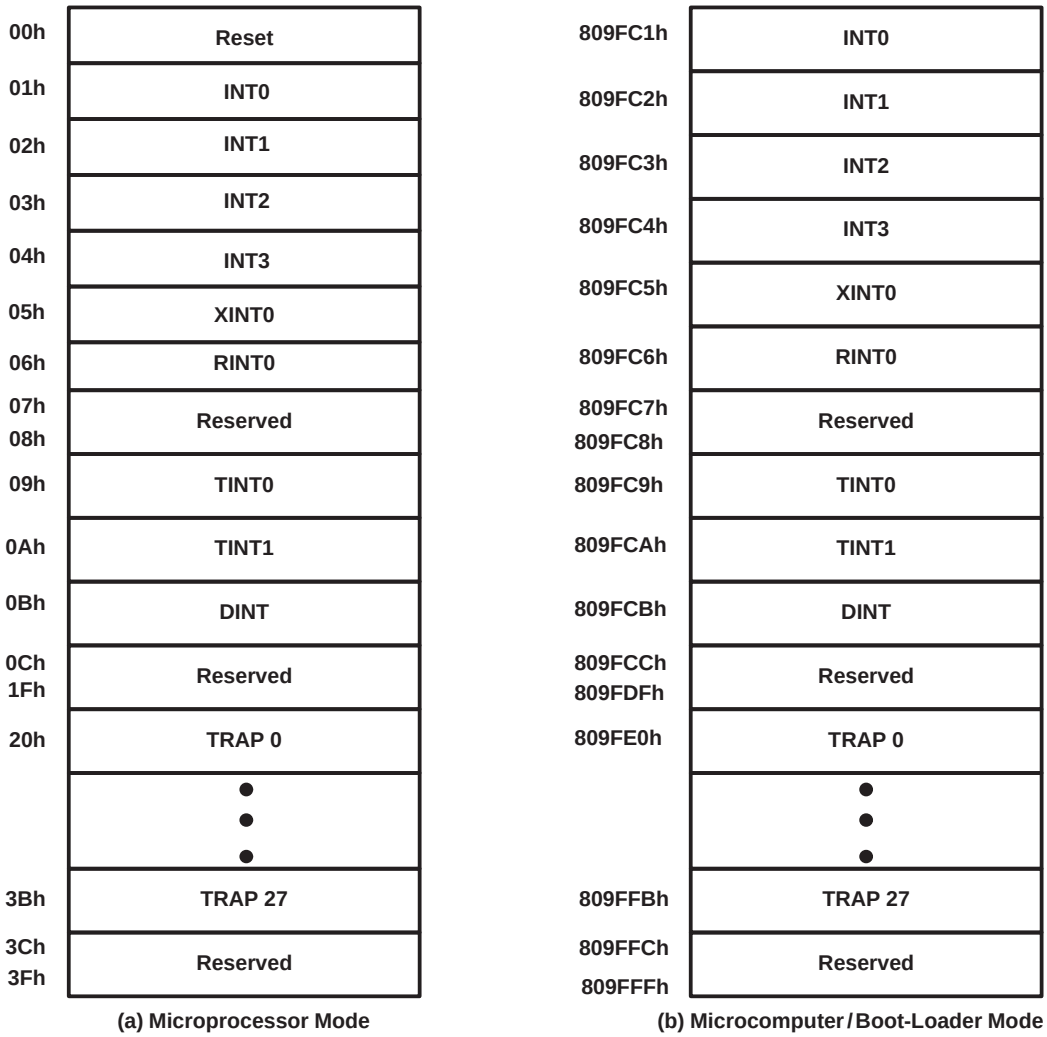


Figure 2. Reset, Interrupt, and Trap Vector/Branches Memory-Map Locations

memory map (continued)

808000h	DMA Global Control
808004h	DMA Source Address
808006h	DMA Destination Address
808008h	DMA Transfer Counter
808020h	Timer 0 Global Control
808024h	Timer 0 Counter
808028h	Timer 0 Period Register
808030h	Timer 1 Global Control
808034h	Timer 1 Counter
808038h	Timer 1 Period Register
808040h	Serial Global Control
808042h	FSX/DX/CLKX Serial Port Control
808043h	FSR/DR/CLKR Serial Port Control
808044h	Serial R/X Timer Control
808045h	Serial R/X Timer Counter
808046h	Serial R/X Timer Period Register
808048h	Data-Transmit
80804Ch	Data-Receive
808064h	Primary-Bus Control

†Shading denotes reserved address locations

Figure 3. Peripheral Bus Memory-Mapped Registers†

absolute maximum ratings over specified temperature range (unless otherwise noted)†

		'C31	'LC31
Supply voltage range, V_{DD} (see Note 1)		–0.3 V to 7 V	–0.3 V to 5 V
Input voltage range, V_I		–0.3 V to 7 V	–0.3 V to 5 V
Output voltage range, V_O		–0.3 V to 7 V	–0.3 V to 5 V
Continuous power dissipation (worst case) (see Note 5)		2.6 W (for TMS320C31-80)	850 mW (for TMS320LC31-33)
Operating case temperature range, T_C	PQL (commercial)	0°C to 85°C	0°C to 85°C
	PQA (industrial)	– 40°C to 125°C	
Storage temperature range, T_{stg}		– 55°C to 150°C	– 55°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 4. All voltage values are with respect to V_{SS}.

5. Actual operating power is less. This value was obtained under specially produced worst-case test conditions for the TMS320C31, which are not sustained during normal device operation. These conditions consist of continuous parallel writes of a checkerboard pattern to both primary and extension buses at the maximum rate possible. See normal (I_{CC}) current specification in the electrical characteristics table and also read *Calculation of TMS320C30 Power Dissipation Application Report* (literature number SPRA020).

recommended operating conditions (see Note 6)

		'C31			'LC31			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{DD}	Supply voltage (DV_{DD}, etc.)	4.75	5	5.25	3.13	3.3	3.47	V
V_{SS}	Supply voltage (CV_{SS}, etc.)		0			0		V
V_{IH}	High-level input voltage	2		V_{DD} + 0.3‡	1.8		V_{DD} + 0.3‡	V
V_{IL}	Low-level input voltage	– 0.3‡		0.8	– 0.3‡		0.6	V
I_{OH}	High-level output current			– 300			– 300	μA
I_{OL}	Low-level output current			2			2	mA
T_C	Operating case temperature (commercial)	0		85	0		85	°C
	Operating case temperature (industrial)	– 40		125				°C
V_{TH}	High-level input voltage for CLKIN	2.6		V_{DD} + 0.3‡	2.5		V_{DD} + 0.3‡	V

‡ These values are derived from characterization and not tested.

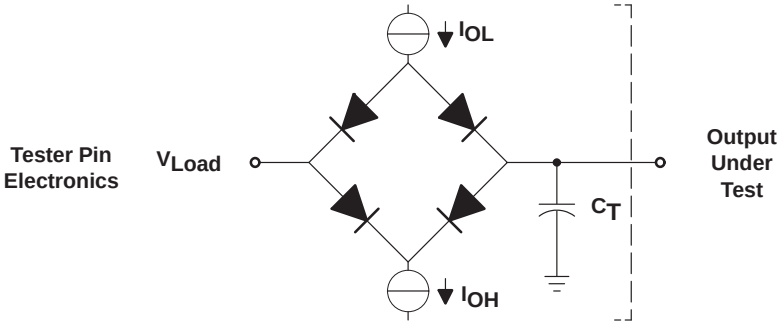
NOTE 6: All voltage values are with respect to V_{SS}. All input and output voltage levels are TTL-compatible. CLKIN can be driven by a CMOS clock.

electrical characteristics over recommended ranges of supply voltage (unless otherwise noted) (see Note 3)†

PARAMETER		TEST CONDITIONS				'C31			'LC31			UNIT
						MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{OH}	High-level output voltage	V_{DD} = MIN, I_{OH} = MAX				2.4	3		2			V
V_{OL}	Low-level output voltage	V_{DD} = MIN, I_{OH} = MAX					0.3	0.6			0.4	V
I_Z	High-impedance current	V_{DD} = MAX				– 20		+ 20	– 20		+ 20	µA
I_I	Input current	$V_I = V_{SS}$ to V_{DD}				– 10		+ 10	– 10		+ 10	µA
I_{IP}	Input current (with internal pullup)	Inputs with internal pullups§				– 600		20	– 600		10	µA
I_{CC}	Supply current¶#	T_A = 25°C, V_{DD} = MAX	f_X = 33 MHz	'LC31-33			150	325		120	250	mA
			f_X = 33 MHz	'C31-33 (ext. temp)			150	325				
			f_X = 40 MHz	'C31-40			160	390		150	300	
			f_X = 50 MHz	'C31-50			200	425				
			f_X = 60 MHz	'C31-60			225	475				
			f_X = 80 MHz	'C31-80			275	550				
I_{DD}	Supply current	Standby, IDLE2 Clocks shut off					50			20		µA
C_i	Input capacitance	All inputs except CLKIN						15‖			15‖	pF
		CLKIN						25			25	
C_o	Output capacitance							20‖			20‖	pF

† All input and output voltage levels are TTL compatible.
‡ For 'C31, all typical values are at V_{DD} = 5 V, T_A (air temperature) = 25°C. For 'LC31, all typical values are at V_{DD} = 3.3 V, T_A (air temperature) = 25°C.
§ Pins with internal pullup devices: $\overline{INT3}$ – $\overline{INT0}$, MCBL / $\overline{MP}$.
¶ Actual operating current is less than this maximum value. This value was obtained under specially produced worst-case test conditions, which are not sustained during normal device operation. These conditions consist of continuous parallel writes of a checkerboard pattern at the maximum rate possible. See *Calculation of TMS320C30 Power Dissipation Application Report* (literature number SPRA020).
# f_X is the input clock frequency.
‖ Specified by design but not tested
NOTE 6: All voltage values are with respect to V_{SS}. All input and output voltage levels are TTL-compatible. CLKIN can be driven by a CMOS clock.

PARAMETER MEASUREMENT INFORMATION



Where: I_{OL} = 2 mA (all outputs)
I_{OH} = 300 µA (all outputs)
V_{LOAD} = 2.15 V
C_T = 80-pF typical load-circuit capacitance

Figure 4. TMS320C31 Test Load Circuit

signal transition levels for ’C31 (see Figure 5 and Figure 6)

TTL-level outputs are driven to a minimum logic-high level of 2.4 V and to a maximum logic-low level of 0.6 V. Output transition times are specified as follows:

- For a high-to-low transition on a TTL-compatible output signal, the level at which the output is said to be no longer high is 2 V and the level at which the output is said to be low is 1 V.
- For a low-to-high transition, the level at which the output is said to be no longer low is 1 V and the level at which the output is said to be high is 2 V.

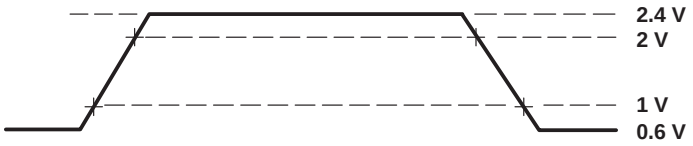


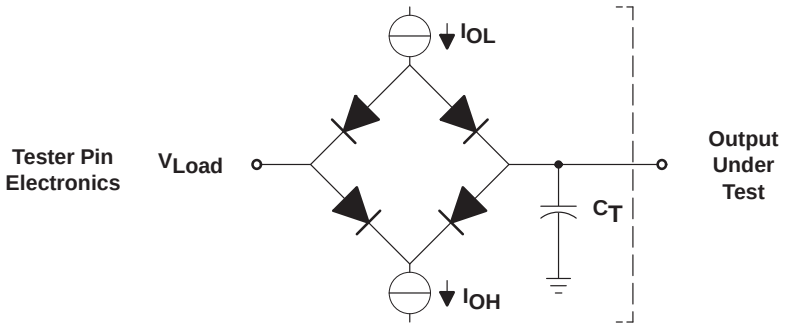
Figure 5. TTL-Level Outputs

Transition times for TTL-compatible inputs are specified as follows:

- For a high-to-low transition on an input signal, the level at which the input is said to be no longer high is 2 V and the level at which the input is said to be low is 0.8 V.
- For a low-to-high transition on an input signal, the level at which the input is said to be no longer low is 0.8 V and the level at which the input is said to be high is 2 V.

Figure 6. TTL-Level Inputs

PARAMETER MEASUREMENT INFORMATION



Where: I_{OL} = 2 mA (all outputs)
I_{OH} = 300 µA (all outputs)
V_{LOAD} = 2.15 V
C_T = 80-pF typical load-circuit capacitance

Figure 7. TMS320LC31 Test Load Circuit

signal transition levels for ’LC31 (see Figure 8 and Figure 9)

Outputs are driven to a minimum logic-high level of 2 V and to a maximum logic-low level of 0.4 V. Output transition times are specified as follows:

- For a high-to-low transition on an output signal, the level at which the output is said to be no longer high is 2 V and the level at which the output is said to be low is 1 V.
- For a low-to-high transition, the level at which the output is said to be no longer low is 1 V and the level at which the output is said to be high is 2 V.

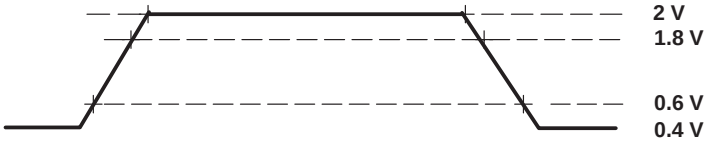


Figure 8. ’LC31 Output Levels

Transition times for inputs are specified as follows:

- For a high-to-low transition on an input signal, the level at which the input is said to be no longer high is 1.8 V and the level at which the input is said to be low is 0.6 V.
- For a low-to-high transition on an input signal, the level at which the input is said to be no longer low is 0.6 V and the level at which the input is said to be high is 1.8 V.

Figure 9. ’LC31 Input Levels

PARAMETER MEASUREMENT INFORMATION

timing parameter symbology

Timing parameter symbols used herein were created in accordance with JEDEC Standard 100-A. In order to shorten the symbols, some of the pin names and other related terminology have been abbreviated as follows, unless otherwise noted:

A	A23 – A0	H	H1 and H3
ASYNCH	Asynchronous reset signals	HOLD	$\overline{\text{HOLD}}$
C	CLKX0	HOLDA	$\overline{\text{HOLDA}}$
CI	CLKIN	IACK	$\overline{\text{IACK}}$
CLKR	CLKR0	INT	$\overline{\text{INT3}}$ – $\overline{\text{INT0}}$
CONTROL	Control signals	RDY	$\overline{\text{RDY}}$
D	D31 – D0	RW	R / $\overline{\text{W}}$
DR	DR	RESET	$\overline{\text{RESET}}$
DX	DX	S	$\overline{\text{STRB}}$
FS	FSX/R	SCK	CLKX/R
FSX	FSX0	SHZ	$\overline{\text{SHZ}}$
FSR	FSR0	TCLK	TCLK0, TCLK1, or TCLKx
GPI	General-purpose input	XF	XF0, XF1, or XFx
GPIO	General-purpose input/output; peripheral pin	XFIO	XFx switching from input to output
GPO	General-purpose output		

timing

Timing specifications apply to the TMS320C31 and TMS320LC31.

X2/CLKIN, H1, and H3 timing

The following table defines the timing parameters for the X2/CLKIN, H1, and H3 interface signals. The numbers shown in Figure 10 and Figure 11 correspond with those in the NO. column of the table below.

timing parameters for X2/CLKIN, H1, H3 (see Figure 10 and Figure 11)

NO.			’LC31		’C31-40 ’LC31-40		’C31-50		’C31-60		’C31-80		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
1	$t_{f(CI)}$	Fall time, CLKIN		5†		5†		5†		4†		4†	ns
2	$t_{w(CIL)}$	Pulse duration, CLKIN low $t_{c(CI)}$ = min	10		9		7		6		5		ns
3	$t_{w(CIH)}$	Pulse duration, CLKIN high $t_{c(CI)}$ = min	10		9		7		6		5		ns
4	$t_{r(CI)}$	Rise time, CLKIN		5†		5†		5†		4†		4†	ns
5	$t_{c(CI)}$	Cycle time, CLKIN	30	303	25	303	20	303	16.67	303	12.5	303	ns
6	$t_{f(H)}$	Fall time, H1 and H3		3		3		3		3		3	ns
7	$t_{w(HL)}$	Pulse duration, H1 and H3 low	P–6‡		P–5‡		P–5‡		P–4‡		P–3‡		ns
8	$t_{w(HH)}$	Pulse duration, H1 and H3 high	P–7‡		P–6‡		P–6‡		P–5‡		P–4‡		ns
9	$t_{r(H)}$	Rise time, H1 and H3		4		3		3		3		3	ns
10	$t_{d(HL-HH)}$	Delay time. from H1 low to H3 high or from H3 low to H1 high	0	5	0	4	0	4	0	4	0	3	ns
11	$t_{c(H)}$	Cycle time, H1 and H3	60	606	50	606	40	606	33.3	606	25	606	ns

† Specified by design but not tested
‡ P = $t_{c(CI)}$

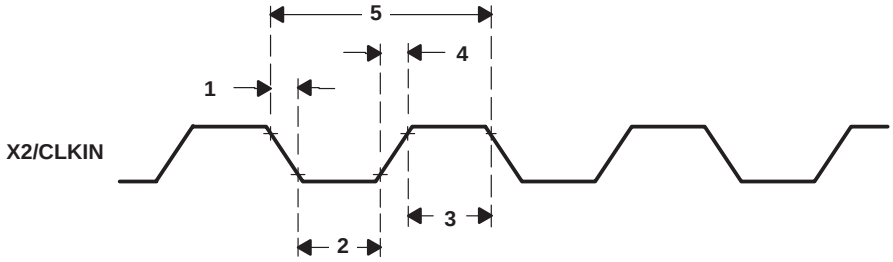


Figure 10. Timing for X2/CLKIN

X2/CLKIN, H1, and H3 timing (continued)

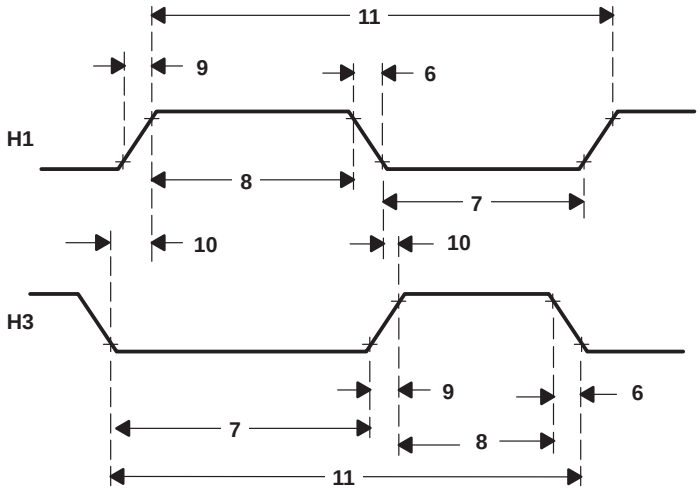


Figure 11. Timing for H1 and H3

memory read/write timing

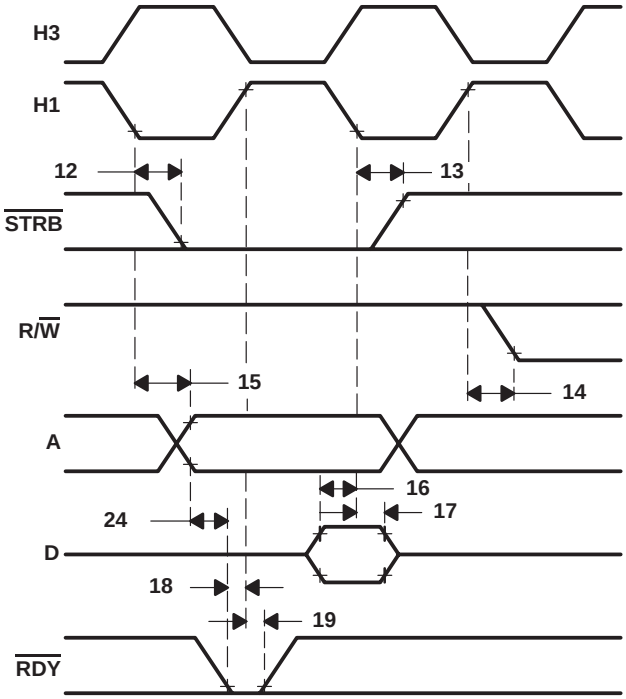
The following table defines memory read/write timing parameters for $\overline{STRB}$. The numbers shown in Figure 12 and Figure 13 correspond with those in the NO. column of the table below.

timing parameters for memory ($\overline{STRB}$ = 0) read/write (see Figure 12 and Figure 13)†

NO.			’LC31-33		’C31-40 ’LC31-40		’C31-50		’C31-60		’C31-80		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
12	$t_{d(H1L-SL)}$	Delay time, H1 low to $\overline{STRB}$ low	0‡	10	0‡	6	0‡	5	0‡	5	0‡	5	ns
13	$t_{d(H1L-SH)}$	Delay time, H1 low to $\overline{STRB}$ high	0‡	10	0‡	6	0‡	5	0‡	5	0‡	5	ns
14	$t_{d(H1H-RWL)R}$	Delay time, H1 high to R/$\overline{W}$ low (read)	0‡	10	0‡	9	0‡	7	0‡	6	0‡	4	ns
15	$t_{d(H1L-A)}$	Delay time, H1 low to A valid	0‡	14	0‡	11	0‡	9	0‡	8	0‡	7	ns
16	$t_{su(D-H1L)R}$	Setup time, D before H1 low (read)	16		14		10		9		8		ns
17	$t_{h(H1L-D)R}$	Hold time, D after H1 low (read)	0		0		0		0		0		ns
18	$t_{su(RDY-H1H)}$	Setup time, $\overline{RDY}$ before H1 high	8		8		6		5		4		ns
19	$t_{h(H1H-RDY)}$	Hold time, $\overline{RDY}$ after H1 high	0		0		0		0		0		ns
20	$t_{d(H1H-RWH)W}$	Delay time, H1 high to R/$\overline{W}$ high (write)		10		9		7		6		4	ns
21	$t_{v(H1L-D)W}$	Valid time, D after H1 low (write)		20		17		14		12		8	ns
22	$t_{h(H1H-D)W}$	Hold time, D after H1 high (write)	0		0		0		0		0		ns
23	$t_{d(H1H-A)W}$	Delay time, H1 high to A valid on back-to-back write cycles (write)		18		15		12		10		8	ns
24	$t_{d(A-RDY)}$	Delay time, $\overline{RDY}$ from A valid		8‡		7‡		6‡		6‡		P - 8§	ns
24A	T_{aa}	Address valid to data valid (read)		30		25		21		16		10	ns

† See Figure 14 for address bus timing variation with load capacitance greater than typical load-circuit capacitance (C_T = 80 pF).
‡ This value is characterized but not tested
§ In earlier data sheets, this parameter was shown as an “at speed” value. It is in fact a synchronized signal and therefore relative to $T_{c(H)}$ where $P = t_{c(C1)} = t_{c(H)}/2$.

memory read/write timing (continued)



NOTE A: $\overline{\text{STRB}}$ remains low during back-to-back read operations.

Figure 12. Timing for Memory ($\overline{\text{STRB}}$ = 0) Read

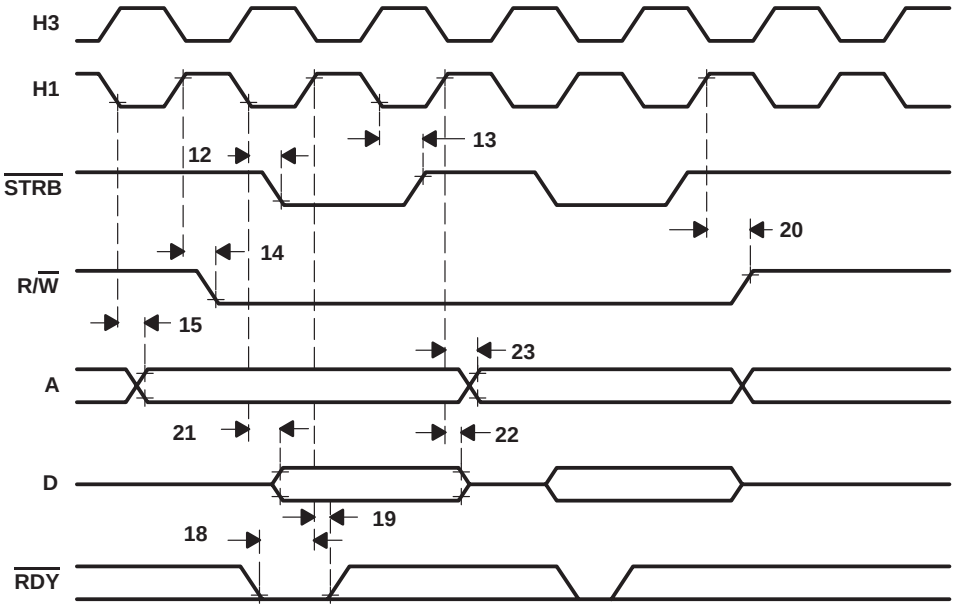
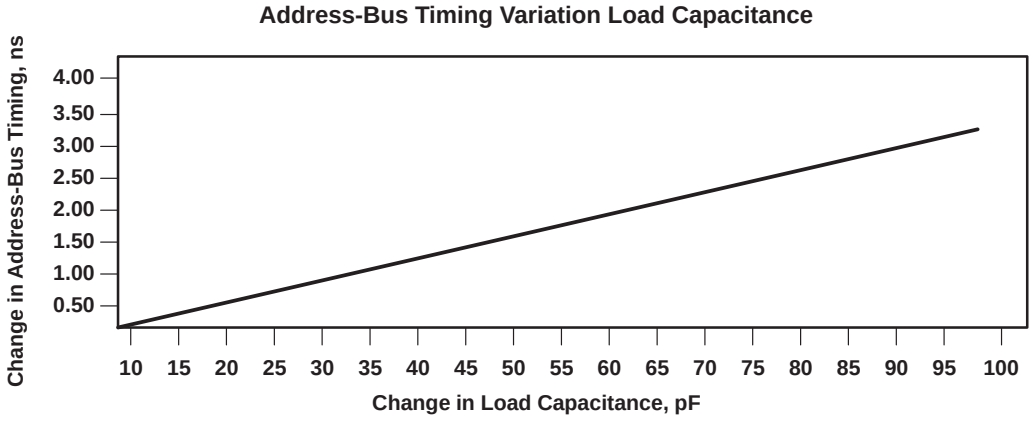


Figure 13. Timing for Memory ($\overline{\text{STRB}}$ = 0) Write

memory read/write timing (continued)



NOTE A: 30 pF/ns slope

Figure 14. Address-Bus Timing Variation With Load Capacitance (see Note A)

XF0 and XF1 timing when executing LDFI or LDII

The following tables define the timing parameters for XF0 and XF1 during execution of LDFI or LDII. The numbers shown in Figure 15 correspond with those in the NO. column of the tables below.

timing parameters for XF0 and XF1 when executing LDFI or LDII for TMS320C31 (see Figure 15)

NO.			'LC31-33		'C31-40 'LC31-40		'C31-50		'C31-60		'C31-80		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
25	$t_{d(H3H-XF0L)}$	Delay time, H3 high to XF0 low		15		13		12		11		8	ns
26	$t_{su(XF1-H1L)}$	Setup time, XF1 before H1 low	10		9		9		8		6		ns
27	$t_{h(H1L-XF1)}$	Hold time, XF1 after H1 low	0		0		0		0		0		ns

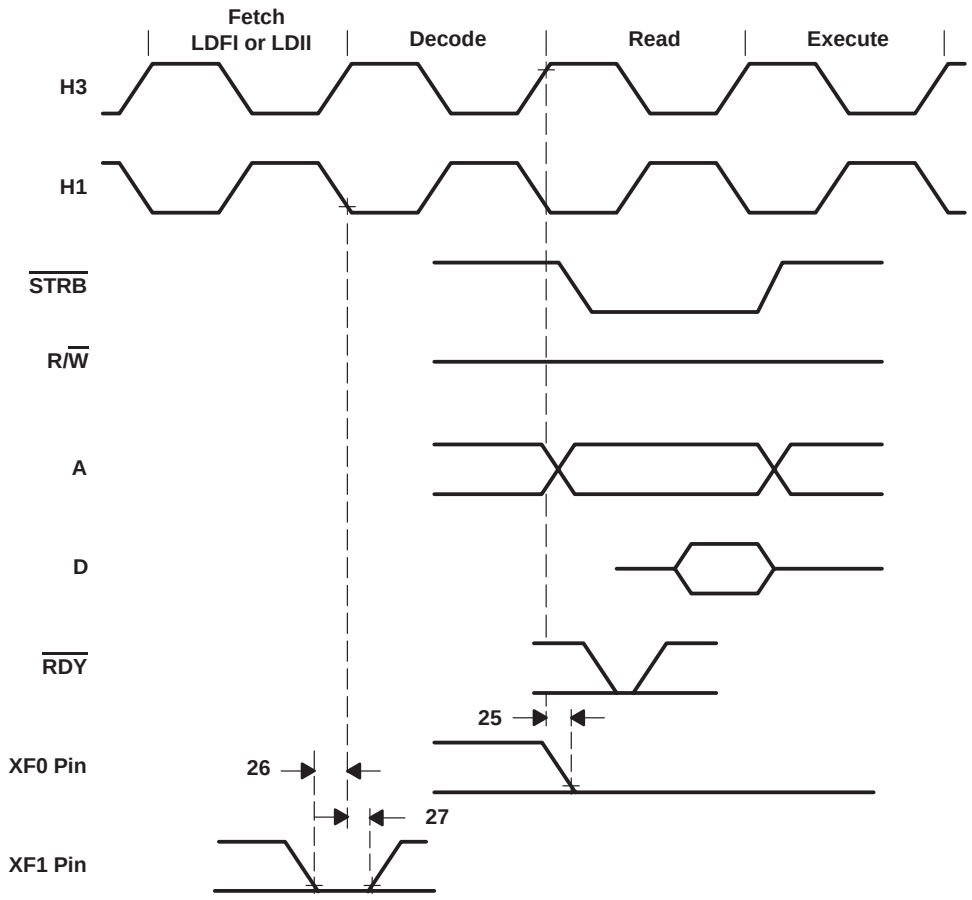


Figure 15. Timing for XF0 and XF1 When Executing LDFI or LDII

XF0 timing when executing STFI and STII†

The following table defines the timing parameters for the XF0 pin during execution of STFI or STII. The number shown in Figure 16 corresponds with the number in the NO. column of the table below.

timing parameters for XF0 when executing STFI or STII (see Figure 16)

NO.			'LC31-33		'C31-40 'LC31-40		'C31-50		'C31-60		'C31-80		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
28	$t_{d(H3H-XF0H)}$	Delay time, H3 high to XF0 high		15		13		12		11		8	ns

† XF0 is always set high at the beginning of the execute phase of the interlock-store instruction. When no pipeline conflicts occur, the address of the store is also driven at the beginning of the execute phase of the interlock-store instruction. However, if a pipeline conflict prevents the store from executing, the address of the store will not be driven until the store can execute.

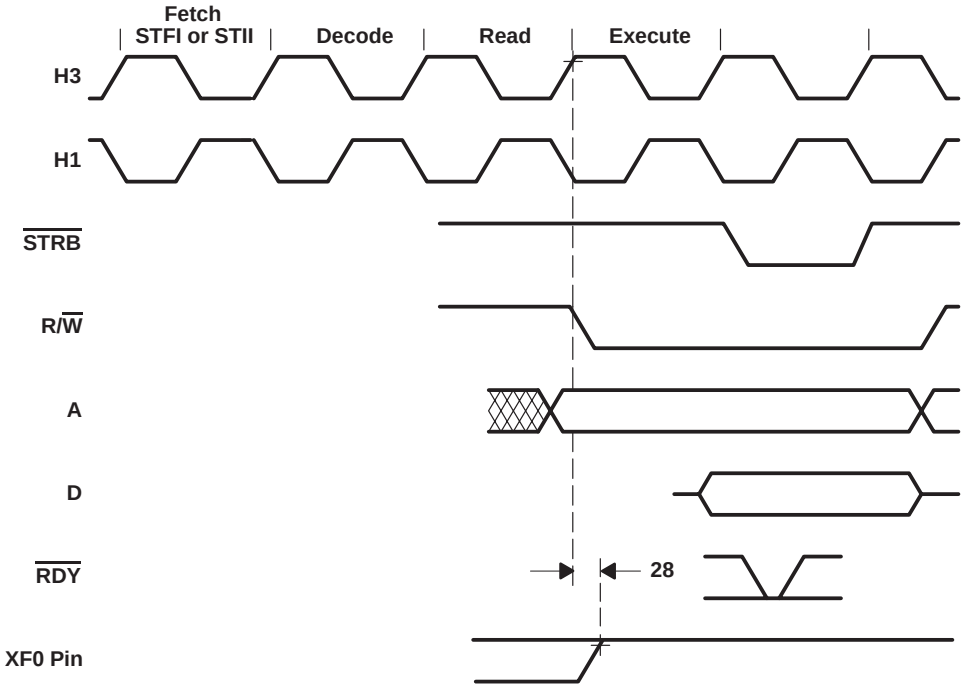


Figure 16. Timing for XF0 When Executing an STFI or STII

XF0 and XF1 timing when executing SIGI

The following tables define the timing parameters for the XF0 and XF1 pins during execution of SIGI. The numbers shown in Figure 17 correspond with those in the NO. column of the tables below.

timing parameters for XF0 and XF1 when executing SIGI for TMS320C31 (see Figure 17)

NO.			’LC31-33		’C31-40 ’LC31-40		’C31-50		’C31-60		’C31-80		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
29	$t_{d(H3H-XF0L)}$	Delay time, H3 high to XF0 low		15		13		12		11		8	ns
30	$t_{d(H3H-XF0H)}$	Delay time, H3 high to XF0 high		15		13		12		11		8	ns
31	$t_{su(XF1-H1L)}$	Setup time, XF1 before H1 low	10		9		9		8		6		ns
32	$t_{h(H1L-XF1)}$	Hold time, XF1 after H1 low	0		0		0		0		0		ns

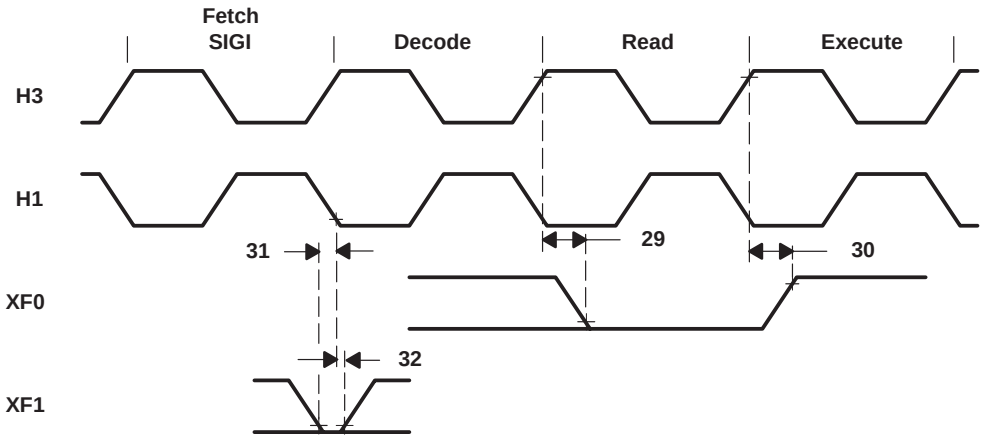


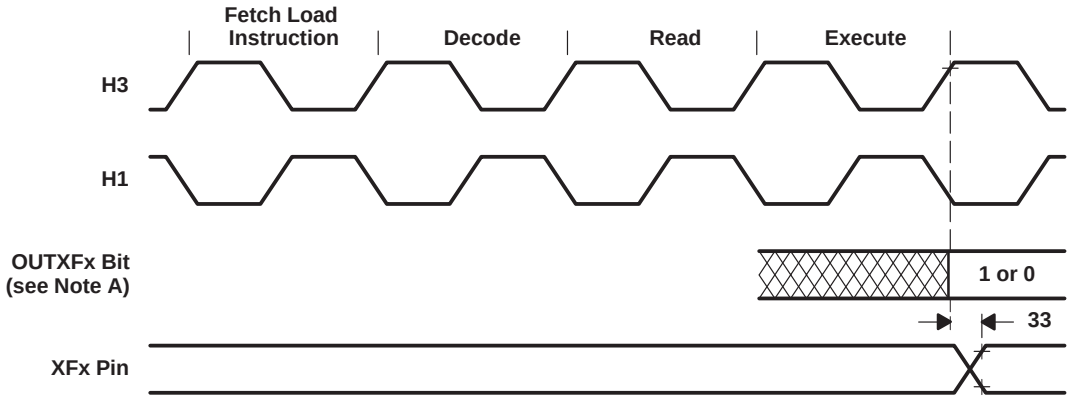
Figure 17. Timing for XF0 and XF1 When Executing SIGI

loading when XF is configured as an output

The following table defines the timing parameter for loading the XF register when the XFx pin is configured as an output. The number shown in Figure 18 corresponds with the number in the NO. column of the table below.

timing parameters for loading the XF register when configured as an output pin (see Figure 18)

NO.			'LC31-33		'C31-40 'LC31-40		'C31-50		'C31-60		'C31-80		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
33	$t_{v(H3H-XF)}$	Valid time, H3 high to XFx		15		13		12		11		8	ns



NOTE A: OUTXFx represents either bit 2 or 6 of the IOF register.

Figure 18. Timing for Loading XF Register When Configured as an Output Pin

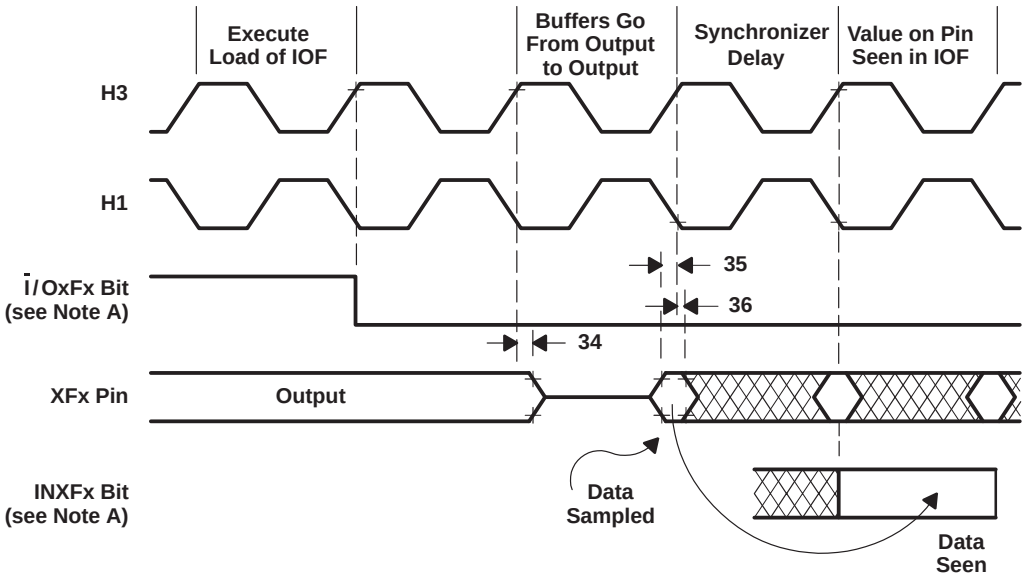
changing XFx from an output to an input

The following table defines the timing parameters for changing the XFx pin from an output pin to an input pin. The numbers shown in Figure 19 correspond with those in the NO. column of the table below.

timing parameters of XFx changing from output to input mode for TMS320C31 (see Figure 19)

NO.			'LC31-33		'C31-40 'LC31-40		'C31-50		'C31-60		'C31-80		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
34	$t_{h(H3H-XF)}$	Hold time, XFx after H3 high		15†		13†		12†		11†		9†	ns
35	$t_{su(XF-H1L)}$	Setup time, XFx before H1 low	10		9		9		8		6		ns
36	$t_{h(H1L-XF)}$	Hold time, XFx after H1 low	0		0		0		0		0		ns

† This value is characterized but not tested.



NOTE A: Ī/OxFx represents either bit 1 or bit 5 of the IOF register, and INXFx represents either bit 3 or bit 7 of the IOF register.

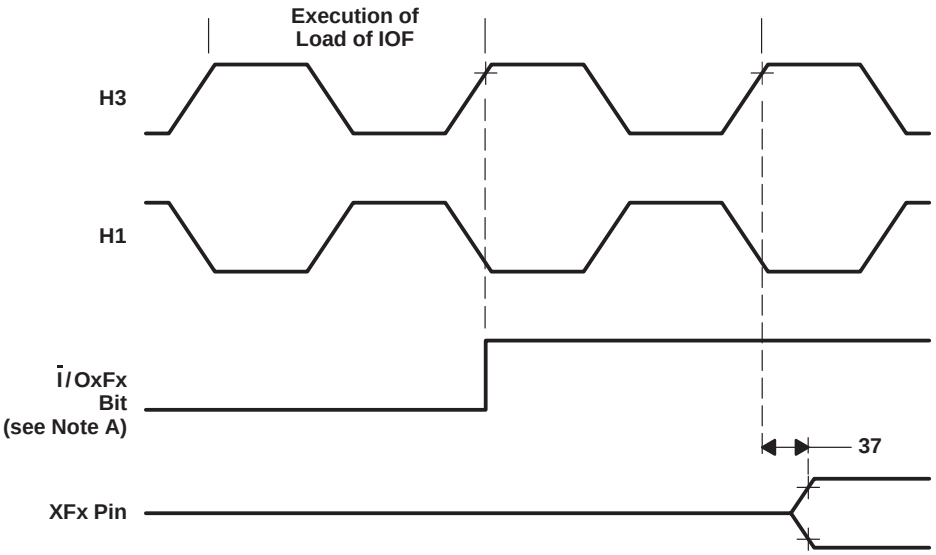
Figure 19. Timing for Change of XFx From Output to Input Mode

changing XFx from an input to an output

The following table defines the timing parameter for changing the XFx pin from an input pin to an output pin. The number shown in Figure 20 corresponds with the number in the NO. column of the table below.

timing parameters of XFx changing from input to output mode (see Figure 20)

NO.			'LC31-33		'C31-40 'LC31-40		'C31-50		'C31-60		'C31-80		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
37	$t_{d(H3H-XFIO)}$	Delay time, H3 high to XFx switching from input to output		20		17		17		16		9	ns



NOTE A: Ī/OxFx represents either bit 1 or bit 5 of the IOF register.

Figure 20. Timing for Change of XFx From Input to Output Mode

reset timing

$\overline{\text{RESET}}$ is an asynchronous input that can be asserted at any time during a clock cycle. If the specified timings are met, the exact sequence shown in Figure 21 occurs; otherwise, an additional delay of one clock cycle is possible.

The asynchronous reset signals include XF0/1, CLKX0, DX0, FSX0, CLKR0, DR0, FSR0, and TCLK0/1.

The following table defines the timing parameters for the $\overline{\text{RESET}}$ signal. The numbers shown in Figure 21 correspond with those in the NO. column of the following table.

Resetting the device initializes the bus control register to seven software wait states and therefore results in slow external accesses until these registers are initialized.

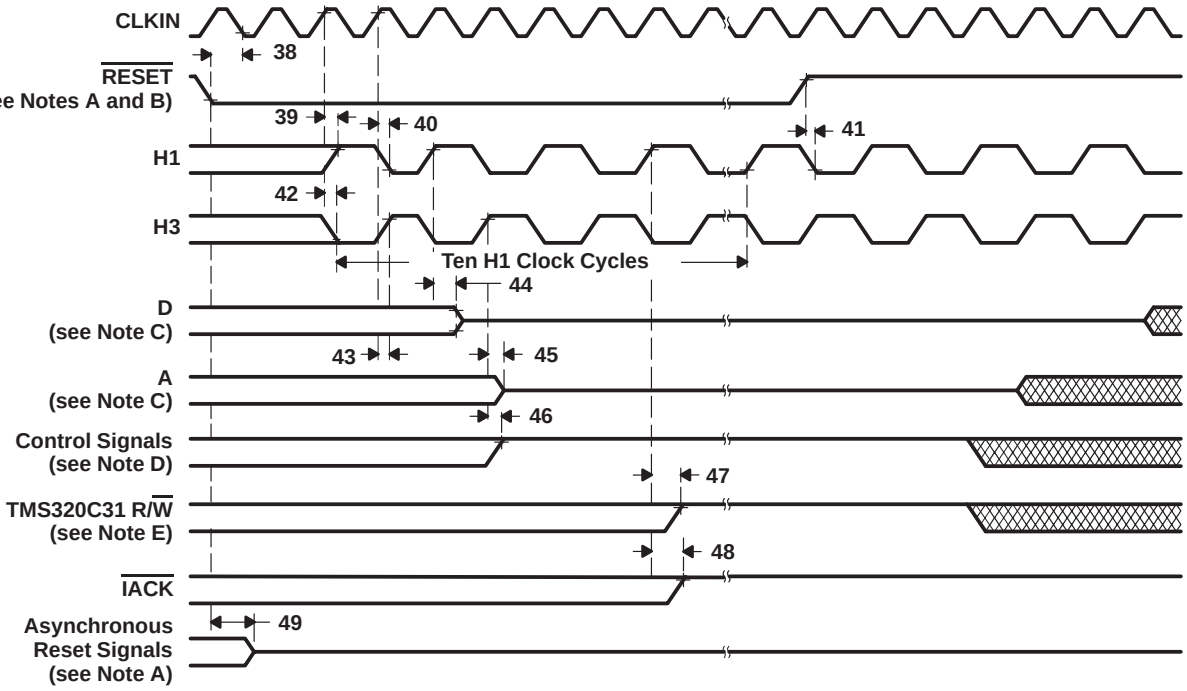
$\overline{\text{HOLD}}$ is an asynchronous input and can be asserted during reset.

timing parameters for $\overline{\text{RESET}}$ for the TMS320C31 and TMS320LC31 (see Figure 21)

NO.			'LC31-33		'C31-40 'LC31-40		'LC31-40		'C31-50		'C31-60		'C31-80		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
38	$t_{su(RESET-CIL)}$	Setup time, $\overline{\text{RESET}}$ before CLKIN low	10	P†‡	10	P†‡	10	P†‡	10	P†‡	7	P†‡	4	P†‡	ns
39	$t_{d(CLKINH-H1H)}$	Delay time, CLKIN high to H1 high§	2	12	2	12¶	2	14	2	10	2	10	2	8	ns
40	$t_{d(CLKINH-H1L)}$	Delay time, CLKIN high to H1 low§	2	12	2	12¶	2	14	2	10	2	10	2	8	ns
41	$t_{su(RESETH-H1L)}$	Setup time, $\overline{\text{RESET}}$ high before H1 low and after ten H1 clock cycles	10		9		9		7		6		5		ns
42	$t_{d(CLKINH-H3L)}$	Delay time, CLKIN high to H3 low§	2	12¶	2	12	2	14	2	10	2	10	2	8	ns
43	$t_{d(CLKINH-H3H)}$	Delay time, CLKIN high to H3 high§	2	12¶	2	12	2	14	2	10	2	10	2	8	ns
44	$t_{dis(H1H-DZ)}$	Disable time, H1 high to D (high impedance)		15#		13#		13#		12#		11#		9#	ns
45	$t_{dis(H3H-AZ)}$	Disable time, H3 high to A (high impedance)		10#		9#		9#		8#		7#		6#	ns
46	$t_{d(H3H-CONTROLH)}$	Delay time, H3 high to control signals high		10#		9#		9#		8#		7#		6#	ns
47	$t_{d(H1H-RWH)}$	Delay time, H1 high to R/$\overline{\text{W}}$ high		10#		9#		9#		8#		7#		6#	ns
48	$t_{d(H1H-IACKH)}$	Delay time, H1 high to $\overline{\text{IACK}}$ high		10#		9#		9#		8#		7#		6#	ns
49	$t_{dis(RESETL-ASYNCH)}$	Disable time, $\overline{\text{RESET}}$ low to asynchronous reset signals disabled (high impedance)		25#		21#		21#		17#		14#		12#	ns

† $P = t_{c(CI)}$
‡ Specified by design but not tested
§ See Figure 22 for temperature dependence .
¶ 14 ns for the extended temperature 'C31-40
# This value is characterized but not tested

timing parameters for $\overline{\text{RESET}}$ for the TMS320C31 and TMS320LC31 (continued)



NOTES: A. Asynchronous reset signals include XF0/1, CLKX0, DX0, FSX0, CLKR0, DR0, FSR0, and TCLK0/1.
B. $\overline{\text{RESET}}$ is an asynchronous input and can be asserted at any point during a clock cycle. If the specified timings are met, the exact sequence shown occurs; otherwise, an additional delay of one clock cycle is possible.
C. In microprocessor mode, the reset vector is fetched twice, with seven software wait states each time. In microcomputer mode, the reset vector is fetched twice, with no software wait states.
D. Control signals include $\overline{\text{STRB}}$.
E. The R/$\overline{\text{W}}$ outputs are placed in a high-impedance state during reset and can be provided with a resistive pullup, nominally 18–22 kΩ, if undesirable spurious writes are caused when these outputs go low.

Figure 21. Timing for $\overline{\text{RESET}}$

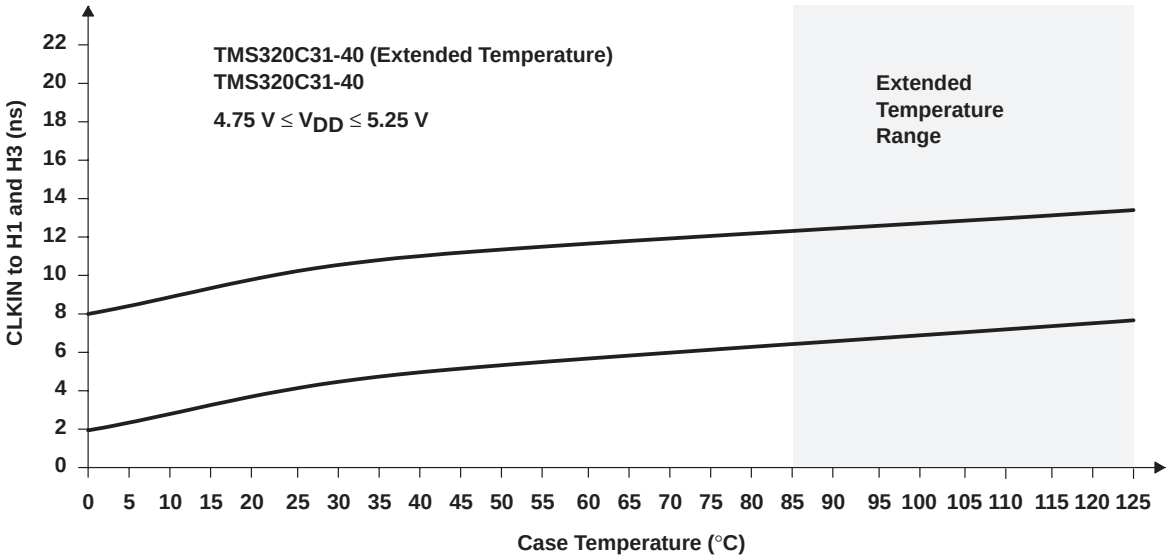


Figure 22. CLKIN to H1 and H3 as a Function of Temperature

interrupt response timing

The following table defines the timing parameters for the $\overline{INT}$ signals. The numbers shown in Figure 23 correspond with those in the NO. column of the table below.

timing parameters for $\overline{INT3}$–$\overline{INT0}$ response (see Figure 23)

NO.			'LC31-33		'C31-40 'LC31-40		'C31-50		'C31-60		'C31-80		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
50	$t_{su(INT-H1L)}$	Setup time, $\overline{INT3}$–$\overline{INT0}$ before H1 low	15		13		10		8		5		ns
51	$t_{w(INT)}$	Pulse duration, interrupt to ensure only one interrupt	P	2P†‡	P	2P†‡	P	2P†‡	P	2P†‡	P	2P†‡	ns

† This value is characterized but not tested.
‡ $P = t_{c(H)}$

The interrupt ($\overline{INT}$) pins are asynchronous inputs that can be asserted at any time during a clock cycle. The TMS320C3x interrupts are level-sensitive, not edge-sensitive. Interrupts are detected on the falling edge of H1. Therefore, interrupts must be set up and held to the falling edge of H1 for proper detection. The CPU and DMA respond to detected interrupts on instruction-fetch boundaries only.

For the processor to recognize only one interrupt on a given input, an interrupt pulse must be set up and held to:

- A minimum of one H1 falling edge
- No more than two H1 falling edges

The TMS320C3x can accept an interrupt from the same source every two H1 clock cycles.

If the specified timings are met, the exact sequence shown in Figure 23 occurs; otherwise, an additional delay of one clock cycle is possible.

timing parameters for $\overline{INT3}$–$\overline{INT0}$ response (continued)

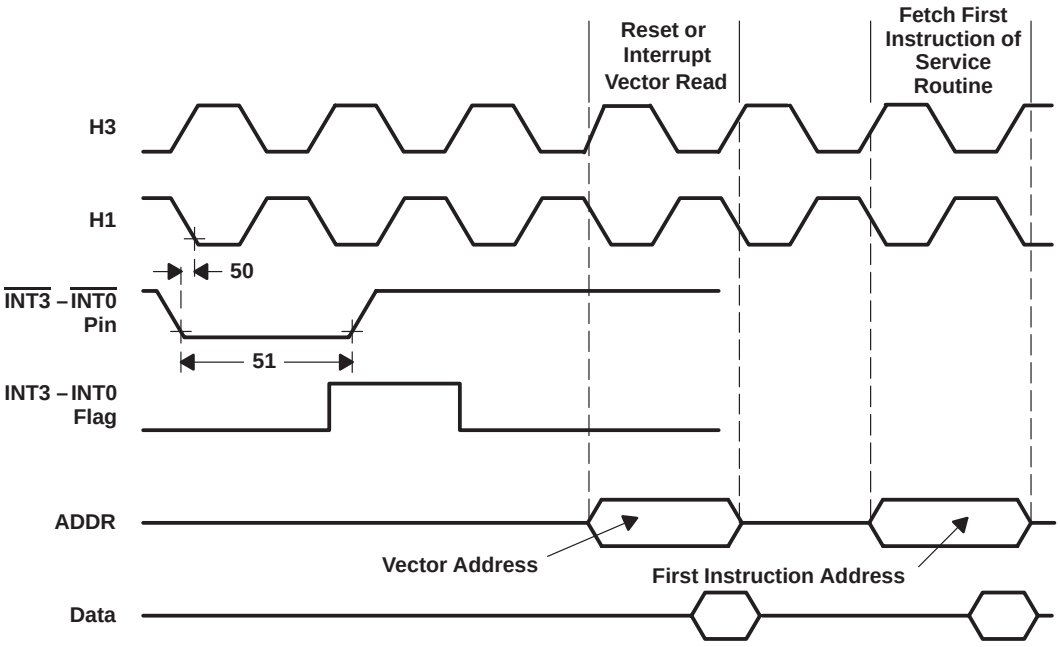


Figure 23. Timing for $\overline{INT3}$–$\overline{INT0}$ Response

interrupt-acknowledge timing

The $\overline{\text{IACK}}$ output goes active on the first half-cycle (HI rising) of the decode phase of the IACK instruction and goes inactive at the first half-cycle (HI rising) of the read phase of the IACK instruction.

The following table defines the timing parameters for the $\overline{\text{IACK}}$ signal. The numbers shown in Figure 24 correspond with those in the NO. column of the table below.

timing parameters for $\overline{\text{IACK}}$ (see Note 7 and Figure 24)

NO.			’LC31-33		’C31-40 ’LC31-40		’C31-50		’C31-60		’C31-80		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
52	$t_{d(H1H-IACKL)}$	Delay time, H1 high to $\overline{\text{IACK}}$ low		10		9		7		6		5	ns
53	$t_{d(H1H-IACKH)}$	Delay time, H1 high to $\overline{\text{IACK}}$ high		10		9		7		6		5	ns

NOTE 7: $\overline{\text{IACK}}$ goes active on the first half-cycle (H1 rising) of the decode phase of the IACK instruction and goes inactive at the first half-cycle (H1 rising) of the read phase of the IACK instruction. Because of pipeline conflicts, $\overline{\text{IACK}}$ remains low for one cycle even if the decode phase of the IACK instruction is extended.

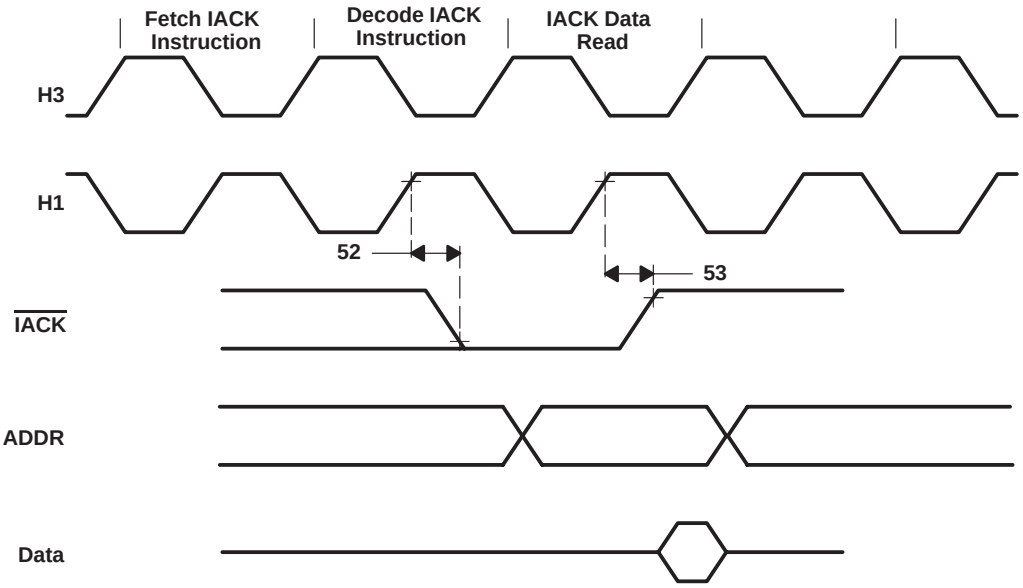


Figure 24. Timing for $\overline{\text{IACK}}$

serial-port timing parameters for TMS320C31-33 and TMS320LC31-33 (see Figure 25 and Figure 26)

NO.				'LC31-33 MIN	'LC31-33 MAX	UNIT
54	$t_{d(H1H-SCK)}$	Delay time, H1 high to internal CLKX/R			15	ns
55	$t_{c(SCK)}$	Cycle time, CLKX/R	CLKX/R ext	$t_{c(H)}$x2.6		ns
			CLKX/R int	$t_{c(H)}$x2	$t_{c(H)}$x2^{32}	
56	$t_{w(SCK)}$	Pulse duration, CLKX/R high/low	CLKX/R ext	$t_{c(H)}$+12		ns
			CLKX/R int	[$t_{c(SCK)}$/2]–15	[$t_{c(SCK)}$/2]+5	
57	$t_{r(SCK)}$	Rise time, CLKX/R			8	ns
58	$t_{f(SCK)}$	Fall time, CLKX/R			8	ns
59	$t_{d(C-DX)}$	Delay time, CLKX to DX valid	CLKX ext		35	ns
			CLKX int		20	
60	$t_{su(DR-CLKRL)}$	Setup time, DR before CLKR low	CLKR ext	10		ns
			CLKR int	25		
61	$t_{h(CLKRL-DR)}$	Hold time, DR from CLKR low	CLKR ext	10		ns
			CLKR int	0		
62	$t_{d(C-FSX)}$	Delay time, CLKX to internal FSX high/low	CLKX ext		32	ns
			CLKX int		17	
63	$t_{su(FSR-CLKRL)}$	Setup time, FSR before CLKR low	CLKR ext	10		ns
			CLKR int	10		
64	$t_{h(SCKL-FS)}$	Hold time, FSX/R input from CLKX/R low	CLKX/R ext	10		ns
			CLKX/R int	0		
65	$t_{su(FSX-C)}$	Setup time, external FSX before CLKX	CLKX ext	–[$t_{c(H)}$–8]†	[$t_{c(SCK)}$/2]–10†	ns
			CLKX int	[$t_{c(H)}$–21]†	$t_{c(SCK)}$/2†	
66	$t_{d(CH-DX)V}$	Delay time, CLKX to first DX bit, FSX precedes CLKX high	CLKX ext		36†	ns
			CLKX int		21†	
67	$t_{d(FSX-DX)V}$	Delay time, FSX to first DX bit, CLKX precedes FSX			36†	ns
68	$t_{d(CH-DXZ)}$	Delay time, CLKX high to DX high impedance following last data bit			20†	ns

† This value is characterized but not tested

serial-port timing parameters for TMS320C31-40 and TMS320LC31-40 (see Figure 25 and Figure 26)

NO.				’C31-40 ’LC31-40		UNIT
				MIN	MAX	
54	$t_{d(H1H-SCK)}$	Delay time, H1 high to internal CLKX/R			13	ns
55	$t_{c(SCK)}$	Cycle time, CLKX/R	CLKX/R ext	$t_{c(H)}$x2.6		ns
			CLKX/R int	$t_{c(H)}$x2	$t_{c(H)}$x2^{32}	
56	$t_{w(SCK)}$	Pulse duration, CLKX/R high/low	CLKX/R ext	$t_{c(H)}$+10		ns
			CLKX/R int	[$t_{c(SCK)}$/2]–5	[$t_{c(SCK)}$/2]+5	
57	$t_{r(SCK)}$	Rise time, CLKX/R			7	ns
58	$t_{f(SCK)}$	Fall time, CLKX/R			7	ns
59	$t_{d(C-DX)}$	Delay time, CLKX to DX valid	CLKX ext		30	ns
			CLKX int		17	
60	$t_{su(DR-CLKRL)}$	Setup time, DR before CLKR low	CLKR ext	9		ns
			CLKR int	21		
61	$t_{h(CLKRL-DR)}$	Hold time, DR from CLKR low	CLKR ext	9		ns
			CLKR int	0		
62	$t_{d(C-FSX)}$	Delay time, CLKX to internal FSX high/low	CLKX ext		27	ns
			CLKX int		15	
63	$t_{su(FSR-CLKRL)}$	Setup time, FSR before CLKR low	CLKR ext	9		ns
			CLKR int	9		
64	$t_{h(SCKL-FS)}$	Hold time, FSX/R input from CLKX/R low	CLKX/R ext	9		ns
			CLKX/R int	0		
65	$t_{su(FSX-C)}$	Setup time, external FSX before CLKX	CLKX ext	–[$t_{c(H)}$–8]†	[$t_{c(SCK)}$/2]–10†	ns
			CLKX int	[$t_{c(H)}$–21]†	$t_{c(SCK)}$/2†	
66	$t_{d(CH-DX)V}$	Delay time, CLKX to first DX bit, FSX precedes CLKX high	CLKX ext		30†	ns
			CLKX int		18†	
67	$t_{d(FSX-DX)V}$	Delay time, FSX to first DX bit, CLKX precedes FSX			30†	ns
68	$t_{d(CH-DXZ)}$	Delay time, CLKX high to DX high impedance following last data bit			17†	ns

† This value is characterized but not tested

serial-port timing parameters for TMS320C31-50 (see Figure 25 and Figure 26)

NO.				’C31-50 MIN	’C31-50 MAX	UNIT
54	$t_{d(H1H-SCK)}$	Delay time, H1 high to internal CLKX/R			10	ns
55	$t_{c(SCK)}$	Cycle time, CLKX/R	CLKX/R ext	$t_{c(H)}$x2.6		ns
			CLKX/R int	$t_{c(H)}$x2	$t_{c(H)}$x2[32]	
56	$t_{w(SCK)}$	Pulse duration, CLKX/R high/low	CLKX/R ext	$t_{c(H)}$+10		ns
			CLKX/R int	[$t_{c(SCK)}$/2]–5	[$t_{c(SCK)}$/2]+5	
57	$t_{r(SCK)}$	Rise time, CLKX/R			6	ns
58	$t_{f(SCK)}$	Fall time, CLKX/R			6	ns
59	$t_{d(C-DX)}$	Delay time, CLKX to DX valid	CLKX ext		24	ns
			CLKX int		16	
60	$t_{su(DR-CLKRL)}$	Setup time, DR before CLKR low	CLKR ext	9		ns
			CLKR int	17		
61	$t_{h(CLKRL-DR)}$	Hold time, DR from CLKR low	CLKR ext	7		ns
			CLKR int	0		
62	$t_{d(C-FSX)}$	Delay time, CLKX to internal FSX high/low	CLKX ext		22	ns
			CLKX int		15	
63	$t_{su(FSR-CLKRL)}$	Setup time, FSR before CLKR low	CLKR ext	7		ns
			CLKR int	7		
64	$t_{h(SCKL-FS)}$	Hold time, FSX/R input from CLKX/R low	CLKX/R ext	7		ns
			CLKX/R int	0		
65	$t_{su(FSX-C)}$	Setup time, external FSX before CLKX	CLKX ext	$-[t_{c(H)}-8]^{\dagger}$	$[t_{c(SCK)}/2]-10^{\dagger}$	ns
			CLKX int	$-[t_{c(H)}-21]^{\dagger}$	$t_{c(SCK)}/2^{\dagger}$	
66	$t_{d(CH-DX)V}$	Delay time, CLKX to first DX bit, FSX precedes CLKX high	CLKX ext		$24^{\dagger}$	ns
			CLKX int		$14^{\dagger}$	
67	$t_{d(FSX-DX)V}$	Delay time, FSX to first DX bit, CLKX precedes FSX			$24^{\dagger}$	ns
68	$t_{d(CH-DXZ)}$	Delay time, CLKX high to DX high impedance following last data bit			$14^{\dagger}$	ns

† This value is characterized but not tested

serial-port timing parameters for TMS320C31-60 (see Figure 25 and Figure 26)

NO.				’C31-60 MIN	’C31-60 MAX	UNIT
54	$t_{d(H1H-SCK)}$	Delay time, H1 high to internal CLKX/R			8	ns
55	$t_{c(SCK)}$	Cycle time, CLKX/R	CLKX/R ext	$t_{c(H)}$x2.6		ns
			CLKX/R int	$t_{c(H)}$x2	$t_{c(H)}$x2^{32}	
56	$t_{w(SCK)}$	Pulse duration, CLKX/R high/low	CLKX/R ext	$t_{c(H)}$+10		ns
			CLKX/R int	[$t_{c(SCK)}$/2]–5	[$t_{c(SCK)}$/2]+5	
57	$t_{r(SCK)}$	Rise time, CLKX/R			5	ns
58	$t_{f(SCK)}$	Fall time, CLKX/R			5	ns
59	$t_{d(C-DX)}$	Delay time, CLKX to DX valid	CLKX ext		20	ns
			CLKX int		15	
60	$t_{su(DR-CLKRL)}$	Setup time, DR before CLKR low	CLKR ext	8		ns
			CLKR int	15		
61	$t_{h(CLKRL-DR)}$	Hold time, DR from CLKR low	CLKR ext	6		ns
			CLKR int	0		
62	$t_{d(C-FSX)}$	Delay time, CLKX to internal FSX high/low	CLKX ext		20	ns
			CLKX int		14	
63	$t_{su(FSR-CLKRL)}$	Setup time, FSR before CLKR low	CLKR ext	6		ns
			CLKR int	6		
64	$t_{h(SCKL-FS)}$	Hold time, FSX/R input from CLKX/R low	CLKX/R ext	6		ns
			CLKX/R int	0		
65	$t_{su(FSX-C)}$	Setup time, external FSX before CLKX	CLKX ext	–[$t_{c(H)}$–8]†	[$t_{c(SCK)}$/2]–10†	ns
			CLKX int	–[$t_{c(H)}$–21]†	$t_{c(SCK)}$/2†	
66	$t_{d(CH-DX)V}$	Delay time, CLKX to first DX bit, FSX precedes CLKX high	CLKX ext		20†	ns
			CLKX int		12†	
67	$t_{d(FSX-DX)V}$	Delay time, FSX to first DX bit, CLKX precedes FSX			20†	ns
68	$t_{d(CH-DXZ)}$	Delay time, CLKX high to DX high impedance following last data bit			12†	ns

† This value is characterized but not tested

serial-port timing parameters for TMS320C31-80 (see Figure 25 and Figure 26)

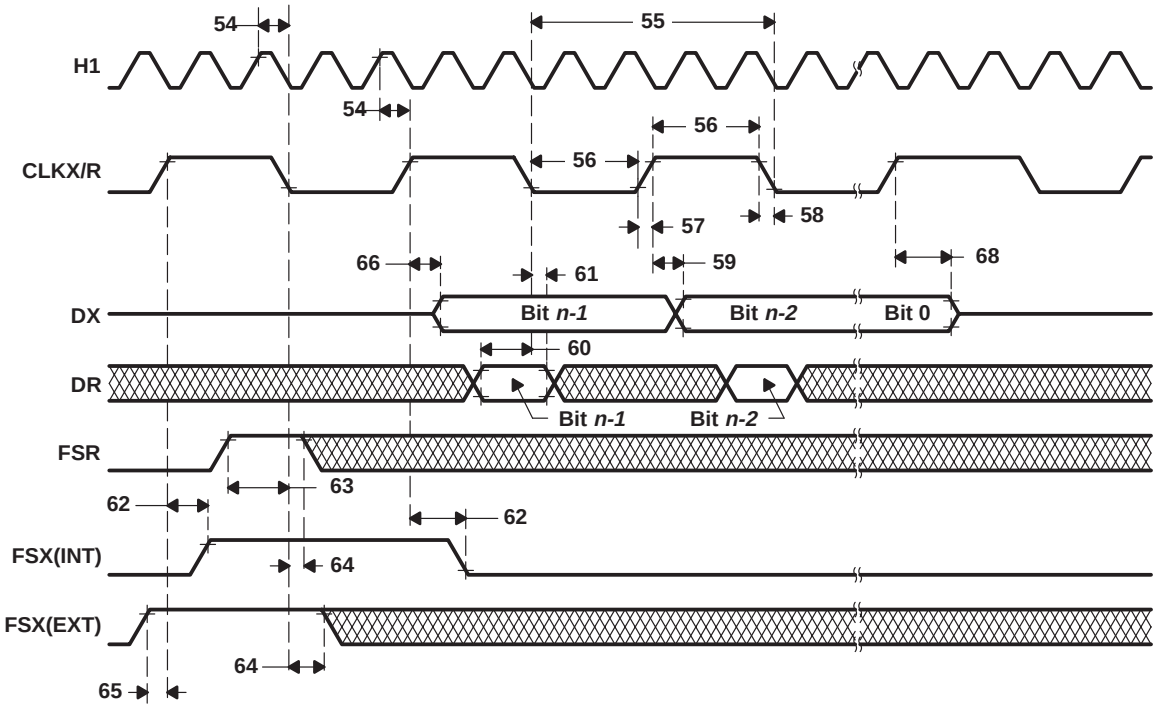
NO.				’C31-80 MIN	’C31-80 MAX	UNIT
54	$t_{d(H1H-SCK)}$	Delay time, H1 high to internal CLKX/R			7	ns
55	$t_{c(SCK)}$	Cycle time, CLKX/R	CLKX/R ext	$t_{c(H)}$x2.6		ns
			CLKX/R int	$t_{c(H)}$x2	$t_{c(H)}$x2^{32}	
56	$t_{w(SCK)}$	Pulse duration, CLKX/R high/low	CLKX/R ext	$t_{c(H)}$+6		ns
			CLKX/R int	[$t_{c(SCK)}$/2]–5	[$t_{c(SCK)}$/2]+5	
57	$t_{r(SCK)}$	Rise time, CLKX/R			3	ns
58	$t_{f(SCK)}$	Fall time, CLKX/R			3	ns
59	$t_{d(C-DX)}$	Delay time, CLKX to DX valid	CLKX ext		16	ns
			CLKX int		11	
60	$t_{su(DR-CLKRL)}$	Setup time, DR before CLKR low	CLKR ext	6		ns
			CLKR int	13		
61	$t_{h(CLKRL-DR)}$	Hold time, DR from CLKR low	CLKR ext	5		ns
			CLKR int	0		
62	$t_{d(C-FSX)}$	Delay time, CLKX to internal FSX high/low	CLKX ext		16	ns
			CLKX int		12	
63	$t_{su(FSR-CLKRL)}$	Setup time, FSR before CLKR low	CLKR ext	5		ns
			CLKR int	5		
64	$t_{h(SCKL-FS)}$	Hold time, FSX/R input from CLKX/R low	CLKX/R ext	5		ns
			CLKX/R int	0		
65	$t_{su(FSX-C)}$	Setup time, external FSX before CLKX	CLKX ext	–[$t_{c(H)}$–8]†	[$t_{c(SCK)}$/2]–10†	ns
			CLKX int	–[$t_{c(H)}$–21]†	$t_{c(SCK)}$/2†	
66	$t_{d(CH-DX)V}$	Delay time, CLKX to first DX bit, FSX precedes CLKX high	CLKX ext		16	ns
			CLKX int		10	
67	$t_{d(FSX-DX)V}$	Delay time, FSX to first DX bit, CLKX precedes FSX			16	ns
68	$t_{d(CH-DXZ)}$	Delay time, CLKX high to DX high impedance following last data bit			10	ns

† This value is characterized but not tested

data-rate timing modes

Unless otherwise indicated, the data-rate timings shown in Figure 25 and Figure 26 are valid for all serial-port modes, including handshake. For a functional description of serial-port operation refer to subsection 8.2.12 of the *TMS320C3x User's Guide* (literature number SPRU031).

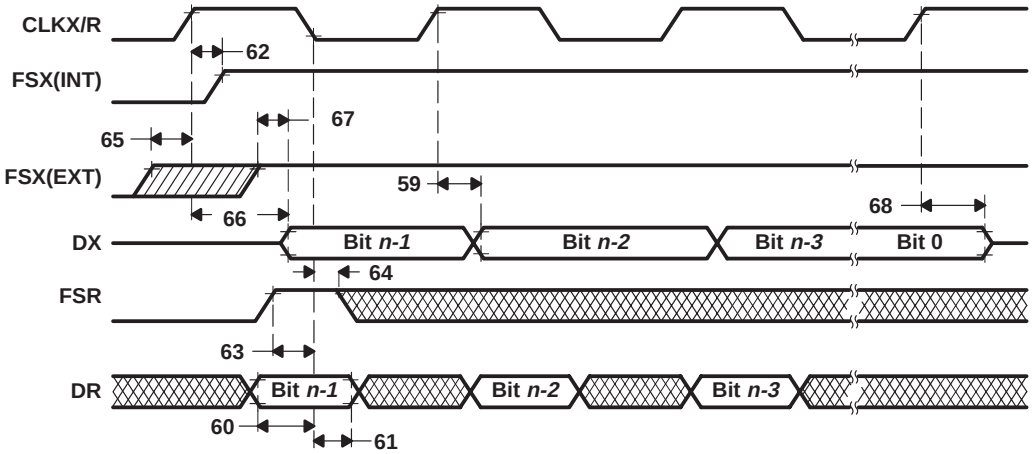
The serial-port timing parameters for seven 'C3x devices are defined in the preceding "serial-port timing parameters" tables (such as "serial-port timing parameters for TMS320C31-60"). The numbers shown in Figure 25 and Figure 26 correspond with those in the NO. column of each table.



NOTES: A. Timing diagrams show operations with CLKXP = CLKRP = FSXP = FSRP = 0.
B. Timing diagrams depend on the length of the serial-port word, where n = 8, 16, 24, or 32 bits, respectively.

Figure 25. Timing for Fixed Data-Rate Mode

data-rate timing modes (continued)



NOTES: A. Timing diagrams show operation with CLKXP = CLKRP = FSXP = FSRP = 0.
B. Timing diagrams depend on the length of the serial-port word, where n = 8, 16, 24, or 32 bits, respectively.
C. The timings that are not specified expressly for the variable data-rate mode are the same as those that are specified for the fixed data-rate mode.

Figure 26. Timing for Variable Data-Rate Mode

$\overline{\text{HOLD}}$ timing

$\overline{\text{HOLD}}$ is an asynchronous input that can be asserted at any time during a clock cycle. If the specified timings are met, the exact sequence shown in Figure 27 occurs; otherwise, an additional delay of one clock cycle is possible.

The table, "timing parameters for $\overline{\text{HOLD}}$/$\overline{\text{HOLDA}}$", defines the timing parameters for the $\overline{\text{HOLD}}$ and $\overline{\text{HOLDA}}$ signals. The numbers shown in Figure 27 correspond with those in the NO. column of the table.

The NOHOLD bit of the primary-bus control register overrides the $\overline{\text{HOLD}}$ signal. When this bit is set, the device comes out of hold and prevents future hold cycles.

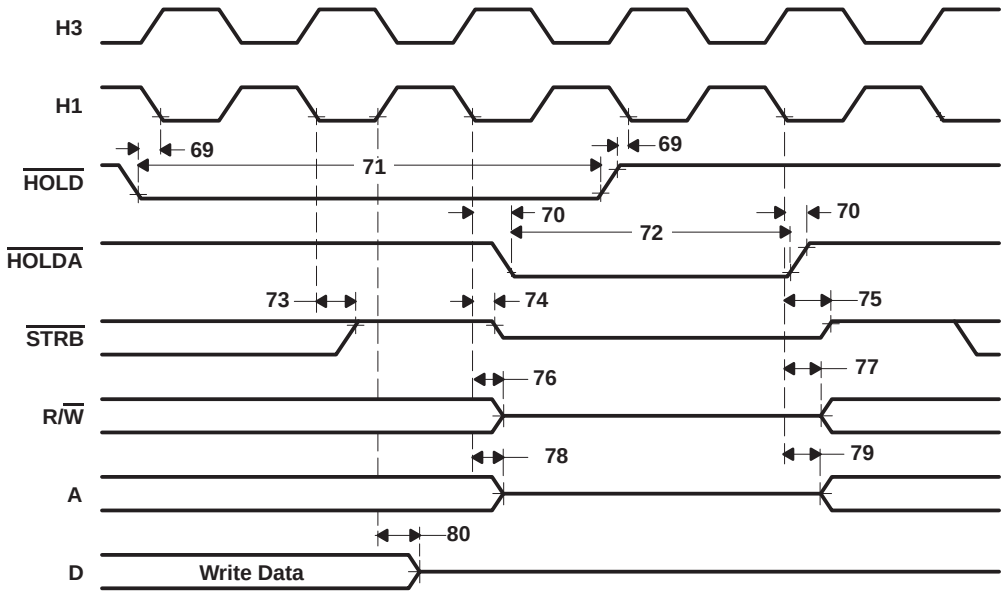
Asserting $\overline{\text{HOLD}}$ prevents the processor from accessing the primary bus. Program execution continues until a read from or a write to the primary bus is requested. In certain circumstances, the first write is pending, thus allowing the processor to continue until a second write is encountered.

timing parameters for $\overline{\text{HOLD}}$/$\overline{\text{HOLDA}}$ (see Figure 27)

NO.			'LC31-33		'C31-40 'LC31-40		'C31-50		'C31-60		'C31-80		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
69	$t_{su(HOLD-H1L)}$	Setup time, $\overline{\text{HOLD}}$ before H1 low	15		13		10		8		5		ns
70	$t_{v(H1L-HOLDA)}$	Valid time, $\overline{\text{HOLDA}}$ after H1 low	0†	10	0†	9	0†	7	0†	6	0†	5	ns
71	$t_{w(HOLD)}$‡	Pulse duration, $\overline{\text{HOLD}}$ low	$2t_{c(H)}$		$2t_{c(H)}$		$2t_{c(H)}$		$2t_{c(H)}$		$2t_{c(H)}$		ns
72	$t_{w(HOLDA)}$	Pulse duration, $\overline{\text{HOLDA}}$ low	$t_{cH}-5$†		$t_{cH}-5$†		$t_{cH}-5$†		$t_{cH}-5$†		$t_{cH}-5$†		ns
73	$t_{d(H1L-SH)H}$	Delay time, H1 low to $\overline{\text{STRB}}$ high for a $\overline{\text{HOLD}}$	0§	10	0§	9	0§	7	0§	6	0§	4	ns
74	$t_{dis(H1L-S)}$	Disable time, H1 low to $\overline{\text{STRB}}$ to the high-impedance state	0§	10†	0§	9†	0§	8†	0§	7†	0§	7†	ns
75	$t_{en(H1L-S)}$	Enable time, H1 low to $\overline{\text{STRB}}$ enabled (active)	0§	10	0§	9	0§	7	0§	6	0§	6	ns
76	$t_{dis(H1L-RW)}$	Disable time, H1 low to R/$\overline{\text{W}}$ to the high-impedance state	0†	10†	0†	9†	0†	8†	0†	7†	0†	6†	ns
77	$t_{en(H1L-RW)}$	Enable time, H1 low to R/$\overline{\text{W}}$ enabled (active)	0†	10	0†	9	0†	7	0†	6	0†	6	ns
78	$t_{dis(H1L-A)}$	Disable time, H1 low to address to the high-impedance state	0§	10†	0§	10†	0§	8†	0§	7†	0§	7†	ns
79	$t_{en(H1L-A)}$	Enable time, H1 low to address enabled (valid)	0§	15	0§	13	0§	12	0§	11	0§	10	ns
80	$t_{dis(H1H-D)}$	Disable time, H1 high to data to the high-impedance state	0§	10†	0§	9†	0§	8†	0§	7†	0§	6†	ns

† This value is characterized but not tested
‡ $\overline{\text{HOLD}}$ is an asynchronous input and can be asserted at any point during a clock cycle. If the specified timings are met, the exact sequence shown in Figure 27 occurs; otherwise, an additional delay of one clock cycle is possible.
§ Not tested

$\overline{\text{HOLD}}$ timing (continued)



NOTE A: $\overline{\text{HOLDA}}$ goes low in response to $\overline{\text{HOLD}}$ going low and continues to remain low until one H1 cycle after $\overline{\text{HOLD}}$ goes back high.

Figure 27. Timing for $\overline{\text{HOLD}}$/$\overline{\text{HOLDA}}$

general-purpose I/O timing

Peripheral pins include CLKX0, CLKR0, DX0, DR0, FSX0, FSR0, and TCLK0/1. The contents of the internal control registers associated with each peripheral define the modes for these pins.

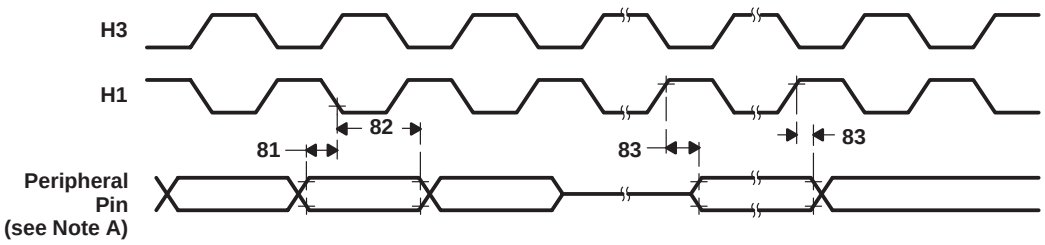
peripheral pin I/O timing

The table, timing parameters for peripheral pin general-purpose I/O, defines peripheral pin general-purpose I/O timing parameters. The numbers shown in Figure 28 correspond with those in the NO. column of the table below.

timing parameters for peripheral pin general-purpose I/O (see Note 8 and Figure 28)

NO.			LC31-33		’C31-40 ’LC31-40		’C31-50		’C31-60		’C31-80		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
81	$t_{su(GPIO-H1L)}$	Setup time, general-purpose input before H1 low	12		10		9		8		7		ns
82	$t_{h(H1L-GPIO)}$	Hold time, general-purpose input after H1 low	0		0		0		0		0		ns
83	$t_{d(H1H-GPIO)}$	Delay time, general-purpose output after H1 high		15		13		10		8		6	ns

NOTE 8: Peripheral pins include CLKX0, CLKR0, DX0, DR0, FSX0, FSR0, and TCLK0/1. The modes of these pins are defined by the contents of internal-control registers associated with each peripheral.



NOTE A: Peripheral pins include CLKX0, CLKR0, DX0, DR0, FSX0, FSR0, and TCLK0/1.

Figure 28. Timing for Peripheral Pin General-Purpose I/O

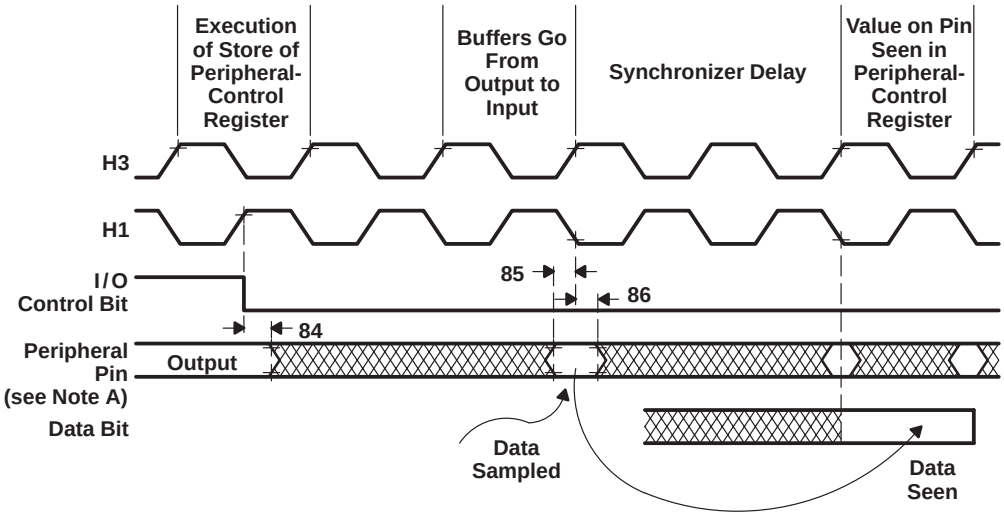
changing the peripheral pin I/O modes

The following tables show the timing parameters for changing the peripheral pin from a general-purpose output pin to a general-purpose input pin and vice versa. The numbers shown in Figure 29 and Figure 30 correspond to those shown in the NO. column of the tables below.

timing parameters for peripheral pin changing from general-purpose output to input mode (see Note 8 and Figure 29)

NO.			'LC31-33		'C31-40 'LC31-40		'C31-50		'C31-60		'C31-80		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
84	$t_{h(H1H)}$	Hold time, peripheral pin after H1 high		15		13		10		8		6	ns
85	$t_{su(GPIO-H1L)}$	Setup time, peripheral pin before H1 low	10		9		9		8		7		ns
86	$t_{h(H1L-GPIO)}$	Hold time, peripheral pin after H1 low	0		0		0		0		0		ns

NOTE 8: Peripheral pins include CLKX0, CLKR0, DX0, DR0, FSX0, FSR0, and TCLK0/1. The modes of these pins are defined by the contents of internal-control registers associated with each peripheral.



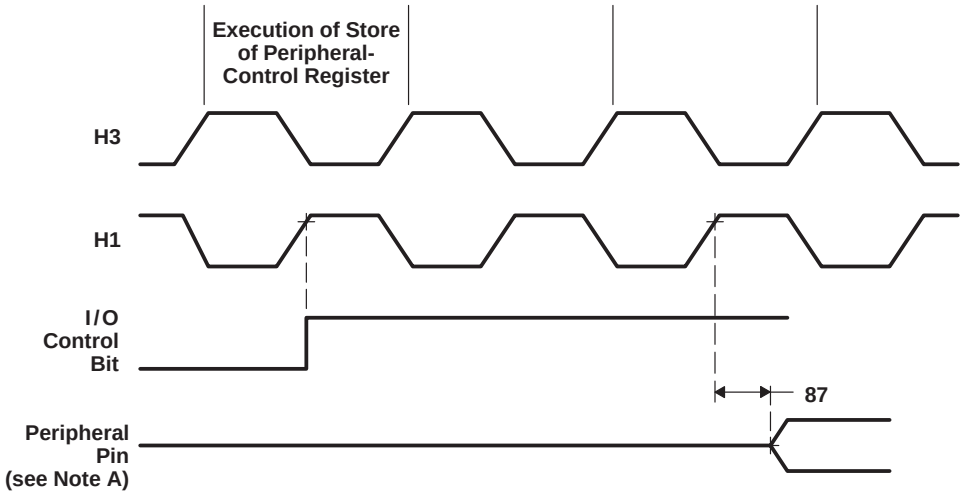
NOTE A: Peripheral pins include CLKX0, CLKR0, DX0, DR0, FSX0, FSR0, and TCLK0/1.

Figure 29. Timing for Change of Peripheral Pin From General-Purpose Output to Input Mode

timing parameters for peripheral pin changing from general-purpose input to output mode (see Note 8 and Figure 30)

NO.			’LC31-33		’C31-40 ’LC31-40		’C31-50		’C31-60		’C31-80		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
87	$t_{d(H1H-GPIO)}$	Delay time, H1 high to peripheral pin switching from input to output		15		13		10		8		6	ns

NOTE 8: Peripheral pins include CLKX0, CLKR0, DX0, DR0, FSX0, FSR0, and TCLK0/1. The modes of these pins are defined by the contents of internal-control registers associated with each peripheral.



NOTE A: Peripheral pins include CLKX0, CLKR0, DX0, DR0, FSX0, FSR0, and TCLK0/1.

Figure 30. Timing for Change of Peripheral Pin From General-Purpose Input to Output Mode

timer pin timing

Valid logic-level periods and polarity are specified by the contents of the internal control registers.

The following tables define the timing parameters for the timer pin. The numbers shown in Figure 31 correspond with those in the NO. column of the tables below.

timing parameters for timer pin for TMS320LC31-33 (see Figure 31) †

NO.	DESCRIPTION‡			'LC31-33		'C31-40, 'LC31-40		UNIT
				MIN	MAX	MIN	MAX	
88	$t_{su(TCLK-H1L)}$	Setup time, TCLK external before H1 low		12		10		ns
89	$t_{h(H1L-TCLK)}$	Hold time, TCLK external after H1 low		0		0		ns
90	$t_{d(H1H-TCLK)}$	Delay time, H1 high to TCLK internal valid			10		9	ns
91	$t_{c(TCLK)}$	Cycle time, TCLK	TCLK ext	$t_{c(H)}\times 2.6$		$t_{c(H)}\times 2.6$		ns
			TCLK int	$t_{c(H)}\times 2$	$t_{c(H)}\times 2^{32}$‡	$t_{c(H)}\times 2$	$t_{c(H)}\times 2^{32}$‡	
92	$t_{w(TCLK)}$	Pulse duration, TCLK high/low	TCLK ext	$t_{c(H)}+12$		$t_{c(H)}+10$		ns
			TCLK int	$[t_{c(TCLK)}/2]-15$	$[t_{c(TCLK)}/2]+5$	$[t_{c(TCLK)}/2]-5$	$[t_{c(TCLK)}/2]+5$	

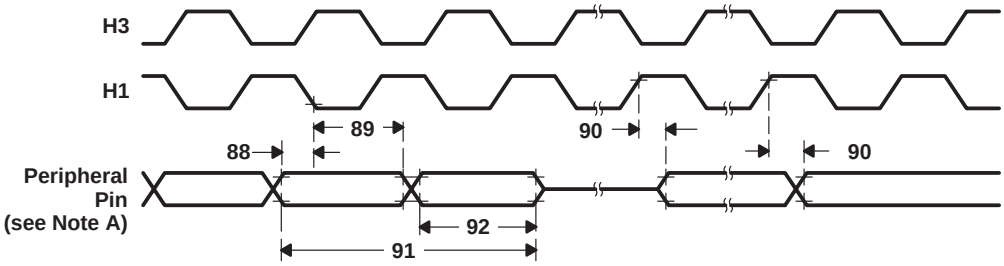
† Timing parameters 88 and 89 are applicable for a synchronous input clock. Timing parameters 91 and 92 are applicable for an asynchronous input clock.
‡ Specified by design but not tested

timing parameters for timer pin for TMS320LC31-40, TMS320C31-50, and TMS320C31-60 (see Figure 31) †

NO.	DESCRIPTION‡		'C31-50		'C31-60		'C31-80		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
88	$t_{su(TCLK-H1L)}$	Setup time, TCLK external before H1 low	8		6		5		ns
89	$t_{h(H1L-TCLK)}$	Hold time, TCLK external after H1 low	0		0		0		ns
90	$t_{d(H1H-TCLK)}$	Delay time, H1 high to TCLK internal valid		9		8		6	ns
91	$t_{c(TCLK)}$	TCLK ext	$t_{c(H)}\times 2.6$		$t_{c(H)}\times 2.6$		$t_{c(H)}\times 2.6$		ns
		TCLK int	$t_{c(H)}\times 2$	$t_{c(H)}\times 2^{32}$‡	$t_{c(H)}\times 2$	$t_{c(H)}\times 2^{32}$‡	$t_{c(H)}\times 2$	$t_{c(H)}\times 2^{32}$‡	
92	$t_{w(TCLK)}$	TCLK ext	$t_{c(H)}+10$		$t_{c(H)}+10$		$t_{c(H)}+6$		ns
		TCLK int	$[t_{c(TCLK)}/2]-5$	$[t_{c(TCLK)}/2]+5$	$[t_{c(TCLK)}/2]-5$	$[t_{c(TCLK)}/2]+5$	$[t_{c(TCLK)}/2]-5$	$[t_{c(TCLK)}/2]+5$	

† Timing parameters 88 and 89 are applicable for a synchronous input clock. Timing parameters 91 and 92 are applicable for an asynchronous input clock.
‡ Specified by design but not tested

timer pin timing (continued)



NOTE A: $\overline{\text{HOLDA}}$ goes low in response to $\overline{\text{HOLD}}$ going low and continues to remain low until one H1 cycle after $\overline{\text{HOLD}}$ goes back high.

Figure 31. Timing for Timer Pin

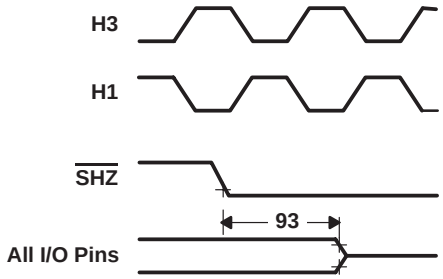
$\overline{\text{SHZ}}$ pin timing

The following table defines the timing parameter for the $\overline{\text{SHZ}}$ pin. The number shown in Figure 32 corresponds with that in the NO. column of the table below.

timing parameters for $\overline{\text{SHZ}}$ (see Figure 32)

NO.			'C31 'LC31 MIN	'C31 'LC31 MAX	UNIT
93	$t_{dis(SHZ)}$	Disable time, $\overline{\text{SHZ}}$ low to all O, I/O pins disabled (high impedance)	0†	2P†‡	ns

† This value is characterized but not tested
‡ P = $t_{c(CI)}$



NOTE A: Enabling $\overline{\text{SHZ}}$ destroys TMS320C3x register and memory contents. Assert $\overline{\text{SHZ}}$ = 1 and reset the TMS320C3x to restore it to a known condition.

Figure 32. Timing for $\overline{\text{SHZ}}$

$\overline{\text{SHZ}}$ pin timing (continued)

Table 1. Thermal Resistance Characteristics

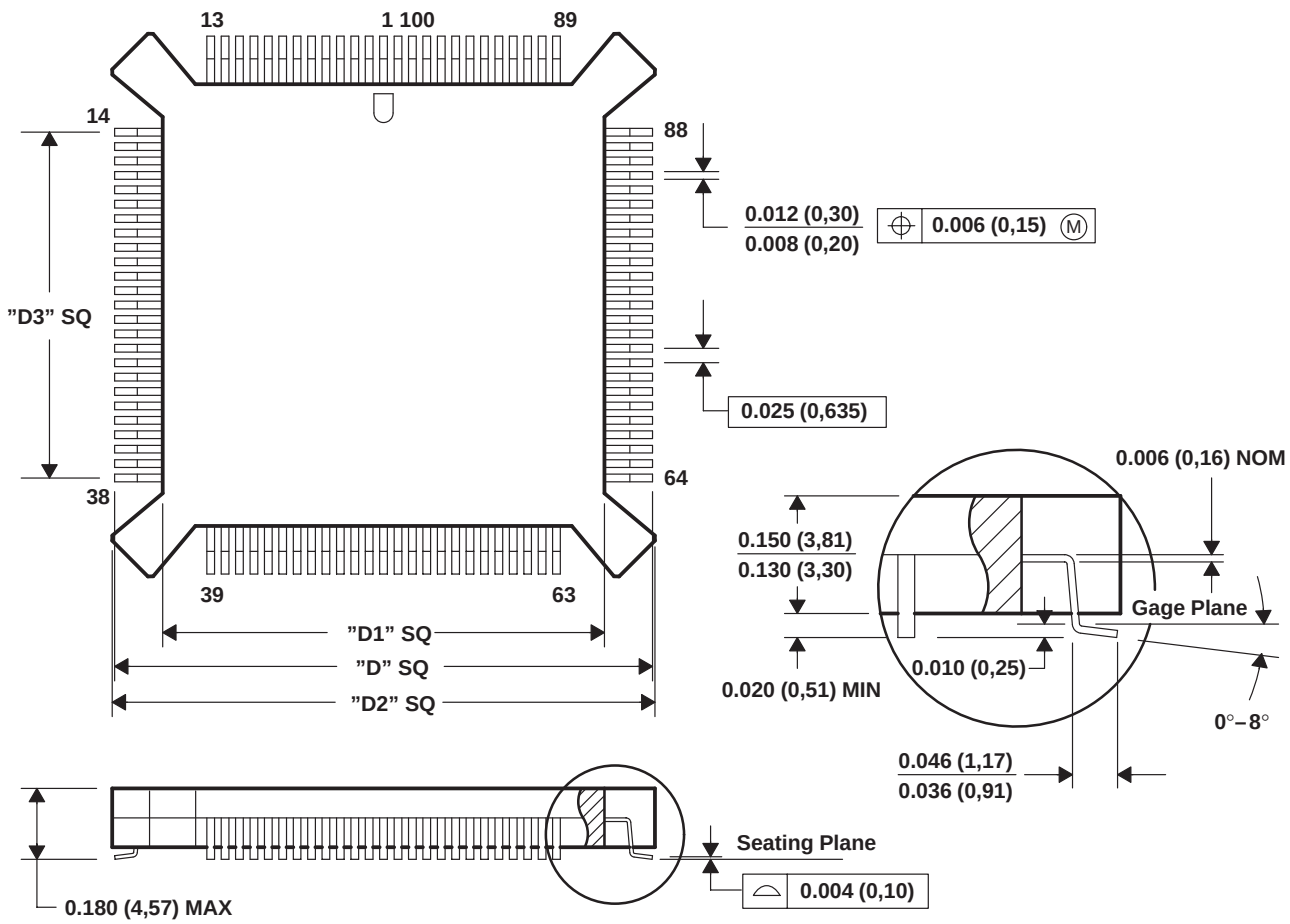
PARAMETER	°C/W	AIR FLOW LFPM
$R_{\theta JC}$†	11.0	N/A
$R_{\theta JA}$‡	49.0	0
$R_{\theta JA}$‡	35.5	200
$R_{\theta JA}$‡	28.0	400
$R_{\theta JA}$‡	23.5	600
$R_{\theta JA}$‡	21.6	800
$R_{\theta JA}$‡	20.0	1000

† $R_{\Theta SC}$ = junction-to-case
‡ $R_{\Theta JA}$ = junction-to-free air

MECHANICAL DATA

PQ (S-PQFP-G*)** **PLASTIC QUAD FLATPACK**

100 LEAD SHOWN



DIM \ LEADS ***		100	132
"D"	MAX	0.890 (22,61)	1.090 (27,69)
	MIN	0.870 (22,10)	1.070 (27,18)
"D1"	MAX	0.766 (19,46)	0.966 (24,54)
	MIN	0.734 (18,64)	0.934 (23,72)
"D2"	MAX	0.912 (23,16)	1.112 (28,25)
	MIN	0.888 (22,56)	1.088 (27,64)
"D3"	NOM	0.600 (15,24)	0.800 (20,32)

4040045/C 11/95

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO-069

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