TMS470R1B512
16/32-Bit RISC Flash Microcontroller

SPNS107–SEPTEMBER 2005

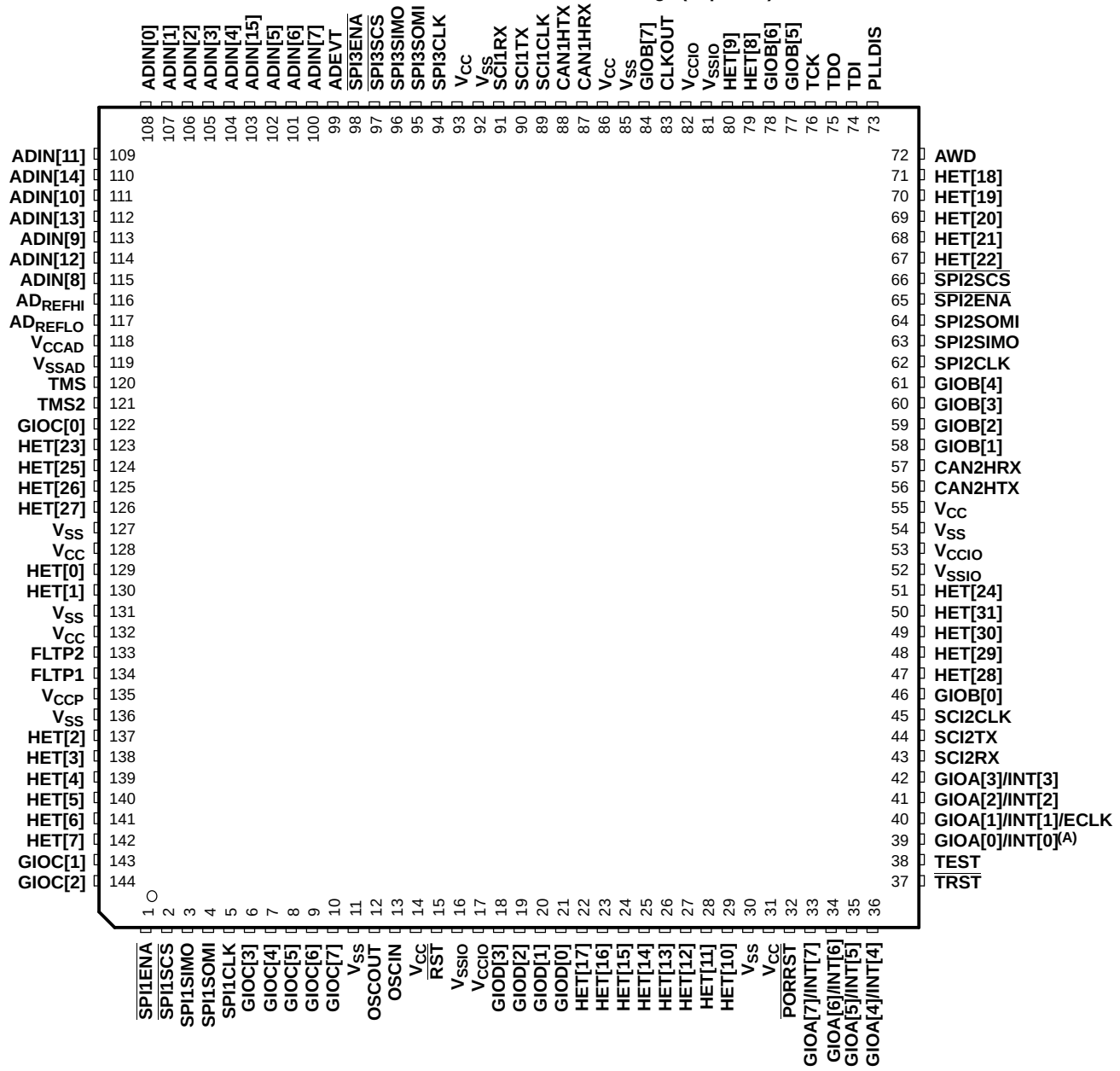
ADVANCE INFORMATION

FEATURES

- High-Performance Static CMOS Technology
- TMS470R1x 16/32-Bit RISC Core (ARM7TDMI™)
  - 24-MHz System Clock (60-MHz Pipeline Mode)
  - Independent 16/32-Bit Instruction Set
  - Open Architecture With Third-Party Support
  - Built-In Debug Module
  - Utilizes Big-Endian Format
- Integrated Memory
  - 512K-Byte Program Flash
    - 2 Banks With 14 Contiguous Sectors
    - Internal State Machine for Programming and Erase
  - 32K-Byte Static RAM (SRAM)
- 27 Dedicated GIO Pins, 1 Input-Only GIO Pin, and 59 Additional Peripheral I/Os
- Operating Features
  - Core Supply Voltage (V CC): 1.81 V – 2.05 V
  - I/O Supply Voltage (VCCIO): 3.0 V – 3.6 V
  - Low-Power Modes: STANDBY and HALT
  - Extended Industrial Temperature Range
- 470+ System Module
  - 32-Bit Address Space Decoding
  - Bus Supervision for Memory and Peripherals
  - Analog Watchdog (AWD) Timer
  - Real-Time Interrupt (RTI)
  - System Integrity and Failure Detection
  - Interrupt Expansion Module (IEM)
- Direct Memory Access (DMA) Controller
  - 32 Control Packets and 16 Channels
- Zero-Pin Phase-Locked Loop (ZPLL)-Based Clock Module With Prescaler
  - Multiply-by-4 or -8 Internal ZPLL Option
  - ZPLL Bypass Mode
- External Clock Prescale (ECP) Module
  - Programmable Low-Frequency External Clock (CLK)
- Seven Communication Interfaces:
  - Three Serial Peripheral Interfaces (SPIs)
    - 255 Programmable Baud Rates
  - Two Serial Communications Interfaces (SCIs)
    - 2^{24} Selectable Baud Rates
    - Asynchronous/Isosynchronous Modes
    - Two High-End CAN Controllers (HECCs)
    - 32-Mailbox Capacity Each
    - Fully Compliant With CAN Protocol, Version 2.0B
- High-End Timer (HET)
  - 32 Programmable I/O Channels:
    - 24 High-Resolution Pins
    - 8 Standard-Resolution Pins
  - High-Resolution Share Feature (XOR)
  - High-End Timer RAM
    - 128-Instruction Capacity
- 16-Channel 10-Bit Multi-Buffered ADC (MibADC)
  - 128-Word FIFO Buffer
  - Single- or Continuous-Conversion Modes
  - 1.55 µs Minimum Sample and Conversion Time
  - Calibration Mode and Self-Test Features
- Eight External Interrupts
- Flexible Interrupt Handling
- On-Chip Scan-Base Emulation Logic, IEEE Standard 1149.1(1) (JTAG) Test-Access Port
- 144-Pin Plastic Low-Profile Quad Flatpack (PGE Suffix)

(1) The test-access port is compatible with the IEEE Standard 1149.1-1990, *IEEE Standard Test-Access Port and Boundary Scan Architecture* specification. Boundary scan is not supported on this device.

TMS470R1B512 144-Pin PGE Package (Top View)



A. GIOA[0]/INT0 (pin 39) is an input-only GIO pin.

ADVANCE INFORMATION

DESCRIPTION

The TMS470R1B512(1) device is a member of the Texas Instruments (TI) TMS470R1x family of general-purpose16/32-bit reduced instruction set computer (RISC) microcontrollers. The B512 microcontroller offers high performance utilizing the high-speed ARM7TDMI 16/32-bit RISC central processing unit (CPU), resulting in a high instruction throughput while maintaining greater code efficiency. The ARM7TDMI 16/32-bit RISC CPU views memory as a linear collection of bytes numbered upwards from zero. The B512 utilizes the big-endian format, where the most significant byte of a word is stored at the lowest numbered byte and the least significant byte at the highest numbered byte.

High-end embedded control applications demand more performance from their controllers while maintaining low costs. The B512 RISC core architecture offers solutions to these performance and cost demands while maintaining low power consumption.

The B512 device contains the following:

- ARM7TDMI 16/32-Bit RISC CPU
- TMS470R1x system module (SYS) with 470+ enhancements [including an interrupt expansion module (IEM) and a 16-channel direct-memory access (DMA) controller]
- 512K-byte flash
- 32K-byte SRAM
- Zero-pin phase-locked loop (ZPLL) clock module
- Analog watchdog (AWD) timer
- Real-time interrupt (RTI) module
- Three serial peripheral interface (SPI) modules
- Two serial communications interface (SCI) modules
- Two high-end CAN controller (HECC) modules
- 10-bit multi-buffered analog-to-digital converter (MibADC) with 16 input channels
- High-end timer (HET) controlling 32 I/Os
- External clock prescale (ECP) module
- Up to 86 I/O pins and 1 input-only pin

The functions performed by the 470+ system module (SYS) include:

- Address decoding
- Memory protection
- Memory and peripherals bus supervision
- Reset and abort exception management
- Expanded interrupt capability with prioritization for all internal interrupt sources
- Device clock control
- Direct-memory access (DMA) and control
- Parallel signature analysis (PSA).

This data sheet includes device-specific information such as memory and peripheral select assignment, interrupt priority, and a device memory map. For a more detailed functional description of the SYS module, see the *TMS470R1x System Module Reference Guide* (literature number SPNU189). For a more detailed functional description of the IEM module, see the *TMS470R1x Interrupt Expansion Module (IEM) Reference Guide* (literature number SPNU211). For a more detailed functional description of the DMA module, see the *TMS470R1x Direct Memory Access (DMA) Controller Reference Guide* (literature number SPNU194).

The B512 memory includes general-purpose SRAM supporting single-cycle read/write accesses in byte, half-word, and word modes.

(1) The TMS470R1B512 device name will be referred to as either the full device name or as B512 throughout the remainder of this document.

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The flash memory on this device is a nonvolatile, electrically erasable and programmable memory implemented with a 32-bit-wide data bus interface.The flash operates with a system clock frequency of up to 24 MHz. When in pipeline mode, the flash operates with a system clock frequency of up to 60 MHz. For more detailed information on the F05 devices flash, see the *F05 Flash* section of this data sheet and the *TMS470R1x F05 Flash Reference Guide* (literature number SPNU213).

The B512 device has seven communication interfaces: three SPIs, two SCIs, and two HECCs. The SPI provides a convenient method of serial interaction for high-speed communications between similar shift-register type devices. The SCI is a full-duplex, serial I/O interface intended for asynchronous communication between the CPU and other peripherals using the standard non-return-to-zero (NRZ) format. The HECC uses a serial, multimaster communication protocol that efficiently supports distributed real-time control with robust communication rates of up to 1 megabit per second (Mbps). The HECC is ideal for applications operating in noisy and harsh environments (e.g., industrial fields) that require reliable serial communication or multiplexed wiring. For more detailed functional information on the SPI, SCI, and HECC peripherals, see the specific reference guides (literature numbers SPNU195, SPNU196, and SPNU197, respectively).

The HET is an advanced intelligent timer that provides sophisticated timing functions for real-time applications. The timer is software-controlled, using a reduced instruction set, with a specialized timer micromachine and an attached I/O port. The HET can be used for compare, capture, or general-purpose I/O. It is especially well suited for applications requiring multiple sensor information and drive actuators with complex and accurate time pulses. For more detailed functional information on the HET, see the *TMS470R1x High-End Timer (HET) Reference Guide* (literature number SPNU199).

The B512 HET peripheral contains the XOR-share feature. This feature allows two adjacent HET high- resolution channels to be XORed together, making it possible to output smaller pulses than a standard HET. For more detailed information on the HET XOR-share feature, see the *TMS470R1x High-End Timer (HET) Reference Guide* (literature number SPNU199).

The B512 device has a 10-bit-resolution, 16-channel sample-and-hold MibADC. The MibADC channels can be converted individually or can be grouped by software for sequential conversion sequences. There are three separate groupings, two of which can be triggered by an external event. Each sequence can be converted once when triggered or configured for continuous conversion mode. For more detailed functional information on the MibADC, see the *TMS470R1x Multi-Buffered Analog-to-Digital Converter (MibADC) Reference Guide* (literature number SPNU206).

The zero-pin phase-locked loop (ZPLL) clock module contains a phase-locked loop, a clock-monitor circuit, a clock-enable circuit, and a prescaler (with prescale values of 1-8). The function of the ZPLL is to multiply the external frequency reference to a higher frequency for internal use. The ZPLL provides ACLK to the system (SYS) module. The SYS module subsequently provides system clock (SYSCLK), real-time interrupt clock (RTICLK), CPU clock (MCLK), and peripheral interface clock (ICLK) to all other B512 device modules. For more detailed functional information on the ZPLL, see the *TMS470R1x Zero-Pin Phase-Locked Loop (ZPLL) Clock Module Reference Guide* (literature number SPNU212).

NOTE:

ACLK should not be confused with the MibADC internal clock, ADCLK. ACLK is the continuous system clock from an external resonator/crystal reference.

The B512 device also has an external clock prescaler (ECP) module that when enabled, outputs a continuous external clock (ECLK) on a specified GIO pin. The ECLK frequency is a user-programmable ratio of the peripheral interface clock (ICLK) frequency. For more detailed functional information on the ECP, see the *TMS470R1x External Clock Prescaler (ECP) Reference Guide* (literature number SPNU202).

Device Characteristics

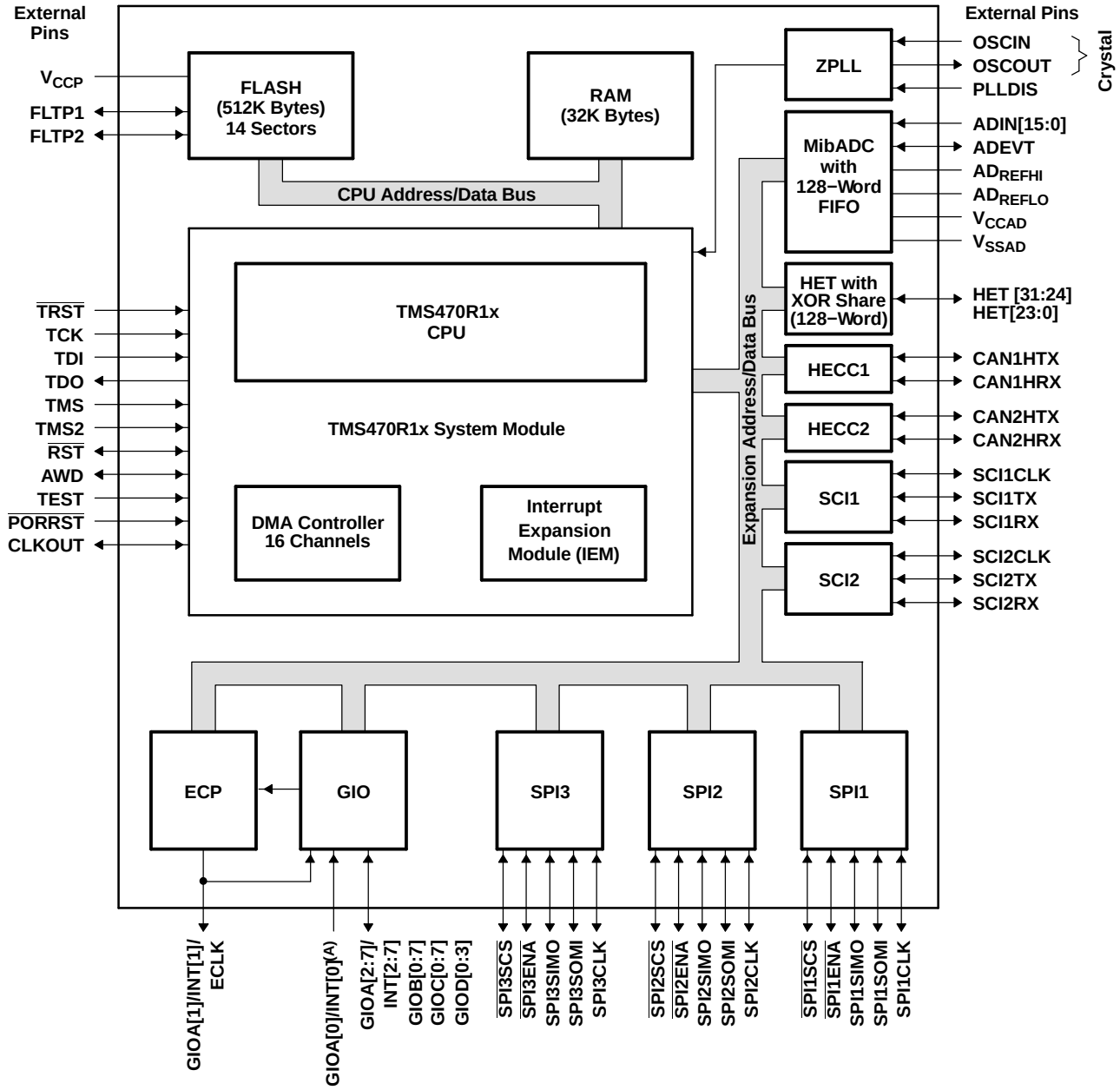
The B512 device is a derivative of the F05 system emulation device SE470R1VB8AD. Table 1 identifies all the characteristics of the B512 device except the SYSTEM and CPU, which are generic.

Table 1. Device Characteristics

CHARACTERISTICS	DEVICE DESCRIPTION TMS470R1B512	COMMENTS
MEMORY		
For the number of memory selects on this device, see Table 3, *Memory Selection Assignment*.		
INTERNAL MEMORY	Pipeline/Non-Pipeline 512K-Byte flash 32K-Byte SRAM	Flash is pipeline-capable. The B512 RAM is implemented in one 32K array selected by two memory-select signals (see Table 3, *Memory Selection Assignment*).
PERIPHERALS		
For the device-specific interrupt priority configurations, see Table 7, *Interrupt Priority (IEM and CIM)*. And for the 1K peripheral address ranges and their peripheral selects, see Table 5, *A512 Peripherals, System Module, and Flash Base Addresses*.		
CLOCK	ZPLL	Zero-pin PLL has no external loop filter pins.
GENERAL-PURPOSE I/Os	27 I/O 1 Input only	Ports A, B, and C each have eight (8) external pins. Port D has four (4) external pins.
ECP	YES	
SCI	2 (3-pin)	SCI1 and SCI2
CAN (HECC and/or SCC)	2 HECCs	Two high-end CAN controller modules (HECC1 and HECC2)
SPI (5-pin, 4-pin or 3-pin)	3 (5-pin)	SPI1, SPI2, and SPI3
HET with XOR Share	32 I/O	The B512 device has both the logic and registers for a full 32-I/O HET implemented and all 32 pins are available externally. The high-resolution (HR) SHARE feature allows even HR pins to share the next higher odd HR pin structures. This HR sharing is independent of whether or not the odd pin is available externally. If an odd pin is available externally and shared, then the odd pin can only be used as a general-purpose I/O. For more information on HR SHARE, see the *TMS470R1x High-End Timer (HET) Reference Guide* (literature number SPNU199).
HET RAM	128-Instruction Capacity	
MibADC	10-bit, 16-channel 128-word FIFO	The B512 device has both the logic and registers for a full 16-channel MibADC implemented and all 16 pins are available externally.
CORE VOLTAGE	1.81 – 2.05 V	
I/O VOLTAGE	3.0 – 3.6 V	
PINS	144	
PACKAGE	PGE	

ADVANCE INFORMATION

Functional Block Diagram



A. GIOA[0]/INT0 is an input-only pin.

Table 2. Terminal Functions

TERMINAL		TYPE(1)(2)	INTERNAL PULLUP/ PULLDOWN(3)	DESCRIPTION
NAME	NO.			
HIGH-END TIMER (HET)				
HET[0]	129	3.3-V I/O	IPD (20 µA)	The B512 device has both the logic and registers for a full 32-I/O HET implemented and all 32 pins are available externally. Timer input capture or output compare. The HET[31:0] applicable pins can be programmed as general-purpose input/output (GIO) pins. HET[23:0] are high-resolution pins and HET[31:24] are standard-resolution pins. The high-resolution (HR) SHARE feature allows even HR pins to share the next higher odd HR pin structures. This HR sharing is independent of whether or not the odd pin is available externally. If an odd pin is available externally and shared, then the odd pin can only be used as a general-purpose I/O. For more information on HR SHARE, see the *TMS470R1x High-End Timer (HET) Reference Guide* (literature number SPNU199).
HET[1]	130			
HET[2]	137			
HET[3]	138			
HET[4]	139			
HET[5]	140			
HET[6]	141			
HET[7]	142			
HET[8]	79			
HET[9]	80			
HET[10]	29			
HET[11]	28			
HET[12]	27			
HET[13]	26			
HET[14]	25			
HET[15]	24			
HET[16]	23			
HET[17]	22			
HET[18]	71			
HET[19]	70			
HET[20]	69			
HET[21]	68			
HET[22]	67			
HET[23]	123			
HET[24]	51			
HET[25]	124			
HET[26]	125			
HET[27]	126			
HET[28]	47			
HET[29]	48			
HET[30]	49			
HET[31]	50			
HIGH-END CAN CONTROLLER 1 (HECC1)				
CAN1HTX	88	3.3-V I/O	IPU (20 µA)	HECC1 transmit pin or GIO pin
CAN1HRX	87	3.3-V I/O		HECC1 receive pin or GIO pin
HIGH-END CAN CONTROLLER 2 (HECC2)				
CAN2HTX	56	3.3-V I/O	IPU (20 µA)	HECC2 transmit pin or GIO pin
CAN2HRX	57	3.3-V I/O		HECC2 receive pin or GIO pin

(1) I = input, O = output, PWR = power, GND = ground, REF = reference voltage, NC = no connect
(2) All I/O pins, except $\overline{\text{RST}}$, are configured as inputs while $\overline{\text{PORRST}}$ is low and immediately after $\overline{\text{PORRST}}$ goes high.
(3) IPD = internal pulldown, IPU = internal pullup (all internal pullups and pulldowns are active on input pins, independent of the $\overline{\text{PORRST}}$ state.)

ADVANCE INFORMATION

Table 2. Terminal Functions (continued)

TERMINAL		TYPE[1][2]	INTERNAL PULLUP/ PULLDOWN[3]	DESCRIPTION
NAME	NO.			
GENERAL-PURPOSE I/O (GIO)				
GIOA[0]/INT0	39	3.3-V I	IPD (20 µA)	General-purpose input/output pins. GIOA[0]/INT[0] is an input-only pin. GIOA[7:0]/INT[7:0] are interrupt-capable pins. The GIOA[1]/INT[1]/ECLK pin is multiplexed with the external clock-out function of the external clock prescale (ECP) module.
GIOA[1]/INT1/ECLK	40	3.3-V I/O		
GIOA[2]/INT2	41			
GIOA[3]/INT3	42			
GIOA[4]/INT4	36			
GIOA[5]/INT5	35			
GIOA[6]/INT6	34			
GIOA[7]/INT7	33			
GIOB[0]	46			
GIOB[1]	58			
GIOB[2]	59			
GIOB[3]	60			
GIOB[4]	61			
GIOB[5]	77			
GIOB[6]	78			
GIOB[7]	84			
GIOC[0]	122			
GIOC[1]	143			
GIOC[2]	144			
GIOC[3]	6			
GIOC[4]	7			
GIOC[5]	8			
GIOC[6]	9			
GIOC[7]	10			
GIOD[0]	21			
GIOD[1]	20			
GIOD[2]	19			
GIOD[3]	18			
MULTI-BUFFERED ANALOG-TO-DIGITAL CONVERTER (MibADC)				
ADEVT	99	3.3-V I/O	IPD (20 µA)	MibADC event input. ADEVT can be programmed as a GIO pin.
ADIN[0]	108	3.3-V I		MibADC analog input pins
ADIN[1]	107			
ADIN[2]	106			
ADIN[3]	105			
ADIN[4]	104			
ADIN[5]	102			
ADIN[6]	101			
ADIN[7]	100			
ADIN[8]	115			
ADIN[9]	113			
ADIN[10]	111			
ADIN[11]	109			
ADIN[12]	114			

Table 2. Terminal Functions (continued)

TERMINAL		TYPE[1][2]	INTERNAL PULLUP/ PULLDOWN[3]	DESCRIPTION
NAME	NO.			
MULTI-BUFFERED ANALOG-TO-DIGITAL CONVERTER (MibADC) (CONTINUED)				
ADIN[13]	112	3.3-V I		MibADC analog input pins
ADIN[14]	110			
ADIN[15]	103			
AD_{REFHI}	116	3.3-V REF I		MibADC module high-voltage reference input
AD_{REFLO}	117	GND REF I		MibADC module low-voltage reference input
V_{CCAD}	118	3.3-V PWR		MibADC analog supply voltage
V_{SSAD}	119	GND		MibADC analog ground reference
SERIAL PERIPHERAL INTERFACE 1 (SPI1)				
SPI1CLK	5	3.3-V I/O	IPD (20 µA)	SPI1 clock. SPI1CLK can be programmed as a GIO pin.
$\overline{\text{SPI1ENA}}$	1			SPI1 chip enable. $\overline{\text{SPI1ENA}}$ can be programmed as a GIO pin.
$\overline{\text{SPI1SCS}}$	2			SPI1 slave chip select. $\overline{\text{SPI1SCS}}$ can be programmed as a GIO pin.
SPI1SIMO	3			SPI1 data stream. Slave in/master out. SPI1SIMO can be programmed as a GIO pin.
SPI1SOMI	4			SPI1 data stream. Slave out/master in. SPI1SOMI can be programmed as a GIO pin.
SERIAL PERIPHERAL INTERFACE 2 (SPI2)				
SPI2CLK	62	3.3-V I/O	IPD (20 µA)	SPI2 clock. SPI2CLK can be programmed as a GIO pin.
$\overline{\text{SPI2ENA}}$	65			SPI2 chip enable. $\overline{\text{SPI2ENA}}$ can be programmed as a GIO pin.
$\overline{\text{SPI2SCS}}$	66			SPI2 slave chip select. $\overline{\text{SPI2SCS}}$ can be programmed as a GIO pin.
SPI2SIMO	63			SPI2 data stream. Slave in/master out. SPI2SIMO can be programmed as a GIO pin.
SPI2SOMI	64			SPI2 data stream. Slave out/master in. SPI2SOMI can be programmed as a GIO pin.
SERIAL PERIPHERAL INTERFACE 3 (SPI3)				
SPI3CLK	94	3.3-V I/O	IPD (20 µA)	SPI3 clock. SPI3CLK can be programmed as a GIO pin.
$\overline{\text{SPI3ENA}}$	98			SPI3 chip enable. $\overline{\text{SPI3ENA}}$ can be programmed as a GIO pin.
$\overline{\text{SPI3SCS}}$	97			SPI3 slave chip select. $\overline{\text{SPI3SCS}}$ can be programmed as a GIO pin.
SPI3SIMO	96			SPI3 data stream. Slave in/master out. SPI3SIMO can be programmed as a GIO pin.
SPI3SOMI	95			SP3 data stream. Slave out/master in. SPI3SOMI can be programmed as a GIO pin.
ZERO-PIN PHASE-LOCKED LOOP (ZPLL)				
OSCIN	13	1.8-V I		Crystal connection pin or external clock input
OSCOUT	12	1.8-V O		External crystal connection pin
PLLDIS	73	3.3-V I	IPD (20 µA)	Enable/disable the ZPLL. The ZPLL can be bypassed and the oscillator becomes the system clock. If not in bypass mode, TI recommends that this pin be connected to ground or pulled down to ground by an external resistor.
SERIAL COMMUNICATIONS INTERFACE 1 (SCI1)				
SCI1CLK	89	3.3-V I/O	IPD (20 µA)	SCI1 clock. SCI1CLK can be programmed as a GIO pin.
SCI1RX	91	3.3-V I/O	IPU (20 µA)	SCI1 data receive. SCI1RX can be programmed as a GIO pin.
SCI1TX	90	3.3-V I/O	IPU (20 µA)	SCI1 data transmit. SCI1TX can be programmed as a GIO pin.
SERIAL COMMUNICATIONS INTERFACE 2 (SCI2)				
SCI2CLK	45	3.3-V I/O	IPD (20 µA)	SCI2 clock. SCI2CLK can be programmed as a GIO pin.
SCI2RX	43	3.3-V I/O	IPU (20 µA)	SCI2 data receive. SCI2RX can be programmed as a GIO pin.
SCI2TX	44	3.3-V I/O	IPU (20 µA)	SCI2 data transmit. SCI2TX can be programmed as a GIO pin.

Table 2. Terminal Functions (continued)

TERMINAL		TYPE(1)(2)	INTERNAL PULLUP/ PULLDOWN(3)	DESCRIPTION
NAME	NO.			
SYSTEM MODULE (SYS)				
CLKOUT	83	3.3-V I/O	IPD (20 μA)	Bidirectional pin. CLKOUT can be programmed as a GIO pin or the output of SYSCLK, ICLK, or MCLK.
$\overline{\text{PORRST}}$	32	3.3-V I	IPD (20 μA)	Input master chip power-up reset. External V CC monitor circuitry must assert a power-on reset.
$\overline{\text{RST}}$	15	3.3-V I/O	IPU (20 μA)	Bidirectional reset. The internal circuitry can assert a reset, and an external system reset can assert a device reset. On this pin, the output buffer is implemented as an open drain (drives low only). To ensure an external reset is not arbitrarily generated, TI recommends that an external pullup resistor be connected to this pin.
WATCHDOG/REAL-TIME INTERRUPT (WD/RTI)				
AWD	72	3.3-V I/O	IPD (20 μA)	Analog watchdog reset. The AWD pin provides a system reset if the WD KEY is not written in time by the system, providing an external RC network circuit is connected. If the user is not using AWD, TI recommends that this pin be connected to ground or pulled down to ground by an external resistor. For more details on the external RC network circuit, see the TMS470R1x System Module Reference Guide (literature number SPNU189).
TEST/DEBUG (T/D)				
TCK	76	3.3-V I	IPD (20 μA)	Test clock. TCK controls the test hardware (JTAG)
TDI	74	3.3-V I	IPU (20 μA)	Test data in. TDI inputs serial data to the test instruction register, test data register, and programmable test address (JTAG).
TDO	75	3.3-V O	IPD (20 μA)	Test data out. TDO outputs serial data from the test instruction register, test data register, identification register, and programmable test address (JTAG).
TEST	38	3.3-V I	IPD (20 μA)	Test enable. Reserved for internal use only. TI recommends that this pin be connected to ground or pulled down to ground by an external resistor.
TMS	120	3.3-V I	IPU (20 μA)	Serial input for controlling the state of the CPU test access port (TAP) controller (JTAG)
TMS2	121	3.3-V I	IPU (20 μA)	Serial input for controlling the second TAP. TI recommends that this pin be connected to VCCIO or pulled up to VCCIO by an external resistor.
$\overline{\text{TRST}}$	37	3.3-V I	IPD (20 μA)	Test hardware reset to TAP1 and TAP2. IEEE Standard 1149-1 (JTAG) Boundary-Scan Logic. TI recommends that this pin be pulled down to ground by an external resistor.
FLASH				
FLTP1	134	NC		Flash test pad 1. **For proper operation, this pin must not be connected [no connect (NC)].**
FLTP2	133	NC		Flash test pad 2. **For proper operation, this pin must not be connected [no connect (NC)].**
V_{CCP}	135	3.3-V PWR		Flash external pump voltage (3.3 V). This pin is required for both flash read and flash program and erase operations.
SUPPLY VOLTAGE CORE (1.8 V)				
V_{CC}	14 31 55 86 93 128 132	1.8-V PWR		Core logic supply voltage

Table 2. Terminal Functions (continued)

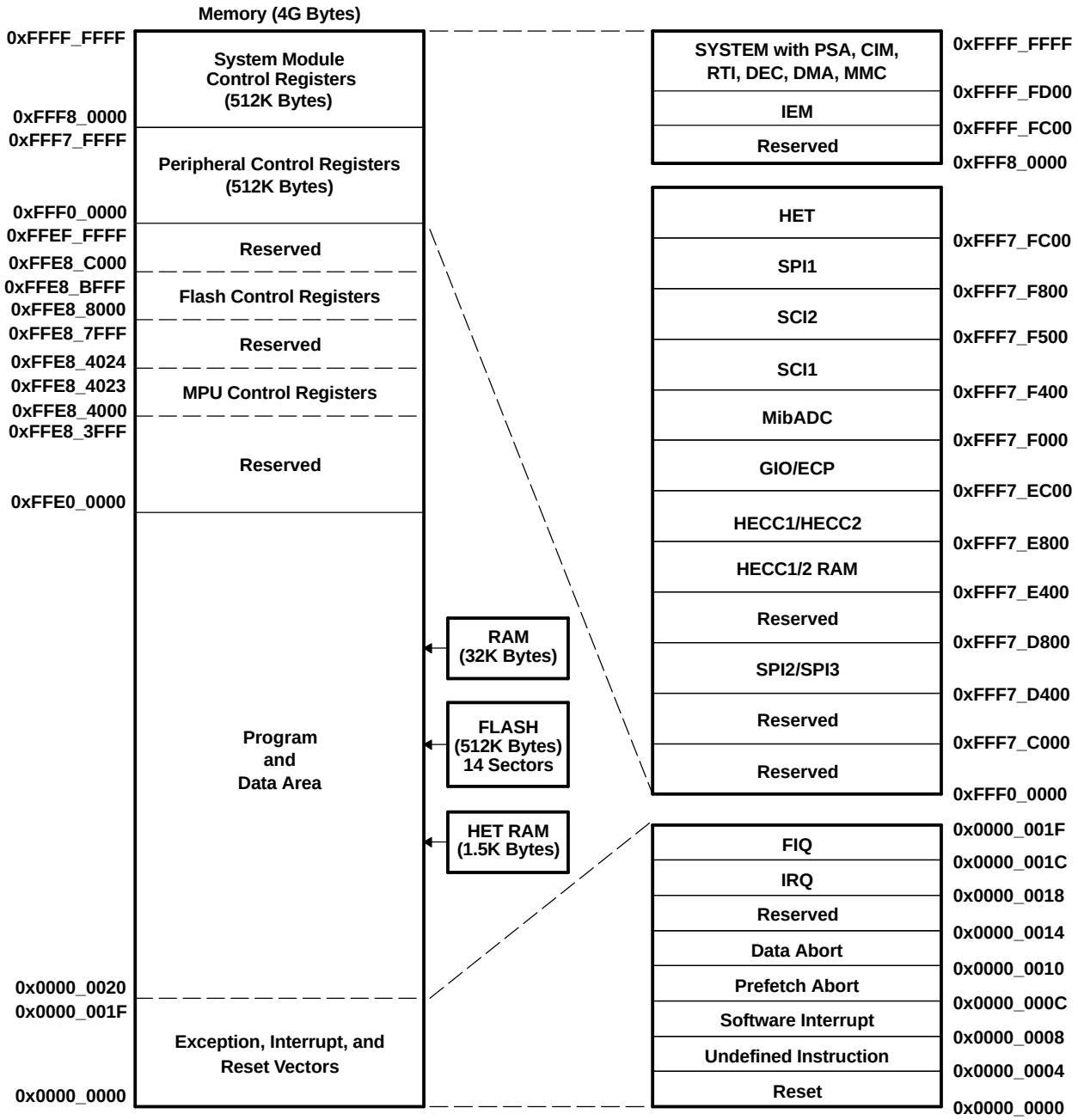
TERMINAL		TYPE(1)(2)	INTERNAL PULLUP/ PULLDOWN(3)	DESCRIPTION
NAME	NO.			
SUPPLY VOLTAGE DIGITAL I/O (3.3 V)				
V_{CCIO}	17	3.3-V PWR		Digital I/O supply voltage
	53			
	82			
SUPPLY GROUND CORE				
V_{SS}	11	GND		Core supply ground reference
	30			
	54			
	85			
	92			
	127			
	131			
	136			
SUPPLY GROUND DIGITAL I/O				
V_{SSIO}	16	GND		Digital I/O supply ground reference
	52			
	81			

ADVANCE INFORMATION

B512 Device-Specific Information

Memory

Figure 1 shows the memory map of the B512 device.



A. Memory addresses are configurable by the system (SYS) module within the range of 0x0000_0000 to 0xFFE0_0000.

B. The CPU registers are not a part of the memory map.

Figure 1. Memory Map

Memory Selects

Memory selects allow the user to address memory arrays (i.e., flash, RAM, and HET RAM) at user-defined addresses. Each memory select has its own set (low and high) of memory base address registers (MFBAHRx and MFBALRx) that, together, define the array's starting (base) address, block size, and protection.

The base address of each memory select is configurable to any memory address boundary that is a multiple of the decoded block size. For more information on how to control and configure these memory select registers, see the bus structure and memory sections of the *TMS470R1x System Module Reference Guide* (literature number SPNU189).

For the memory selection assignments and the memory selected, see Table 3.

Table 3. Memory Selection Assignment

MEMORY SELECT	MEMORY SELECTED (ALL INTERNAL)	MEMORY SIZE	MPU	MEMORY BASE ADDRESS REGISTER	STATIC MEM CTL REGISTER
0 (fine)	FLASH	512K	NO	MFBAHR0 and MFBALR0	
1 (fine)	FLASH		NO	MFBAHR1 and MFBALR1	
2 (fine)	RAM	32K(1)	YES	MFBAHR2 and MFBALR2	
3 (fine)	RAM		YES	MFBAHR3 and MFBALR3	
4 (fine)	HET RAM	1.5K		MFBAHR4 and MFBALR4	SMCR1

(1) The starting addresses for both RAM memory-select signals cannot be offset from each other by a multiple of the user-defined block size in the memory-base address register.

RAM

The B512 device contains 32K bytes of internal static RAM configurable by the SYS module to be addressed within the range of 0x0000_0000 to 0xFFE0_0000. This B512 RAM is implemented in one 32K array selected by two memory-select signals. This B512 configuration imposes an additional constraint on the memory map for RAM; the starting addresses for both RAM memory selects cannot be offset from each other by the multiples of the size of the physical RAM (i.e., 32K for the B512 device). The B512 RAM is addressed through memory selects 2 and 3.

The RAM can be protected by the memory protection unit (MPU) portion of the SYS module, allowing the user finer blocks of memory protection than is allowed by the memory selects. The MPU is ideal for protecting an operating system while allowing access to the current task. For more detailed information on the MPU portion of the SYS module and memory protection, see the memory section of the *TMS470R1x System Module Reference Guide* (literature number SPNU189).

F05 Flash

The F05 flash memory is a nonvolatile electrically erasable and programmable memory implemented with a 32-bit-wide data bus interface. The F05 flash has an external state machine for program and erase functions. See the flash read and flash program and erase sections below. For more detailed functional information on the F05 flash module, see the *TMS470R1x F05 Flash Reference Guide* (literature number SPNU213).

Flash Protection Keys

The B512 device provides flash protection keys. These four 32-bit protection keys prevent program/erase/compaction operations from occurring until after the four protection keys have been matched by the CPU loading the correct user keys into the FMPKEY control register. The protection keys on the B512 are located in the last 4 words of the first 16K sector. For more detailed information on the flash protection keys and the FMPKEY control register, see the "Optional Quadruple Protection Keys" and "Programming the Protection Keys" portions of the *TMS470R1x F05 Flash Reference Guide* (literature number SPNU213).

Flash Read

The B512 flash memory is configurable by the SYS module to be addressed within the range of 0x0000_0000 to 0xFFE0_0000. The flash is addressed through memory selects 0 and 1.

NOTE:

The flash external pump voltage (V_{CCP}) is required for all operations (program, erase, and read).

Flash Pipeline Mode

When in pipeline mode, the flash operates with a system clock frequency of up to 60 MHz. In normal mode, the flash operates with a system clock frequency in normal mode of up to 24 MHz. Flash in pipeline mode is capable of accessing 64-bit words and provides two 32-bit pipelined words to the CPU. Also in pipeline mode, the flash can be read with no wait states when memory addresses are contiguous (after the initial 1-or 2-wait-state reads).

NOTE:

After a system reset, pipeline mode is disabled (FMREGOPT[0] = 0). In other words, the B512 device powers up and comes out of reset in non-pipeline mode. Furthermore, setting the flash configuration mode bit (GBLCTRL[4]) will override pipeline mode.

Flash Program and Erase

The B512 device flash contains two 256K-byte memory arrays (or banks) for a total of 512K bytes of flash and consists of fourteen sectors. These fourteen sectors are sized as follows:

Table 4. B512 Flash Memory Banks and Sectors

SECTOR NO.	SEGMENT	LOW ADDRESS	HIGH ADDRESS	MEMORY ARRAYS (OR BANKS)
0	16K Bytes	0x00000000	0x00003FFF	BANK0 (256K Bytes)
1	16K Bytes	0x00004000	0x00007FFF	
2	32K Bytes	0x00008000	0x0000FFFF	
3	32K Bytes	0x00010000	0x00017FFF	
4	32K Bytes	0x00018000	0x0001FFFF	
5	32K Bytes	0x00020000	0x00027FFF	
6	32K Bytes	0x00028000	0x0002FFFF	
7	32K Bytes	0x00030000	0x00037FFF	
8	16K Bytes	0x00038000	0x0003BFFF	
9	16K Bytes	0x0003C000	0x0003FFFF	
0	64K Bytes	0x00040000	0x0004FFFF	BANK1 (256K Bytes)
1	64K Bytes	0x00050000	0x0005FFFF	
2	64K Bytes	0x00060000	0x0006FFFF	
3	64K Bytes	0x00070000	0x0007FFFF	

The minimum size for an erase operation is one sector. The maximum size for a program operation is one 16-bit word.

NOTE:

The flash external pump voltage (V_{CCP}) is required for all operations (program, erase, and read).

For more detailed information on flash program and erase operations, see the *TMS470R1x F05 Flash Reference Guide* (literature number SPNU213).

HET RAM

The B512 device contains HET RAM. The HET RAM has a 128-instruction capability. The HET RAM is configurable by the SYS module to be addressed within the range of 0x0000_0000 to 0xFFE0_0000. The HET RAM is addressed through memory select 4.

Peripheral Selects and Base Addresses

The B512 device uses 8 of the 16 peripheral selects to decode the base addresses of the peripherals. These peripheral selects are fixed and transparent to the user since they are part of the decoding scheme used by the SYS module. Control registers for the peripherals, SYS module, and flash begin at the base addresses shown in Table 5.

Table 5. B512 Peripherals, System Module, and Flash Base Addresses

CONNECTING MODULE	ADDRESS RANGE		PERIPHERAL SELECTS
	BASE ADDRESS	ENDING ADDRESS	
SYSTEM	0 x FFFF_FFD0	0 x FFFF_FFFF	N/A
RESERVED	0 x FFFF_FF60	0 x FFFF_FFCF	N/A
PSA	0 x FFFF_FF40	0 x FFFF_FF5F	N/A
CIM	0 x FFFF_FF20	0 x FFFF_FF3F	N/A
RTI	0 x FFFF_FF00	0 x FFFF_FF1F	N/A
DMA	0 x FFFF_FE80	0 x FFFF_FEFF	N/A
DEC	0 x FFFF_FE00	0 x FFFF_FE7F	N/A
MMC	0 x FFFF_FD00	0 x FFFF_FD7F	N/A
IEM	0 x FFFF_FC00	0 x FFFF_FCFF	N/A
RESERVED	0 x FFFF_FB00	0 X FFFF_FBFF	N/A
RESERVED	0 x FFFF_FA00	0 X FFFF_FAFF	N/A
DMA CMD BUFFER	0 x FFFF_F800	0 x FFFF_F9FF	N/A
RESERVED	0 x FFF8_0000	0 x FFFF_F7FF	N/A
RESERVED	0 x FFF7_FD00	0 x FFF7_FFFF	PS[0]
HET	0 x FFF7_FC00	0 x FFF7_FCFF	
RESERVED	0 x FFF7_F900	0 x FFF7_FBFF	PS[1]
SPI1	0 x FFF7_F800	0 x FFF7_F8FF	
RESERVED	0 x FFF7_F600	0 x FFF7_F7FF	PS[2]
SCI2	0 x FFF7_F500	0 X FFF7_F5FF	
SCI1	0 x FFF7_F400	0 x FFF7_F4FF	
RESERVED	0 x FFF7_F100	0 x FFF7_F3FF	PS[3]
MibADC	0 x FFF7_F000	0 x FFF7_F0FF	
ECP	0 x FFF7_EF00	0 x FFF7_EFFF	PS[4]
RESERVED	0 x FFF7_ED00	0 x FFF7_EEFF	
GIO	0 x FFF7_EC00	0 x FFF7_ECFF	
HECC2	0 x FFF7_EA00	0 x FFF7_EBFF	PS[5]
HECC1	0 x FFF7_E800	0 x FFF7_E9FF	
HECC2 RAM	0 x FFF7_E600	0 x FFF7_E7FF	PS[6]
HECC1 RAM	0 x FFF7_E400	0 x FFF7_E5FF	
RESERVED	0 x FFF7_E000	0 x FFF7_E3FF	PS[7]
RESERVED	0 x FFF7_DC00	0 x FFF7_DFFF	PS[8]
RESERVED	0 x FFF7_D800	0 x FFF7_DBFF	PS[9]
RESERVED	0 x FFF7_D600	0 x FFF7_D7FF	PS[10]
SPI3	0 x FFF7_D500	0 x FFF7_D5FF	
SPI2	0 x FFF7_D400	0 x FFF7_D4FF	
RESERVED	0 x FFF7_C000	0 x FFF7_D3FF	PS[11] – PS[15]

Table 5. B512 Peripherals, System Module, and Flash Base Addresses (continued)

CONNECTING MODULE	ADDRESS RANGE		PERIPHERAL SELECTS
	BASE ADDRESS	ENDING ADDRESS	
RESERVED	0 x FFF0_0000	0 x FFF7_BFFF	N/A
FLASH CONTROL REGISTERS	0 x FFE8_8000	0 x FFE8_BFFF	N/A
MPU CONTROL REGISTERS	0 x FFE8_4000	0 x FFE8_4023	N/A

Direct-Memory Access (DMA)

The direct-memory access (DMA) controller transfers data to and from any specified location in the B512 memory map (except for restricted memory locations like the system control registers area). The DMA manages up to 16 channels, and supports data transfer for both on-chip and off-chip memories and peripherals. The DMA controller is connected to both the CPU and Peripheral busses, enabling these data transfers to occur in parallel with CPU activity and thus, maximizing overall system performance.

Although the DMA controller has two possible configurations, for the B512 device, the DMA controller configuration is 32 control packets and 16 channels. For the B512 DMA request hardwired configuration, see Table 6. For a more detailed functional description of the DMA module, see the *TMS470R1x Direct Memory Access (DMA) Controller Reference Guide* (literature number SPNU194).

Table 6. DMA Request Lines Connections

MODULES	DMA REQUEST INTERRUPT SOURCES		DMA CHANNEL
RESERVED			DMAREQ[0]
SPI1	SPI1 end-receive	SPI1DMA0	DMAREQ[1]
SPI1	SPI1 end-transmit	SPI1DMA1	DMAREQ[2]
MibADC(1)	MibADC event	MibADCDMA0	DMAREQ[3]
MibADC(1)/SCI1	MibADC G1/SCI1 end-receive	MibADCDMA1/SCI1DMA0	DMAREQ[4]
MibADC(1)/SCI1	MibADC G2/SCI1 end-transmit	MibADCDMA2/SCI1DMA1	DMAREQ[5]
RESERVED			DMAREQ[6]
SPI2	SPI2 end-receive	SPI2DMA0	DMAREQ[7]
SPI2	SPI2 end-transmit	SPI2DMA1	DMAREQ[8]
RESERVED			DMAREQ[9]
RESERVED			DMAREQ[10]
RESERVED			DMAREQ[11]
RESERVED			DMAREQ[12]
RESERVED			DMAREQ[13]
SCI2/SPI3	SCI2 end-receive/SPI3 end-receive	SCI2DMA0/SPI3DMA0	DMAREQ[14]
SCI2/SPI3	SCI2 end-transmit/SPI3 end-transmit	SCI2DMA1/SPI3DMA1	DMAREQ[15]

(1) The MibADC is capable of being serviced by the DMA when the device is in buffered mode. For more information on buffered mode, see the MibADC section of this data sheet and the *TMS470R1x Multi-Buffered Analog-to-Digital Converter (MibADC) Reference Guide* (literature number SPNU206).

Each channel has two control packets attached to it, allowing the DMA to continuously load RAM and generate periodic interrupts so that the data can be read by the CPU. The control packets allow for the interrupt enable, and the channels determine the priority level of the interrupt.

DMA transfers occur in one of two modes:

- Non-request mode (used when transferring from memory to memory)
- Request mode (used when transferring from memory to peripheral)

For more detailed functional information on the DMA controller, see the *TMS470R1x Direct Memory Access (DMA) Controller Reference Guide* (literature number SPNU194).

Interrupt Priority (IEM to CIM)

Interrupt requests originating from the B512 peripheral modules (i.e., SPI1, SPI2, or SPI3; SCI1 or SCI2; HECC1 or HECC2; RTI; etc.) are assigned to channels within the 48-channel interrupt expansion module (IEM) where, via programmable register mapping, these channels are then mapped to the 32-channel central interrupt manager (CIM) portion of the SYS module.

Programming multiple interrupt sources in the IEM to the same CIM channel effectively shares the CIM channel between sources.

The CIM request channels are maskable so that individual channels can be selectively disabled. All interrupt requests can be programmed in the CIM to be of either type:

- Fast interrupt request (FIQ)
- Normal interrupt request (IRQ)

The CIM prioritizes interrupts. The precedences of request channels decrease with ascending channel order in the CIM (0 [highest] and 31 [lowest] priority). For IEM-to-CIM default mapping, channel priorities, and their associated modules, see Table 7.

Table 7. Interrupt Priority (IEM and CIM)

MODULES	INTERRUPT SOURCES	DEFAULT CIM INTERRUPT LEVEL/CHANNEL	IEM CHANNEL
SPI1	SPI1 end-transfer/overrun	0	0
RTI	COMP2 interrupt	1	1
RTI	COMP1 interrupt	2	2
RTI	TAP interrupt	3	3
SPI2	SPI2 end-transfer/overrun	4	4
GIO	GIO interrupt A	5	5
RESERVED		6	6
HET	HET interrupt 1	7	7
RESERVED		8	8
SCI1/SCI2	SCI1 or SCI2 error interrupt	9	9
SCI1	SCI1 receive interrupt	10	10
RESERVED		11	11
RESERVED		12	12
HECC1	HECC1 interrupt A	13	13
RESERVED		14	14
SPI3	SPI3 end-transfer/overrun	15	15
MibADC	MibADC end event conversion	16	16
SCI2	SCI2 receive interrupt	17	17
DMA	DMA interrupt 0	18	18
RESERVED		19	19
SCI1	SCI1 transmit interrupt	20	20
System	SW interrupt (SSI)	21	21
RESERVED		22	22
HET	HET interrupt 2	23	23
HECC1	HECC1 interrupt B	24	24
RESERVED		25	25
SCI2	SCI2 transmit interrupt	26	26
MibADC	MibADC end Group 1 conversion	27	27
DMA	DMA interrupt 1	28	28
GIO	GIO interrupt B	29	29
MibADC	MibADC end Group 2 conversion	30	30
RESERVED		31	31

Table 7. Interrupt Priority (IEM and CIM) (continued)

MODULES	INTERRUPT SOURCES	DEFAULT CIM INTERRUPT LEVEL/CHANNEL	IEM CHANNEL
RESERVED		31	32
RESERVED		31	33
RESERVED		31	34
RESERVED		31	35
RESERVED		31	36
RESERVED		31	37
HECC2	HECC2 interrupt A	31	38
HECC2	HECC2 interrupt B	31	39
RESERVED		31	40
RESERVED		31	41
RESERVED		31	42
RESERVED		31	43
RESERVED		31	44
RESERVED		31	45
RESERVED		31	46
RESERVED		31	47

For more detailed functional information on the IEM, see the *TMS470R1x Interrupt Expansion Module (IEM) Reference Guide* (literature number SPNU211). For more detailed functional information on the CIM, see the *TMS470R1x System Module Reference Guide* (literature number SPNU189).

MibADC

The multi-buffered analog-to-digital converter (MibADC) accepts an analog signal and converts the signal to a 10-bit digital value.

The B512 MibADC module can function in two modes: compatibility mode, where its programmer's model is compatible with the TMS470R1x ADC module and its digital results are stored in digital result registers; or in buffered mode, where the digital result registers are replaced with three FIFO buffers, one for each conversion group [event, group1 (G1), and group2 (G2)]. In buffered mode, the MibADC buffers can be serviced by interrupts or by the DMA.

MibADC Event Trigger Enhancements

The MibADC includes two major enhancements over the event-triggering capability of the TMS470R1x ADC.

- Both group1 and the event group can be configured for event-triggered operation, providing up to two event-triggered groups.
- The trigger source and polarity can be selected individually for both group 1 and the event group from the three options identified in Table 8.

Table 8. MibADC Event Hookup Configuration

EVENT NO.	SOURCE SELECT BITS FOR G1 OR EVENT (G1SRC[1:0] OR EVSRC[1:0])	SIGNAL PIN NAME
EVENT1	00	ADEVT
EVENT2	01	HET18
EVENT3	10	HET19
EVENT4	11	RESERVED

For group 1, these event-triggered selections are configured via the group 1 source select bits (G1SRC[1:0]) in the AD event source register (ADEVTSRC[5:4]). For the event group, these event-triggered selections are configured via the event group source select bits (EVSRC[1:0]) in the AD event source register (ADEVTSRC[1:0]).

For more detailed functional information on the MibADC, see the *TMS470R1x Multi-Buffered Analog-to-Digital Converter (MibADC) Reference Guide* (literature number SPNU206).

Documentation Support

Extensive documentation supports all of the TMS470 microcontroller family generation of devices. The types of documentation available include: data sheets with design specifications; complete user's guides for all devices and development support tools; and hardware and software applications. Useful reference documentation includes:

- Bulletin
  - *TMS470 Microcontroller Family Product Bulletin* (literature number SPNB086)
- User's Guides
  - *TMS470R1x System Module Reference Guide* (literature number SPNU189)
  - *TMS470R1x General Purpose Input/Output (GIO) Reference Guide* (literature number SPNU192)
  - *TMS470R1x Direct Memory Access (DMA) Controller Reference Guide* (literature number SPNU194)
  - *TMS470R1x Serial Peripheral Interface (SPI) Reference Guide* (literature number) SPNU195
  - *TMS470R1x Serial Communication Interface (SCI) Reference Guide* (literature number SPNU196)
  - *TMS470R1x Controller Area Network (CAN) Reference Guide* (literature number SPNU197)
  - *TMS470R1x High End Timer (HET) Reference Guide* (literature number SPNU199)
  - *TMS470R1x External Clock Prescale (ECP) Reference Guide* (literature number SPNU202)
  - *TMS470R1x MultiBuffered Analog to Digital (MibADC) Reference Guide* (literature number SPNU206)
  - *TMS470R1x ZeroPin Phase Locked Loop (ZPLL) Clock Module Reference Guide* (literature number SPNU212)
  - *TMS470R1x F05 Flash Reference Guide* (literature number SPNU213)
  - *TMS470R1x Class II Serial Interface B (C2SIb) Reference Guide* (literature number SPNU214)
  - *TMS470R1x Class II Serial Interface A (C2SIa) Reference Guide* (literature number SPNU218)
  - *TMS470R1x JTAG Security Module (JSM) Reference Guide* (literature number SPNU245)
  - *TMS470R1x Memory Security Module (MSM) Reference Guide* (literature number SPNU246)
  - *TMS470 Peripherals Overview Reference Guide* (literature number SPNU248)
- Errata Sheet
  - *TMS470R1B512 TMS470 Microcontrollers Silicon Errata* (literature number SPNZ141)

Device Numbering Conventions

Figure 2 illustrates the numbering and symbol nomenclature for the TMS470R1x family.

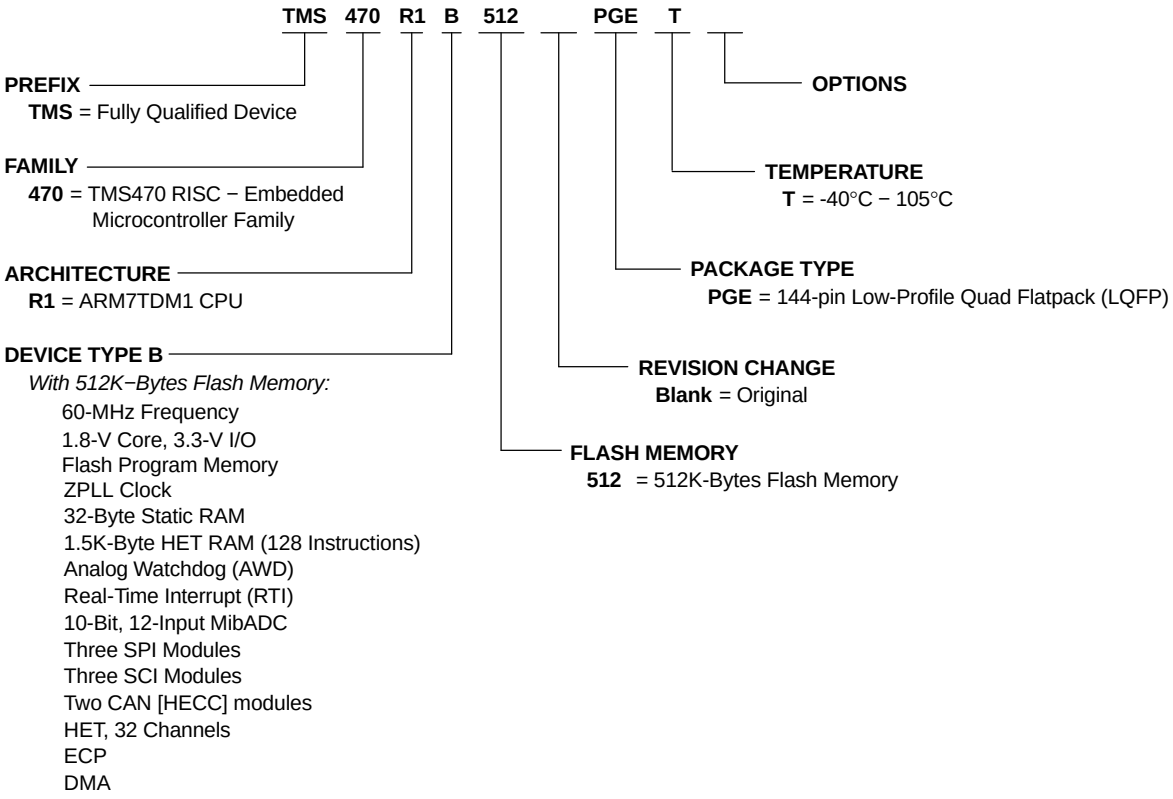


Figure 2. TMS470R1x Family Nomenclature

ADVANCE INFORMATION

Device Identification Code Register

The device identification code register identifies the silicon version, the technology family (TF), a ROM or flash device, and an assigned device-specific part number (see Figure 3). The B512 device identification code register value is 0xn92Fh.

Figure 3. TMS470 Device ID Bit Allocation Register [offset = FFFF_FFF0h]

31	16
Reserved	

15	12	11	10	9	3	2	1	0
VERSION		TF	R/F	PART NUMBER		1	1	1
R-K		R-K	R-K	R-K		R-1	R-1	R-1

LEGEND:
R = Read only, -K = Value constant after $\overline{\text{RST}}$; -*n* = Value after $\overline{\text{RST}}$

Table 9. TMS470 Device ID Bit Allocation Register Field Descriptions

Bit	Field	Value	Description
31-16	Reserved		Reads are undefined and writes have no effect.
15-12	VERSION		Silicon version (revision) bits. These bits identify the silicon version of the device. Initial device version numbers start at 0000. The current revision for the B512 device is 0010.
11	TF		Technology family bit. This bit distinguishes the technology family core power supply:
		0	3.3 V for F10/C10 devices
		1	1.8 V for F05/C05 devices
10	R/F		ROM/flash bit. This bit distinguishes between ROM and flash devices:
		0	Flash device
		1	ROM device
9-3	PART NUMBER		Device-specific part number bits. These bits identify the assigned device-specific part number. The assigned device-specific part number for the B512 device is 0100101.
2-0	1		Mandatory High. Bits 2, 1, and 0 are tied high by default.

ADVANCE INFORMATION

Device Electrical Specifications and Timing Parameters

Absolute Maximum Ratings

over operating free-air temperature range, T version (unless otherwise noted)(1)

Supply voltage range:	V_{CC} (2)	-0.3 V to 2.5 V
Supply voltage range:	V_{CCIO} , V_{CCAD} , V_{CCP} (flash pump)(2)	-0.3 V to 4.1V
Input voltage range:	All input pins	-0.3 V to 4.1V
Input clamp current:	I_{IK} (V_I < 0 or V_I > V_{CCIO})	
	All pins except ADIN[0:11], $\overline{\text{PORRST}}$, $\overline{\text{TRST}}$, TEST, and TCK	±20 mA
	I_{IK} (V_I < 0 or V_I > V_{CCAD})	
	ADIN[0:15]	±10 mA
Operating free-air temperature range, T_A: T version		-40°C to 105°C
Operating junction temperature ranges, T_J		-40°C to 150°C
Storage temperature range, T_{stg}		-65°C to 150°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to their associated grounds.

Device Recommended Operating Conditions(1)

			MIN	NOM	MAX	UNIT
V_{CC}	Digital logic supply voltage (Core)		1.81		2.05	V
V_{CCIO}	Digital logic supply voltage (I/O)		3	3.3	3.6	V
V_{CCAD}	MibADC supply voltage		3	3.3	3.6	V
V_{CCP}	Flash pump supply voltage		3	3.3	3.6	V
V_{SS}	Digital logic supply ground			0		V
V_{SSAD}	MibADC supply ground		-0.1		0.1	V
T_A	Operating free-air temperature	T version	-40		105	° C
T_J	Operating junction temperature		-40		150	° C

(1) All voltages are with respect to V_{SS}, except V_{CCAD}, which is with respect to V_{SSAD}.

ADVANCE INFORMATION

Electrical Characteristics

over recommended operating free-air temperature range, T version (unless otherwise noted)(1)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{hys}	Input hysteresis			0.15			V
V_{IL}	Low-level input voltage	All inputs(2) except OSCIN		-0.3		0.8	V
		OSCIN only		-0.3		0.35 V_{CC}	
V_{IH}	High-level input voltage	All inputs except OSCIN		2		V_{CCIO} + 0.3	V
		OSCIN only		0.65 V_{CC}		V_{CC} + 0.3	
V_{th}	Input threshold voltage	AWD only		1.35		1.8	V
RDS_{ON}	Drain to source on resistance	AWD only(3)	V_{OL} = 0.35 V @ I_{OL} = 8 mA			45	Ω
V_{OL}	Low-level output voltage(4)		I_{OL} = I_{OL} MAX			0.2 V_{CCIO}	V
			I_{OL} = 50 µA			0.2	
V_{OH}	High-level output voltage(4)		I_{OH} = I_{OH} MIN	0.8 V_{CCIO}			V
			I_{OH} = 50 µA	V_{CCIO} - 0.2			
I_{IC}	Input clamp current (I/O pins)(5)		V_I < V_{SSIO} - 0.3 or V_I > V_{CCIO} + 0.3	-2		2	mA
I_I	Input current (I/O pins)	I_{IL} Pulldown	V_I = V_{SS}	-1		1	µA
		I_{IH} Pulldown	V_I = V_{CCIO}	5		40	
		I_{IL} Pullup	V_I = V_{SS}	-40		-5	
		I_{IH} Pullup	V_I = V_{CCIO}	-1		1	
		All other pins	No pullup or pulldown	-1		1	
I_{OL}	Low-level output current	CLKOUT, AWD, TDO	V_{OL} = V_{OL} MAX			8	mA
		$\overline{RST}$, SPInCLK, SPInSOMI, SPInSIMO				4	
		All other output pins(6)				2	
I_{OH}	High-level output current	CLKOUT, TDO	V_{OH} = V_{OH} MIN	-8			mA
		$\overline{RST}$, SPInCLK, SPInSOMI, SPInSIMO		-4			
		All other output pins except $\overline{RST}$(6)		-2			
I_{CC}	V_{CC} Digital supply current (operating mode)		SYSCLK = 60 MHz, ICLK = 20 MHz, V_{CC} = 2.05 V			125	mA
			SYSCLK = 24 MHz, ICLK = 12 MHz, V_{CC} = 2.05 V			85	mA
	V_{CC} Digital supply current (standby mode)(7)		OSCIN = 6 MHz, V_{CC} = 2.05 V			4.0	mA
	V_{CC} Digital supply current (halt mode)(7)		All frequencies, V_{CC} = 2.05 V			2.0	mA

(1) Source currents (out of the device) are negative while sink currents (into the device) are positive.
(2) This does not apply to the $\overline{PORRST}$ pin. For $\overline{PORRST}$ exceptions, see the *$\overline{RST}$ and $\overline{PORRST}$ timings* section.
(3) These values help to determine the external RC network circuit. For more details, see the *TMS470R1x System Module Reference Guide* (literature number SPNU189).
(4) V_{OL} and V_{OH} are linear with respect to the amount of load current (I_{OL}/I_{OH}) applied.
(5) Parameter does not apply to input-only or output-only pins.
(6) The 2 mA buffers on this device are called zero-dominant buffers. If two of these buffers are shorted together and one is outputting a low level and the other is outputting a high level, the resulting value will always be low.
(7) For flash pumps/banks in sleep mode.

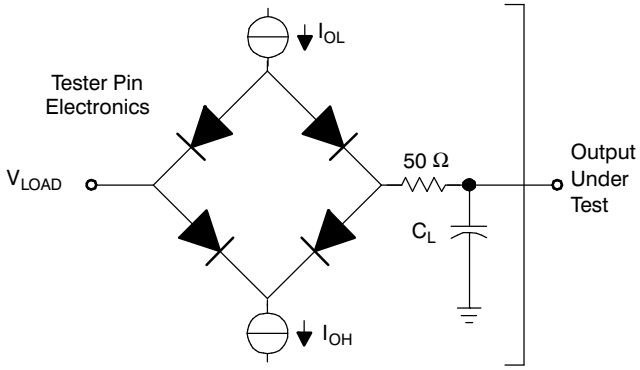
Electrical Characteristics (continued)

over recommended operating free-air temperature range, T version (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CCIO}	V_{CCIO} Digital supply current (operating mode)	No DC load, V_{CCIO} = 3.6 V(8)			10	mA
	V_{CCIO} Digital supply current (standby mode)	No DC load, V_{CCIO} = 3.6 V(8)			300	µA
	V_{CCIO} Digital supply current (halt mode)	No DC load, V_{CCIO} = 3.6 V(8)			300	µA
I_{CCAD}	V_{CCAD} supply current (operating mode)	All frequencies, V_{CCAD} = 3.6 V			15	mA
	V_{CCAD} supply current (standby mode)	All frequencies, V_{CCAD} = 3.6 V			20	µA
	V_{CCAD} supply current (halt mode)	All frequencies, V_{CCAD} = 3.6 V			20	µA
I_{CCP}	V_{CCP} pump supply current	V_{CCP} = 3.6 V read operation			55	mA
		V_{CCP} = 3.6 V program and erase			70	mA
		V_{CCP} = 3.6 V standby mode operation(7)			20	µA
		V_{CCP} = 3.6 V halt mode operation(7)			20	µA
C_I	Input capacitance			2		pF
C_O	Output capacitance			3		pF

(8) I/O pins configured as inputs or outputs with no load. All pulldown inputs ≤ 0.2 V. All pullup inputs ≥ V_{CCIO} - 0.2 V.

Parameter Measurement Information



Where: I_{OL} = I_{OL} MAX for the respective pin (A)
I_{OH} = I_{OH} MIN for the respective pin(A)
V_{LOAD} = 1.5 V
C_L = 150-pF typical load-circuit capacitance(B)

A. For these values, see the "Electrical Characteristics over Recommended Operating Free-Air Temperature Range" table.

B. All timing parameters measured using an external load capacitance of 150 pF unless otherwise noted.

Figure 4. Test Load Circuit

ADVANCE INFORMATION

Timing Parameter Symbology

Timing parameter symbols have been created in accordance with JEDEC Standard 100. To shorten the symbols, some of the pin names and other related terminology have been abbreviated as follows:

CM	Compaction, CMPCT	RD	Read
CO	CLKOUT	RST	Reset, $\overline{\text{RST}}$
ER	Erase	RX	SCInRX
ICLK	Interface clock	S	Slave mode
M	Master mode	SCC	SCInCLK
OSC, OSCI	OSCIN	SIMO	SPInSIMO
OSCO	OSCOUT	SOMI	SPInSOMI
P	Program, PROG	SPC	SPInCLK
R	Ready	SYS	System clock
R0	Read margin 0, RDMRGN0	TX	SCInTX
R1	Read margin 1, RDMRGN1		

Lowercase subscripts and their meanings are:

a	access time	r	rise time
c	cycle time (period)	su	setup time
d	delay time	t	transition time
f	fall time	v	valid time
h	hold time	w	pulse duration (width)

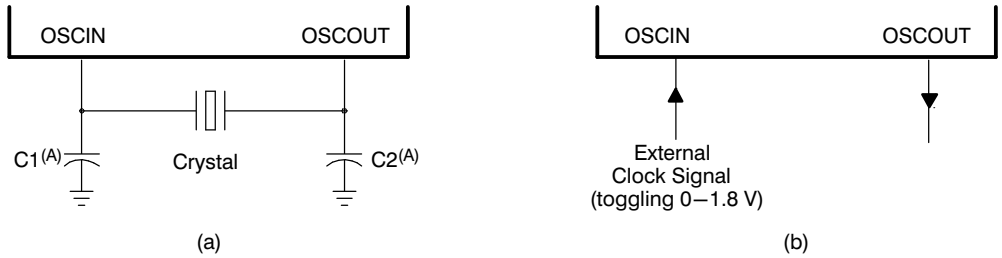
The following additional letters are used with these meanings:

H	High	X	Unknown, changing, or don't care level
L	Low	Z	High impedance
V	Valid		

External Reference Resonator/Crystal Oscillator Clock Option

The oscillator is enabled by connecting the appropriate fundamental 4–20 MHz resonator/crystal and load capacitors across the external OSCIN and OSCOUT pins as shown in Figure 5a. The oscillator is a single-stage inverter held in bias by an integrated bias resistor. This resistor is disabled during leakage test measurement and HALT mode. **TI strongly encourages each customer to submit samples of the device to the resonator/crystal vendors for validation.** The vendors are equipped to determine what load capacitors will best tune their resonator/crystal to the microcontroller device for optimum start-up and operation over temperature/voltage extremes.

An external oscillator source can be used by connecting a 1.8-V clock signal to the OSCIN pin and leaving the OSCOUT pin unconnected (open) as shown in Figure 5b.



A. The values of C1 and C2 should be provided by the resonator/crystal vendor.

Figure 5. Crystal/Clock Connection

ADVANCE INFORMATION

ZPLL AND CLOCK SPECIFICATIONS

Timing Requirements for ZPLL Circuits Enabled or Disabled

		MIN	MAX	UNIT
$f_{(OSC)}$	Input clock frequency	4	20	MHz
$t_{c(OSC)}$	Cycle time, OSCIN	50		ns
$t_{w(OSCIL)}$	Pulse duration, OSCIN low	15		ns
$t_{w(OSCIH)}$	Pulse duration, OSCIN high	15		ns
$f_{(OSCRST)}$	OSC FAIL frequency (1)		53	kHz

(1) Causes a device reset (specifically a clock reset) by setting the RST OSC FAIL (GLBCTRL.15) and the OSC FAIL flag (GLBSTAT.1) bits equal to 1. For more detailed information on these bits and device resets, see the *TMS470R1x System Module Reference Guide* (literature number SPNU189).

Switching Characteristics Over Recommended Operating Conditions for Clocks (1) (2)

PARAMETER		TEST CONDITIONS (3)	MIN	MAX	UNIT
$f_{(SYS)}$	System clock frequency (4)	Pipeline mode enabled		60	MHz
		Pipeline mode disabled		24	MHz
$f_{(CONFIG)}$	System clock frequency	Flash config mode		24	MHz
$f_{(ICLK)}$	Interface clock frequency			25	MHz
$f_{(ECLK)}$	External clock output frequency for ECP module	Pipeline mode enabled		25	MHz
		Pipeline mode disabled		24	MHz
$t_{c(SYS)}$	Cycle time, system clock	Pipeline mode enabled	16.7		ns
		Pipeline mode disabled	41.6		ns
$t_{c(CONFIG)}$	Cycle time, system clock	Flash config mode	41.6		ns
$t_{c(ICLK)}$	Cycle time, interface clock		40		ns
$t_{c(ECLK)}$	Cycle time, ECP module external clock output	Pipeline mode enabled	40		ns
		Pipeline mode disabled	41.6		ns

(1) When PLLDIS = 0, $f_{(SYS)} = M \times f_{(OSC)} / R$, where M = {4 or 8}, R = {1,2,3,4,5,6,7,8}. R is the system-clock divider determined by the CLKDIVPRE [2:0] bits in the global control register (GLBCTRL[2:0]) and M is the PLL multiplier determined by the MULT4 bit (GLBCTRL.3).
When PLLDIS = 1, $f_{(SYS)} = f_{(OSC)} / R$, where R = {1,2,3,4,5,6,7,8}.
$f_{(ICLK)} = f_{(SYS)} / X$, where X = {1,2,3,4,5,6,7,8,9,10,11,12,13,14,15,16}. X is the interface clock divider ratio determined by the PCR0[4:1] bits in the SYS module.
(2) $f_{(ECLK)} = f_{(ICLK)} / N$, where N = {1 to 256}. N is the ECP prescale value defined by the ECPCTRL[7:0] register bits in the ECP module.
(3) Pipeline mode enabled or disabled is determined by the ENPIPE bit (FMREGOPT.0).
(4) Flash Vread must be set to 5V to achieve maximum system clock frequency.

ADVANCE INFORMATION

Switching Characteristics Over Recommended Operating Conditions for External Clocks[1][2][3]

(see Figure 6 and Figure 7)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$t_{w(COL)}$	Pulse duration, CLKOUT low	SYSCLK or MCLK[4]	$0.5t_{c(SYS)} - t_f$		ns
		ICLK: X is even or 1[5]	$0.5t_{c(ICLK)} - t_f$		
		ICLK: X is odd and not 1[5]	$0.5t_{c(ICLK)} + 0.5t_{c(SYS)} - t_f$		
$t_{w(COH)}$	Pulse duration, CLKOUT high	SYSCLK or MCLK[4]	$0.5t_{c(SYS)} - t_r$		ns
		ICLK: X is even or 1[5]	$0.5t_{c(ICLK)} - t_r$		
		ICLK: X is odd and not 1[5]	$0.5t_{c(ICLK)} - 0.5t_{c(SYS)} - t_r$		
$t_{w(EOL)}$	Pulse duration, ECLK low	N is even and X is even or odd	$0.5t_{c(ECLK)} - t_f$		ns
		N is odd and X is even	$0.5t_{c(ECLK)} - t_f$		
		N is odd and X is odd and not 1	$0.5t_{c(ECLK)} + 0.5t_{c(SYS)} - t_f$		
$t_{w(EOH)}$	Pulse duration, ECLK high	N is even and X is even or odd	$0.5t_{c(ECLK)} - t_r$		ns
		N is odd and X is even	$0.5t_{c(ECLK)} - t_r$		
		N is odd and X is odd and not 1	$0.5t_{c(ECLK)} - 0.5t_{c(SYS)} - t_r$		

(1) X = {1,2,3,4,5,6,7,8,9,10,11,12,13,14,15,16}. X is the interface clock divider ratio determined by the PCR0[4:1] bits in the SYS module.
(2) N = {1 to 256}. N is the ECP prescale value defined by the ECPCTRL[7:0] register bits in the ECP module.
(3) CLKOUT/ECLK pulse durations (low/high) are a function of the OSCIN pulse durations when PLLDIS is active.
(4) Clock source bits are selected as either SYSCLK (CLKCNTL[6:5] = 11 binary) or MCLK (CLKCNTL[6:5] = 10 binary).
(5) Clock source bits are selected as ICLK (CLKCNTL[6:5] = 01 binary).

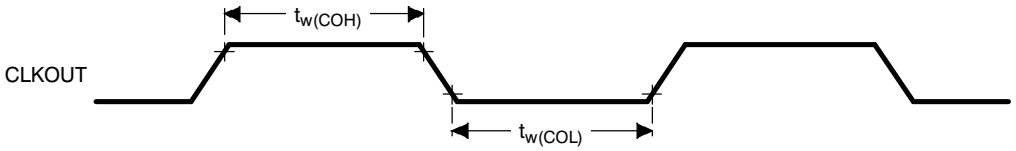


Figure 6. CLKOUT Timing Diagram

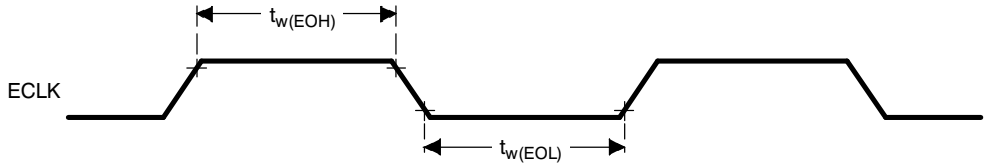


Figure 7. ECLK Timing Diagram

ADVANCE INFORMATION

RST AND PORRST TIMINGS

Timing Requirements for PORRST

(see Figure 8)

		MIN	MAX	UNIT
V_{CCPORL}	V_{CC} low supply level when PORRST must be active during power up		0.6	V
V_{CCPORH}	V_{CC} high supply level when PORRST must remain active during power up and become active during power down	1.5		V
$V_{CCIOPORL}$	V_{CCIO} low supply level when PORRST must be active during power up		1.1	V
$V_{CCIOPORH}$	V_{CCIO} high supply level when PORRST must remain active during power up and become active during power down		2.75	V
V_{IL}	Low-level input voltage after $V_{CCIO} > V_{CCIOPORH}$		0.2 V_{CCIO}	V
$V_{IL(PORRST)}$	Low-level input voltage of PORRST before V CCIO > $V_{CCIOPORL}$		0.5	V
$t_{su(PORRST)r}$	Setup time, PORRST active before $V_{CCIO} > V_{CCIOPORL}$ during power up	0		ms
$t_{su(VCCIO)r}$	Setup time, $V_{CCIO} > V_{CCIOPORL}$ before $V_{CC} > V_{CCPORL}$	0		ms
$t_{h(PORRST)r}$	Hold time, PORRST active after $V_{CC} > V_{CCPORH}$	1		ms
$t_{su(PORRST)f}$	Setup time, PORRST active before $V_{CC} \leq V_{CCPORH}$ during power down	8		µs
$t_{h(PORRST)rio}$	Hold time, PORRST active after $V_{CC} > V_{CCIOPORH}$	1		ms
$t_{h(PORRST)d}$	Hold time, PORRST active after $V_{CC} < V_{CCPORL}$	0		ms
$t_{su(PORRST)fio}$	Setup time, PORRST active before $V_{CC} \leq V_{CCIOPORH}$ during power down	0		ns
$t_{su(VCCIO)f}$	Setup time, $V_{CC} < V_{CCPORL}$ before $V_{CCIO} < V_{CCIOPORL}$	0		ns

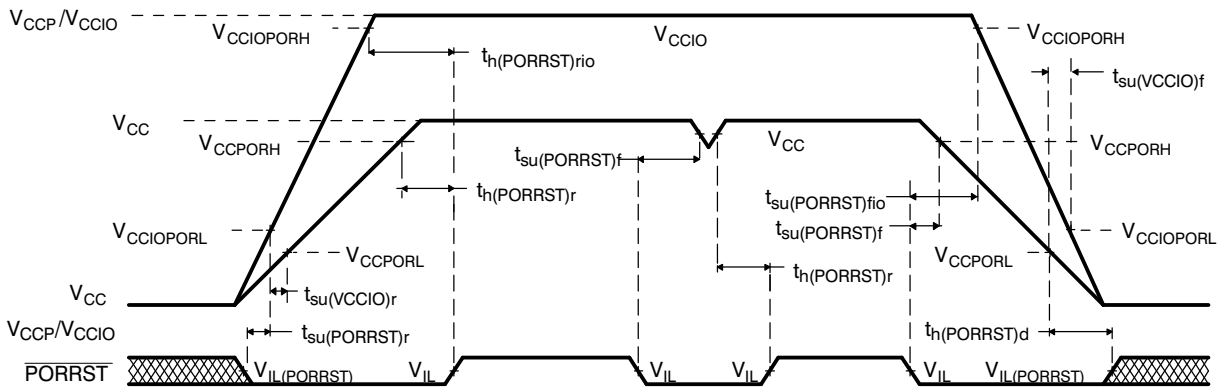


Figure 8. PORRST Timing Diagram

Switching Characteristics Over Recommended Operating Conditions for RST(1)

PARAMETER		MIN	MAX	UNIT
$t_{v(RST)}$	Valid time, RST active after PORRST inactive	$4112t_{c(OSC)}$		ns
	Valid time, RST active (all others)	$8t_{c(SYS)}$		
t_{fsu}	Flash start up time, from RST inactive to fetch of first instruction from flash (flash pump stabilization time)	$716t_{c(OSC)}$		ns

(1) Specified values do NOT include rise/fall times. For rise and fall timings, see the "Switching Characteristics for Output Timings versus Load Capacitance" table.

JTAG SCAN INTERFACE TIMING

(JTAG Clock Specification 10-MHz and 50-pF Load on TDO Output)

		MIN	MAX	UNIT
$t_{c(JTAG)}$	Cycle time, JTAG low and high period	50		ns
$t_{su(TDI/TMS - TCKr)}$	Setup time, TDI, TMS before TCK rise (TCKr)	15		ns
$t_{h(TCKr -TDI/TMS)}$	Hold time, TDI, TMS after TCKr	15		ns
$t_{h(TCKf -TDO)}$	Hold time, TDO after TCKf	10		ns
$t_{d(TCKf -TDO)}$	Delay time, TDO valid after TCK fall (TCKf)		45	ns

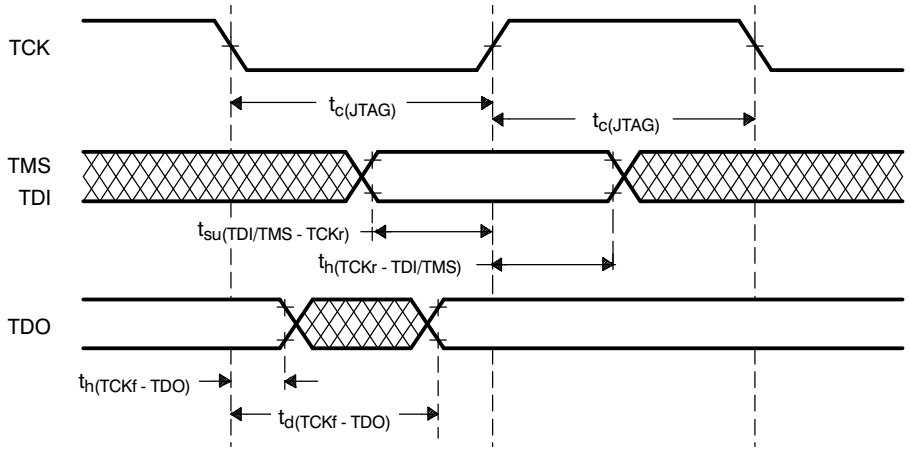


Figure 9. JTAG Scan Timings

ADVANCE INFORMATION

OUTPUT TIMINGS

Switching Characteristics for Output Timings versus Load Capacitance (C_L)

(see Figure 10)

PARAMETER			MIN	MAX	UNIT
t_r	Rise time, CLKOUT, AWD, TDO	C_L = 15 pF	0.5	2.5	ns
		C_L = 50 pF	1.5	5	
		C_L = 100 pF	3	9	
		C_L = 150 pF	4.5	12.5	
t_f	Fall time, CLKOUT, AWD, TDO	C_L = 15 pF	0.5	2.5	ns
		C_L = 50 pF	1.5	5	
		C_L = 100 pF	3	9	
		C_L = 150 pF	4.5	12.5	
t_r	Rise time, SPInCLK, SPInSOMI, SPInSIMO(1)	C_L = 15 pF	2.5	8	ns
		C_L = 50 pF	5	14	
		C_L = 100 pF	9	23	
		C_L = 150 pF	13	32	
t_f	Fall time, $\overline{RST}$, SPInCLK, SPInSOMI, SPInSIMO(1)	C_L = 15 pF	2.5	8	ns
		C_L = 50 pF	5	14	
		C_L = 100 pF	9	23	
		C_L = 150 pF	13	32	
t_r	Rise time, all other output pins	C_L = 15 pF	2.5	12	ns
		C_L = 50 pF	6.0	28	
		C_L = 100 pF	12	50	
		C_L = 150 pF	18	73	
t_f	Fall time, all other output pins	C_L = 15 pF	3	12	ns
		C_L = 50 pF	8.5	28	
		C_L = 100 pF	16	50	
		C_L = 150 pF	23	73	

(1) Where n = 1–3.

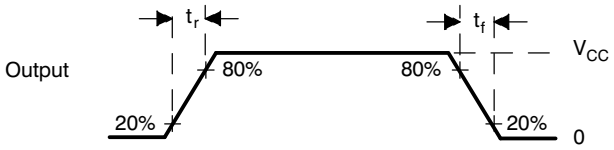


Figure 10. CMOS-Level Outputs

INPUT TIMINGS

Timing Requirements for Input Timings(1)

(see Figure 11)

		MIN	MAX	UNIT
t_{pw}	Input minimum pulse width	$t_{c(ICLK)}$ + 10		ns

(1) $t_{c(ICLK)}$ = interface clock cycle time = 1 / $f_{(ICLK)}$

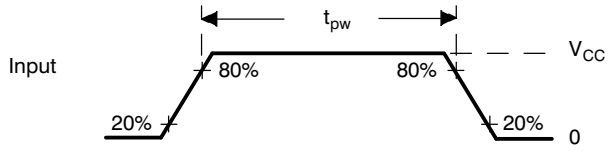


Figure 11. CMOS-Level Inputs

FLASH TIMINGS

Timing Requirements for Program Flash(1)

		MIN	TYP	MAX	UNIT
$t_{prog(16\text{-}bit)}$	Half word (16-bit) programming time	4	16	200	µs
$t_{prog(Total)}$	512K-byte programming time(2)		4	15	s
$t_{erase(sector)}$	Sector erase time		2	15	s
t_{wec}	Write/erase cycles at T_A = 105°C			100	cycles
$t_{fp(\overline{RST})}$	Flash pump setting time from $\overline{RST}$ to SLEEP		$143t_{c(SYS)}$		ns
$t_{fp(SLEEP)}$	Initial flash pump setting time from SLEEP to STANDBY		$143t_{c(SYS)}$		ns
$t_{fp(STDBY)}$	Initial flash pump setting time from STANDBY to ACTIVE		$72t_{c(SYS)}$		ns

(1) For more detailed information on the flash core sectors, see the *flash program and erase* section of this data sheet.
(2) The 512K-byte programming time includes overhead of state machine.

ADVANCE INFORMATION

SPIn MASTER MODE TIMING PARAMETERS

SPIn Master Mode External Timing Parameters

(CLOCK PHASE = 0, SPInCLK = output, SPInSIMO = output, and SPInSOMI = input)(1)(2)(3) (see Figure 12)

NO.			MIN	MAX	UNIT
1	$t_{c(SPC)M}$	Cycle time, SPInCLK(4)	100	$256t_{c(ICLK)}$	ns
2(5)	$t_{w(SPCH)M}$	Pulse duration, SPInCLK high (clock polarity = 0)	$0.5t_{c(SPC)M} - t_r$	$0.5t_{c(SPC)M} + 5$	ns
	$t_{w(SPCL)M}$	Pulse duration, SPInCLK low (clock polarity = 1)	$0.5t_{c(SPC)M} - t_f$	$0.5t_{c(SPC)M} + 5$	
3(5)	$t_{w(SPCL)M}$	Pulse duration, SPInCLK low (clock polarity = 0)	$0.5t_{c(SPC)M} - t_f$	$0.5t_{c(SPC)M} + 5$	ns
	$t_{w(SPCH)M}$	Pulse duration, SPInCLK high (clock polarity = 1)	$0.5t_{c(SPC)M} - t_r$	$0.5t_{c(SPC)M} + 5$	
4(5)	$t_{d(SPCH-SIMO)M}$	Delay time, SPInCLK high to SPInSIMO valid (clock polarity = 0)		10	ns
	$t_{d(SPCL-SIMO)M}$	Delay time, SPInCLK low to SPInSIMO valid (clock polarity = 1)		10	
5(5)	$t_{v(SPCL-SIMO)M}$	Valid time, SPInSIMO data valid after SPInCLK low (clock polarity = 0)	$t_{c(SPC)M} - 5 - t_f$		ns
	$t_{v(SPCH-SIMO)M}$	Valid time, SPInSIMO data valid after SPInCLK high (clock polarity = 1)	$t_{c(SPC)M} - 5 - t_r$		
6(5)	$t_{su(SOMI-SPCL)M}$	Setup time, SPInSOMI before SPInCLK low (clock polarity = 0)	6		ns
	$t_{su(SOMI-SPCH)M}$	Setup time, SPInSOMI before SPInCLK high (clock polarity = 1)	6		
7(5)	$t_{v(SPCL-SOMI)M}$	Valid time, SPInSOMI data valid after SPInCLK low (clock polarity = 0)	4		ns
	$t_{v(SPCH-SOMI)M}$	Valid time, SPInSOMI data valid after SPInCLK high (clock polarity = 1)	4		

(1) The MASTER bit (SPInCTRL2.3) is set and the CLOCK PHASE bit (SPInCTRL2.0) is cleared.
(2) $t_{c(ICLK)}$ = interface clock cycle time = 1 / $f_{(ICLK)}$
(3) For rise and fall timings, see the "Switching Characteristics for Output Timings versus Load Capacitance" table.
(4) When the SPI is in master mode, the following must be true:
For PS values from 1 to 255: $t_{c(SPC)M} \geq (PS + 1)t_{c(ICLK)} \geq 100$ ns, where PS is the prescale value set in the SPInCTL1[12:5] register bits.
For PS values of 0: $t_{c(SPC)M} = 2t_{c(ICLK)} \geq 100$ ns.
(5) The active edge of the SPInCLK signal referenced is controlled by the CLOCK POLARITY bit (SPInCTRL2.1).

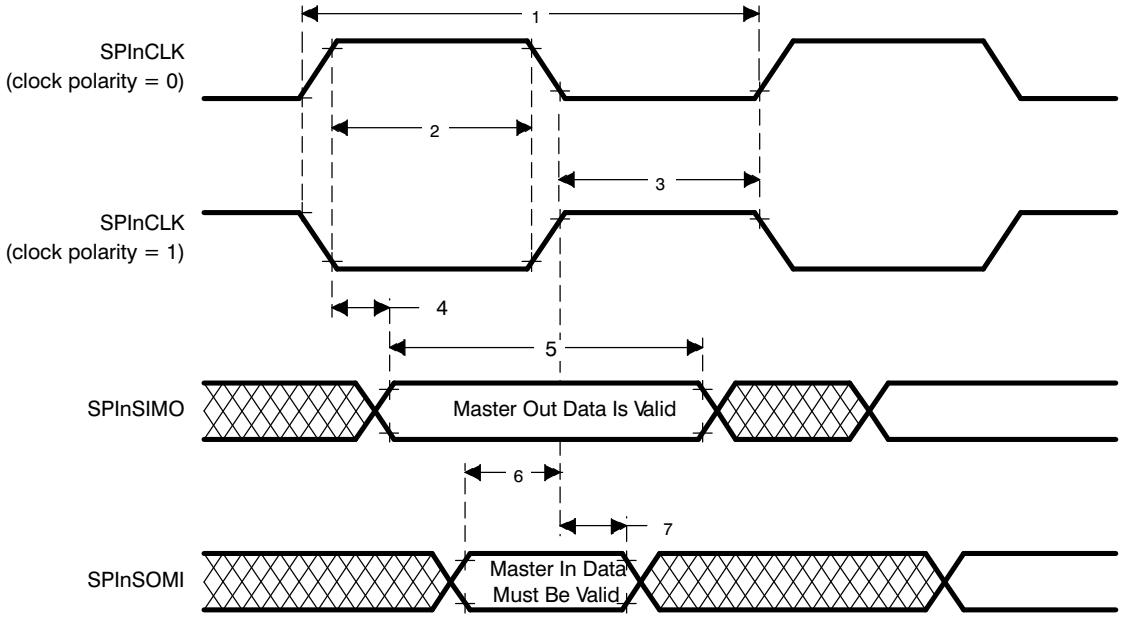


Figure 12. SPIn Master Mode External Timing (CLOCK PHASE = 0)

SPIn Master Mode External Timing Parameters

(CLOCK PHASE = 1, SPInCLK = output, SPInSIMO = output, and SPInSOMI = input)(1)(2)(3) (see Figure 13)

NO.			MIN	MAX	UNIT
1	$t_{c(SPC)M}$	Cycle time, SPInCLK(4)	100	$256t_{c(ICLK)}$	ns
2(5)	$t_{w(SPCH)M}$	Pulse duration, SPInCLK high (clock polarity = 0)	$0.5t_{c(SPC)M} - t_r$	$0.5t_{c(SPC)M} + 5$	ns
	$t_{w(SPCL)M}$	Pulse duration, SPInCLK low (clock polarity = 1)	$0.5t_{c(SPC)M} - t_f$	$0.5t_{c(SPC)M} + 5$	
3(5)	$t_{w(SPCL)M}$	Pulse duration, SPInCLK low (clock polarity = 0)	$0.5t_{c(SPC)M} - t_f$	$0.5t_{c(SPC)M} + 5$	ns
	$t_{w(SPCH)M}$	Pulse duration, SPInCLK high (clock polarity = 1)	$0.5t_{c(SPC)M} - t_r$	$0.5t_{c(SPC)M} + 5$	
4(5)	$t_{v(SIMO-SPCH)M}$	Valid time, SPInCLK high after SPInSIMO data valid (clock polarity = 0)	$0.5t_{c(SPC)M} - 15$		ns
	$t_{v(SIMO-SPCL)M}$	Valid time, SPInCLK low after SPInSIMO data valid (clock polarity = 1)	$0.5t_{c(SPC)M} - 15$		
5(5)	$t_{v(SPCH-SIMO)M}$	Valid time, SPInSIMO data valid after SPInCLK high (clock polarity = 0)	$0.5t_{c(SPC)M} - 5 - t_r$		ns
	$t_{v(SPCL-SIMO)M}$	Valid time, SPInSIMO data valid after SPInCLK low (clock polarity = 1)	$0.5t_{c(SPC)M} - 5 - t_f$		
6(5)	$t_{su(SOMI-SPCH)M}$	Setup time, SPInSOMI before SPInCLK high (clock polarity = 0)	6		ns
	$t_{su(SOMI-SPCL)M}$	Setup time, SPInSOMI before SPInCLK low (clock polarity = 1)	6		
7(5)	$t_{v(SPCH-SOMI)M}$	Valid time, SPInSOMI data valid after SPInCLK high (clock polarity = 0)	4		ns
	$t_{v(SPCL-SOMI)M}$	Valid time, SPInSOMI data valid after SPInCLK low (clock polarity = 1)	4		

(1) The MASTER bit (SPInCTRL2.3) is set and the CLOCK PHASE bit (SPInCTRL2.0) is set.
(2) $t_{c(ICLK)}$ = interface clock cycle time = 1 / $f_{(ICLK)}$
(3) For rise and fall timings, see the "Switching Characteristics for Output Timings versus Load Capacitance" table.
(4) When the SPI is in master mode, the following must be true:
For PS values from 1 to 255: $t_{c(SPC)M} \geq (PS + 1)t_{c(ICLK)} \geq 100$ ns, where PS is the prescale value set in the SPInCTL1[12:5] register bits.
For PS values of 0: $t_{c(SPC)M} = 2t_{c(ICLK)} \geq 100$ ns.
(5) The active edge of the SPInCLK signal referenced is controlled by the CLOCK POLARITY bit (SPInCTRL2.1).

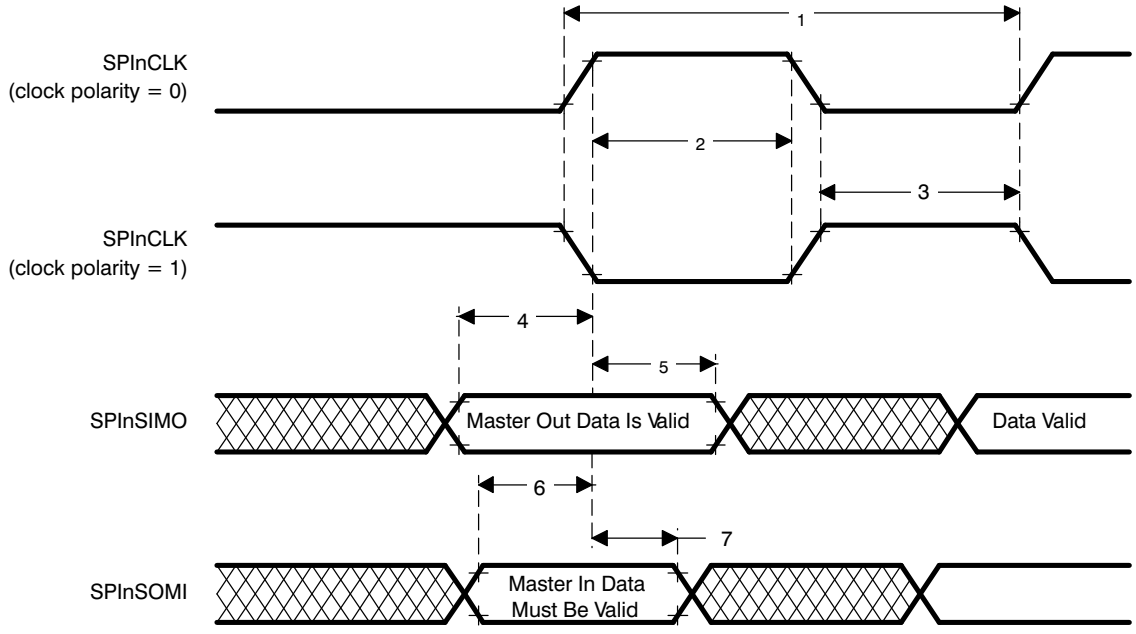


Figure 13. SPIn Master Mode External Timing (CLOCK PHASE = 1)

ADVANCE INFORMATION

SPIn SLAVE MODE TIMING PARAMETERS

SPIn Slave Mode External Timing Parameters

(CLOCK PHASE = 0, SPInCLK = input, SPInSIMO = input, and SPInSOMI = output)(1)(2)(3)(4) (see Figure 14)

NO.			MIN	MAX	UNIT
1	$t_{c(SPC)S}$	Cycle time, SPInCLK(5)	100	$256t_{c(ICLK)}$	ns
2(6)	$t_{w(SPCH)S}$	Pulse duration, SPInCLK high (clock polarity = 0)	$0.5t_{c(SPC)S}$ - $0.25t_{c(ICLK)}$	$0.5t_{c(SPC)S}$ + $0.25t_{c(ICLK)}$	ns
	$t_{w(SPCL)S}$	Pulse duration, SPInCLK low (clock polarity = 1)	$0.5t_{c(SPC)S}$ - $0.25t_{c(ICLK)}$	$0.5t_{c(SPC)S}$ + $0.25t_{c(ICLK)}$	
3(6)	$t_{w(SPCL)S}$	Pulse duration, SPInCLK low (clock polarity = 0)	$0.5t_{c(SPC)S}$ - $0.25t_{c(ICLK)}$	$0.5t_{c(SPC)S}$ + $0.25t_{c(ICLK)}$	ns
	$t_{w(SPCH)S}$	Pulse duration, SPInCLK high (clock polarity = 1)	$0.5t_{c(SPC)S}$ - $0.25t_{c(ICLK)}$	$0.5t_{c(SPC)S}$ + $0.25t_{c(ICLK)}$	
4(6)	$t_{d(SPCH-SOMI)S}$	Delay time, SPInCLK high to SPInSOMI valid (clock polarity = 0)		$6 + t_r$	ns
	$t_{d(SPCL-SOMI)S}$	Delay time, SPInCLK low to SPInSOMI valid (clock polarity = 1)		$6 + t_f$	
5(6)	$t_{v(SPCH-SOMI)S}$	Valid time, SPInSOMI data valid after SPInCLK high (clock polarity = 0)	$t_{c(SPC)S}$ - 6 - t_r		ns
	$t_{v(SPCL-SOMI)S}$	Valid time, SPInSOMI data valid after SPInCLK low (clock polarity = 1)	$t_{c(SPC)S}$ - 6 - t_f		
6(6)	$t_{su(SIMO-SPCL)S}$	Setup time, SPInSIMO before SPInCLK low (clock polarity = 0)	6		ns
	$t_{su(SIMO-SPCH)S}$	Setup time, SPInSIMO before SPInCLK high (clock polarity = 1)	6		
7(6)	$t_{v(SPCL-SIMO)S}$	Valid time, SPInSIMO data valid after SPInCLK low (clock polarity = 0)	6		ns
	$t_{v(SPCH-SIMO)S}$	Valid time, SPInSIMO data valid after SPInCLK high (clock polarity = 1)	6		

(1) The MASTER bit (SPInCTRL2.3) is cleared and the CLOCK PHASE bit (SPInCTRL2.0) is cleared.
(2) If the SPI is in slave mode, the following must be true: $t_{c(SPC)S} \geq (PS + 1)\ t_{c(ICLK)}$, where PS = prescale value set in SPInCTL1[12:5].
(3) For rise and fall timings, see the "Switching Characteristics for Output Timings versus Load Capacitance" table.
(4) $t_{c(ICLK)}$ = interface clock cycle time = $1 / f_{(ICLK)}$
(5) When the SPIn is in slave mode, the following must be true:
For PS values from 1 to 255: $t_{c(SPC)S} \geq (PS + 1)t_{c(ICLK)} \geq 100$ ns, where PS is the prescale value set in the SPInCTL1[12:5] register bits.
For PS values of 0: $t_{c(SPC)S} = 2t_{c(ICLK)} \geq 100$ ns.
(6) The active edge of the SPInCLK signal referenced is controlled by the CLOCK POLARITY bit (SPInCTRL2.1).

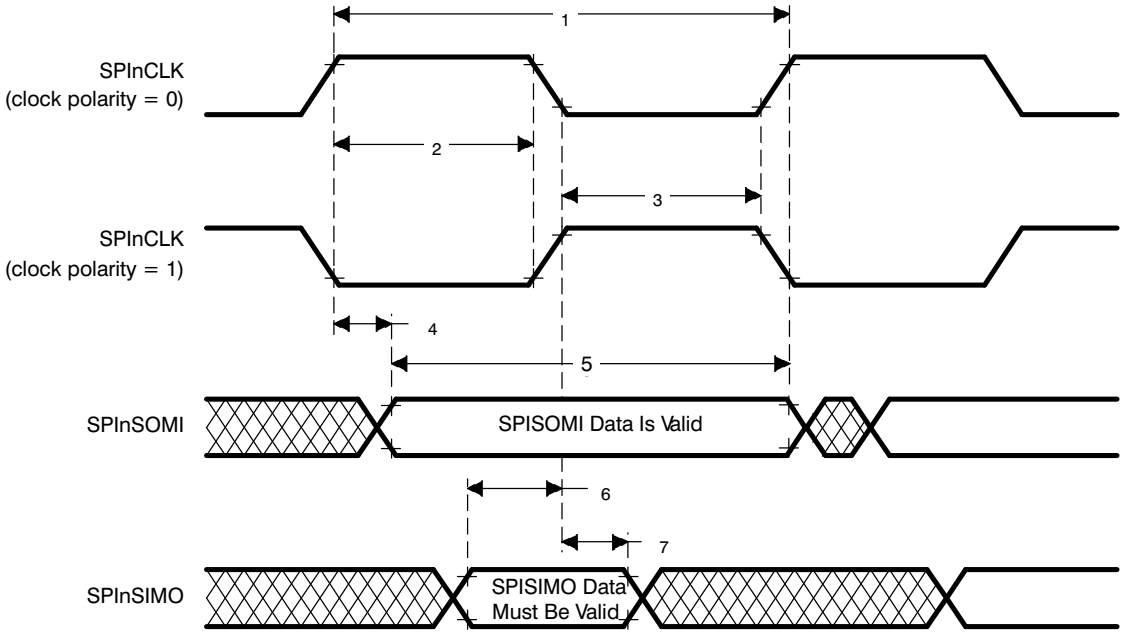


Figure 14. SPIn Slave Mode External Timing (CLOCK PHASE = 0)

SPIn Slave Mode External Timing Parameters

(CLOCK PHASE = 1, SPInCLK = input, SPInSIMO = input, and SPInSOMI = output)(1)(2)(3)(4) (see Figure 15)

NO.			MIN	MAX	UNIT
1	$t_{c(SPC)S}$	Cycle time, SPInCLK(5)	100	$256t_{c(ICLK)}$	ns
2(6)	$t_{w(SPCH)S}$	Pulse duration, SPInCLK high (clock polarity = 0)	$0.5t_{c(SPC)S} - 0.25t_{c(ICLK)}$	$0.5t_{c(SPC)S} + 0.25t_{c(ICLK)}$	ns
	$t_{w(SPCL)S}$	Pulse duration, SPInCLK low (clock polarity = 1)	$0.5t_{c(SPC)S} - 0.25t_{c(ICLK)}$	$0.5t_{c(SPC)S} + 0.25t_{c(ICLK)}$	
3(6)	$t_{w(SPCL)S}$	Pulse duration, SPInCLK low (clock polarity = 0)	$0.5t_{c(SPC)S} - 0.25t_{c(ICLK)}$	$0.5t_{c(SPC)S} + 0.25t_{c(ICLK)}$	ns
	$t_{w(SPCH)S}$	Pulse duration, SPInCLK high (clock polarity = 1)	$0.5t_{c(SPC)S} - 0.25t_{c(ICLK)}$	$0.5t_{c(SPC)S} + 0.25t_{c(ICLK)}$	
4(6)	$t_{v(SOMI-SPCH)S}$	Valid time, SPInCLK high after SPInSOMI data valid (clock polarity = 0)	$0.5t_{c(SPC)S} - 6 - t_r$		ns
	$t_{v(SOMI-SPCL)S}$	Valid time, SPInCLK low after SPInSOMI data valid (clock polarity = 1)	$0.5t_{c(SPC)S} - 6 - t_f$		
5(6)	$t_{v(SPCH-SOMI)S}$	Valid time, SPInSOMI data valid after SPInCLK high (clock polarity = 0)	$0.5t_{c(SPC)S} - 6 - t_r$		ns
	$t_{v(SPCL-SOMI)S}$	Valid time, SPInSOMI data valid after SPInCLK low (clock polarity = 1)	$0.5t_{c(SPC)S} - 6 - t_f$		
6(6)	$t_{su(SIMO-SPCH)S}$	Setup time, SPInSIMO before SPInCLK high (clock polarity = 0)	6		ns
	$t_{su(SIMO-SPCL)S}$	Setup time, SPInSIMO before SPInCLK low (clock polarity = 1)	6		
7(6)	$t_{v(SPCH-SIMO)S}$	Valid time, SPInSIMO data valid after SPInCLK high (clock polarity = 0)	6		ns
	$t_{v(SPCL-SIMO)S}$	Valid time, SPInSIMO data valid after SPInCLK low (clock polarity = 1)	6		

(1) The MASTER bit (SPInCTRL2.3) is cleared and the CLOCK PHASE bit (SPInCTRL2.0) is set.
(2) If the SPI is in slave mode, the following must be true: $t_{c(SPC)S} \geq (PS + 1)\ t_{c(ICLK)}$, where PS = prescale value set in SPInCTL1[12:5].
(3) For rise and fall timings, see the "Switching Characteristics for Output Timings versus Load Capacitance" table.
(4) $t_{c(ICLK)}$ = interface clock cycle time = $1 / f_{(ICLK)}$
(5) When the SPIn is in slave mode, the following must be true:
For PS values from 1 to 255: $t_{c(SPC)S} \geq (PS + 1) t_{c(ICLK)} \geq 100$ ns, where PS is the prescale value set in the SPInCTL1[12:5] register bits.
For PS values of 0: $t_{c(SPC)S} = 2t_{c(ICLK)} \geq 100$ ns.
(6) The active edge of the SPInCLK signal referenced is controlled by the CLOCK POLARITY bit (SPInCTRL2.1).

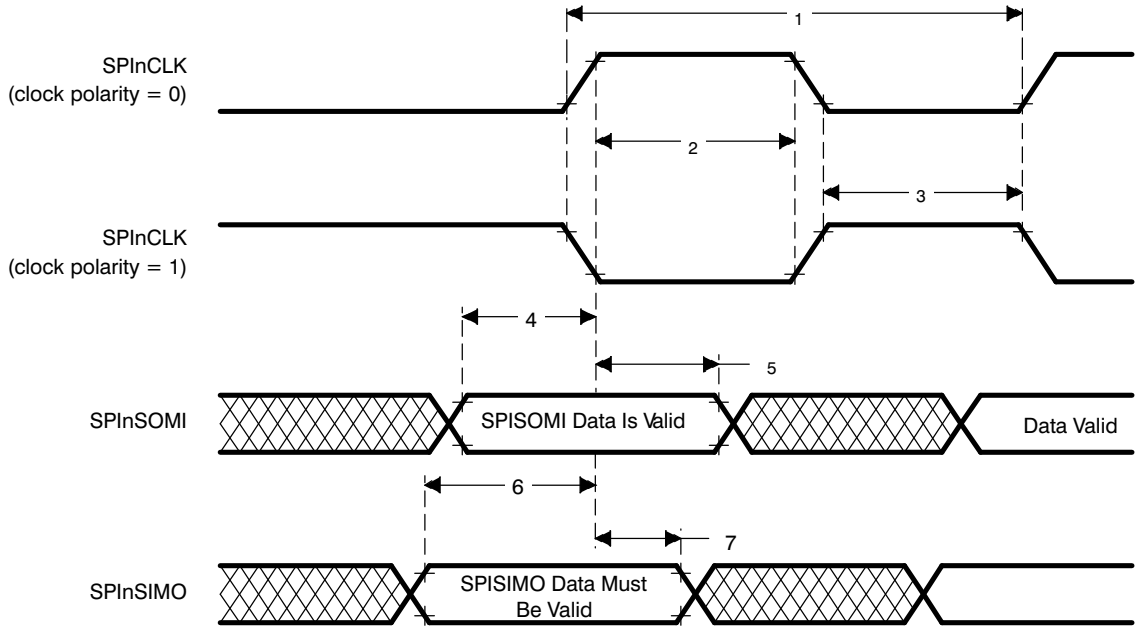


Figure 15. SPIn Slave Mode External Timing (CLOCK PHASE = 1)

ADVANCE INFORMATION

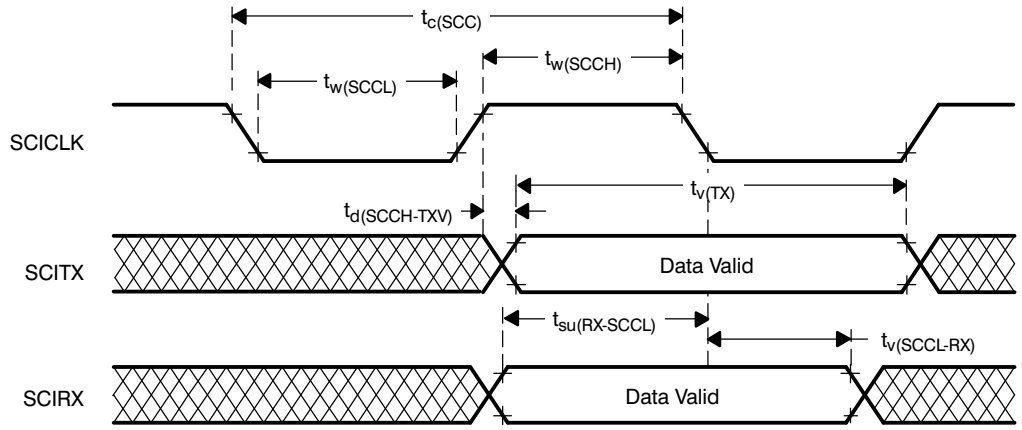
SCIn ISOSYNCHRONOUS MODE TIMINGS INTERNAL CLOCK

Timing Requirements for Internal Clock SCIn Isosynchronous Mode(1)(2)(3)

(see Figure 16)

		(BAUD + 1) IS EVEN OR BAUD = 0		(BAUD + 1) IS ODD AND BAUD ≠ 0		UNIT
		MIN	MAX	MIN	MAX	
$t_{c(SCC)}$	Cycle time, SCInCLK	$2t_{c(ICLK)}$	$2^{24} t_{c(ICLK)}$	$3t_{c(ICLK)}$	$(2^{24} -1) t_{c(ICLK)}$	ns
$t_{w(SCCL)}$	Pulse duration, SCInCLK low	$0.5t_{c(SCC)} - t_f$	$0.5t_{c(SCC)} + 5$	$0.5t_{c(SCC)} + 0.5t_{c(ICLK)} - t_f$	$0.5t_{c(SCC)} + 0.5t_{c(ICLK)}$	ns
$t_{w(SCCH)}$	Pulse duration, SCInCLK high	$0.5t_{c(SCC)} - t_r$	$0.5t_{c(SCC)} + 5$	$0.5t_{c(SCC)} - 0.5t_{c(ICLK)} - t_r$	$0.5t_{c(SCC)} - 0.5t_{c(ICLK)}$	ns
$t_{d(SCCH-TXV)}$	Delay time, SCInCLK high to SCInTX valid		10		10	ns
$t_{v(TX)}$	Valid time, SCInTX data after SCInCLK low	$t_{c(SCC)} - 10$		$t_{c(SCC)} - 10$		ns
$t_{su(RX-SCCL)}$	Setup time, SCInRX before SCInCLK low	$t_{c(ICLK)} + t_f + 20$		$t_{c(ICLK)} + t_f + 20$		ns
$t_{v(SCCL-RX)}$	Valid time, SCInRX data after SCInCLK low	$-t_{c(ICLK)} + t_f + 20$		$- t_{c(ICLK)} + t_f + 20$		ns

(1) BAUD = 24-bit concatenated value formed by the SCI[H,M,L]BAUD registers.
(2) $t_{c(ICLK)}$ = interface clock cycle time = $1/f_{(ICLK)}$
(3) For rise and fall timings, see the "Switching Characteristics for Output Timings versus Load Capacitance" table.



A. Data transmission/reception characteristics for isosynchronous mode with internal clocking are similar to the asynchronous mode. Data transmission occurs on the SCICLK rising edge, and data reception occurs on the SCICLK falling edge.

Figure 16. SCIn Isosynchronous Mode Timing Diagram for Internal Clock

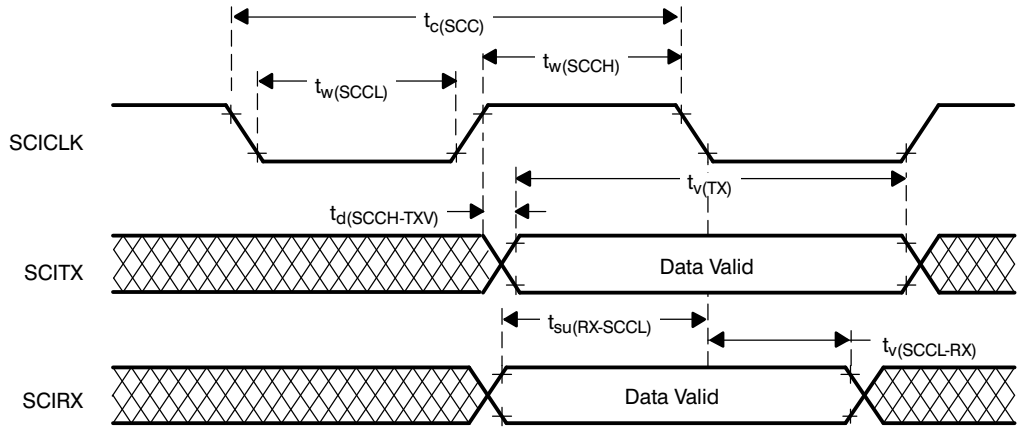
SCIn ISOSYNCHRONOUS MODE TIMINGS EXTERNAL CLOCK

Timing Requirements for External Clock SCIn Isosynchronous Mode(1)(2)

(see Figure 17)

		MIN	MAX	UNIT
$t_{c(SCC)}$	Cycle time, SCInCLK(3)	$8t_{c(ICLK)}$		ns
$t_{w(SCCH)}$	Pulse duration, SCInCLK high	$0.5t_{c(SCC)} - 0.25t_{c(ICLK)}$	$0.5t_{c(SCC)} + 0.25t_{c(ICLK)}$	ns
$t_{w(SCCL)}$	Pulse duration, SCInCLK low	$0.5t_{c(SCC)} - 0.25t_{c(ICLK)}$	$0.5t_{c(SCC)} + 0.25t_{c(ICLK)}$	ns
$t_{d(SCCH-TXV)}$	Delay time, SCInCLK high to SCInTX valid		$2t_{c(ICLK)} + 12 + t_r$	ns
$t_{v(TX)}$	Valid time, SCInTX data after SCInCLK low	$2t_{c(SCC)} -10$		ns
$t_{su(RX-SCCL)}$	Setup time, SCInRX before SCInCLK low	0		ns
$t_{v(SCCL-RX)}$	Valid time, SCInRX data after SCInCLK low	$2t_{c(ICLK)} + 10$		ns

(1) $t_{c(ICLK)}$ = interface clock cycle time = 1 / $f_{(ICLK)}$
(2) For rise and fall timings, see the "Switching Characteristics for Output Timings versus Load Capacitance" table.
(3) When driving an external SCInCLK, the following must be true: $t_{c(SCC)} \geq 8t_{c(ICLK)}$.



A. Data transmission / reception characteristics for isosynchronous mode with external clocking are similar to the asynchronous mode. Data transmission occurs on the SCICLK rising edge, and data reception occurs on the SCICLK falling edge.

Figure 17. SCIn Isosynchronous Mode Timing Diagram for External Clock

ADVANCE INFORMATION

HIGH-END TIMER (HET) TIMINGS

Minimum PWM Output Pulse Width:

This is equal to one high resolution clock period (HRP). The HRP is defined by the 6-bit high resolution prescale factor (hr), which is user defined, giving prescale factors of 1 to 64, with a linear increment of codes.

Therefore, the minimum PWM output pulse width = HRP(min) = hr(min)/SYSCLK = 1/SYSCLK

For example, for a SYSCLK of 30 MHz, the minimum PWM output pulse width = 1/30 = 33.33ns

Minimum Input Pulses that Can Be Captured:

The input pulse width must be greater or equal to the low resolution clock period (LRP), i.e., the HET loop (the HET program must fit within the LRP). The LRP is defined by the 3-bit loop-resolution prescale factor (lr), which is user defined, with a power of 2 increment of codes. That is, the value of lr can be 1, 2, 4, 8, 16, or 32.

Therefore, the minimum input pulse width = LRP(min) = hr(min) * lr(min)/SYSCLK = 1 * 1/SYSCLK

For example, with a SYSCLK of 30 MHz, the minimum input pulse width = 1 * 1/30 = 33.33 ns

NOTE:

Once the input pulse width is greater than LRP, the resolution of the measurement is still HRP. (That is, the captured value gives the number of HRP clocks inside the pulse.)

Abbreviations:

hr = HET high resolution divide rate = 1, 2, 3,...63, 64

lr = HET low resolution divide rate = 1, 2, 4, 8, 16, 32

High resolution clock period = HRP = hr/SYSCLK

Loop resolution clock period = LRP = hr*lr/SYSCLK

HIGH-END CAN CONTROLLER (HECCn) MODE TIMINGS

Dynamic Characteristics for the CANnHTX and CANnHRX Pins

PARAMETER		MIN	MAX	UNIT
$t_{d(CANnHTX)}$	Delay time, transmit shift register to CANnHTX pin(1)		15	ns
$t_{d(CANnHRX)}$	Delay time, CANnHRX pin to receive shift register		5	ns

(1) These values do not include rise/fall times of the output buffer.

MULTI-BUFFERED A-TO-D CONVERTER (MibADC)

The multi-buffered A-to-D converter (MibADC) has a separate power bus for its analog circuitry that enhances the A-to-D performance by preventing digital switching noise on the logic circuitry, which could be present on V_{SS} and V_{CC}, from coupling into the A-to-D analog stage. All A-to-D specifications are given with respect to AD_{REFLO} unless otherwise noted.

Resolution	10 bits (1024 values)
Monotonic	Assured
Output conversion code	00h to 3FFh [00 for $V_{AI} \leq AD_{REFLO}$; 3FF for $V_{AI} \geq AD_{REFHI}$]

Table 10. MibADC Recommended Operating Conditions(1)

		MIN	MAX	UNIT
AD_{REFHI}	A-to-D high-voltage reference source	V_{SSAD}	V_{CCAD}	V
AD_{REFLO}	A-to-D low-voltage reference source	V_{SSAD}	V_{CCAD}	V
V_{AI}	Analog input voltage	V_{SSAD} - 0.3	V_{CCAD} + 0.3	V
I_{AIC}	Analog input clamp current(2) ($V_{AI} < V_{SSAD}$ - 0.3 or $V_{AI} > V_{CCAD}$ + 0.3)	-2	2	mA

(1) For V_{CCAD} and V_{SSAD} recommended operating conditions, see the "device recommended operating conditions" table.
(2) Input currents into any ADC input channel outside the specified limits could affect conversion results of other channels.

Table 11. Operating Characteristics Over Full Ranges of Recommended Operating Conditions(1)(2)

PARAMETER		DESCRIPTION/CONDITIONS		MIN	TYP	MAX	UNIT
R_i	Analog input resistance	See Figure 18.			250	500	Ω
C_i	Analog input capacitance	See Figure 18.	Conversion			10	pF
			Sampling			30	pF
I_{AIL}	Analog input leakage current	See Figure 18.		-1		1	µA
$I_{ADREFHI}$	AD_{REFHI} input current	AD_{REFHI} = 3.6 V, $AD_{REFLO} = V_{SSAD}$				5	mA
CR	Conversion range over which specified accuracy is maintained	AD_{REFHI} - AD_{REFLO}		3		3.6	V
E_{DNL}	Differential nonlinearity error	Difference between the actual step width and the ideal value. See Figure 19.				±1.5	LSB
E_{INL}	Integral nonlinearity error	Maximum deviation from the best straight line through the MibADC. MibADC transfer characteristics, excluding the quantization error. See Figure 20.				±2	LSB
E_{TOT}	Total error/absolute accuracy	Maximum value of the difference between an analog value and the ideal midstep value. See Figure 21.				±2	LSB

(1) $V_{CCAD} = AD_{REFHI}$
(2) 1 LSB = (AD_{REFHI} - AD_{REFLO})/ 2^{10} for the MibADC

ADVANCE INFORMATION

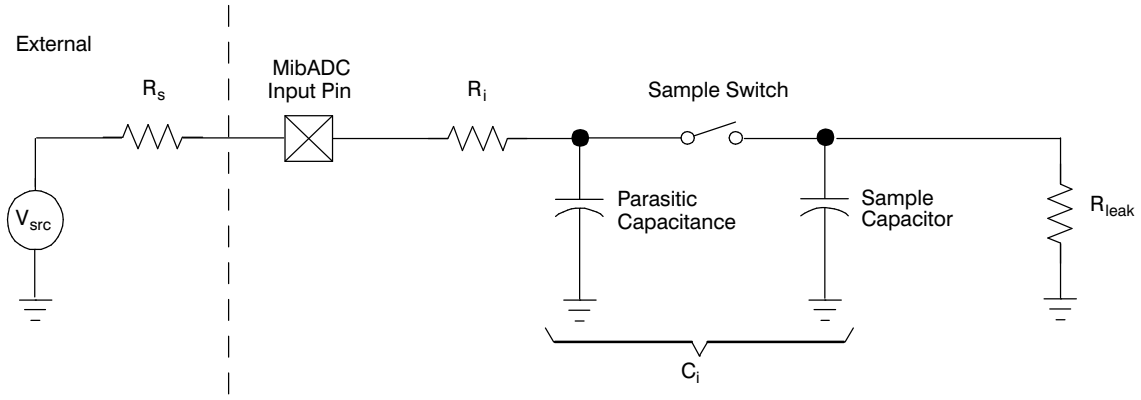


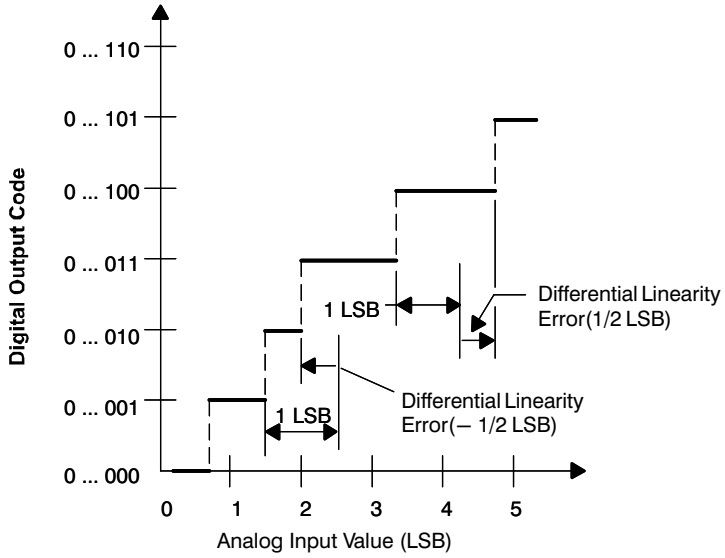
Figure 18. MibADC Input Equivalent Circuit

Multi-Buffer ADC Timing Requirements

		MIN	NOM	MAX	UNIT
$t_{c(ADCLK)}$	Cycle time, MibADC clock	0.05			µs
$t_{d(SH)}$	Delay time, sample and hold time	1			µs
$t_{d(C)}$	Delay time, conversion time	0.55			µs
$t_{d(SHC)}$ (1)	Delay time, total sample/hold and conversion time	1.55			µs

(1) This is the minimum sample/hold and conversion time that can be achieved. These parameters are dependent on many factors; for more details, see the *TMS470R1x Multi-Buffered Analog-to-Digital Converter (MibADC) Reference Guide* (literature number SPNU206).

The differential nonlinearity error shown in Figure 19 (sometimes referred to as differential linearity) is the difference between an actual step width and the ideal value of 1 LSB.

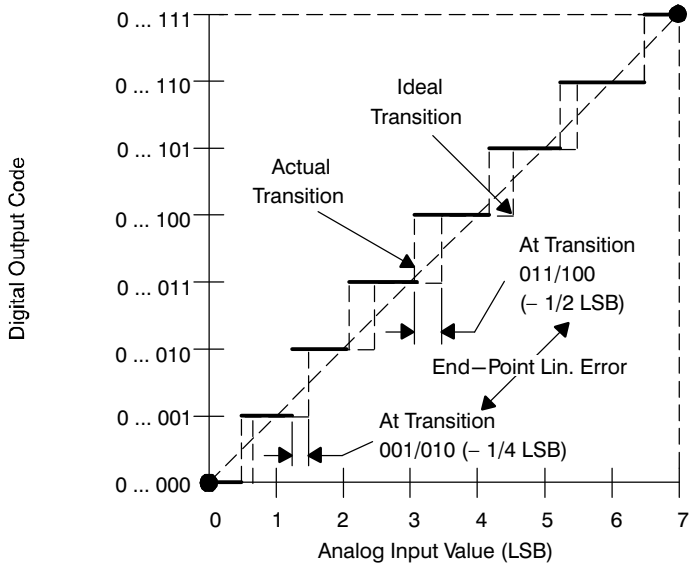


A. 1 LSB = $(AD_{REFHI} - AD_{REFLO})/2^{10}$

Figure 19. Differential Nonlinearity (DNL)

ADVANCE INFORMATION

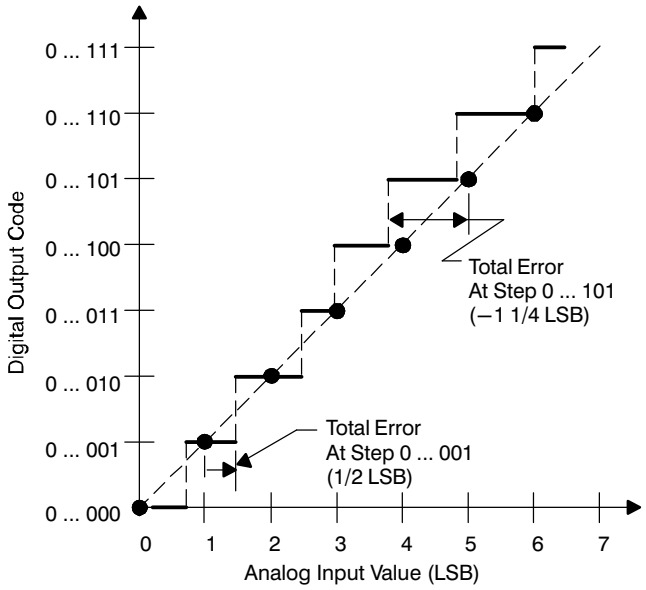
The integral nonlinearity error shown in Figure 20 (sometimes referred to as linearity error) is the deviation of the values on the actual transfer function from a straight line.



A. 1 LSB = $(AD_{REFHI} - AD_{REFLO})/2^{10}$

Figure 20. Integral Nonlinearity (INL) Error

The absolute accuracy or total error of an MibADC as shown in Figure 21 is the maximum value of the difference between an analog value and the ideal midstep value.



A. 1 LSB = $(AD_{REFHI} - AD_{REFLO})/2^{10}$

Figure 21. Absolute Accuracy (Total) Error

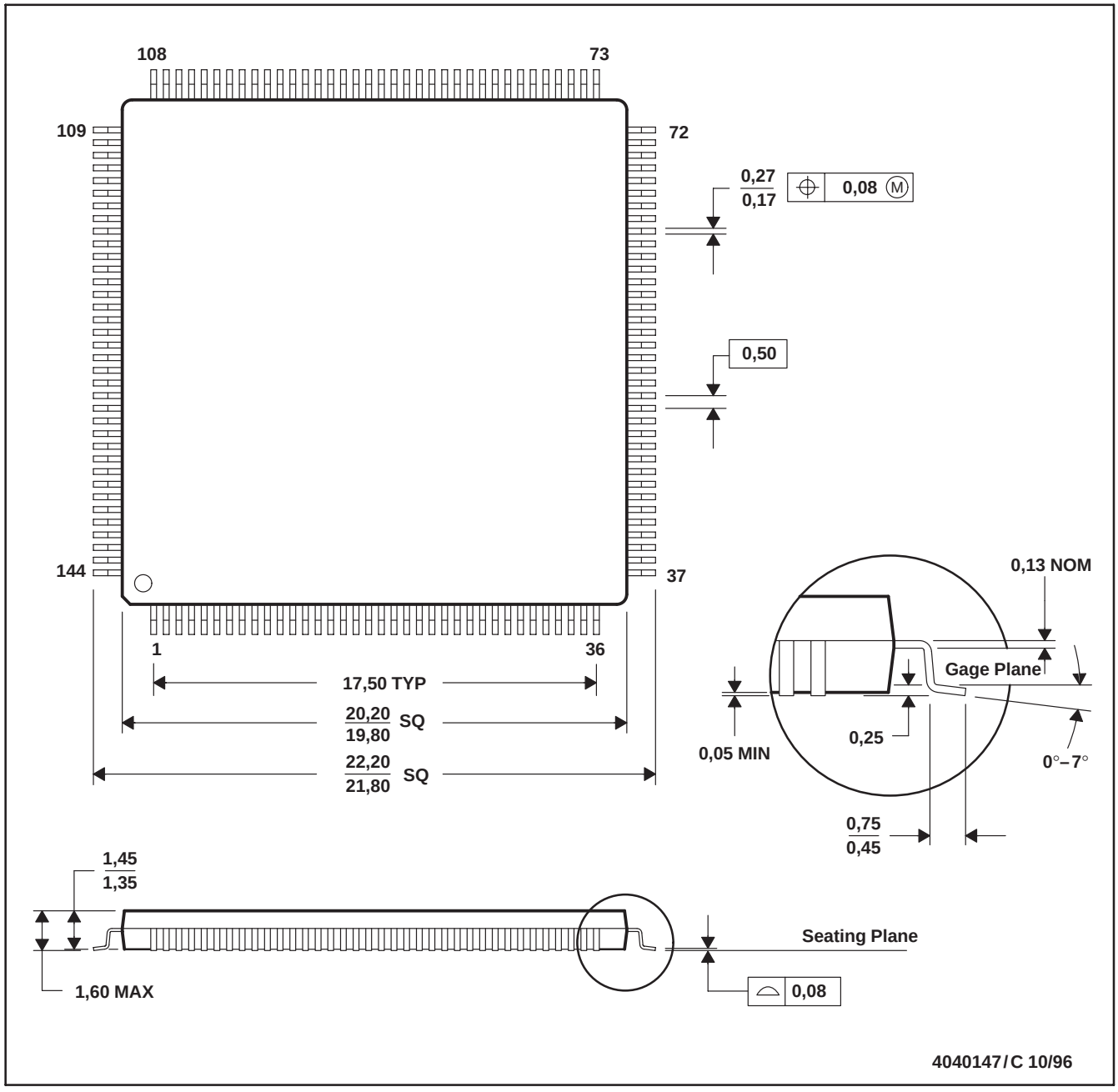
ADVANCE INFORMATION

THERMAL RESISTANCE CHARACTERISTICS

PARAMETER	°C/W
$R_{\Theta JA}$	43
$R_{\Theta JC}$	6.5

MTQF017A – OCTOBER 1994 – REVISED DECEMBER 1996

PGE (S-PQFP-G144) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

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