TMS470R1VF67A
16/32-BIT RISC FLASH MICROCONTROLLER

SPNS004I – NOVEMBER 2002 – REVISED OCTOBER 2005

- High-Performance Static CMOS Technology
- TMS470R1x 16/32-Bit RISC Core (ARM7TDMI™)
  - 24-MHz System Clock (60-MHz Pipeline)
  - Independent 16/32-Bit Instruction Set
  - Open Architecture With Third-Party Support
  - Built-In Debug Module
  - Utilizes Big-Endian Format
- Integrated Memory
  - 512K-Byte Program Flash
    - Two Banks With 14 Contiguous Sectors
    - Internal State Machine for Program and Erase
  - 32K-Byte Static RAM (SRAM)
- Operating Features
  - Core Supply Voltage (V_{CC}): 1.81 V - 2.05 V
  - I/O Supply Voltage (V_{CCIO}): 3.0 V - 3.6 V
  - Low-Power Modes: STANDBY and HALT
  - Industrial and Automotive Temperature Ranges
- 470+ System Module
  - 32-Bit Address Space Decoding
  - Bus Supervision for Memory and Peripherals
  - Analog Watchdog (AWD) Timer
  - Real-Time Interrupt (RTI)
  - System Integrity and Failure Detection
- Direct Memory Access (DMA) Controller
  - 32 Control Packets and 16 Channels
- Frequency-Modulated Phase-Locked Loop (FMPLL)-Based Clock Module With Prescaler
  - Multiply-by-4 or -8 Internal FMPLL Option
- Seven Communication Interfaces:
  - Two Serial Peripheral Interfaces (SPIs)
    - 255 Programmable Baud Rates
  - Serial Communications Interfaces (SCI)
    - 2^{24} Selectable Baud Rates
    - Asynchronous/Isosynchronous Modes
  - Two High-End CAN Controllers:
    - 32-Mailbox Capacity
    - Fully Compliant With CAN Protocol, Version 2.0B
  - Multi-Buffered Serial Peripheral Interface (MibSPI)
    - 128-Word Buffer
    - Four DMA Channels
    - Six Chip Selects
  - Class II Serial Interface (C2SIb)
    - Two Selectable Data Rates
    - Normal Mode 10.4 Kbps and 4X Mode 41.6 Kbps
- High-End Timer (HET)
  - 32 Programmable I/O Channels:
    - 30 High-Resolution Pins
    - 2 Standard-Resolution Pins
  - High-Resolution Share Feature (XOR)
  - High-End Timer RAM
    - 128-Instruction Capacity
- Two 10-Bit, 16-Channel Multi-Buffered ADCs
  - 128-Word FIFO Buffer
  - Single- or Continuous-Conversion Modes
  - 1.55 μs Minimum Sample and Conversion Time
  - Calibration Mode and Self-Test Features
- Four External Interrupts
- Flexible Interrupt Handling
- 3 Dedicated General-Purpose I/O (GIO) Pins, 1 Input-Only GIO Pin, and 65 Additional Peripheral I/Os
- Compatible ROM Device (Planned)
- On-Chip Scan-Base Emulation Logic, IEEE Standard 1149.1† (JTAG) Test-Access Port
- 176-Pin Plastic Ball Grid Array (GJZ Suffix)
- Development System Support Tools Available
  - Code Composer Studio™ Integrated Development Environment (IDE)
  - HET Assembler and Simulator
  - Real-Time In-Circuit Emulation
  - Flash Programming
- External Clock Prescale (ECP) Module
  - Programmable Low-Frequency External Clock (CLK)

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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† The test-access port is compatible with the IEEE Standard 1149.1-1990, *IEEE Standard Test-Access Port and Boundary Scan Architecture* specification. Boundary scan is not supported on this device.

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description

The TMS470R1VF67A† device is a member of the Texas Instruments TMS470R1x family of general-purpose 16/32-bit reduced instruction set computer (RISC) microcontrollers. The VF67A microcontroller offers high performance utilizing the high-speed ARM7TDMI 16/32-bit RISC central processing unit (CPU), resulting in a high instruction throughput while maintaining greater code efficiency. The ARM7TDMI 16/32-bit RISC CPU views memory as a linear collection of bytes numbered upwards from zero. The TMS470R1VF67A utilizes the big-endian format where the most significant byte of a word is stored at the lowest numbered byte and the least significant byte at the highest numbered byte.

High-end embedded control applications demand more performance from their controllers while maintaining low costs. The VF67A RISC core architecture offers solutions to these performance and cost demands while maintaining low power consumption.

The VF67A device contains the following:

- ARM7TDMI 16/32-Bit RISC CPU
- TMS470R1x system module (SYS) with 470+ enhancements [including a 16-channel direct-memory access (DMA) controller
- 512K-byte flash
- 32K-byte SRAM
- Frequency-modulated phase-locked loop (FMPLL) clock module
- Analog watchdog (AWD) timer
- Real-time interrupt (RTI) module
- Two serial peripheral interface (SPI) modules
- One serial communications interface (SCI) module
- Two high-end CAN controllers (HECC)
- Class II serial interface (C2SIb)
- Two 10-bit multi-buffered analog-to-digital converters (MibADC), 16-input channels
- Multi-buffered serial peripheral interface (MibSPI) module
- High-end timer (HET) controlling 32 I/Os
- External Clock Prescale (ECP) module
- Up to 68 I/O pins and 1 input-only pin

The functions performed by the 470+ system module (SYS) include: address decoding; memory protection; memory and peripherals bus supervision; reset and abort exception management; prioritization for all internal interrupt sources; device clock control; and parallel signature analysis (PSA). This data sheet includes device-specific information such as memory and peripheral select assignment, interrupt priority, and a device memory map. For a more detailed functional description of the SYS module, see the *TMS470R1x System Module Reference Guide* (literature number SPNU189).

The VF67A memory includes general-purpose SRAM supporting single-cycle read/write accesses in byte, half-word, and word modes.

The flash memory on this device is a nonvolatile, electrically erasable and programmable memory implemented with a 32-bit-wide data bus interface.The flash operates with a system clock frequency of up to 24 MHz. When in pipeline mode, the flash operates with a system clock frequency of up to 60 MHz. For more detailed information on the flash, see the *flash* section of this data sheet and the *TMS470R1x F05 Flash Reference Guide* (literature number SPNU213).

† Throughout the remainder of this document, the TMS470R1VF67A device name shall be referred to as TMS470R1VF67A or VF67A.

description (continued)

The VF67A device has seven communication interfaces: a MibSPI, two SPIs, two HECCs, an SCI, and a C2SIb. The SPI provides a convenient method of serial interaction for high-speed communications between similar shift-register type devices. The SCI is a full-duplex, serial I/O interface intended for asynchronous communication between the CPU and other peripherals using the standard Non-Return-to-Zero (NRZ) format. The HECC uses a serial, multimaster communication protocol that efficiently supports distributed real-time control with robust communication rates of up to1 megabit per second (Mbps). The HECC is ideal for applications operating in harsh environments (e.g., automotive and industrial fields) that require reliable serial communication or multiplexed wiring. The MibSPI is a high-speed synchronous serial input/output port that allows a serial bit stream of programmed length to be shifted into and out of the device at a programmed bit-transfer rate. The C2SIb allows the VF67A to transmit and receive messages on a class II network following an SAE J1850† standard. For more detailed functional information on the SPI, SCI, and HECC peripherals, see the specific reference guides (literature numbers SPNU195, SPNU196, and SPNU197, respectively). For more detailed functional information on the C2SIb peripheral, see the *TMS470R1x Class II Serial Interface B (C2SIb) Reference Guide* (literature number SPNU214). For more information on the MibSPI peripheral, see the *TMS470R1x Multi-Buffered Serial Peripheral Interface (MibSPI) Reference Guide* (literature number SPNU217).

The HET is an advanced intelligent timer that provides sophisticated timing functions for real-time applications. The timer is software-controlled, using a reduced instruction set, with a specialized timer micromachine and an attached I/O port. The HET can be used for compare, capture, or general-purpose I/O. It is especially well suited for applications requiring multiple sensor information and drive actuators with complex and accurate time pulses. For more detailed functional information on the HET, see the *TMS470R1x High-End Timer (HET) Reference Guide* (literature number SPNU199). The VF67A HET peripheral contains the XOR-share feature. This feature allows two adjacent HET high- resolution channels to be XORed together, making it possible to output smaller pulses than a standard HET. For more detailed information on the HET XOR-share feature, see the *TMS470R1x High-End Timer (HET) Reference Guide* (literature number SPNU199).

The VF67A device has two 10-bit-resolution sample-and-hold MibADCs. The MibADC channels can be converted individually or can be grouped by software for sequential conversion sequences. There are three separate groupings, two of which are triggerable by an external event. Each sequence can be converted once when triggered or configured for continuous conversion mode. For more detailed functional information on the MibADC, see the *TMS470R1x Multi-Buffered Analog-to-Digital Converter (MibADC) Reference Guide* (literature number SPNU206).

The frequency-modulated phase-locked loop (FMPLL) clock module contains a phase-locked loop, a clock-monitor circuit, a clock-enable circuit, and a prescaler (with prescale values of 1–8). The function of the FMPLL is to multiply the external frequency reference to a higher frequency for internal use. The FMPLL provides ACLK‡ to the system (SYS) module. The SYS module subsequently provides system clock (SYSCLK), real-time interrupt clock (RTICLK), CPU clock (MCLK), and peripheral interface clock (ICLK) to all other VF67A device modules. For more detailed functional information on the FMPLL, see the *TMS470R1x Frequency-Modulated Phase-Locked Loop (FMPLL) Clock Module Reference Guide* (literature number SPNU221).

† SAE Standard J1850 Class B Data Communication Network Interface

‡ ACLK should not be confused with the MibADC internal clock, ADCLK. ACLK is the continuous system clock from an external resonator/crystal reference.

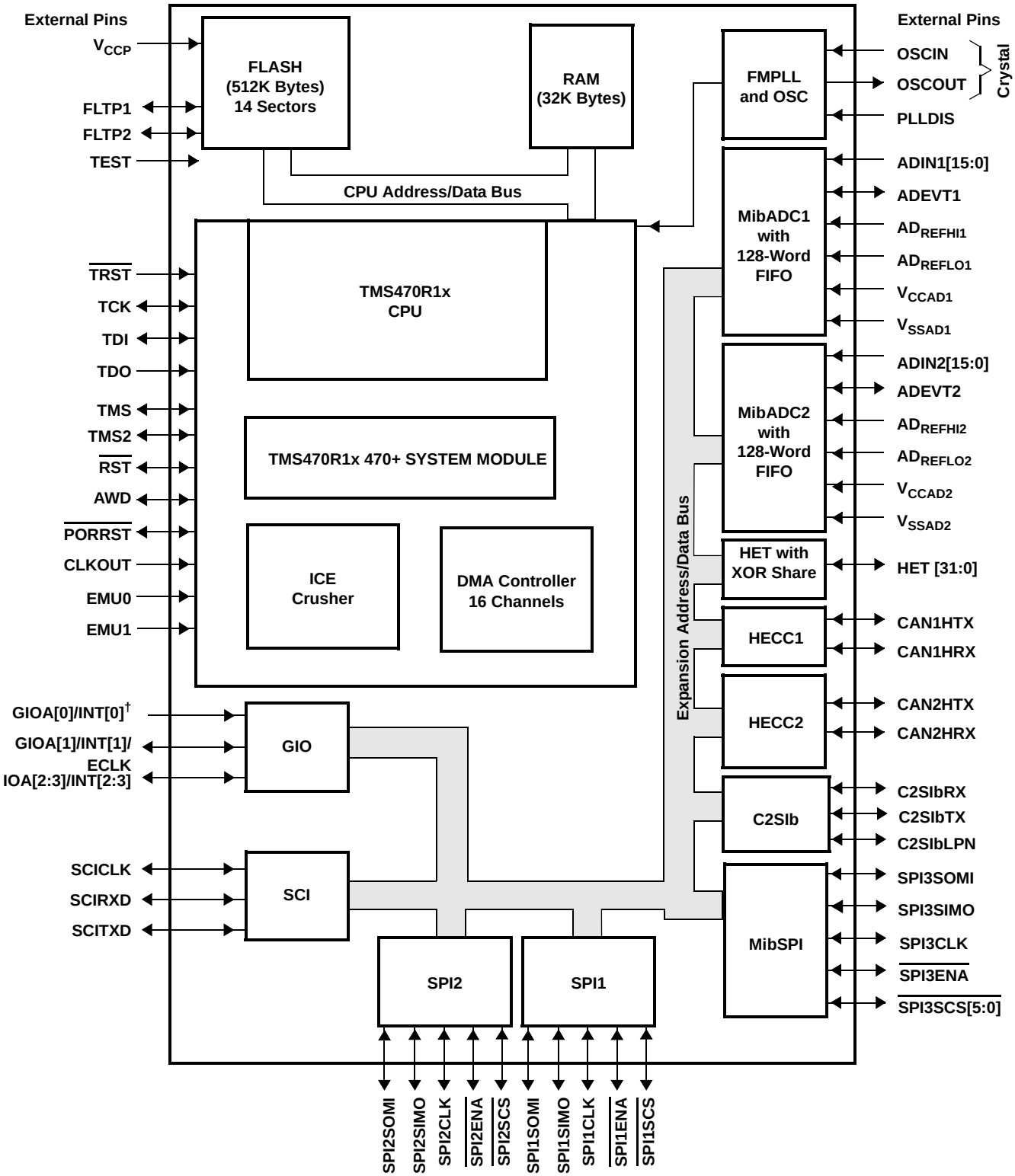
device characteristics

The TMS470R1VF67A device is a derivative of the F05 system emulation device SE470R1VB8AD. Table 1 identifies all the characteristics of the TMS470R1VF67A device except the SYSTEM and CPU, which are generic. The COMMENTS column aids the user in software-programming and references device-specific information.

Table 1. Device Characteristics

CHARACTERISTICS	DEVICE DESCRIPTION TMS470R1VF67A	COMMENTS FOR VF67A
MEMORY		
For the number of memory selects on this device, see the Memory Selection Assignment table (Table 2).		
INTERNAL MEMORY	512K-Byte flash 32K-Byte SRAM	Flash is pipeline-capable The VF67A RAM is implemented in one 32K array selected by two memory-select signals (see the Memory Selection Assignment table, Table 2).
PERIPHERALS		
For the device-specific interrupt priority configurations, see the Interrupt Priority table (Table 6). And for the 1K peripheral address ranges and their peripheral selects, see the VF67A Peripherals, System Module, and Flash Base Addresses table (Table 4).		
CLOCK	FMPLL	FMPLL has no external loop filter pins.
GENERAL-PURPOSE I/Os	3 I/O 1 Input only	Only four (4) external pins
C2SIb	1	
SCI	1 (3-pin)	
CAN (HECC and/or SCC)	2 HECC	High-end CAN controller. HECC1 and HECC2
SPI (5-pin, 4-pin or 3-pin)	2 (5-pin)	SPI1 and SPI2
MibSPI (5-pin, 4-pin or 3-pin)	1 (5-pin)	
HET with XOR Share	32 I/O	The high-resolution (HR) SHARE feature allows even HR pins to share the next higher odd HR pin structures. This HR sharing is independent of whether or not the odd pin is available externally. If an odd pin is available externally and *shared*, then the odd pin can only be used as a general-purpose I/O. For more information on HR SHARE, see the *TMS470R1x High-End Timer (HET) Reference Guide* (literature number SPNU199).
HET RAM	128-Instruction Capacity	
MibADC	2 10-bit, 16-channel 128-word FIFO	MibADC1 and MibADC2
CORE VOLTAGE	1.8 V	
I/O VOLTAGE	3.3 V	
PINS	176	
PACKAGE	GJZ	

functional block diagram



† GIOA[0]/INT[0] is an input-only GIO pin.

Terminal Functions

TERMINAL NAME	TERMINAL BALL NO.	TYPE[†‡]	INTERNAL PULLUP/ PULLDOWN[§]	DESCRIPTION
HIGH-END TIMER (HET)				
HET[0]	H1	3.3-V I/O	IPD	The VF67A device has both the logic and registers for a full 32-I/O HET implemented. Timer input capture or output compare. The HET[31:0] applicable pins can be programmed as general-purpose input/output (GIO) pins. HET[29:0] are high-resolution pins and HET[31:30] are loop-resolution pins. The high-resolution (HR) SHARE feature allows even HR pins to share the next higher odd HR pin structures. This HR sharing is independent of whether or not the odd pin is available externally. If an odd pin is available externally and *shared*, then the odd pin can only be used as a general-purpose I/O. For more information on HR SHARE, see the*TMS470R1x High-End Timer (HET) Reference Guide* (literature number SPNU199).
HET[1]	J1			
HET[2]	M5			
HET[3]	M4			
HET[4]	M3			
HET[5]	N3			
HET[6]	N4			
HET[7]	N5			
HET[8]	A14			
HET[9]	A13			
HET[10]	M8			
HET[11]	N8			
HET[12]	P8			
HET[13]	P9			
HET[14]	N7			
HET[15]	P7			
HET[16]	M6			
HET[17]	N6			
HET[18]	B14			
HET[19]	C14			
HET[20]	C13			
HET[21]	B12			
HET[22]	D13			
HET[23]	M7			
HET[24]	G14			
HET[25]	H2			
HET[26]	J2			
HET[27]	B13			
HET[28]	J13			
HET[29]	H13			
HET[30]	G13			
HET[31]	H14			
HIGH-END CAN CONTROLLER 1 (HECC1)				
CAN1HRX	B11	3.3-V I/O		HECC1 receive pin or GIO pin
CAN1HTX	B10	3.3-V I/O		HECC1 transmit pin or GIO pin
HIGH-END CAN CONTROLLER 2 (HECC2)				
CAN2HRX	K1	3.3-V I/O		HECC2 receive pin or GIO pin
CAN2HTX	L1	3.3-V I/O		HECC2 transmit pin or GIO pin
CLASS II SERIAL INTERFACE (C2SIB)				
C2SIbLPN	G11	3.3-V I/O	IPD	C2SIb module loopback enable pin or GIO pin
C2SIbRX	H12	3.3-V I/O		C2SIb module receive data input pin or GIO pin
C2SIbTX	G12	3.3-V I/O	IPD	C2SIb module transmit data output pin or GIO pin

† I = input, O = output, PWR = power, GND = ground, REF = reference voltage, NC = no connect

‡ All I/O pins, except $\overline{\text{RST}}$, are configured as inputs while $\overline{\text{PORRST}}$ is low and immediately after $\overline{\text{PORRST}}$ goes high.

§ IPD = internal pulldown, IPU = internal pullup (all internal pullups and pulldowns are active on input pins, independent of the $\overline{\text{PORRST}}$ state.)

Terminal Functions (Continued)

TERMINAL NAME	TERMINAL BALL NO.	TYPE†‡	INTERNAL PULLUP/ PULLDOWN§	DESCRIPTION
GENERAL-PURPOSE I/O (GIO)				
GIOA[0]/INT0	K14	3.3-V I	IPD	General-purpose input/output pins. GIOA[0]/INT[0] is an input-only pin. GIOA[3:0]/INT[3:0] are interrupt-capable pins. GIOA[1]/INT[1]/ECLK pin is multiplexed with the external clock-out function of the external clock prescale (ECP) module.
GIOA[1]/INT1/ECLK	J14	3.3-V I/O		
GIOA[2]/INT2	J4			
GIOA[3]/INT3	J3			
MULTI-BUFFERED ANALOG-TO-DIGITAL CONVERTER 1 (MibADC1)				
ADEVT1	B2	3.3-V I/O	IPD	MibADC1 event input. Can be programmed as a GIO pin.
ADIN1[0]	D4	3.3-V I		MibADC1 analog input pins
ADIN1[1]	D3			
ADIN1[2]	D2			
ADIN1[3]	D1			
ADIN1[4]	C5			
ADIN1[5]	C3			
ADIN1[6]	C2			
ADIN1[7]	C1			
ADIN1[8]	G4			
ADIN1[9]	G2			
ADIN1[10]	E4			
ADIN1[11]	D5			
ADIN1[12]	G3			
ADIN1[13]	F4			
ADIN1[14]	E3			
ADIN1[15]	C4			
AD_{REFHI1}	E2	3.3-V REF I		MibADC1 module high-voltage reference input
AD_{REFLO1}	F3	GND REF I		MibADC1 module low-voltage reference input
V_{CCAD1}	E1	3.3-V PWR		MibADC1 analog supply voltage
V_{SSAD1}	F1	GND		MibADC1 analog ground reference
MULTI-BUFFERED ANALOG-TO-DIGITAL CONVERTER 2 (MibADC2)				
ADEVT2	K13	3.3-V I/O	IPD	MibADC2 event input. Can be programmed as a GIO pin.
ADIN2[0]	K12	3.3-V I		MibADC2 analog input pins
ADIN2[1]	L10			
ADIN2[2]	L11			
ADIN2[3]	L12			
ADIN2[4]	L13			
ADIN2[5]	L14			
ADIN2[6]	K11			
ADIN2[7]	M10			
ADIN2[8]	M11			
ADIN2[9]	M12			
ADIN2[10]	M13			
ADIN2[11]	M14			

† I = input, O = output, PWR = power, GND = ground, REF = reference voltage, NC = no connect

‡ All I/O pins, except $\overline{RST}$, are configured as inputs while $\overline{PORRST}$ is low and immediately after $\overline{PORRST}$ goes high.

§ IPD = internal pulldown, IPU = internal pullup (all internal pullups and pulldowns are active on input pins, independent of the $\overline{PORRST}$ state.)

Terminal Functions (Continued)

TERMINAL NAME	TERMINAL BALL NO.	TYPE†‡	INTERNAL PULLUP/ PULLDOWN§	DESCRIPTION
MULTI-BUFFERED ANALOG-TO-DIGITAL CONVERTER 2 (MibADC2) (CONTINUED)				
ADIN2[12]	N10	3.3-V I		MibADC2 analog input pins
ADIN2[13]	N11			
ADIN2[14]	N14			
ADIN2[15]	P14			
AD_{REFH2I}	N13	3.3-V REF I		MibADC2 module high-voltage reference input
AD_{REFLO2}	N12	GND REF I		MibADC2 module low-voltage reference input
V_{CCAD2}	P13	3.3-V PWR		MibADC2 analog supply voltage
V_{SSAD2}	P12	GND		MibADC2 analog ground reference
SERIAL PERIPHERAL INTERFACE 1 (SPI1)				
SPI1CLK	N1	3.3-V I/O	IPD	SPI1 clock. SPI1CLK can be programmed as a GIO pin.
$\overline{\text{SPI1ENA}}$	L5			SPI1 chip enable. $\overline{\text{SPI1ENA}}$ can be programmed as a GIO pin.
$\overline{\text{SPI1SCS}}$	L6			SPI1 slave chip select. $\overline{\text{SPI1SCS}}$ can be programmed as a GIO pin.
SPI1SIMO	M2			SPI1 data stream. Slave in/master out. SPI1SIMO can be programmed as a GIO pin.
SPI1SOMI	N2			SPI1 data stream. Slave out/master in. SPI1SOMI can be programmed as a GIO pin.
SERIAL PERIPHERAL INTERFACE 2 (SPI2)				
SPI2CLK	D12	3.3-V I/O	IPD	SPI2 clock. SPI2CLK can be programmed as a GIO pin.
$\overline{\text{SPI2ENA}}$	D10			SPI2 chip enable. $\overline{\text{SPI2ENA}}$ can be programmed as a GIO pin.
$\overline{\text{SPI2SCS}}$	C11			SPI2 slave chip select. $\overline{\text{SPI2SCS}}$ can be programmed as a GIO pin.
SPI2SIMO	C12			SPI2 data stream. Slave in/master out. SPI2SIMO can be programmed as a GIO pin.
SPI2SOMI	D11			SPI2 data stream. Slave out/master in. SPI2SOMI can be programmed as a GIO pin.
MULTI-BUFFER SERIAL PERIPHERAL INTERFACE (SPI3)				
SPI3CLK	A10	3.3-V I/O	IPD	SPI3 clock. SPI3CLK can be programmed as a GIO pin.
$\overline{\text{SPI3ENA}}$	C7			SPI3 chip enable. $\overline{\text{SPI3ENA}}$ can be programmed as a GIO pin.
$\overline{\text{SPI3SCS5}}$	B1			SPI3 slave chip select 5. $\overline{\text{SPI2SCS5}}$ can be programmed as a GIO pin.
$\overline{\text{SPI3SCS4}}$	A1			SPI3 slave chip select 4. $\overline{\text{SPI2SCS4}}$ can be programmed as a GIO pin.
$\overline{\text{SPI3SCS3}}$	A2			SPI3 slave chip select 3. $\overline{\text{SPI2SCS3}}$ can be programmed as a GIO pin.
$\overline{\text{SPI3SCS2}}$	A3			SPI3 slave chip select 2. $\overline{\text{SPI2SCS2}}$ can be programmed as a GIO pin.
$\overline{\text{SPI3SCS1}}$	B4			SPI3 slave chip select 1. $\overline{\text{SPI2SCS1}}$ can be programmed as a GIO pin.
$\overline{\text{SPI3SCS0}}$	A4			SPI3 slave chip select 0. $\overline{\text{SPI2SCS0}}$ can be programmed as a GIO pin.
SPI3SIMO	A9			SPI3 data stream. Slave in/master out. SPI3SIMO can be programmed as a GIO pin.
SPI3SOMI	A8			SPI3 data stream. Slave out/master in. SPI3SOMI can be programmed as a GIO pin.
FREQUENCY-MODULATED PLL (FMPLL)				
OSCIN	P4	1.8-V I		Crystal connection pin or external clock input
OSCOUT	P3	1.8-V O		External crystal connection pin
PLLDIS	D8	3.3-V I	IPD	Enable/disable the ZPLL. The ZPLL can be bypassed and the oscillator becomes the system clock. If not in bypass mode, TI recommends that this pin be connected to ground or pulled down to ground by an external resistor.

† I = input, O = output, PWR = power, GND = ground, REF = reference voltage, NC = no connect

‡ All I/O pins, except $\overline{\text{RST}}$, are configured as inputs while $\overline{\text{PORRST}}$ is low and immediately after $\overline{\text{PORRST}}$ goes high.

† IPD = internal pulldown, IPU = internal pullup (all internal pullups and pulldowns are active on input pins, independent of the $\overline{\text{PORRST}}$ state.)

Terminal Functions (Continued)

TERMINAL NAME	TERMINAL BALL NO.	TYPE†‡	INTERNAL PULLUP/ PULLDOWN§	DESCRIPTION
SERIAL COMMUNICATIONS INTERFACE (SCI)				
SCICLK	G7	3.3-V I/O	IPD	SCI clock. SCICLK can be programmed as a GIO pin.
SCIRXD	B9	3.3-V I/O		SCI data receive. SCIRXD can be programmed as a GIO pin.
SCITXD	B8	3.3-V I/O		SCI data transmit. SCITXD can be programmed as a GIO pin.
SYSTEM MODULE (SYS)				
CLKOUT	F8	3.3-V I/O	IPD	Bidirectional pin. CLKOUT can be programmed as a GIO pin or the output of SYSCLK, ICLK, or MCLK.
$\overline{\text{PORRST}}$	N9	3.3-V I	IPD	Input master chip power-up reset. External V_{CC} monitor circuitry must assert a power-on reset.
$\overline{\text{RST}}$	J6	3.3-V I/O	IPU	Bidirectional reset. The internal circuitry can assert a reset, and an external system reset can assert a device reset. On this pin, the output buffer is implemented as an open drain (drives low only). To ensure an external reset is not arbitrarily generated, TI recommends that an external pullup resistor be connected to this pin.
WATCHDOG/REAL-TIME INTERRUPT (WD/RTI)				
AWD	D9	3.3-V I/O		Analog watchdog reset. The AWD pin provides a system reset if the WD KEY is not written in time by the system, providing an external RC network circuit is connected. If the user is not using AWD, TI recommends that this pin be connected to ground or pulled down to ground by an external resistor. For more details on the external RC network circuit, see the *TMS470R1x System Module Reference Guide* (literature number SPNU189) and the application note *Analog Watchdog Resistor, Capacitor and Discharge Interval Selection Constraints* (literature number SPNA005).
TEST/DEBUG (T/D)				
EMU0	H3	3.3-V I/O	IPU	Emulation pin 0
EMU1	H4	3.3-V I/O	IPU	Emulation pin 1
TCK	C8	3.3-V I	IPD	Test clock. TCK controls the test hardware (JTAG).
TDI	C10	3.3-V I	IPU	Test data in. TDI inputs serial data to the test instruction register, test data register, and programmable test address (JTAG).
TDO	C9	3.3-V O	IPD	Test data out. TDO outputs serial data from the test instruction register, test data register, identification register, and programmable test address (JTAG).
TEST	J9	3.3-V I	IPD	Test enable. Reserved for internal use only. TI recommends that this pin be connected to ground or pulled down to ground by an external resistor.
TMS	B3	3.3-V I	IPU	Serial input for controlling the state of the CPU test access port (TAP) controller (JTAG).
TMS2	G8	3.3-V I	IPU	Serial input for controlling the second TAP. TI recommends that this pin be connected to V_{CCIO} or pulled up to V_{CCIO} by an external resistor.
$\overline{\text{TRST}}$	J12	3.3-V I	IPD	Test hardware reset to TAP1 and TAP2. IEEE Standard 1149-1 (JTAG) Boundary-Scan Logic. TI recommends that this pin be pulled down to ground by an external resistor.
FLASH				
FLTP1	H8	NC		Flash test pad 1. **For proper operation, this pin must not be connected [no connect (NC)].**
FLTP2	H7	NC		Flash test pad 2. **For proper operation, this pin must not be connected [no connect (NC)].**
V_{CCP}	M1	3.3-V PWR		Flash external pump voltage (3.3 V)

† I = input, O = output, PWR = power, GND = ground, REF = reference voltage, NC = no connect

‡ All I/O pins, except $\overline{\text{RST}}$, are configured as inputs while $\overline{\text{PORRST}}$ is low and immediately after $\overline{\text{PORRST}}$ goes high.

§ IPD = internal pulldown, IPU = internal pullup (all internal pullups and pulldowns are active on input pins, independent of the $\overline{\text{PORRST}}$ state.)

Terminal Functions (Continued)

TERMINAL NAME	TERMINAL BALL NO.	TYPE†‡	INTERNAL PULLUP/ PULLDOWN§	DESCRIPTION
SUPPLY VOLTAGE CORE (1.8 V)				
V_{CC}	A5 D6 F11 F14 K4 K2 L7 P1	1.8-V PWR		Core logic supply voltage
SUPPLY VOLTAGE DIGITAL I/O (3.3 V)				
V_{CCIO}	A7 A11 D14 G1 P6 P10	3.3-V PWR		Digital I/O supply voltage
SUPPLY GROUND CORE				
V_{SS}	A6 D7 E11 E14 L2 L4 L8 P2	GND		Core supply ground reference
V_{SS}	F6 F7 F9 G6 G9 H6 H9 H11 J7 J8 J11	GND		Core supply ground reference These V_{SS} balls in the center of the package act as both electrical grounds and thermal relief. They are all tied to ground, which is the method used for thermal dissipation.
SUPPLY GROUND DIGITAL I/O				
V_{SSIO}	A12 B7 E13 F2 P5 P11	GND		Digital I/O supply ground reference

† I = input, O = output, PWR = power, GND = ground, REF = reference voltage, NC = no connect

‡ All I/O pins, except $\overline{RST}$, are configured as inputs while $\overline{PORRST}$ is low and immediately after $\overline{PORRST}$ goes high.

§ IPD = internal pulldown, IPU = internal pullup (all internal pullups and pulldowns are active on input pins, independent of the $\overline{PORRST}$ state.)

Terminal Functions (Continued)

TERMINAL NAME	TERMINAL BALL NO.	TYPE†‡	INTERNAL PULLUP/ PULLDOWN§	DESCRIPTION
NO CONNECTS				
NC	K3	NC		No connect
	L3			
	B5			
	B6			
	C6			
	E12			
	F12			
	F13			

† I = input, O = output, PWR = power, GND = ground, REF = reference voltage, NC = no connect

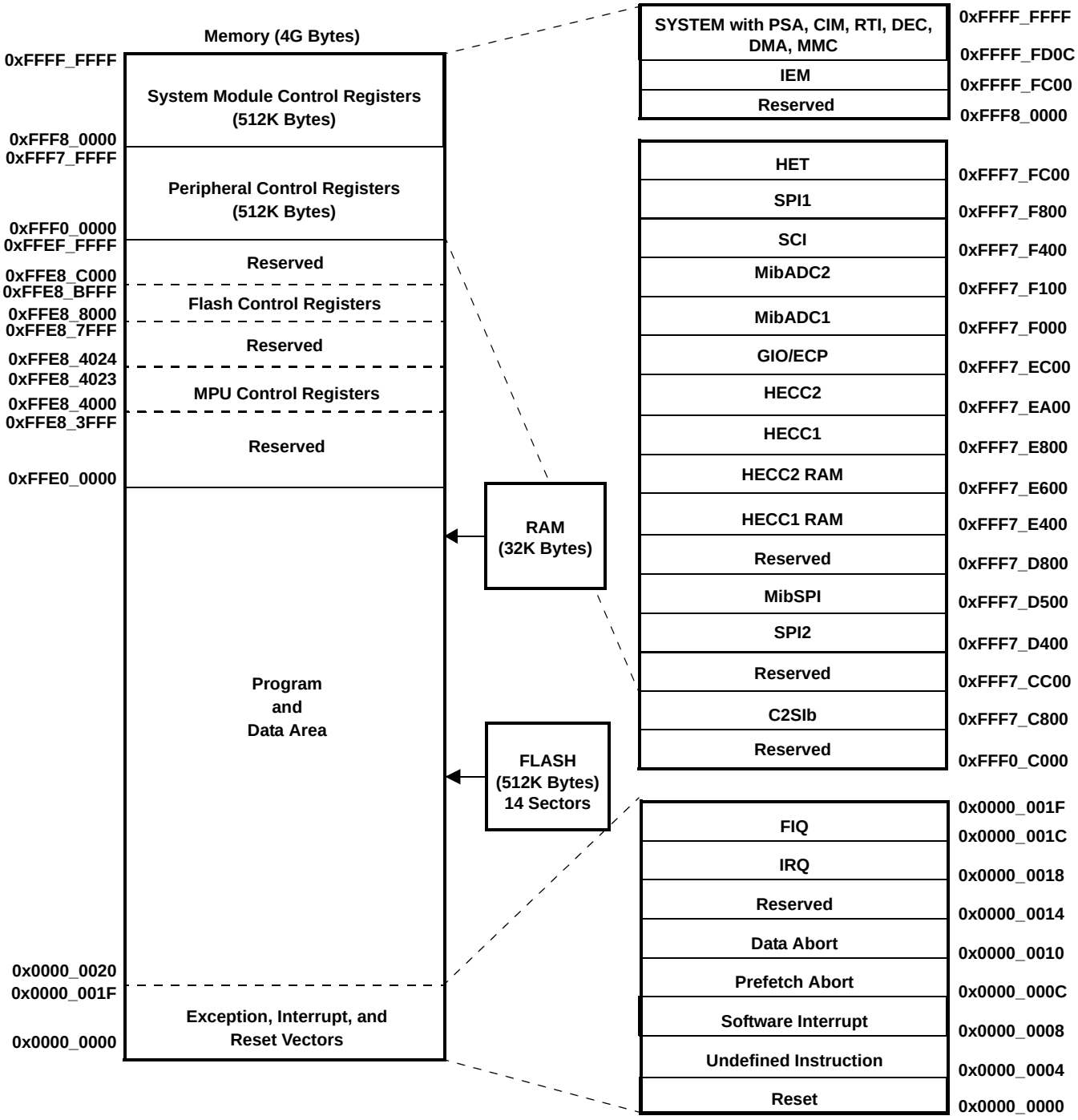
‡ All I/O pins, except $\overline{\text{RST}}$, are configured as inputs while $\overline{\text{PORRST}}$ is low and immediately after $\overline{\text{PORRST}}$ goes high.

§ IPD = internal pulldown, IPU = internal pullup (all internal pullups and pulldowns are active on input pins, independent of the $\overline{\text{PORRST}}$ state.)

VF67A DEVICE-SPECIFIC INFORMATION

memory

Figure 1 shows the memory map of the VF67A device.



NOTES: A. Memory addresses are configurable by the system (SYS) module within the range of 0x0000_0000 to 0xFFE0_0000.
B. The CPU registers are not a part of the memory map.

Figure 1. Memory Map

memory selects

Memory selects allow the user to address memory arrays (i.e., flash, RAM, and HET RAM) at user-defined addresses. Each memory select has its own set (low and high) of memory base address registers (MFBAHRx and MFBALRx) that, together, define the array's starting (base) address, block size, and protection.

The base address of each memory select is configurable to any memory address boundary that is a multiple of the decoded block size. For more information on how to control and configure these memory select registers, see the bus structure and memory sections of the *TMS470R1x System Module Reference Guide* (literature number SPNU189).

For the memory selection assignments and the memory selected, see Table 2.

Table 2. Memory Selection Assignment

MEMORY SELECT	MEMORY SELECTED (ALL INTERNAL)	MEMORY SIZE	MPU	MEMORY BASE ADDRESS REGISTER	STATIC MEM CTL REGISTER
0 (fine)	FLASH	512K	NO	MFBAHR0 and MFBALR0	
1 (fine)	FLASH		NO	MFBAHR1 and MFBALR1	
2 (fine)	RAM	32K†	YES, illegal writes blocked	MFBAHR2 and MFBALR2	
3 (fine)	RAM		YES, illegal writes blocked	MFBAHR3 and MFBALR3	
4 (fine)	HET RAM	1.5K	No	MFBAHR4 and MFBALR4	SMCR1
5 (fine)	MibSPI RAM	1K	No	MFBAHR5 and MFBALR5	SMCR2
	MibADC1 RAM	1K	No	n/a	
	MibADC2 RAM	1K	No	n/a	

† The starting addresses for both RAM memory-select signals *cannot* be offset from each other by a multiple of the user-defined block size in the memory-base address register.

JTAG security module

The VF67A device includes a JTAG security module to provide maximum security to the memory contents. The visible unlock code can be in the OTP sector or in the first bank of the user-programmable memory. For the VF67A, the visible unlock code is in the OTP sector at address 0x0000_01F8.

RAM

The VF67A device contains 32K bytes of internal static RAM configurable by the SYS module to be addressed within the range of 0x0000_0000 to 0xFFE0_0000. This VF67A RAM is implemented in one 32K array selected by two memory-select signals. This VF67A configuration imposes an additional constraint on the memory map for RAM; the starting addresses for both RAM memory selects *cannot* be offset from each other by the multiples of the size of the physical RAM (i.e., 32K for the VF67A). The VF67A RAM is addressed through memory selects 2 and 3.

The RAM can be protected by the memory protection unit (MPU) portion of the SYS module, allowing the user finer blocks of memory protection than is allowed by the memory selects. The MPU is ideal for protecting an operating system while allowing access to the current task. For more detailed information on the MPU portion of the SYS module and memory protection, see the memory section of the *TMS470R1x System Module Reference Guide* (literature number SPNU189).

F05 flash

The F05 flash memory is a nonvolatile electrically erasable and programmable memory implemented with a 32-bit-wide data bus interface. The F05 flash has an external state machine for programming and erase functions. See the *flash read* and *flash program and erase* sections below.

flash protection keys

The VF67A device provides flash protection keys. These four 32-bit protection keys prevent program/erase/compaction operations from occurring until after the four protection keys have been matched by the CPU loading the correct user keys into the FMPKEY control register. The protection keys on the VF67A are located in the last four words of the first 8K sector. For more detailed information on the flash protection keys and the FMPKEY control register, see the "Optional Quadruple Protection Keys" and "Programming the Protection Keys" portions of the *TMS470R1x F05 Flash Reference Guide* (literature number SPNU213).

flash read

The VF67A flash memory is configurable by the SYS module to be addressed within the range of 0x0000_0000 to 0xFFE0_0000. The flash is addressed through memory selects 0 and 1.

NOTE

The flash external pump voltage (V_{CCP}) is required for all operations (program, erase, and read).

flash pipeline mode

When in pipeline mode, the flash operates with a system clock of up to 60 MHz (versus a system clock in normal mode of up to 24 MHz). Flash in pipeline mode is capable of accessing 64-bit words and provides two 32-bit pipelined words to the CPU. Also, in pipeline mode, the flash can be read with no wait states when memory addresses are contiguous (after the initial 1- or 2-wait-state reads).

NOTE

After a system reset, pipeline mode is disabled (ENPIPE bit [FMREGOPT.0] is a 0). In other words, the VF67A device powers up and comes out of reset in non-pipeline mode. Furthermore, setting the flash configuration mode bit (GBLCTRL.4) will override pipeline mode.

flash program and erase

The VF67A device flash has two 265K-byte banks that consists of a total of fourteen sectors. These fourteen sectors are sized as in Table 3.

Table 3. Flash Sector Addresses

SECTOR NO.	SEGMENT	LOW ADDRESS	HIGH ADDRESS	MEMORY ARRAYS (OR BANKS)
OTP	2K Bytes	0x0000_0000	0x0000_07FF	BANK0 (256K Bytes)
0	16K Bytes	0x00000000	0x00003FFF	
1	16K Bytes	0x00004000	0x00007FFF	
2	32K Bytes	0x00008000	0x0000FFFF	
3	32K Bytes	0x00010000	0x00017FFF	
4	32K Bytes	0x00018000	0x0001FFFF	
5	32K Bytes	0x00020000	0x00027FFF	
6	32K Bytes	0x00028000	0x0002FFFF	
7	32K Bytes	0x00030000	0x00037FFF	
8	16K Bytes	0x00038000	0x0003BFFF	
9	16K Bytes	0x0003C000	0x0003FFFF	
0	64K Bytes	0x00040000	0x0004FFFF	BANK1 (256K Bytes)
1	64K Bytes	0x00050000	0x0005FFFF	
2	64K Bytes	0x00060000	0x0006FFFF	
3	64K Bytes	0x00070000	0x0007FFFF	

The minimum size for an erase operation is one sector. The maximum size for a program operation is one 16-bit word.

NOTE

The flash external pump voltage (V_{CCP}) is required for all operations (program, erase, and read).

Execution can occur from one bank while programming/erasing any or all sectors of another bank. However, execution cannot occur from any sector within a bank that is being programmed or erased.

NOTE

When the OTP sector is enabled, the rest of flash memory is disabled. The OTP memory can only be read or programmed from code executed out of RAM.

For more detailed information on flash program and erase operations, see the *TMS470R1x F05 Flash Reference Guide* (literature number SPNU213).

HET RAM

The VF67A device contains HET RAM. The HET RAM has a 128-instruction capability. The HET RAM is configurable by the SYS module to be addressed within the range of 0x0000_0000 to 0xFFE0_0000. The HET RAM is addressed through memory select 4.

peripheral selects and base addresses

The VF67A device uses ten of the sixteen peripheral selects to decode the base addresses of the peripherals. These peripheral selects are fixed and transparent to the user since they are part of the decoding scheme used by the SYS module.

Control registers for the peripherals, SYS module, and flash begin at the base addresses shown in Table 4.

Table 4. VF67A Peripherals, System Module, and Flash Base Addresses

CONNECTING MODULE	ADDRESS RANGE		PERIPHERAL SELECTS
	BASE ADDRESS	ENDING ADDRESS	
SYSTEM	0xFFFF_FFCC	0xFFFF_FFFF	N/A
RESERVED	0xFFFF_FF60	0xFFFF_FFCB	N/A
PSA	0xFFFF_FF40	0xFFFF_FF5F	N/A
CIM	0xFFFF_FF20	0xFFFF_FF3F	N/A
RTI	0xFFFF_FF00	0xFFFF_FF1F	N/A
DMA	0xFFFF_FE80	0xFFFF_FEFF	N/A
DEC	0xFFFF_FE00	0xFFFF_FE7F	N/A
MMC	0xFFFF_FD00	0xFFFF_FD7F	N/A
IEM	0xFFFF_FC00	0xFFFF_FCFF	N/A
RESERVED	0xFFFF_FB00	0xFFFF_FBFF	N/A
RESERVED	0xFFFF_FA00	0xFFFF_FAFF	N/A
DMA CMD BUFFER	0xFFFF_F800	0xFFFF_F9FF	N/A
RESERVED	0xFFF8_0000	0xFFFF_F7FF	N/A
RESERVED	0xFFF7_FD00	0xFFF7_FFFF	PS[0]
HET	0xFFF7_FC00	0xFFF7_FCFF	
RESERVED	0xFFF7_F900	0xFFF7_FBFF	PS[1]
SPI1	0xFFF7_F800	0xFFF7_F8FF	
RESERVED	0xFFF7_F500	0xFFF7_F7FF	PS[2]
SCI	0xFFF7_F400	0xFFF7_F4FF	
RESERVED	0xFFF7_F200	0xFFF7_F3FF	PS[3]
MibADC2	0xFFF7_F100	0xFFF7_F1FF	
MibADC1	0xFFF7_F000	0xFFF7_F0FF	
ECP	0xFFF7_EF00	0xFFF7_EFFF	PS[4]
RESERVED	0xFFF7_ED00	0xFFF7_EEFF	
GIO	0xFFF7_EC00	0xFFF7_ECFF	
HECC2	0xFFF7_EA00	0xFFF7_EBFF	PS[5]
HECC1	0xFFF7_E800	0xFFF7_E9FF	
HECC2 RAM	0xFFF7_E600	0xFFF7_E7FF	PS[6]
HECC1 RAM	0xFFF7_E400	0xFFF7_E5FF	
RESERVED	0xFFF7_E000	0xFFF7_E3FF	PS[7]
RESERVED	0xFFF7_DC00	0xFFF7_DFFF	PS[8]
RESERVED	0xFFF7_D800	0xFFF7_DBFF	PS[9]
RESERVED	0xFFF7_D600	0xFFF7_D7FF	PS[10]
SPI3 (MibSPI)	0xFFF7_D500	0xFFF7_D5FF	
SPI2	0xFFF7_D400	0xFFF7_D4FF	

peripheral selects and base addresses (continued)

Table 4. VF67A Peripherals, System Module, and Flash Base Addresses (Continued)

CONNECTING MODULE	ADDRESS RANGE		PERIPHERAL SELECTS
	BASE ADDRESS	ENDING ADDRESS	
RESERVED	0xFFF7_CC00	0xFFF7_D3FF	PS[11] - PS[12]
RESERVED	0xFFF7_C900	0xFFF7_CBFF	PS[13]
C2SIb	0xFFF7_C800	0xFFF7_C8FF	
RESERVED	0xFFF7_C000	0xFFF7_C7FF	PS[14] - PS[15]
RESERVED	0xFFF0_0000	0xFFF7_BFFF	N/A
Flash Control Registers	0xFFE8_8000	0xFFE8_BFFF	N/A
MPU Control Registers	0xFFE8_4000	0xFFE8_4023	N/A

direct-memory access (DMA)

The direct-memory access (DMA) controller transfers data to and from any specified location in the VF67A memory map (except for restricted memory locations like the system control registers area). The DMA manages up to 16 channels, and supports data transfer for both on-chip and off-chip memories and peripherals. The DMA controller is connected to both the CPU and Peripheral busses, enabling these data transfers to occur in parallel with CPU activity and thus, maximizing overall system performance.

Although the DMA controller has two possible configurations, for the VF67A device, the DMA controller configuration is 32 control packets and 16 channels.

For the VF67A DMA request hardwired configuration, see Table 5.

Table 5. DMA Request Lines Connections

MODULES	DMA REQUEST INTERRUPT SOURCES	DMA CHANNEL
MibADC2†	MibADC2 event	DMAREQ[0]
MibADC2†/SPI1	MibADC2 G1/SPI1 end-receive	DMAREQ[1]
MibADC2†/SPI1	MibADC2 G2/SPI1 end-transmit	DMAREQ[2]
MibADC1†	MibADC1 event	DMAREQ[3]
MibADC1†/SCI1	MibADC G1/SCI1 end-receive	DMAREQ[4]
MibADC1†/SCI1	MibADC G2/SCI1 end-transmit	DMAREQ[5]
MibADC2†	MibADC2 G1	DMAREQ[6]
MibSPI/SPI2	MIBSPI_DMA_REQ(3)/SPI2 end-receive	DMAREQ[7]
MibSPI/SPI2	MIBSPI_DMA_REQ(2)/SPI2 end-transmit	DMAREQ[8]
C2SIb	C2SIb end-receive	DMAREQ[9]
C2SIb	C2SIb end-transmit	DMAREQ[10]
MibADC2†	MibADC2 G2	DMAREQ[11]
MibADC1†	MibADC1 G1	DMAREQ[12]
MibADC1†	MibADC1 G2	DMAREQ[13]
MibSPI	MIBSPI_DMA_REQ(1)	DMAREQ[14]
MibSPI	MIBSPI_DMA_REQ(0)	DMAREQ[15]

† The MibADC is capable of being serviced by the DMA when the device is in buffered mode. For more information on buffered mode, see the MibADC section of this data sheet and the *TMS470R1x Multi-Buffered Analog-to-Digital Converter (MibADC) Reference Guide* (literature number SPNU206).

Each channel has two control packets attached to it, allowing the DMA to continuously load RAM and generate periodic interrupts so that the data can be read by the CPU. The control packets allow for the interrupt enable, and the channels determine the priority level of the interrupt.

DMA transfers occur in one of two modes:

- Non-request mode (used when transferring from memory to memory)
- Request mode (used when transferring from memory to peripheral)

For more detailed functional information on the DMA controller, see the *TMS470R1x Direct Memory Access (DMA) Controller Reference Guide* (literature number SPNU194).

interrupt priority

The central interrupt manager (CIM) portion of the SYS module manages the interrupt requests from the device modules (i.e., SPI1 or SPI2, SCI1 or SCI2, and RTI, etc.).

Although the CIM can accept up to 32 interrupt request signals, the VF67A device only uses 21 of those interrupt request signals. The request channels are maskable so that individual channels can be selectively disabled. All interrupt requests can be programmed in the CIM to be of either type:

- Fast interrupt request (FIQ)
- Normal interrupt request (IRQ)

The precedences of request channels decrease with ascending channel order in the CIM (0 [highest] and 31 [lowest] priority). For these channel priorities and the associated modules, see Table 6.

Table 6. Interrupt Priority

MODULES	INTERRUPT SOURCES	DEFAULT CIM INTERRUPT LEVEL/ CHANNEL	IEM CHANNEL
SPI1	SPI1 end-transfer/overrun	0	0
RTI	COMP2 interrupt	1	1
RTI	COMP1 interrupt	2	2
RTI	TAP interrupt	3	3
SPI2	SPI2 end-transfer/overrun	4	4
GIO	Interrupt A	5	5
RESERVED		6	6
HET	Interrupt 1	7	7
SPI3 - MibSPI	Interrupt 1	8	8
SCI	SCI exception interrupt	9	9
SCI	SCI receive interrupt	10	10
C2SIb	C2SIb interrupt	11	11
MibADC2	End event conversion	12	12
HECC1	Interrupt A	13	13
RESERVED		14	14
SPI3 - MibSPI	Interrupt 2	15	15
MibADC1	End event conversion	16	16
MibADC2	End Group 1 conversion	17	17
DMA	Interrupt 0	18	18
MibADC2	End Group 2 conversion	19	19
SCI	SCI transmit interrupt	20	20
System	SW interrupt (SSI)	21	21
RESERVED		22	22
HET	Interrupt 2	23	23
HECC1	Interrupt B	24	24
RESERVED		25	25
RESERVED		26	26
MibADC1	End Group 1 conversion	27	27
DMA	Interrupt 2	28	28
GIO	Interrupt B	29	29

interrupt priority (continued)

Table 6. Interrupt Priority (Continued)

MODULES	INTERRUPT SOURCES	DEFAULT CIM INTERRUPT LEVEL/ CHANNEL	IEM CHANNEL
MibADC1	End Group 2 conversion	30	30
RESERVED		31	31
RESERVED		31	32
RESERVED		31	33
RESERVED		31	34
RESERVED		31	35
RESERVED		31	36
RESERVED		31	37
HECC2	Interrupt A	31	38
HECC2	Interrupt B	31	39
RESERVED		31	40
RESERVED		31	41
RESERVED		31	42
RESERVED		31	43
RESERVED		31	44
RESERVED		31	45
RESERVED		31	46
RESERVED		31	47

MibADC

The multi-buffered analog-to-digital converter (MibADC) accepts an analog signal and converts the signal to a 10-bit digital value.

The VF67A MibADC module can function in two modes: compatibility mode, where its programmer's model is compatible with the TMS470R1x ADC module and its digital results are stored in digital result registers; or in buffered mode, where the digital result registers are replaced with three FIFO buffers, one for each conversion group [event, group1 (G1), and group2 (G2)]. In buffered mode, the MibADC buffers can be serviced by interrupts or by the DMA.

MibADC event trigger enhancements

The MibADC includes two major enhancements over the event-triggering capability of the TMS470R1x ADC.

- Both group1 and the event group can be configured for event-triggered operation, providing up to two event-triggered groups.
- The trigger source and polarity can be selected individually for both group 1 and the event group from the three options identified in Table 7.

Table 7. MibADC Event Hookup Configuration

EVENT #	SOURCE SELECT BITS FOR G1 OR EVENT (G1SRC[1:0] or EVSRC[1:0])	SIGNAL PIN NAME
MibADC1EVENT0	00	ADEVT1
MibADC1EVENT1	01	HET[18]
MibADC1EVENT2	10	HET[19]
MibADC1EVENT3	11	RESERVED
MibADC2EVENT0	00	ADEVT2
MibADC2EVENT1	01	HET[18]
MibADC2EVENT2	10	HET[19]
MibADC2EVENT3	11	RESERVED

For group 1, these event-triggered selections are configured via the group 1 source select bits (G1SRC[1:0]) in the AD event source register (ADEVTSRC.[5:4]). For the event group, these event-triggered selections are configured via the event group source select bits (EVSRC[1:0]) in the AD event source register (ADEVTSRC.[1:0]).

For more detailed functional information on the MibADC, see the *TMS470R1x Multi-Buffered Analog-to-Digital Converter (MibADC) Reference Guide* (literature number SPNU206).

MibSPI

The MibSPI is a high-speed synchronous serial input/output port that allows a serial bit stream of programmed length (one to 16 bits) to be shifted into and out of the device at a programmed bit-transfer rate. The MibSPI is normally used for communication between the microcontroller and external peripherals or another microcontroller. Typical applications include interface to external I/O or peripheral expansion via devices such as shift registers, display drivers, and analog-to-digital converters.

Table 7 shows the trigger sources for MibSPI.

Table 8. MibSPI Event Hookup Configuration

EVENT #	SIGNAL PIN NAME
EVENT0	RESERVED
EVENT1	GIOA[0]
EVENT2	GIOA[2]
EVENT3	GIOA[3]
EVENT4	RESERVED
EVENT5	HET[20]
EVENT6	HET[21]
EVENT7	HET[22]
EVENT8	HET[23]
EVENT9	HET[25]
EVENT10	HET[26]
EVENT11	HET[27]
EVENT12	ADEVT1
EVENT13	ADEVT2
EVENT14	Internal Tick Counter

development system support

Texas Instruments provides extensive hardware and software development support tools for the TMS470R1x family. These support tools include:

- Code Composer Studio™ Integrated Development Environment (IDE)
  - Fully integrated suite of software development tools
  - Includes Compiler/Assembler/Linker, Debugger, and Simulator
  - Supports Real-Time analysis, data visualization, and open API
- Optimizing C compiler
  - Supports high-level language programming
  - Full implementation of the standard ANSI C language
  - Powerful optimizer that improves code-execution speed and reduces code size
  - Extensive run-time support library included
  - TMS470R1x control registers easily accessible from the C program
  - Interfaces C functions and assembly functions easily
  - Establishes comprehensive, easy-to-use tool set for the development of high-performance microcontroller applications in C/C++
- Assembly language tools (assembler and linker)
  - Provides extensive macro capability
  - Allows high-speed operation
  - Allows extensive control of the assembly process using assembler directives
  - Automatically resolves memory references as C and assembly modules are combined
- TMS470R1x CPU Simulator
  - Provides capability to simulate CPU operation without emulation hardware
  - Allows inspection and modifications of memory locations
  - Allows debugging programs in C or assembly language
- XDS emulation communication kits
  - Allow high-speed JTAG communication to the TMS470R1x emulator or target board

For information on pricing and availability, contact the nearest TI field office or authorized distributor.

Code Composer Studio is a trademark of Texas Instruments.

documentation support

Extensive documentation supports all of the TMS470 microcontroller family generation of devices. The types of documentation available include: data sheets with design specifications; complete user's guides for all devices and development support tools; and hardware and software applications. Useful reference documentation includes:

- User's Guides:
  - *TMS470R1x 32-Bit RISC Microcontroller Family User's Guide* (literature number SPNU134)
  - *TMS470R1x C/C++ Compiler User's Guide* (literature number SPNU151)
  - *TMS470R1x Code Generation Tools Getting Started Guide* (literature number SPNU117)
  - *TMS470R1x C Source Debugger User's Guide* (literature number SPNU124)
  - *TMS470R1x Assembly Language Tools User's Guide* (literature number SPNU118)
  - *TMS470R1x System Module Reference Guide* (literature number SPNU189)
  - *TMS470R1x Direct Memory Access (DMA) Controller Reference Guide* (literature number SPNU194)
  - *TMS470R1x Serial Peripheral Interface (SPI) Reference Guide* (literature number SPNU195)
  - *TMS470R1x Controller Area Network (CAN) Reference Guide* (literature number SPNU197)
  - *TMS470R1x High-End Timer (HET) Reference Guide* (literature number SPNU199)
  - *TMS470R1x External Clock Prescale (ECP) Reference Guide* (literature number SPNU202)
  - *TMS470R1x Multi-Buffered Analog-to-Digital Converter (MibADC) Reference Guide* (literature number SPNU206)
  - *TMS470R1x F05 Flash Reference Guide* (literature number SPNU213)
  - *TMS470R1x Class II Serial Interface B (C2SIb) Reference Guide* (literature number SPNU214)
  - *TMS470R1x Frequency-Modulated Phase-Locked Loop (FMPLL) Clock Module Reference Guide* (literature number SPNU221)
  - *TMS470R1x Multi-Buffered Serial Peripheral Interface (MibSPI) Reference Guide* (literature number SPNU217)
- Application Reports:
  - *Analog Watchdog Resistor, Capacitor and Discharge Interval Selection Constraints* (literature number SPNA005)
  - *F05/C05 Power Up Reset and Power Sequencing Requirements* (literature number SPNA009)

device numbering conventions

Figure 2 illustrates the numbering and symbol nomenclature for the TMS470R1x family.

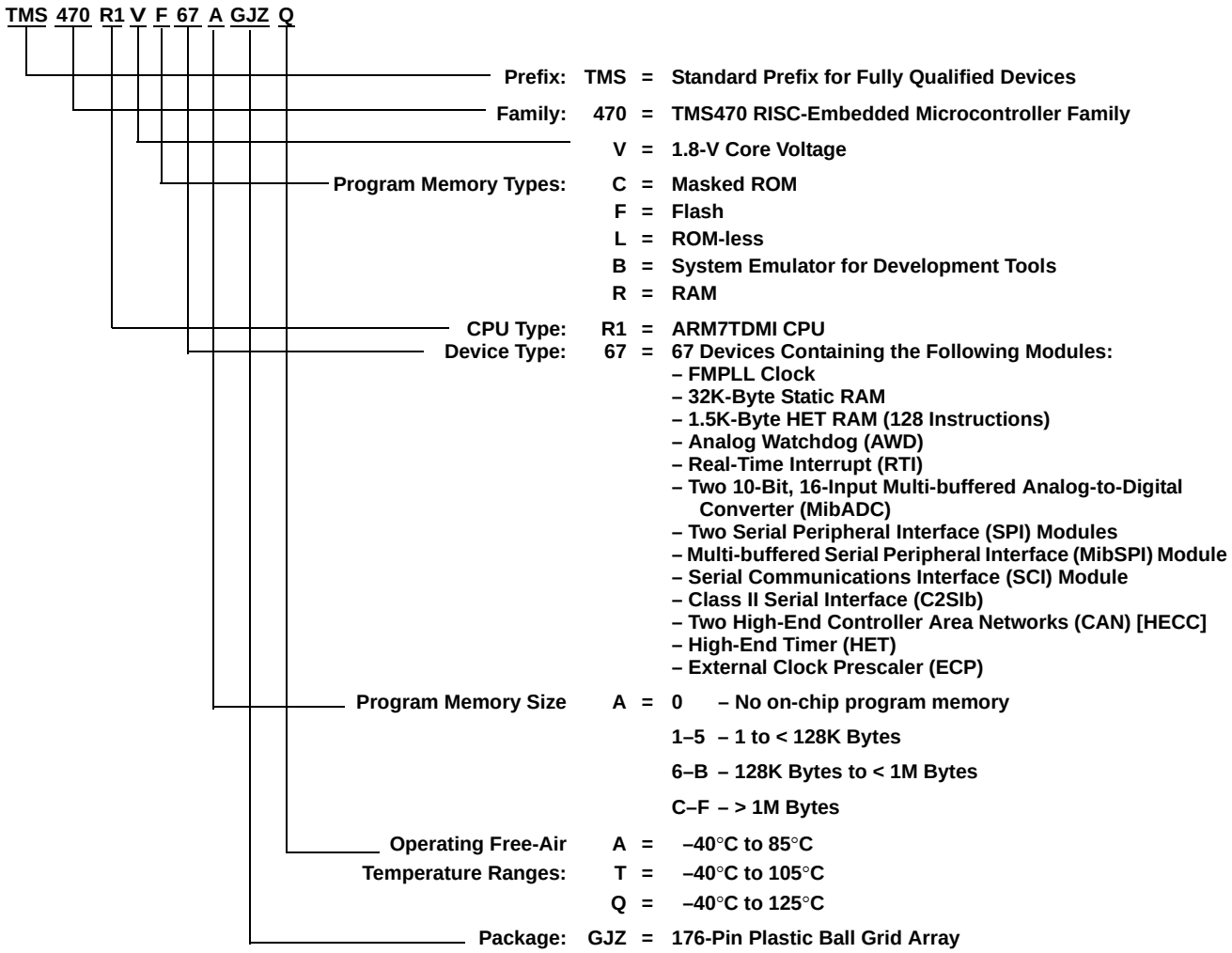


Figure 2. TMS470R1x Family Nomenclature

device identification code register

The device identification code register identifies the silicon version, the technology family (TF), a ROM or flash device, and an assigned device-specific part number (see Table 9). The VF67A device identification code register value is 0x093F.

Table 9. TMS470 Device ID Bit Allocation Register

	BIT 31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	BIT 16
FFFF_FFF0	RESERVED															
	R-K															

	BIT 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	BIT 0
	VERSION				TF	R/F	PART NUMBER							1	1	1
	R-K				R-K	R-K	R-K							R-1	R-1	R-1

LEGEND:
For bits 3–15: R = Read only, -K = Value constant after $\overline{\text{RESET}}$
For bits 0–2: R = Read only, -1 = Value after $\overline{\text{RESET}}$

Bits 31:16 **Reserved.** Reads are undefined and writes have no effect.

Bits 15:12 **VERSION.** Silicon version (revision) bits

These bits identify the silicon version of the device.

Bit 11 **TF.** Technology Family (TF) bit

This bit distinguishes the technology family core power supply:

0 = 3.3 V for F10/C10 devices

1 = 1.8 V for F05/C05 devices

Bit 10 **R/F.** ROM/flash bit

This bit distinguishes between ROM and flash devices:

0 = Flash device

1 = ROM device

Bits 9:3 **PART NUMBER.** Device-specific part number bits

These bits identify the assigned device-specific part number.

The assigned device-specific part number for the VF67A device is: 0100111.

Bits 2:0 **"1" Mandatory High.** Bits 2,1, and 0 are tied high by default.

device part numbers

Table 10 lists all the available TMS470R1VF67A devices.

Table 10. Device Part Number

DEVICE PART NUMBER	PROGRAM MEMORY		PACKAGE TYPE	TEMPERATURE RANGES		
	ROM	FLASH EEPROM	176-PIN PBGA	–40°C TO 85°C	–40°C TO 105°C	–40°C TO 125°C
TMS470R1VF67AGJZA		X	X	X		
TMS470R1VF67AGJZT		X	X		X	
TMS470R1VF67AGJZQ		X	X			X

DEVICE ELECTRICAL SPECIFICATIONS AND TIMING PARAMETERS

absolute maximum ratings over operating free-air temperature range, Q version (unless otherwise noted)†

Supply voltage ranges: V_{CC} (see Note 1) . . . . . −0.5 V to 2.5 V
Supply voltage ranges: V_{CCIO}, V_{CCAD}, V_{CCP} (flash pump) (see Note 1) . . . . . −0.5 V to 4.1 V
Input voltage range: All input pins . . . . . −0.5 V to 4.1 V
Input clamp current: I_{IK} ($V_I < 0$ or $V_I > V_{CCIO}$)
All pins except ADIN[0:11], $\overline{\text{PORRST}}$, $\overline{\text{TRST}}$, TEST and TCK . . . . . ±20 mA
I_{IK} ($V_I < 0$ or $V_I > V_{CCAD}$)
ADIN[0:11] . . . . . ±10 mA
Operating free-air temperature ranges, T_A: A version . . . . . −40°C to 85°C
T version . . . . . −40°C to 105°C
Q version . . . . . −40°C to 125°C
Operating junction temperature range, T_J . . . . . −40°C to 150°C
Storage temperature range, T_{stg} . . . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to their associated grounds.

device recommended operating conditions‡

			MIN	NOM	MAX	UNIT
V_{CC}	Digital logic and flash supply voltage (Core)		1.81	1.95	2.05	V
V_{CCIO}	Digital logic supply voltage (I/O)		3	3.3	3.6	V
V_{CCAD}	ADC supply voltage		3	3.3	3.6	V
V_{CCP}	Flash pump supply voltage		3	3.3	3.6	V
V_{SS}	Digital logic supply ground			0		V
V_{SSAD}	ADC supply ground		−0.1		0.1	V
T_A	Operating free-air temperature	A version	−40		85	°C
		T version	−40		105	°C
		Q version	−40		125	°C
T_J	Operating junction temperature		−40		150	°C

‡ All voltages are with respect to V_{SS}, except V_{CCAD}, which is with respect to V_{SSAD}.

electrical characteristics over recommended operating free-air temperature range, Q version (unless otherwise noted)†

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
V_{hys}	Input hysteresis			0.15		V
V_{IL}	Low-level input voltage	All inputs‡ except OSCIN		– 0.3	0.8	V
		OSCIN only		– 0.3	0.35 V_{CC}	
V_{IH}	High-level input voltage	All inputs except OSCIN		2	V_{CCIO} + 0.3	V
		OSCIN only		0.65 V_{CC}	V_{CC} + 0.3	
V_{th}	Input threshold voltage	AWD only		1.35	1.8	V
RDS_{ON}	Drain to source on resistance	AWD only§	V_{OL} = 0.35V @ I_{OL} = 4mA		90	Ω
V_{OL}	Low-level output voltage¶		I_{OL} = I_{OL} MAX		0.2 V_{CCIO}	V
			I_{OL} = 50 μA		0.2	
V_{OH}	High-level output voltage¶		I_{OH} = I_{OH} MIN	0.8 V_{CCIO}		V
			I_{OH} = 50 μA	V_{CCIO} – 0.2		
I_{IC}	Input clamp current (I/O pins)#		$V_I < V_{SSIO} – 0.3$ or $V_I > V_{CCIO} + 0.3$	–2	2	mA
I_I	Input current (I/O pins)	I_{IL} Pulldown	$V_I = V_{SS}$	–1	1	μA
		I_{IH} Pulldown	$V_I = V_{CCIO}$	5	40	
		I_{IL} Pullup	$V_I = V_{SS}$	–40	–5	
		I_{IH} Pullup	$V_I = V_{CCIO}$	–1	1	
		All other pins	No pullup or pulldown	–1	1	
I_{OL}	Low-level output current	CLKOUT, AWD, TMS, TMS2, $\overline{RST}$	V_{OL} = V_{OL} MAX		4	mA
		All other output pins‖	V_{OL} = V_{OL} MAX		2	mA
I_{OH}	High-level output current	CLKOUT, TMS, TMS2, $\overline{RST}$	V_{OH} = V_{OH} MIN	–4		mA
		All other output pins‖	V_{OH} = V_{OH} MIN	–2		mA

† Source currents (out of the device) are negative while sink currents (into the device) are positive.

‡ This does not apply to the $\overline{PORRST}$ pin. For $\overline{PORRST}$ exceptions, see the $\overline{RST}$ and $\overline{PORRST}$ timings section on page 37.

§ These values help to determine the external RC network circuit. For more details, see the *TMS470R1x System Module Reference Guide* (literature number SPNU189).

¶ V_{OL} and V_{OH} are linear with respect to the amount of load current (I_{OL}/I_{OH}) applied.

Parameter does not apply to input-only or output-only pins.

‖ The 2 mA buffers on this device are called zero-dominant buffers. If two of these buffers are shorted together and one is outputting a low level and the other is outputting a high level, the resulting value will always be low.

☆For flash pumps/banks in sleep mode.

❑I/O pins configured as inputs or outputs with no load. All pulldown inputs ≤ 0.2 V. All pullup inputs ≥ V_{CCIO} – 0.2 V.

electrical characteristics over recommended operating free-air temperature range, Q version (unless otherwise noted)†

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC}	V_{CC} Digital supply current (operating mode)	SYSCLK = 60 MHz, V_{CC} = 2.05 V			118	mA
	V_{CC} Digital supply current (standby mode)☆	OSCIN = 7.5 MHz, V_{CC} = 2.05 V			3.5	mA
	V_{CC} Digital supply current (halt mode)☆	V_{CC} = 2.05 V			1	mA
I_{CCIO}	V_{CCIO} Digital supply current (operating mode)	No DC load, V_{CCIO} = 3.6 V❑			10	mA
	V_{CCIO} Digital supply current (standby mode)	No DC load, V_{CCIO} = 3.6 V❑			100	μA
	V_{CCIO} Digital supply current (halt mode)	No DC load, V_{CCIO} = 3.6 V❑			100	μA
I_{CCADn} (n = 1 or 2)	V_{CCADn} supply current (operating mode)	All frequencies, V_{CCADn} = 3.6 V			15	mA
	V_{CCADn} supply current (standby mode)	No DC load, V_{CCADn} = 3.6 V			20	μA
	V_{CCADn} supply current (halt mode)	V_{CCADn} = 3.6 V			20	μA
I_{CCP}	V_{CCP} pump supply current	V_{CCP} = 3.6 V read operation			60	mA
		V_{CCP} = 3.6 V program and erase			70	mA
		V_{CCP} = 3.6 V standby mode☆			100	μA
		V_{CCP} = 3.6 V halt mode operation☆			20	μA
C_I	Input capacitance			2		pF
C_O	Output capacitance			3		pF

† Source currents (out of the device) are negative while sink currents (into the device) are positive.

‡ This does not apply to the $\overline{\text{PORRST}}$ pin. For $\overline{\text{PORRST}}$ exceptions, see the $\overline{\text{RST}}$ and $\overline{\text{PORRST}}$ timings section on page 37.

§ These values help to determine the external RC network circuit. For more details, see the *TMS470R1x System Module Reference Guide* (literature number SPNU189).

¶ V_{OL} and V_{OH} are linear with respect to the amount of load current (I_{OL}/I_{OH}) applied.

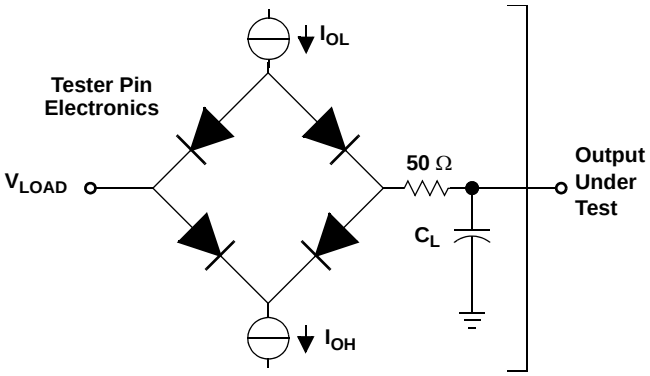
Parameter does not apply to input-only or output-only pins.

‖ The 2 mA buffers on this device are called zero-dominant buffers. If two of these buffers are shorted together and one is outputting a low level and the other is outputting a high level, the resulting value will always be low.

☆For flash pumps/banks in sleep mode.

❑I/O pins configured as inputs or outputs with no load. All pulldown inputs ≤ 0.2 V. All pullup inputs ≥ V_{CCIO} − 0.2 V.

PARAMETER MEASUREMENT INFORMATION



Where:I_{OL}=I_{OL} MAX for the respective pin (see Note A)

I_{OH}=I_{OH} MIN for the respective pin (see Note A)

V_{LOAD}=1.5 V

C_L=150-pF typical load-circuit capacitance (see Note B)

NOTES: A. For these values, see the "electrical characteristics over recommended operating free-air temperature range" table.
B. All timing parameters measured using an external load capacitance of 150 pF unless otherwise noted.

Figure 3. Test Load Circuit

timing parameter symbology

Timing parameter symbols have been created in accordance with JEDEC Standard 100. In order to shorten the symbols, some of the pin names and other related terminology have been abbreviated as follows:

CM	Compaction, CMPCT	RD	Read
CO	CLKOUT	RST	Reset, $\overline{\text{RST}}$
ER	Erase	RX	SCInRX
ICLK	Interface clock	S	Slave mode
M	Master mode	SCC	SCInCLK
OSC, OSCI	OSCIN	SIMO	SPInSIMO
OSCO	OSCOUT	SOMI	SPInSOMI
P	Program, PROG	SPC	SPInCLK
R	Ready	SYS	System clock
R0	Read margin 0, RDMRGN0	TX	SCInTX
R1	Read margin 1, RDMRGN1		

Lowercase subscripts and their meanings are:

a	access time	r	rise time
c	cycle time (period)	su	setup time
d	delay time	t	transition time
f	fall time	v	valid time
h	hold time	w	pulse duration (width)

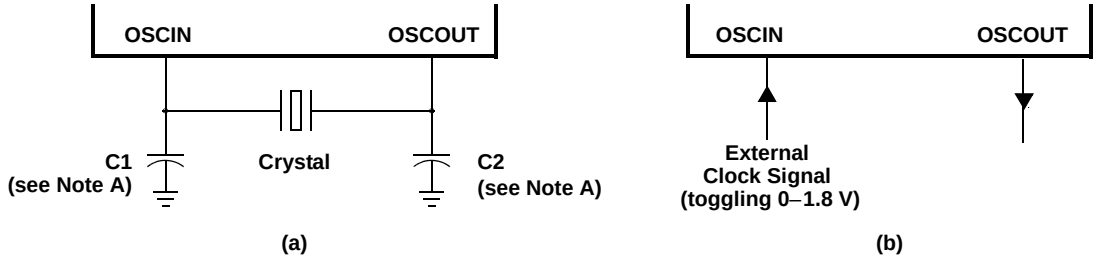
The following additional letters are used with these meanings:

H	High	X	Unknown, changing, or don’t care level
L	Low	Z	High impedance
V	Valid		

external reference resonator/crystal oscillator clock option

The oscillator is enabled by connecting the appropriate fundamental 4–10 MHz resonator/crystal and load capacitors across the external OSCIN and OSCOUT pins as shown in Figure 4a. The oscillator is a single-stage inverter held in bias by an integrated bias resistor. This resistor is disabled during leakage test measurement and HALT mode. **TI strongly encourages each customer to submit samples of the device to the resonator/crystal vendors for validation.** The vendors are equipped to determine what load capacitors will best tune their resonator/crystal to the microcontroller device for optimum start-up and operation over temperature/voltage extremes.

An external oscillator source can be used by connecting a 1.8V clock signal to the OSCIN pin and leaving the OSCOUT pin unconnected (open) as shown in Figure 4b.



NOTE A: The values of C1 and C2 should be provided by the resonator/crystal vendor.

Figure 4. Crystal/Clock Connection

FMPLL and clock specifications

timing requirements for FMPLL circuits enabled or disabled

		MIN	TYP	MAX	UNIT
$f_{(OSC)}$	Input clock frequency	4		10	MHz
$t_{c(OSC)}$	Cycle time, OSCIN	100			ns
$t_{w(OSCIL)}$	Pulse duration, OSCIN low	15			ns
$t_{w(OSCIH)}$	Pulse duration, OSCIN high	15			ns
$f_{(OSCRST)}$	OSC FAIL frequency†		53		kHz

† Causes a device reset (specifically a clock reset) by setting the RST OSC FAIL (GLBCTRL.15) and the OSC FAIL flag (GLBSTAT.1) bits equal to 1. For more detailed information on these bits and device resets, see the *TMS470R1x System Module Reference Guide* (literature number SPNU189).

switching characteristics over recommended operating conditions for clocks‡§

PARAMETER		TEST CONDITIONS¶	MIN	MAX	UNIT
$f_{(SYS)}$	System clock frequency#	pipeline mode disabled		24	MHz
		pipeline mode enabled		60	MHz
$f_{(CONFIG)}$	System clock frequency	flash config mode		24	MHz
$f_{(ICLK)}$	Interface clock frequency	pipeline mode enabled		25	MHz
		pipeline mode disabled		24	MHz
$f_{(ECLK)}$	External clock output frequency for ECP Module	pipeline mode enabled		25	MHz
		pipeline mode disabled		24	MHz
$t_{c(SYS)}$	Cycle time, system clock	pipeline mode disabled	41.6		ns
		pipeline mode enabled	16.7		ns
$t_{c(CONFIG)}$	Cycle time, system clock	flash config mode	41.6		ns
$t_{c(ICLK)}$	Cycle time, interface clock	pipeline mode enabled	40		ns
		pipeline mode disabled	41.6		ns
$t_{c(ECLK)}$	Cycle time, ECP module external clock output	pipeline mode enabled	40		ns
		pipeline mode disabled	41.6		ns

‡ $f_{(SYS)} = M \times f_{(OSC)} / R$, where M = {1,2,4, or 8} when PLLDIS = 0, and M = 1 when PLLDIS = 1; and where R = {1,2,4, or 8}. Please see the *TMS470R1x Frequency-Modulated Phase-Locked Loop (FMPLL) Clock Module Reference Guide* (literature number SPNU221) for details on M and R values.

$f_{(SYS)} = f_{(OSC)} / R$, where R = {1,2,3,4,5,6,7,8} when PLLDIS = 1.

$f_{(ICLK)} = f_{(SYS)} / X$, where X = {1,2,3,4,5,6,7,8,9,10,11,12,13,14,15,16}. X is the interface clock divider ratio determined by the PCR0.[4:1] bits in the SYS module.

§ $f_{(ECLK)} = f_{(ICLK)} / N$, where N = {1 to 256}. N is the ECP prescale value defined by the ECPCTRL.[7:0] register bits in the ECP module.

¶ Pipeline mode enabled or disabled is determined by the ENPIPE bit (FMREGOPT.0).

Flash Vread must be set to 5V to achieve maximum System Clock Frequency.

FMPLL and clock specifications (continued)

switching characteristics over recommended operating conditions for external clocks (see Figure 5 and Figure 6)†‡§

NO.	PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
1	$t_{w(COL)}$	Pulse duration, CLKOUT low	SYSCLK or MCLK¶	$0.5t_{c(SYS)} - t_f$		ns
			ICLK, X is even or 1#	$0.5t_{c(ICLK)} - t_f$		
			ICLK, X is odd and not 1#	$0.5t_{c(ICLK)} + 0.5t_{c(SYS)} - t_f$		
2	$t_{w(COH)}$	Pulse duration, CLKOUT high	SYSCLK or MCLK¶	$0.5t_{c(SYS)} - t_r$		ns
			ICLK, X is even or 1#	$0.5t_{c(ICLK)} - t_r$		
			ICLK, X is odd and not 1#	$0.5t_{c(ICLK)} - 0.5t_{c(SYS)} - t_r$		
3	$t_{w(EOL)}$	Pulse duration, ECLK low	N is even and X is even or odd	$0.5t_{c(ECLK)} - t_f$		ns
			N is odd and X is even	$0.5t_{c(ECLK)} - t_f$		
			N is odd and X is odd and not 1	$0.5t_{c(ECLK)} + 0.5t_{c(SYS)} - t_f$		
4	$t_{w(EOH)}$	Pulse duration, ECLK high	N is even and X is even or odd	$0.5t_{c(ECLK)} - t_r$		ns
			N is odd and X is even	$0.5t_{c(ECLK)} - t_r$		
			N is odd and X is odd and not 1	$0.5t_{c(ECLK)} - 0.5t_{c(SYS)} - t_r$		

† X = {1,2,3,4,5,6,7,8,9,10,11,12,13,14,15,16}. X is the interface clock divider ratio determined by the PCR0.[4:1] bits in the SYS module.
‡ N = {1 to 256}. N is the ECP prescale value defined by the ECPCTRL.[7:0] register bits in the ECP module.
§ CLKOUT/ECLK pulse durations (low/high) are a function of the OSCIN pulse durations when PLLDIS is active.
¶ Clock source bits selected as either SYSCLK (CLKCNTL.[6:5] = 11 binary) or MCLK (CLKCNTL.[6:5] = 10 binary).
# Clock source bits selected as ICLK (CLKCNTL.[6:5] = 01 binary).

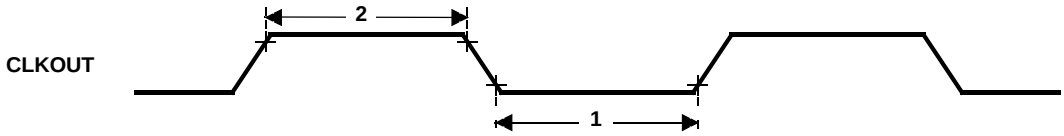


Figure 5. CLKOUT Timing Diagram

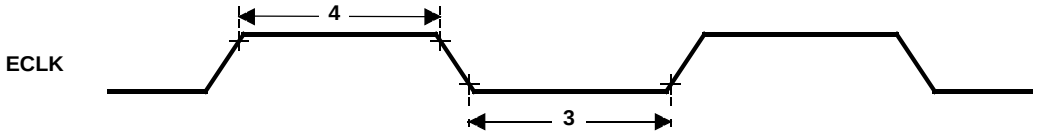


Figure 6. ECLK Timing Diagram

FMPLL and clock specifications (continued)

Table 11 is based on a specific OSCIN, SYSCLK, and modulation depth, varying the number of glitches per four periods in order to obtain the modulation frequency. The numerical integration yields an average frequency that is compared to the base frequency in order to find the maximum, worst-case percentage offset over a given length of time in μs.

Table 11. Average FMPLL Frequency (OSCIN = 7.5MHz, SYSCLK = 60MHz, CAN = 500kHz)

MODULATION FREQUENCY	EXPECTED MODULATION DEPTH	ACTUAL MODULATION DEPTH FROM CHARACTERIZATION	4μs	6μs	8μs	10μs	12μs	14μs
134 kHz	2%	6.89%	1.23%	0.60%	0.26%	0.51%	0.44%	0.22%
117 kHz	2%	6.99%	1.42%	0.81%	0.22%	0.39%	0.49%	0.40%
104 kHz	2%	7.01%	1.65%	1.13%	0.50%	0.23%	0.48%	0.53%
94 kHz	2%	7.05%	1.83%	1.28%	0.76%	0.23%	0.35%	0.53%
134 kHz	1%	5.62%	0.78%	0.42%	0.20%	0.35%	0.30%	0.16%
117 kHz	1%	5.66%	0.91%	0.53%	0.17%	0.28%	0.33%	0.27%
104 kHz	1%	5.63%	1.09%	0.77%	0.35%	0.20%	0.34%	0.37%
94 kHz	1%	5,63%	1.23%	0.87%	0.52%	0.18%	0.26%	0.38%
134 kHz	0.5%	4,42%	0.64%	0.39%	0.21%	0.33%	0.27%	0.17%
104 kHz	0.5%	4,41%	0.81%	0.60%	0.27%	0.18%	0.27%	0.29%
94 kHz	0.5%	4.41%	0.93%	0.67%	0.40%	0.16%	0.22%	0.30%

MODULATION FREQUENCY	EXPECTED MODULATION DEPTH	ACTUAL MODULATION DEPTH FROM CHARACTERIZATION	16μs	18μs	20μs	22μs	24μs	26μs
134 kHz	2%	6.89%	0.22%	0.31%	0.26%	0.09%	0.20%	0.23%
117 kHz	2%	6.99%	0.20%	0.18%	0.30%	0.29%	0.18%	0.10%
104 kHz	2%	7.01%	0.42%	0.22%	0.16%	0.30%	0.33%	0.25%
94 kHz	2%	7.05%	0.53%	0.41%	0.22%	0.14%	0.28%	0.33%
134 kHz	1%	5.62%	0.16%	0.21%	0.19%	0.08%	0.15%	0.16%
117 kHz	1%	5.66%	0.15%	0.15%	0.21%	0.20%	0.14%	0.09%
104 kHz	1%	5.63%	0.30%	0.16%	0.13%	0.21%	0.24%	0.18%
94 kHz	1%	5,63%	0.37%	0.29%	0.17%	0.12%	0.21%	0.23%
134 kHz	0.5%	4,42%	0.17%	0.20%	0.18%	0.09%	0.16%	0.15%
104 kHz	0.5%	4,41%	0.24%	0.14%	0.12%	0.17%	0.19%	0.14%
94 kHz	0.5%	4.41%	0.29%	0.23%	0.14%	0.11%	0.17%	0.19%

$\overline{\text{RST}}$ and $\overline{\text{PORRST}}$ timings

timing requirements for $\overline{\text{PORRST}}$ (see Figure 7)

NO.			MIN	MAX	UNIT
	V_{CCPORL}	V_{CC} low supply level when $\overline{\text{PORRST}}$ must be active during power up		0.6	V
	V_{CCPORH}	V_{CC} high supply level when $\overline{\text{PORRST}}$ must remain active during power up and become active during power down	1.5		V
	$V_{CCIOPORL}$	V_{CCIO} low supply level when $\overline{\text{PORRST}}$ must be active during power up		1.1	V
	$V_{CCIOPORH}$	V_{CCIO} high supply level when $\overline{\text{PORRST}}$ must remain active during power up and become active during power down	2.75		V
	V_{IL}	Low-level input voltage after $V_{CCIO} > V_{CCIOPORH}$		0.2 V_{CCIO}	V
	$V_{IL(PORRST)}$	Low-level input voltage of $\overline{\text{PORRST}}$ before $V_{CCIO} > V_{CCIOPORL}$		0.5	V
3	$t_{su(PORRST)r}$	Setup time, $\overline{\text{PORRST}}$ active before $V_{CCIO} > V_{CCIOPORL}$ during power up	0		ms
5	$t_{su(VCCIO)r}$	Setup time, $V_{CCIO} > V_{CCIOPORL}$ before $V_{CC} > V_{CCPORL}$	0		ms
6	$t_{h(PORRST)r}$	Hold time, $\overline{\text{PORRST}}$ active after $V_{CC} > V_{CCPORH}$	1		ms
7	$t_{su(PORRST)f}$	Setup time, $\overline{\text{PORRST}}$ active before $V_{CC} \leq V_{CCPORH}$ during power down	8		μs
8	$t_{h(PORRST)rio}$	Hold time, $\overline{\text{PORRST}}$ active after $V_{CCIO} > V_{CCIOPORH}$	1		ms
9	$t_{h(PORRST)d}$	Hold time, $\overline{\text{PORRST}}$ active after $V_{CC} < V_{CCPORL}$	0		ms
10	$t_{su(PORRST)fio}$	Setup time, $\overline{\text{PORRST}}$ active before $V_{CCIO} \leq V_{CCIOPORH}$ during power down	0		ns
11	$t_{su(VCCIO)f}$	Setup time, $V_{CC} < V_{CCPORL}$ before $V_{CCIO} < V_{CCIOPORL}$	0		ns

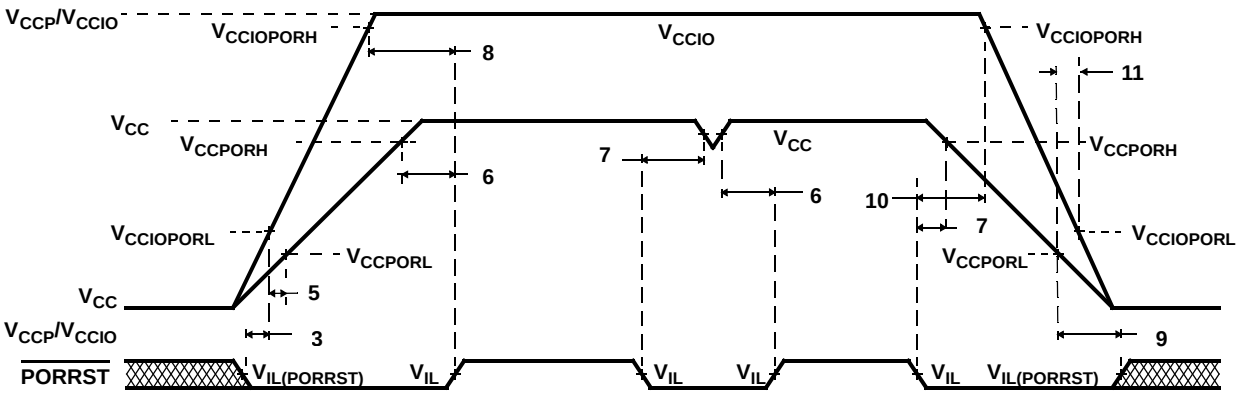


Figure 7. $\overline{\text{PORRST}}$ Timing Diagram

switching characteristics over recommended operating conditions for $\overline{\text{RST}}$†

PARAMETER		MIN	MAX	UNIT
$t_{v(RST)}$	Valid time, $\overline{\text{RST}}$ active after $\overline{\text{PORRST}}$ inactive	$4112t_{c(OSC)}$		ns
	Valid time, $\overline{\text{RST}}$ active (all others)	$8t_{c(SYS)}$		
t_{fsu}	Flash start up time, from $\overline{\text{RST}}$ inactive to fetch of first instruction from flash (flash pump stabilization time)	$836t_{c(OSC)}$		ns

† Specified values do NOT include rise/fall times. For rise and fall timings, see the switching characteristics for output timings versus load capacitance table.

JTAG scan interface timing (JTAG clock specification 10-MHz and 50-pF load on TDO output)

NO.			MIN	MAX	UNIT
1	$t_{c(JTAG)}$	Cycle time, JTAG low and high period	50		ns
2	$t_{su(TDI/TMS - TCKr)}$	Setup time, TDI, TMS before TCK rise (TCKr)	15		ns
3	$t_{h(TCKr -TDI/TMS)}$	Hold time, TDI, TMS after TCKr	15		ns
4	$t_{h(TCKf -TDO)}$	Hold time, TDO after TCKf	10		ns
5	$t_{d(TCKf -TDO)}$	Delay time, TDO valid after TCK fall (TCKf)		45	ns

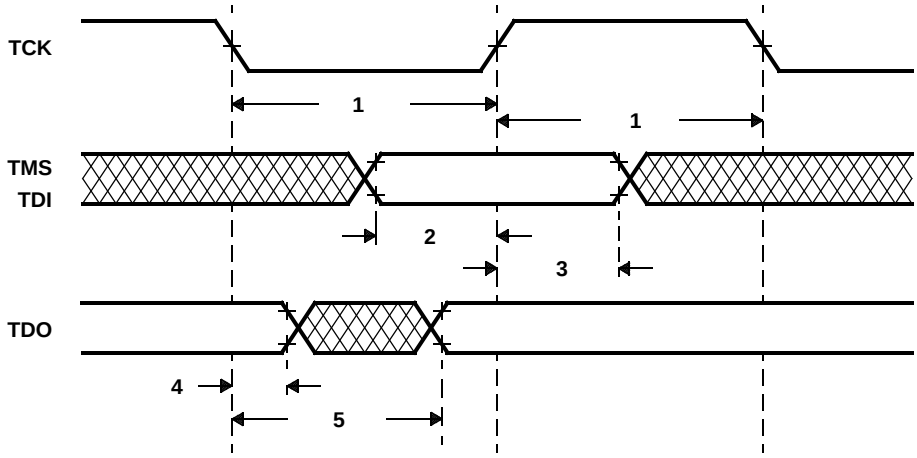


Figure 8. JTAG Scan Timing

output timings

switching characteristics for output timings versus load capacitance (C_L) (see Figure 9)

PARAMETER			MIN	MAX	UNIT
t_r	Rise time, CLKOUT, AWD, TMS, TMS2, $\overline{RST}$	C_L = 15 pF	2.5	8	ns
		C_L= 50 pF	5	14	
		C_L = 100 pF	9	23	
		C_L = 150 pF	13	32	
t_f	Fall time, CLKOUT, AWD, TMS, TMS2, $\overline{RST}$	C_L = 15 pF	2.5	8	ns
		C_L= 50 pF	5	14	
		C_L = 100 pF	9	23	
		C_L = 150 pF	13	32	
t_r	Rise time, all other output pins	C_L = 15 pF	2.5	10	ns
		C_L = 50 pF	6.0	25	
		C_L = 100 pF	12	45	
		C_L = 150 pF	18	65	
t_f	Fall time, all other output pins	C_L = 15 pF	3	10	ns
		C_L = 50 pF	8.5	25	
		C_L = 100 pF	16	45	
		C_L = 150 pF	23	65	

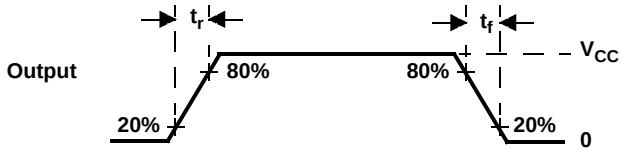


Figure 9. CMOS-Level Outputs

input timings

timing requirements for input timings† (see Figure 10)

		MIN	MAX	UNIT
t_{pw}	Input minimum pulse width	$t_{c(ICLK)}$ + 10		ns

† $t_{c(ICLK)}$ = interface clock cycle time = $1/f_{(ICLK)}$

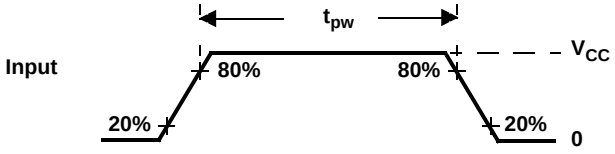


Figure 10. CMOS-Level Inputs

flash timings

timing requirements for program flash†

		MIN	TYP	MAX	UNIT
$t_{prog(16\text{-}bit)}$	Half word (16-bit) programming time	4	16	200	µs
$t_{prog(Total)}$	512K-byte programming time‡		4	15	s
$t_{erase(sector)}$	Sector erase time		2	15	s
t_{wec}	Write/erase cycles at T_A = 125°C			500	cycles
$t_{fp(\overline{RST})}$	Flash pump settling time from $\overline{RST}$ to SLEEP		$167t_{c(SYS)}$		ns
$t_{fp(SLEEP)}$	Initial flash pump settling time from SLEEP to STANDBY		$167t_{c(SYS)}$		ns
$t_{fp(STDBY)}$	Initial flash pump settling time from STANDBY to ACTIVE		$84t_{c(SYS)}$		ns

† For more detailed information on the flash core sectors, see the *flash program and erase* section of this data sheet.
‡ The 512K-byte programming times include overhead of state machine.

SPIn master mode timing parameters

SPIn master mode external timing parameters (CLOCK PHASE = 0, SPInCLK = output, SPInSIMO = output, and SPInSOMI = input)†‡§ (see Figure 11)

NO.			MIN	MAX	UNIT
1	$t_{c(SPC)M}$	Cycle time, SPInCLK ¶	100	$256t_{c(ICLK)}$	ns
2#	$t_{w(SPCH)M}$	Pulse duration, SPInCLK high (clock polarity = 0)	$0.5t_{c(SPC)M} - t_r$	$0.5t_{c(SPC)M} + 5$	
	$t_{w(SPCL)M}$	Pulse duration, SPInCLK low (clock polarity = 1)	$0.5t_{c(SPC)M} - t_f$	$0.5t_{c(SPC)M} + 5$	
3#	$t_{w(SPCL)M}$	Pulse duration, SPInCLK low (clock polarity = 0)	$0.5t_{c(SPC)M} - t_f$	$0.5t_{c(SPC)M} + 5$	
	$t_{w(SPCH)M}$	Pulse duration, SPInCLK high (clock polarity = 1)	$0.5t_{c(SPC)M} - t_r$	$0.5t_{c(SPC)M} + 5$	
4#	$t_{d(SPCH-SIMO)M}$	Delay time, SPInCLK high to SPInSIMO valid (clock polarity = 0)		10	
	$t_{d(SPCL-SIMO)M}$	Delay time, SPInCLK low to SPInSIMO valid (clock polarity = 1)		10	
5#	$t_{v(SPCL-SIMO)M}$	Valid time, SPInSIMO data valid after SPInCLK low (clock polarity = 0)	$t_{c(SPC)M} - 5 - t_f$		
	$t_{v(SPCH-SIMO)M}$	Valid time, SPInSIMO data valid after SPInCLK high (clock polarity = 1)	$t_{c(SPC)M} - 5 - t_r$		
6#	$t_{su(SOMI-SPCL)M}$	Setup time, SPInSOMI before SPInCLK low (clock polarity = 0)	12		
	$t_{su(SOMI-SPCH)M}$	Setup time, SPInSOMI before SPInCLK high (clock polarity = 1)	12		
7#	$t_{v(SPCL-SOMI)M}$	Valid time, SPInSOMI data valid after SPInCLK low (clock polarity = 0)	10		
	$t_{v(SPCH-SOMI)M}$	Valid time, SPInSOMI data valid after SPInCLK high (clock polarity = 1)	10		

† The MASTER bit (SPInCTRL2.3) is set and the CLOCK PHASE bit (SPInCTRL2.0) is cleared.

‡ $t_{c(ICLK)}$ = interface clock cycle time = $1/f_{(ICLK)}$

§ For rise and fall timings, see the "switching characteristics for output timings versus load capacitance" table.

¶ When the SPI is in Master mode, the following must be true:

For PS values from 1 to 255: $t_{c(SPC)M} \geq (PS + 1)t_{c(ICLK)} \geq 100$ ns, where PS is the prescale value set in the SPInCTL1.[12:5] register bits.

For PS values of 0: $t_{c(SPC)M} = 2t_{c(ICLK)} \geq 100$ ns.

The active edge of the SPInCLK signal referenced is controlled by the CLOCK POLARITY bit (SPInCTRL2.1).

SPIn master mode timing parameters (continued)

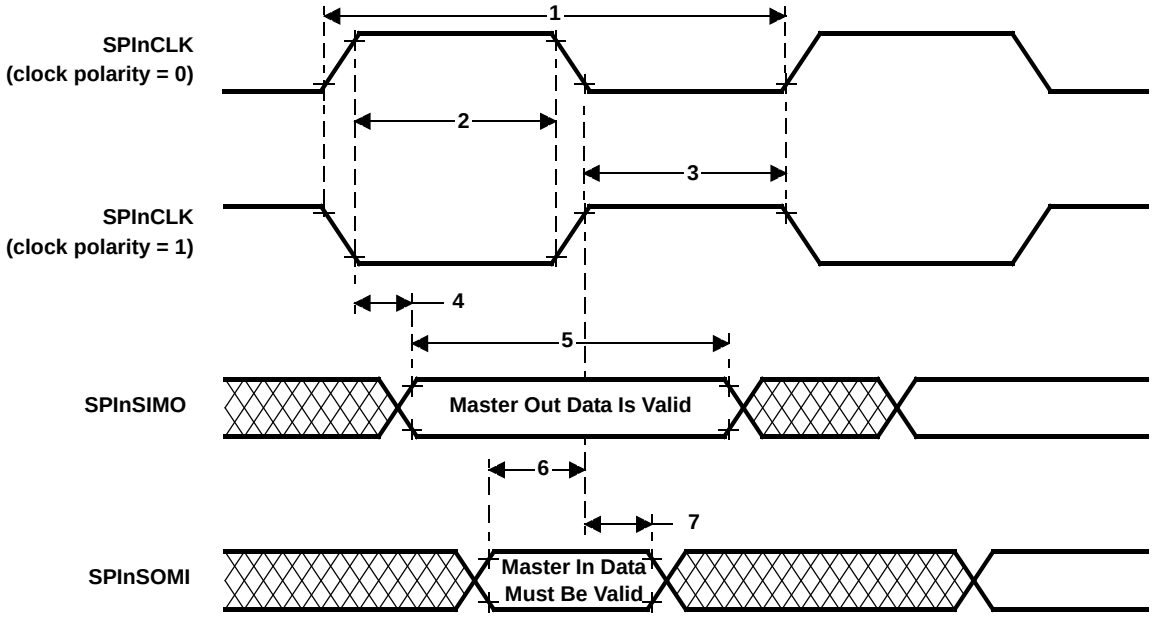


Figure 11. SPIn Master Mode External Timing (CLOCK PHASE = 0)

SPIn master mode timing parameters (continued)

SPIn master mode external timing parameters (CLOCK PHASE = 1, SPInCLK = output, SPInSIMO = output, and SPInSOMI = input)†‡§ (see Figure 12)

NO.			MIN	MAX	UNIT
1	$t_{c(SPC)M}$	Cycle time, SPInCLK ¶	100	$256t_{c(ICLK)}$	ns
2#	$t_{w(SPCH)M}$	Pulse duration, SPInCLK high (clock polarity = 0)	$0.5t_{c(SPC)M} - t_r$	$0.5t_{c(SPC)M} + 5$	
	$t_{w(SPCL)M}$	Pulse duration, SPInCLK low (clock polarity = 1)	$0.5t_{c(SPC)M} - t_f$	$0.5t_{c(SPC)M} + 5$	
3#	$t_{w(SPCL)M}$	Pulse duration, SPInCLK low (clock polarity = 0)	$0.5t_{c(SPC)M} - t_f$	$0.5t_{c(SPC)M} + 5$	
	$t_{w(SPCH)M}$	Pulse duration, SPInCLK high (clock polarity = 1)	$0.5t_{c(SPC)M} - t_r$	$0.5t_{c(SPC)M} + 5$	
4#	$t_{v(SIMO-SPCH)M}$	Valid time, SPInCLK high after SPInSIMO data valid (clock polarity = 0)	$0.5t_{c(SPC)M} - 10$		
	$t_{v(SIMO-SPCL)M}$	Valid time, SPInCLK low after SPInSIMO data valid (clock polarity = 1)	$0.5t_{c(SPC)M} - 10$		
5#	$t_{v(SPCH-SIMO)M}$	Valid time, SPInSIMO data valid after SPInCLK high (clock polarity = 0)	$0.5t_{c(SPC)M} - 5 - t_r$		
	$t_{v(SPCL-SIMO)M}$	Valid time, SPInSIMO data valid after SPInCLK low (clock polarity = 1)	$0.5t_{c(SPC)M} - 5 - t_f$		
6#	$t_{su(SOMI-SPCH)M}$	Setup time, SPInSOMI before SPInCLK high (clock polarity = 0)	12		
	$t_{su(SOMI-SPCL)M}$	Setup time, SPInSOMI before SPInCLK low (clock polarity = 1)	12		
7#	$t_{v(SPCH-SOMI)M}$	Valid time, SPInSOMI data valid after SPInCLK high (clock polarity = 0)	10		
	$t_{v(SPCL-SOMI)M}$	Valid time, SPInSOMI data valid after SPInCLK low (clock polarity = 1)	10		

† The MASTER bit (SPInCTRL2.3) is set and the CLOCK PHASE bit (SPInCTRL2.0) is set.

‡ $t_{c(ICLK)}$ = interface clock cycle time = $1/f_{(ICLK)}$

§ For rise and fall timings, see the "switching characteristics for output timings versus load capacitance" table.

¶ When the SPI is in Master mode, the following must be true:

For PS values from 1 to 255: $t_{c(SPC)M} \geq (PS + 1)t_{c(ICLK)} \geq 100$ ns, where PS is the prescale value set in the SPInCTL1.[12:5] register bits.

For PS values of 0: $t_{c(SPC)M} = 2t_{c(ICLK)} \geq 100$ ns.

The active edge of the SPInCLK signal referenced is controlled by the CLOCK POLARITY bit (SPInCTRL2.1).

SPIn master mode timing parameters (continued)

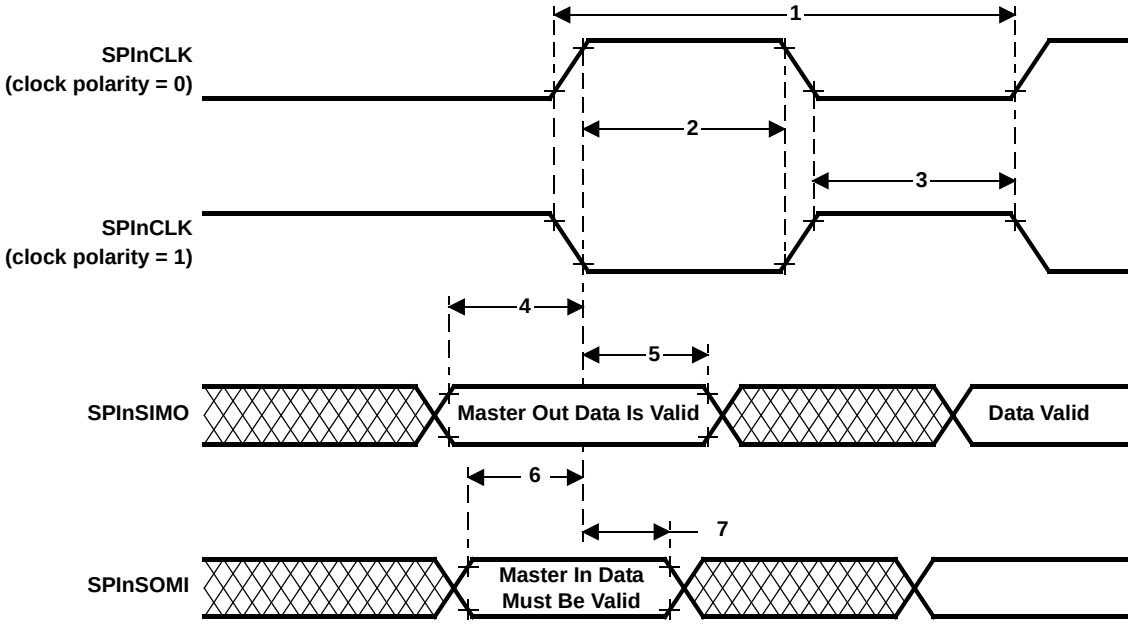


Figure 12. SPIn Master Mode External Timing (CLOCK PHASE = 1)

SPIn slave mode timing parameters

SPIn slave mode external timing parameters (CLOCK PHASE = 0, SPInCLK = input, SPInSIMO = input, and SPInSOMI = output)†‡§¶ (see Figure 13)

NO			MIN	MAX	UNIT
1	$t_{c(SPC)S}$	Cycle time, SPInCLK#	100	$256t_{c(ICLK)}$	ns
2‖	$t_{w(SPCH)S}$	Pulse duration, SPInCLK high (clock polarity = 0)	$0.5t_{c(SPC)S} - 0.25t_{c(ICLK)}$	$0.5t_{c(SPC)S} + 0.25t_{c(ICLK)}$	
	$t_{w(SPCL)S}$	Pulse duration, SPInCLK low (clock polarity = 1)	$0.5t_{c(SPC)S} - 0.25t_{c(ICLK)}$	$0.5t_{c(SPC)S} + 0.25t_{c(ICLK)}$	
3‖	$t_{w(SPCL)S}$	Pulse duration, SPInCLK low (clock polarity = 0)	$0.5t_{c(SPC)S} - 0.25t_{c(ICLK)}$	$0.5t_{c(SPC)S} + 0.25t_{c(ICLK)}$	
	$t_{w(SPCH)S}$	Pulse duration, SPInCLK high (clock polarity = 1)	$0.5t_{c(SPC)S} - 0.25t_{c(ICLK)}$	$0.5t_{c(SPC)S} + 0.25t_{c(ICLK)}$	
4‖	$t_{d(SPCH-SOMI)S}$	Delay time, SPInCLK high to SPInSOMI valid (clock polarity = 0)		$12 + t_r$	
	$t_{d(SPCL-SOMI)S}$	Delay time, SPInCLK low to SPInSOMI valid (clock polarity = 1)		$12 + t_f$	
5‖	$t_{v(SPCH-SOMI)S}$	Valid time, SPInSOMI data valid after SPInCLK high (clock polarity = 0)	$t_{c(SPC)S} - 12 - t_r$		
	$t_{v(SPCL-SOMI)S}$	Valid time, SPInSOMI data valid after SPInCLK low (clock polarity = 1)	$t_{c(SPC)S} - 12 - t_f$		
6‖	$t_{su(SIMO-SPCL)S}$	Setup time, SPInSIMO before SPInCLK low (clock polarity = 0)	10		
	$t_{su(SIMO-SPCH)S}$	Setup time, SPInSIMO before SPInCLK high (clock polarity = 1)	10		
7‖	$t_{v(SPCL-SIMO)S}$	Valid time, SPInSIMO data valid after SPInCLK low (clock polarity = 0)	10		
	$t_{v(SPCH-SIMO)S}$	Valid time, SPInSIMO data valid after SPInCLK high (clock polarity = 1)	10		

† The MASTER bit (SPInCTRL2.3) is cleared and the CLOCK PHASE bit (SPInCTRL2.0) is cleared.

‡ If the SPI is in slave mode, the following must be true: $t_{c(SPC)S} \geq (PS + 1)\ t_{c(ICLK)}$, where PS = prescale value set in SPInCTL1.[12:5].

§ For rise and fall timings, see the "switching characteristics for output timings versus load capacitance" table.

¶ $t_{c(ICLK)}$ = interface clock cycle time = $1/f_{(ICLK)}$

When the SPIn is in Slave mode, the following must be true:

For PS values from 1 to 255: $t_{c(SPC)S} \geq (PS + 1)t_{c(ICLK)} \geq 100$ ns, where PS is the prescale value set in the SPInCTL1.[12:5] register bits.

For PS values of 0: $t_{c(SPC)S} = 2t_{c(ICLK)} \geq 100$ ns.

‖ The active edge of the SPInCLK signal referenced is controlled by the CLOCK POLARITY bit (SPInCTRL2.1).

SPIn slave mode timing parameters (continued)

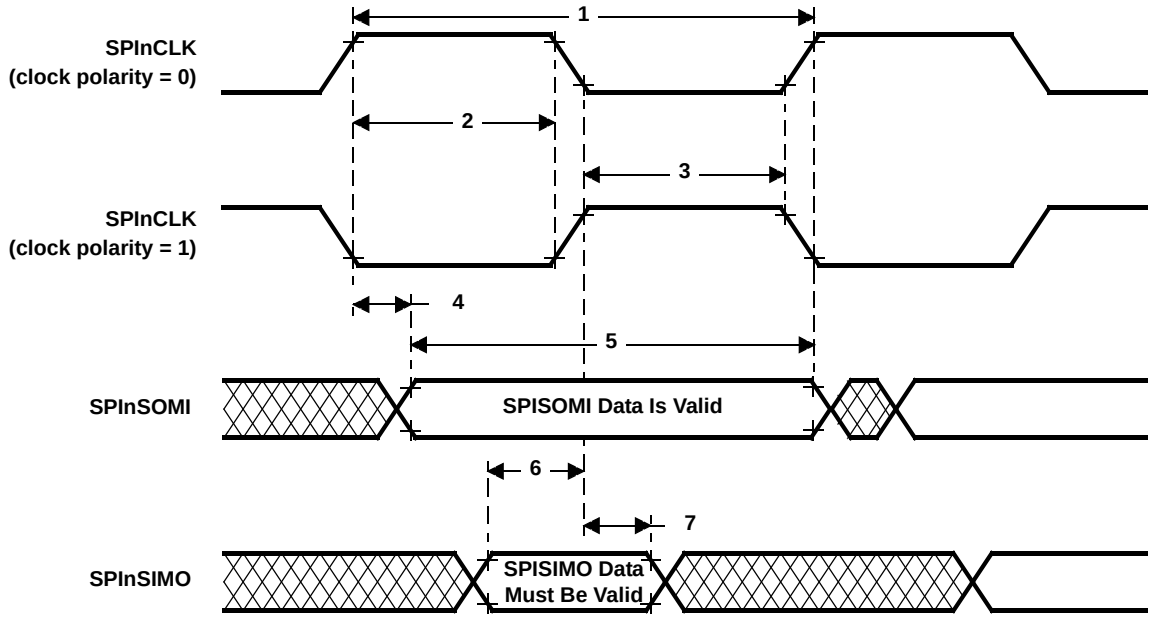


Figure 13. SPIn Slave Mode External Timing (CLOCK PHASE = 0)

SPIn slave mode timing parameters (continued)

SPIn slave mode external timing parameters (CLOCK PHASE = 1, SPInCLK = input, SPInSIMO = input, and SPInSOMI = output)†‡§¶ (see Figure 14)

NO			MIN	MAX	UNIT
1	$t_{c(SPC)S}$	Cycle time, SPInCLK#	100	$256t_{c(ICLK)}$	ns
2‖	$t_{w(SPCH)S}$	Pulse duration, SPInCLK high (clock polarity = 0)	$0.5t_{c(SPC)S}-0.25t_{c(ICLK)}$	$0.5t_{c(SPC)S}+0.25t_{c(ICLK)}$	
	$t_{w(SPCL)S}$	Pulse duration, SPInCLK low (clock polarity = 1)	$0.5t_{c(SPC)S}-0.25t_{c(ICLK)}$	$0.5t_{c(SPC)S}+0.25t_{c(ICLK)}$	
3‖	$t_{w(SPCL)S}$	Pulse duration, SPInCLK low (clock polarity = 0)	$0.5t_{c(SPC)S}-0.25t_{c(ICLK)}$	$0.5t_{c(SPC)S}+0.25t_{c(ICLK)}$	
	$t_{w(SPCH)S}$	Pulse duration, SPInCLK high (clock polarity = 1)	$0.5t_{c(SPC)S}-0.25t_{c(ICLK)}$	$0.5t_{c(SPC)S}+0.25t_{c(ICLK)}$	
4‖	$t_{v(SOMI-SPCH)S}$	Valid time, SPInCLK high after SPInSOMI data valid (clock polarity = 0)	$0.5t_{c(SPC)S}-12-t_r$		
	$t_{v(SOMI-SPCL)S}$	Valid time, SPInCLK low after SPInSOMI data valid (clock polarity = 1)	$0.5t_{c(SPC)S}-12-t_f$		
5‖	$t_{v(SPCH-SOMI)S}$	Valid time, SPInSOMI data valid after SPInCLK high (clock polarity = 0)	$0.5t_{c(SPC)S}-12-t_r$		
	$t_{v(SPCL-SOMI)S}$	Valid time, SPInSOMI data valid after SPInCLK low (clock polarity = 1)	$0.5t_{c(SPC)S}-12-t_f$		
6‖	$t_{su(SIMO-SPCH)S}$	Setup time, SPInSIMO before SPInCLK high (clock polarity = 0)	10		
	$t_{su(SIMO-SPCL)S}$	Setup time, SPInSIMO before SPInCLK low (clock polarity = 1)	10		
7‖	$t_{v(SPCH-SIMO)S}$	Valid time, SPInSIMO data valid after SPInCLK high (clock polarity = 0)	10		
	$t_{v(SPCL-SIMO)S}$	Valid time, SPInSIMO data valid after SPInCLK low (clock polarity = 1)	10		

† The MASTER bit (SPInCTRL2.3) is cleared and the CLOCK PHASE bit (SPInCTRL2.0) is set.

‡ If the SPI is in slave mode, the following must be true: $t_{c(SPC)S} \geq (PS + 1)\ t_{c(ICLK)}$, where PS = prescale value set in SPInCTL1.[12:5].

§ For rise and fall timings, see the "switching characteristics for output timings versus load capacitance" table.

¶ $t_{c(ICLK)}$ = interface clock cycle time = $1/f_{(ICLK)}$

When the SPIn is in Slave mode, the following must be true:

For PS values from 1 to 255: $t_{c(SPC)S} \geq (PS + 1)t_{c(ICLK)} \geq 100$ ns, where PS is the prescale value set in the SPInCTL1.[12:5] register bits.

For PS values of 0: $t_{c(SPC)S} = 2t_{c(ICLK)} \geq 100$ ns.

‖ The active edge of the SPInCLK signal referenced is controlled by the CLOCK POLARITY bit (SPInCTRL2.1).

SPIn slave mode timing parameters (continued)

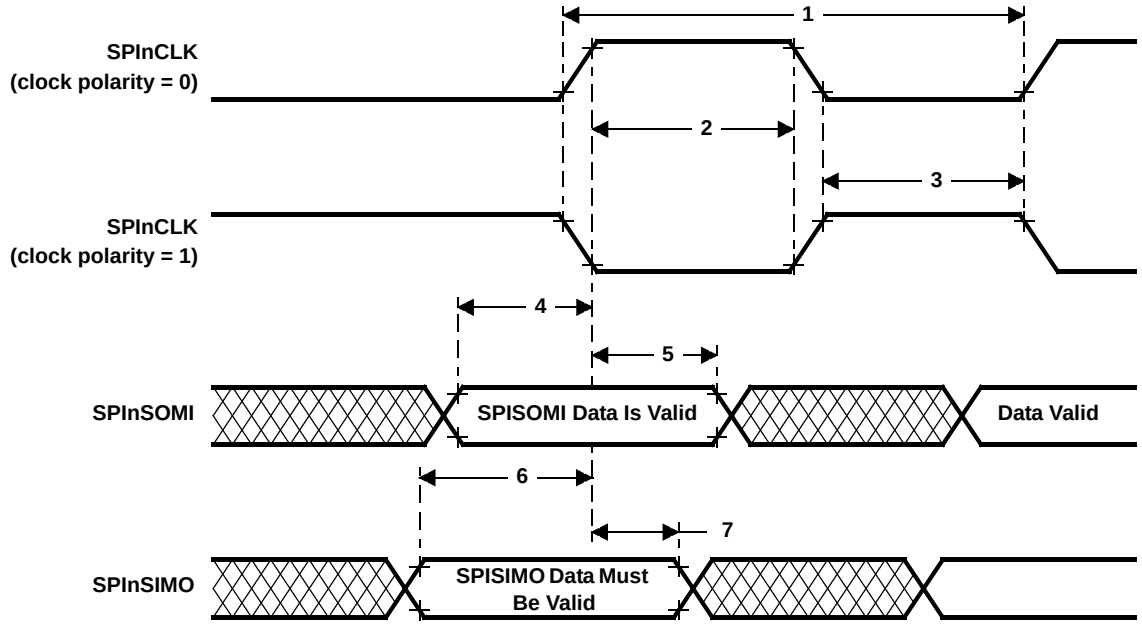


Figure 14. SPIn Slave Mode External Timing (CLOCK PHASE = 1)

MibSPI master mode timing parameters

MibSPI master mode external timing parameters (CLOCK PHASE = 0, SPICLK = output, SPISIMO = output, and SPISOMI = input)†‡§ (see Figure 15)

NO.			MIN	MAX	UNIT
1	$t_{c(SPC)M}$	Cycle time, SPICLK ¶	90	$256t_{c(ICLK)}$	ns
2¶	$t_{w(SPCH)M}$	Pulse duration, SPICLK high (clock polarity = 0)	$0.5t_{c(SPC)M} - t_r$	$0.5t_{c(SPC)M} + 5$	ns
	$t_{w(SPCL)M}$	Pulse duration, SPICLK low (clock polarity = 1)	$0.5t_{c(SPC)M} - t_f$	$0.5t_{c(SPC)M} + 5$	
3¶	$t_{w(SPCL)M}$	Pulse duration, SPICLK low (clock polarity = 0)	$0.5t_{c(SPC)M} - t_f$	$0.5t_{c(SPC)M} + 5$	ns
	$t_{w(SPCH)M}$	Pulse duration, SPICLK high (clock polarity = 1)	$0.5t_{c(SPC)M} - t_r$	$0.5t_{c(SPC)M} + 5$	
4¶	$t_{d(SPCH-SIMO)M}$	Delay time, SPICLK high to SPISIMO valid (clock polarity = 0)		6	ns
	$t_{d(SPCL-SIMO)M}$	Delay time, SPICLK low to SPISIMO valid (clock polarity = 1)		6	
5¶	$t_{v(SPCL-SIMO)M}$	Valid time, SPISIMO data valid after SPICLK low (clock polarity = 0)	$0.5t_{c(SPC)M} - 5$		ns
	$t_{v(SPCH-SIMO)M}$	Valid time, SPISIMO data valid after SPICLK high (clock polarity = 1)	$0.5t_{c(SPC)M} - 5$		
6¶	$t_{su(SOMI-SPCL)M}$	Setup time, SPISOMI before SPICLK low (clock polarity = 0)	$t_{f(SPC)} - 0.5t_{c(ICLK)} + 5$	$t_{f(SPC)} + 5$	ns
	$t_{su(SOMI-SPCH)M}$	Setup time, SPISOMI before SPICLK high (clock polarity = 1)	$t_{r(SPC)} - 0.5t_{c(ICLK)} + 5$	$t_{r(SPC)} + 5$	
7¶	$t_{v(SPCL-SOMI)M}$	Valid time, SPISOMI data valid after SPICLK low (clock polarity = 0)	$0.5t_{c(ICLK)} - t_{f(SPC)} + 5$	$- t_{f(SPC)} + 5$	ns
	$t_{v(SPCH-SOMI)M}$	Valid time, SPISOMI data valid after SPICLK high (clock polarity = 1)	$0.5t_{c(ICLK)} - t_{r(SPC)} + 5$	$- t_{r(SPC)} + 5$	

† The MASTER bit (SPICTRL2.3) is set and the CLOCK PHASE bit (SPICTRL2.0) is cleared.
‡ $t_{c(ICLK)}$ = interface clock cycle time = $1/f_{(ICLK)}$
§ For rise and fall timings, see the "switching characteristics for output timings versus load capacitance" table.
¶ The active edge of the SPICLK signal referenced is controlled by the CLOCK POLARITY bit (SPICTRK2.1).

MibSPI master mode timing parameters (continued)

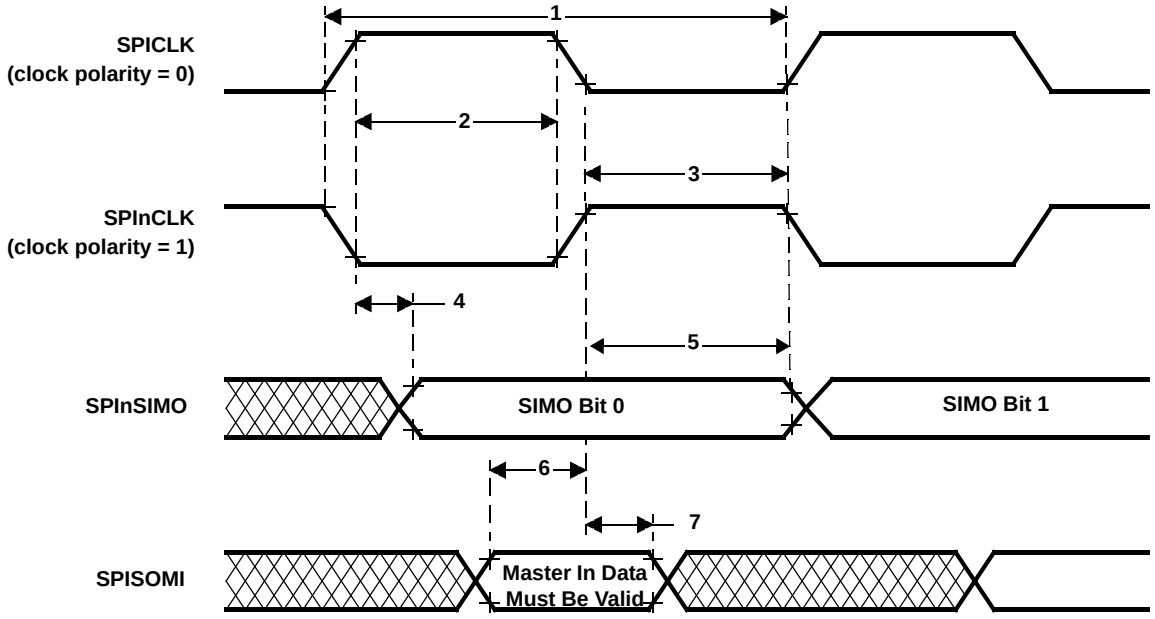


Figure 15. MibSPI Master Mode External Timing (CLOCK PHASE = 0)

MibSPI master mode timing parameters (continued)

MibSPI master mode external timing parameters (CLOCK PHASE = 1, SPICLK = output, SPISIMO = output, and SPISOMI = input)†‡§ (see Figure 16)

NO.			MIN	MAX	UNIT
1	$t_{c(SPC)M}$	Cycle time, SPICLK ¶	90	$256t_{c(ICLK)}$	ns
2¶	$t_{w(SPCH)M}$	Pulse duration, SPICLK high (clock polarity = 0)	$0.5t_{c(SPC)M} - t_r$	$0.5t_{c(SPC)M} + 5$	ns
	$t_{w(SPCL)M}$	Pulse duration, SPICLK low (clock polarity = 1)	$0.5t_{c(SPC)M} - t_f$	$0.5t_{c(SPC)M} + 5$	
3¶	$t_{w(SPCL)M}$	Pulse duration, SPICLK low (clock polarity = 0)	$0.5t_{c(SPC)M} - t_f$	$0.5t_{c(SPC)M} + 5$	ns
	$t_{w(SPCH)M}$	Pulse duration, SPICLK high (clock polarity = 1)	$0.5t_{c(SPC)M} - t_r$	$0.5t_{c(SPC)M} + 5$	
4¶	$t_{v(SIMO-SPCH)M}$	Valid time, SPICLK high after SPISIMO data valid (clock polarity = 0)	$0.5t_{c(SPC)M} - 6$		ns
	$t_{v(SIMO-SPCL)M}$	Valid time, SPICLK low after SPISIMO data valid (clock polarity = 1)	$0.5t_{c(SPC)M} - 6$		
5¶	$t_{v(SPCH-SIMO)M}$	Valid time, SPISIMO data valid after SPICLK high (clock polarity = 0)	$0.5t_{c(SPC)M} - 5$		ns
	$t_{v(SPCL-SIMO)M}$	Valid time, SPISIMO data valid after SPICLK low (clock polarity = 1)	$0.5t_{c(SPC)M} - 5$		
6¶	$t_{su(SOMI-SPCH)M}$	Setup time, SPISOMI before SPICLK high (clock polarity = 0)	$t_{r(SPC)} - 0.5t_{c(ICLK)} + 5$	$t_{r(SPC)} + 5$	ns
	$t_{su(SOMI-SPCL)M}$	Setup time, SPISOMI before SPICLK low (clock polarity = 1)	$t_{f(SPC)} - 0.5t_{c(ICLK)} + 5$	$t_{f(SPC)} + 5$	
7¶	$t_{v(SPCH-SOMI)M}$	Valid time, SPISOMI data valid after SPICLK high (clock polarity = 0)	$0.5t_{c(ICLK)} - t_{r(SPC)} + 5$	$- t_{r(SPC)} + 5$	ns
	$t_{v(SPCL-SOMI)M}$	Valid time, SPISOMI data valid after SPICLK low (clock polarity = 1)	$0.5t_{c(ICLK)} - t_{f(SPC)} + 5$	$- t_{f(SPC)} + 5$	

† The MASTER bit (SPICTRL2.3) is set and the CLOCK PHASE bit (SPICTRL2.0) is set.
‡ $t_{c(ICLK)}$ = interface clock cycle time = $1/f_{(ICLK)}$
§ For rise and fall timings, see the "switching characteristics for output timings versus load capacitance" table.
¶ The active edge of the SPICLK signal referenced is controlled by the CLOCK POLARITY bit (SPICTRL2.1).

MibSPI master mode timing parameters (continued)

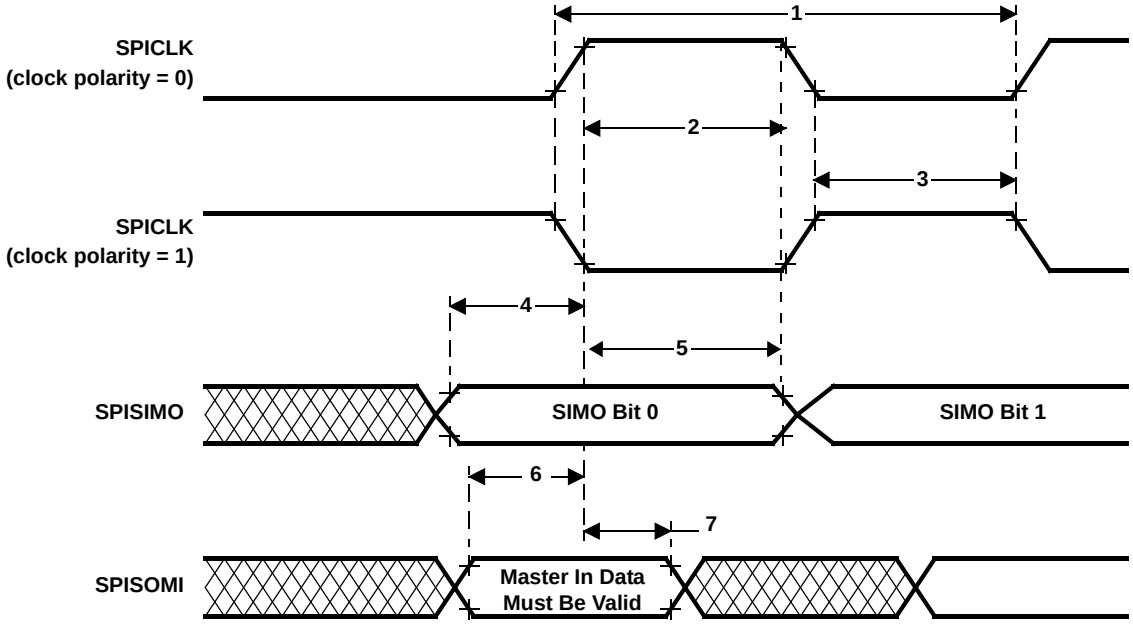


Figure 16. MibSPI Master Mode External Timing (CLOCK PHASE = 1)

MibSPI slave mode timing parameters

MibSPI slave mode external timing parameters (CLOCK PHASE = 0, SPICLK = input, SPISIMO = input, and SPISOMI = output)†‡§¶ (see Figure 17)

NO.			MIN	MAX	UNIT
1	$t_{c(SPC)S}$	Cycle time, SPICLK#	90	$256t_{c(ICLK)}$	ns
2‖	$t_{w(SPCH)S}$	Pulse duration, SPICLK high (clock polarity = 0)	$0.5t_{c(SPC)S} - 0.25t_{c(ICLK)}$	$0.5t_{c(SPC)S} + 0.25t_{c(ICLK)}$	ns
	$t_{w(SPCL)S}$	Pulse duration, SPICLK low (clock polarity = 1)	$0.5t_{c(SPC)S} - 0.25t_{c(ICLK)}$	$0.5t_{c(SPC)S} + 0.25t_{c(ICLK)}$	
3‖	$t_{w(SPCL)S}$	Pulse duration, SPICLK low (clock polarity = 0)	$0.5t_{c(SPC)S} - 0.25t_{c(ICLK)}$	$0.5t_{c(SPC)S} + 0.25t_{c(ICLK)}$	ns
	$t_{w(SPCH)S}$	Pulse duration, SPICLK high (clock polarity = 1)	$0.5t_{c(SPC)S} - 0.25t_{c(ICLK)}$	$0.5t_{c(SPC)S} + 0.25t_{c(ICLK)}$	
4‖	$t_{d(SPCH-SOMI)S}$	Delay time, SPICLK high to SPISOMI valid (clock polarity = 0)☆	$0.5\ t_{c(ICLK)} + t_{rf(SOMI)}$	$1.5\ t_{c(ICLK)} + t_{rf(SOMI)}$	ns
	$t_{d(SPCL-SOMI)S}$	Delay time, SPICLK low to SPISPISOMI valid (clock polarity = 1)☆	$0.5\ t_{c(ICLK)} + t_{rf(SOMI)}$	$1.5\ t_{c(ICLK)} + t_{rf(SOMI)}$	
5‖	$t_{v(SPCH-SOMI)S}$	Valid time, SPISOMI data valid after SPICLK high (clock polarity =0)	$t_{c(SPC)S} - t_{c(ICLK)}$	$t_{c(SPC)S} + t_{c(ICLK)}$	ns
	$t_{v(SPCL-SOMI)S}$	Valid time, SPISOMI data valid after SPICLK low (clock polarity =1)	$t_{c(SPC)S} - t_{c(ICLK)}$	$t_{c(SPC)S} + t_{c(ICLK)}$	
6‖	$t_{su(SIMO-SPCL)S}$	Setup time, SPISIMO before SPICLK low (clock polarity = 0)	$0.5\ t_{c(ICLK)} + 4$		ns
	$t_{su(SIMO-SPCH)S}$	Setup time, SPISIMO before SPICLK high (clock polarity = 1)	$0.5\ t_{c(ICLK)} + 4$		
7‖	$t_{v(SPCL-SIMO)S}$	Valid time, SPISIMO data valid after SPICLK low (clock polarity = 0)	$0.5\ t_{c(ICLK)} + 6$		ns
	$t_{v(SPCH-SIMO)S}$	Valid time, SPISIMO data valid after SPICLK high (clock polarity = 1)	$0.5\ t_{c(ICLK)} + 6$		

† The MASTER bit (SPICTRL2.3) is cleared and the CLOCK PHASE bit (SPICTRL2.0) is cleared.
‡ If the MibSPI is in slave mode, the following must be true: $t_{c(SPC)S} \geq (PS + 1)\ t_{c(ICLK)}$, where PS = prescale value set in SPICTL1.[12:5].
§ For rise and fall timings, see the "switching characteristics for output timings versus load capacitance" table.
¶ $t_{c(ICLK)}$ = interface clock cycle time = $1/f_{(ICLK)}$, $t_{rf(SOMI)}$ = Rise/Fall time of the SOMI pin.
# When the SPI is in Slave mode, the following must be true:
For PS values from 1 to 255: $t_{c(SPC)S} \geq (PS + 1)t_{c(ICLK)} \geq$ Master Clock Period, where PS is the prescale value set in the SPICTL1.[12:5] register bits.
For PS values of 0: $t_{c(SPC)S} = 2t_{c(ICLK)} \geq$ Master Clock Period.
‖ The active edge of the SPICLK signal referenced is controlled by the CLOCK POLARITY bit (SPICTRL2.1).
☆MibSPI in Slave mode transmits data on the SPISOMI pin with respect to the receive edge of SPICLK.

MibSPI slave mode timing parameters (continued)

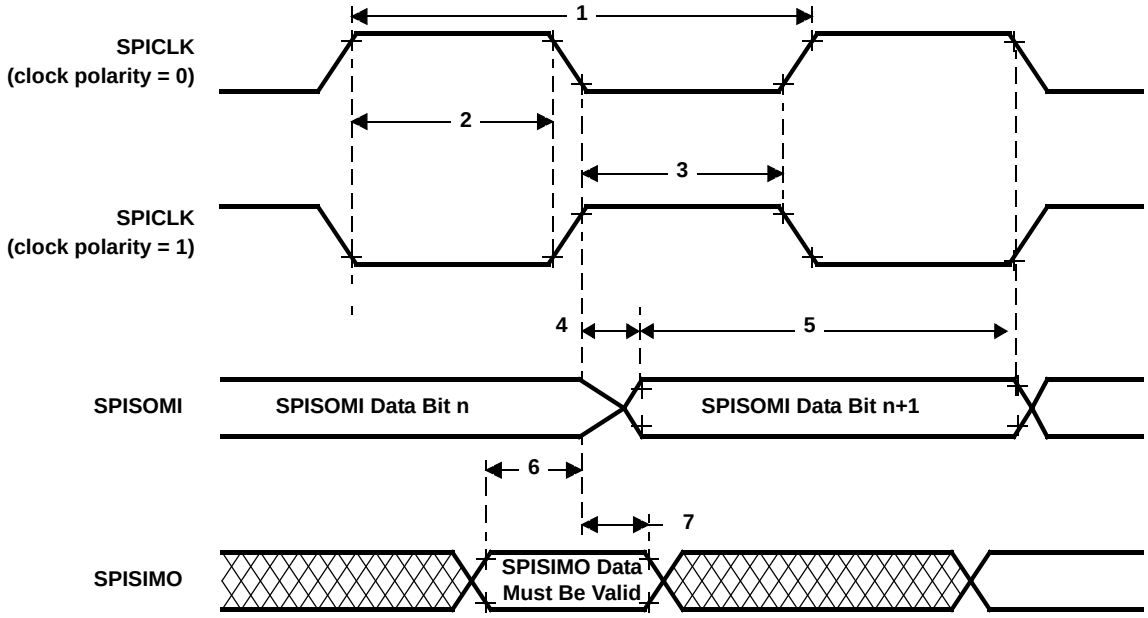


Figure 17. MibSPI Slave Mode External Timing (CLOCK PHASE = 0)

MibSPI slave mode timing parameters (continued)

MibSPI slave mode external timing parameters (CLOCK PHASE = 1, SPICLK = input, SPISIMO = input, and SPISOMI = output)†‡§¶ (see Figure 18)

NO.			MIN	MAX	UNIT
1	$t_{c(SPC)S}$	Cycle time, SPICLK#	$2t_{c(ICLK)}$	$256t_{c(ICLK)}$	ns
2‖	$t_{w(SPCH)S}$	Pulse duration, SPICLK high (clock polarity = 0)	$0.5t_{c(SPC)S}-0.25t_{c(ICLK)}$	$0.5t_{c(SPC)S}+0.25t_{c(ICLK)}$	ns
	$t_{w(SPCL)S}$	Pulse duration, SPICLK low (clock polarity = 1)	$0.5t_{c(SPC)S}-0.25t_{c(ICLK)}$	$0.5t_{c(SPC)S}+0.25t_{c(ICLK)}$	
3‖	$t_{w(SPCL)S}$	Pulse duration, SPICLK low (clock polarity = 0)	$0.5t_{c(SPC)S}-0.25t_{c(ICLK)}$	$0.5t_{c(SPC)S}+0.25t_{c(ICLK)}$	ns
	$t_{w(SPCH)S}$	Pulse duration, SPICLK high (clock polarity = 1)	$0.5t_{c(SPC)S}-0.25t_{c(ICLK)}$	$0.5t_{c(SPC)S}+0.25t_{c(ICLK)}$	
4‖	$t_{v(SOMI-SPCH)S}$	Valid time, SPICLK high after SPISOMI data valid (clock polarity = 0)☆	$0.5\ t_{c(ICLK)}+t_{rf(SOMI)}$	$1.5\ t_{c(ICLK)}+t_{rf(SOMI)}$	ns
	$t_{v(SOMI-SPCL)S}$	Valid time, SPICLK low after SPISOMI data valid (clock polarity = 1)☆	$0.5\ t_{c(ICLK)}+t_{rf(SOMI)}$	$1.5\ t_{c(ICLK)}+t_{rf(SOMI)}$	
5‖	$t_{v(SPCH-SOMI)S}$	Valid time, SPISOMI data valid after SPICLK high (clock polarity = 0)	$t_{c(SPC)S}-t_{c(ICLK)}$	$t_{c(SPC)S}+t_{c(ICLK)}$	ns
	$t_{v(SPCL-SOMI)S}$	Valid time, SPISOMI data valid after SPICLK low (clock polarity = 1)	$t_{c(SPC)S}-t_{c(ICLK)}$	$t_{c(SPC)S}+t_{c(ICLK)}$	
6‖	$t_{su(SIMO-SPCH)S}$	Setup time, SPISIMO before SPICLK high (clock polarity = 0)	$0.5\ t_{c(ICLK)}+4$		ns
	$t_{su(SIMO-SPCL)S}$	Setup time, SPISIMO before SPICLK low (clock polarity = 1)	$0.5\ t_{c(ICLK)}+4$		
7‖	$t_{v(SPCH-SIMO)S}$	Valid time, SPISIMO data valid after SPICLK high (clock polarity = 0)	$0.5\ t_{c(ICLK)}+6$		ns
	$t_{v(SPCL-SIMO)S}$	Valid time, SPISIMO data valid after SPICLK low (clock polarity = 1)	$0.5\ t_{c(ICLK)}+6$		

† The MASTER bit (SPICTRL2.3) is cleared and the CLOCK PHASE bit (SPICTRL2.0) is set.

‡ If the MibSPI is in slave mode, the following must be true: $t_{c(SPC)S} \geq (PS + 1)\ t_{c(ICLK)}$, where PS = prescale value set in SPICTL1.[12:5].

§ For rise and fall timings, see the "switching characteristics for output timings versus load capacitance" table.

¶ $t_{c(ICLK)}$ = interface clock cycle time = $1/f_{(ICLK)}$, $t_{rf(SOMI)}$ = Rise/Fall time of the SOMI pin.

When the MibSPI is in Slave mode, the following must be true:

For PS values from 1 to 255: $t_{c(SPC)S} \geq (PS + 1)t_{c(ICLK)} \geq$ Master Clock Period, where PS is the prescale value set in the SPICTL1.[12:5] register bits.

For PS values of 0: $t_{c(SPC)S} = 2t_{c(ICLK)} \geq$ Master Clock Period.

‖ The active edge of the SPICLK signal referenced is controlled by the CLOCK POLARITY bit (SPICTRL2.1).

☆MibSPI in Slave mode transmits data on the SPISOMI pin with respect to the receive edge of SPICLK.

MibSPI slave mode timing parameters (continued)

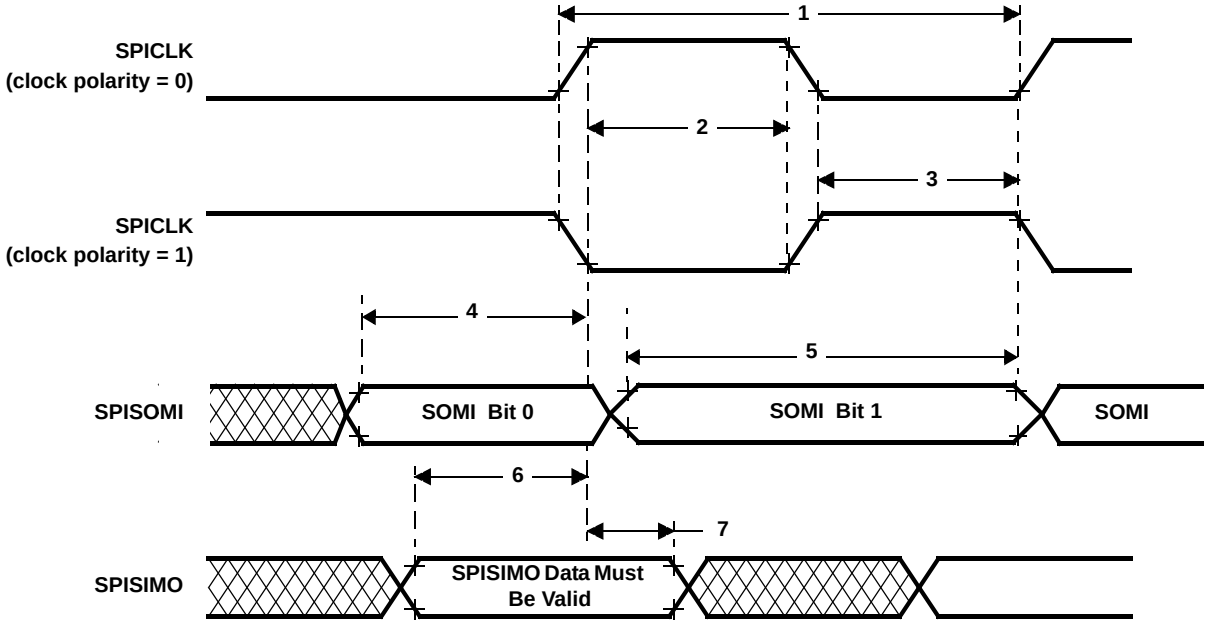


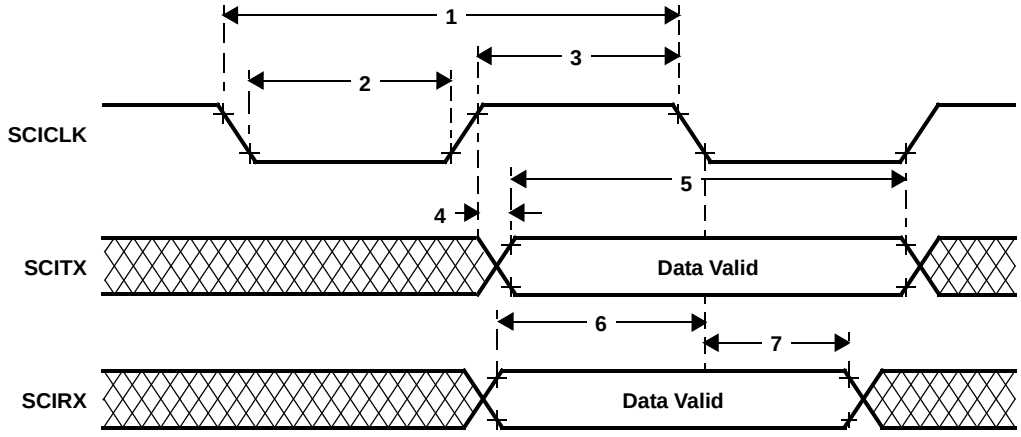
Figure 18. MibSPI Slave Mode External Timing (CLOCK PHASE = 1)

SCIn isosynchronous mode timings — internal clock

timing requirements for internal clock SCIn isosynchronous mode†‡§ (see Figure 19)

NO.			(BAUD + 1) IS EVEN OR BAUD = 0		(BAUD + 1) IS ODD AND BAUD ≠ 0		UNIT
			MIN	MAX	MIN	MAX	
1	$t_{c(SCC)}$	Cycle time, SCInCLK	$2t_{c(ICLK)}$	$2^{24}t_{c(ICLK)}$	$3t_{c(ICLK)}$	$(2^{24}-1)\ t_{c(ICLK)}$	ns
2	$t_{w(SCCL)}$	Pulse duration, SCInCLK low	$0.5t_{c(SCC)} - t_f$	$0.5t_{c(SCC)} + 5$	$0.5t_{c(SCC)} + 0.5t_{c(ICLK)} - t_f$	$0.5t_{c(SCC)} + 0.5t_{c(ICLK)}$	ns
3	$t_{w(SCCH)}$	Pulse duration, SCInCLK high	$0.5t_{c(SCC)} - t_r$	$0.5t_{c(SCC)} + 5$	$0.5t_{c(SCC)} - 0.5t_{c(ICLK)} - t_r$	$0.5t_{c(SCC)} - 0.5t_{c(ICLK)}$	ns
4	$t_{d(SCCH-TXV)}$	Delay time, SCInCLK high to SCInTX valid		10		10	ns
5	$t_{v(TX)}$	Valid time, SCInTX data after SCInCLK low	$t_{c(SCC)} - 10$		$t_{c(SCC)} - 10$		ns
6	$t_{su(RX-SCCL)}$	Setup time, SCInRX before SCInCLK low	$t_{c(ICLK)} + t_f + 20$		$t_{c(ICLK)} + t_f + 20$		ns
7	$t_{v(SCCL-RX)}$	Valid time, SCInRX data after SCInCLK low	$-t_{c(ICLK)} + t_f + 20$		$-t_{c(ICLK)} + t_f + 20$		ns

† BAUD = 24-bit concatenated value formed by the SCI[H,M,L]BAUD registers.
‡ $t_{c(ICLK)}$ = interface clock cycle time = $1/f_{(ICLK)}$
§ For rise and fall timings, see the "switching characteristics for output timings versus load capacitance" table.



NOTE A: Data transmission/reception characteristics for isosynchronous mode with internal clocking are similar to the asynchronous mode. Data transmission occurs on the SCICLK rising edge, and data reception on the SCICLK falling edge.

Figure 19. SCIn Isosynchronous Mode Timing Diagram for Internal Clock

SCIn isosynchronous mode timings — external clock

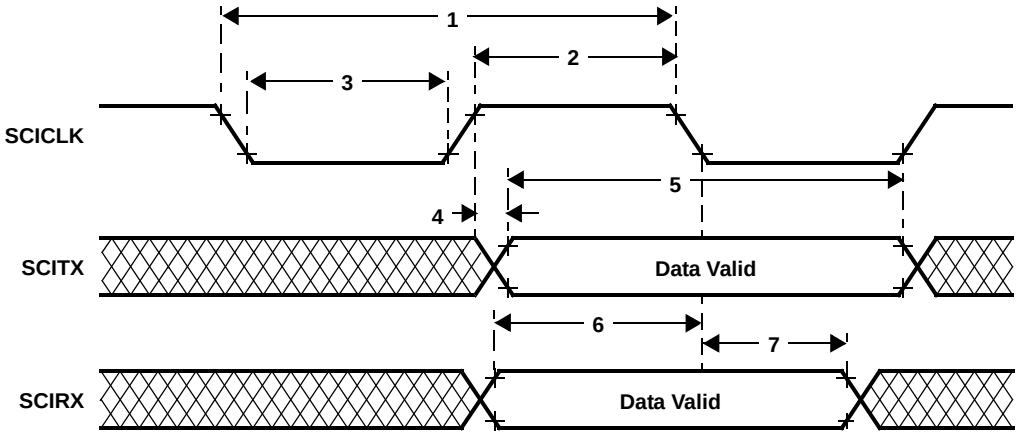
timing requirements for external clock SCIn isosynchronous mode†‡ (see Figure 20)

NO.			MIN	MAX	UNIT
1	$t_{c(SCC)}$	Cycle time, SCInCLK§	$8t_{c(ICLK)}$		ns
2	$t_{w(SCCH)}$	Pulse duration, SCInCLK high	$0.5t_{c(SCC)} - 0.25t_{c(ICLK)}$	$0.5t_{c(SCC)} + 0.25t_{c(ICLK)}$	ns
3	$t_{w(SCCL)}$	Pulse duration, SCInCLK low	$0.5t_{c(SCC)} - 0.25t_{c(ICLK)}$	$0.5t_{c(SCC)} + 0.25t_{c(ICLK)}$	ns
4	$t_{d(SCCH-TXV)}$	Delay time, SCInCLK high to SCInTX valid		$2t_{c(ICLK)} + 12 + t_r$	ns
5	$t_{v(TX)}$	Valid time, SCInTX data after SCInCLK low	$2t_{c(SCC)}-10$		ns
6	$t_{su(RX-SCCL)}$	Setup time, SCInRX before SCInCLK low	0		ns
7	$t_{v(SCCL-RX)}$	Valid time, SCInRX data after SCInCLK low	$2t_{c(ICLK)} + 10$		ns

† $t_{c(ICLK)}$ = interface clock cycle time = $1/f_{(ICLK)}$

‡ For rise and fall timings, see the "switching characteristics for output timings versus load capacitance" table.

§ When driving an external SCInCLK, the following must be true: $t_{c(SCC)} \geq 8t_{c(ICLK)}$



NOTE A: Data transmission/reception characteristics for isosynchronous mode with external clocking are similar to the asynchronous mode. Data transmission occurs on the SCICLK rising edge, and data reception on the SCICLK falling edge.

Figure 20. SCIn Isosynchronous Mode Timing Diagram for External Clock

high-end timer (HET) timings

minimum PWM output pulse width:

This is equal to one High Resolution Clock Period (HRP). The HRP is defined by the 6-bit High Resolution Prescale Factor (hr) which is user defined, giving prescale factors of 1 to 64, with a linear increment of codes.

Therefore, the minimum PWM output pulse width = HRP(min) = hr(min)/SYSCLK = 1/SYSCLK

For example, for a SYSCLK of 30 MHz, the minimum PWM output pulse width = 1/30 = 33.33ns

minimum input pulses we can capture:

The input pulse width must be greater or equal to the Low Resolution Clock Period (LRP), i.e., the HET loop (the HET program must fit within the LRP). The LRP is defined by the 3-bit Loop-Resolution Prescale Factor (lr), which is user defined, with a power of 2 increment of codes. That is, the value of lr can be 1, 2, 4, 8, 16, or 32.

Therefore, the minimum input pulse width = LRP(min) = hr(min) * lr(min)/SYSCLK = 1 * 1/SYSCLK

For example, with a SYSCLK of 30 MHz, the minimum input pulse width = 1 * 1/30 = 33.33 ns

Note: Once the input pulse width is greater than LRP, the resolution of the measurement is still HRP. (That is, the captured value gives the number of HRP clocks inside the pulse.)

Abbreviations:

High resolution clock period = HRP = hr/SYSCLK

Loop resolution clock period = LRP = hr*lr/SYSCLK

hr = HET high resolution divide rate = 1, 2, 3,...63, 64

lr = HET low resolution divide rate = 1, 2, 4, 8, 16, 32

high-end CAN controller (HECCn) mode timings

dynamic characteristics for the CANnHTX and CANnHRX pins

		MIN	MAX	UNIT
t_d(CANnHTX)	Delay time, transmit shift register to CANnHTX pin†		15	ns
t_d(CANnHRX)	Delay time, CANnHRX pin to receive shift register		5	ns

† These values do not include rise/fall times of the output buffer.

class 2 serial interface B (C2SIb) variable pulse width (VPW) modulation

VPW timing requirements

		NORMAL MODE (10.4 KBPS)				4X MODE (41.6 KBPS)				UNIT
		TX		RX		TX		RX		
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
SOF	Start of frame	192	208	163	239	48	52	41	60	µs
Short Pulse	Low = 0	60	68	34	96	14	18	9	24	µs
	High = 1									µs
Long Pulse	Low = 1	122	134	97	163	30	34	24	41	µs
	High = 0									µs
EOD	End of data	193	207	164	239	48	52	41	60	µs
NB	Normalization bit (long)	122	134	97	163	30	34	24	41	µs
	Normalization bit (short)	60	68	34	96	14	18	9	24	µs
EOF	End of frame	271	289	240	320	67	73	60	80	µs
Break	Short	290	-	239	-	290	-	60	-	µs
	Long	758	-	239	-	758	-	60	-	µs

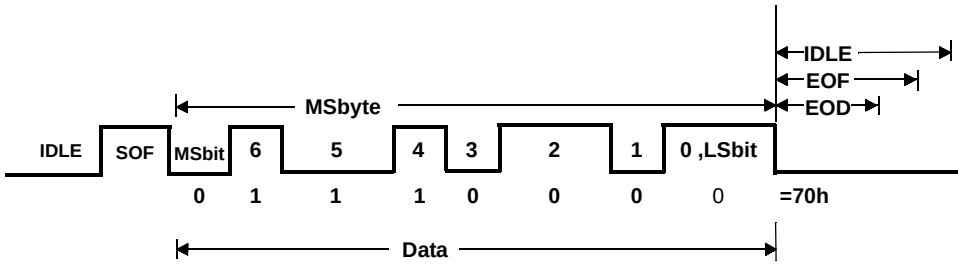


Figure 21. C2SIb Timing Diagram

multi-buffered A-to-D converter (MibADC)

The multi-buffered A-to-D converter (MibADC) has a separate power bus for its analog circuitry that enhances the A-to-D performance by preventing digital switching noise on the logic circuitry which could be present on V_{SS} and V_{CC} from coupling into the A-to-D analog stage. All A-to-D specifications are given with respect to AD_{REFLO} unless otherwise noted.

Resolution . . . . . 10 bits (1024 values)
Monotonic . . . . . Assured
Output conversion code . . . . . 00h to 3FFh [00 for $V_{AI} \leq AD_{REFLO}$; 3FF for $V_{AI} \geq AD_{REFHI}$]

MibADC recommended operating conditions†

		MIN	MAX	UNIT
AD_{REFHI}	A-to-D high-voltage reference source	V_{SSAD}	V_{CCAD}	V
AD_{REFLO}	A-to-D low-voltage reference source	V_{SSAD}	V_{CCAD}	V
V_{AI}	Analog input voltage	V_{SSAD} – 0.3	V_{CCAD} + 0.3	V
I_{AIC}	Analog input clamp current‡ ($V_{AI} < V_{SSAD}$ – 0.3 or $V_{AI} > V_{CCAD}$ + 0.3)	– 2	2	mA

† For V_{CCAD} and V_{SSAD} recommended operating conditions, see the "device recommended operating conditions" table.
‡ Input currents into any ADC input channel outside the specified limits could affect conversion results of other channels.

operating characteristics over full ranges of recommended operating conditions§¶

PARAMETER		DESCRIPTION/CONDITIONS		MIN	TYP	MAX	UNIT
R_a	Analog input resistance	See Figure 22			250	500	Ω
R_b	Sample switch resistance	See Figure 22			250	500	Ω
C_i	Analog input capacitance	See Figure 22	Conversion			10	pF
			Sampling			30	pF
I_{AIL}	Analog input leakage current	See Figure 22		–1		1	µA
$I_{ADREFHI}$	AD_{REFHI} input current	AD_{REFHI} = 3.6 V, $AD_{REFLO} = V_{SSAD}$				5	mA
CR	Conversion range over which specified accuracy is maintained	$AD_{REFHI} - AD_{REFLO}$		3		3.6	V
E_{DNL}	Differential nonlinearity error	Difference between the actual step width and the ideal value. (See Figure 24)				±1.5	LSB
E_{INL}	Integral nonlinearity error	Maximum deviation from the best straight line through the MibADC. MibADC transfer characteristics, excluding the quantization error. (See Figure 25)				±2	LSB
E_{TOT}	Total error/Absolute Accuracy	Maximum value of the difference between an analog value and the ideal midstep value. (See Figure 26)				±2	LSB

§ $V_{CCAD} = AD_{REFHI}$
¶ 1 LSB = $(AD_{REFHI} - AD_{REFLO})/2^{10}$ for the MibADC

multi-buffered A-to-D converter (MibADC) (continued)

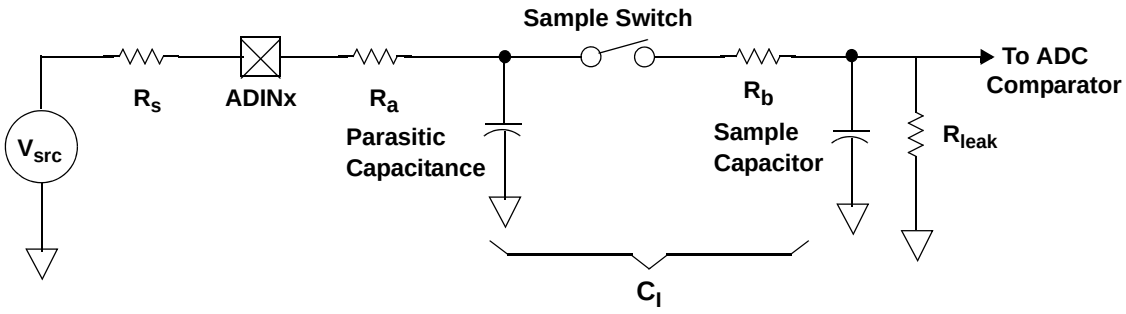


Figure 22. MibADC Input Equivalent Circuit

multi-buffer ADC timing requirements

		MIN	MAX	UNIT
$t_{c(ADCLK)}$	Cycle time, MibADC clock	0.05		µs
$t_{d(SH)}$	Delay time, sample and hold time	1		µs
$t_{d(C)}$	Delay time, conversion time	0.55		µs
$t_{d(SHC)}$ †	Delay time, total sample/hold and conversion time	1.55		µs

† This is the minimum sample/hold and conversion time that can be achieved. These parameters are dependent on many factors; for more details, see the *TMS470R1x Multi-Buffered Analog-to-Digital Converter (MibADC) Reference Guide* (literature number SPNU206).

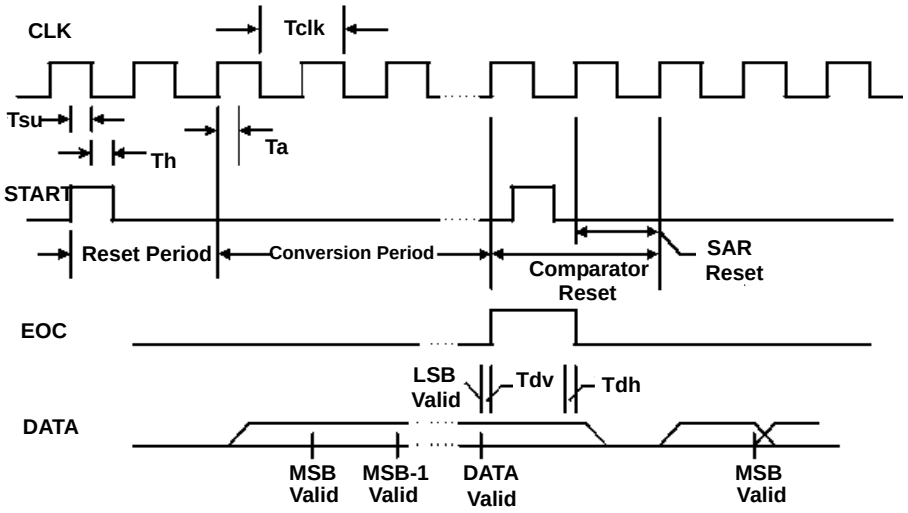
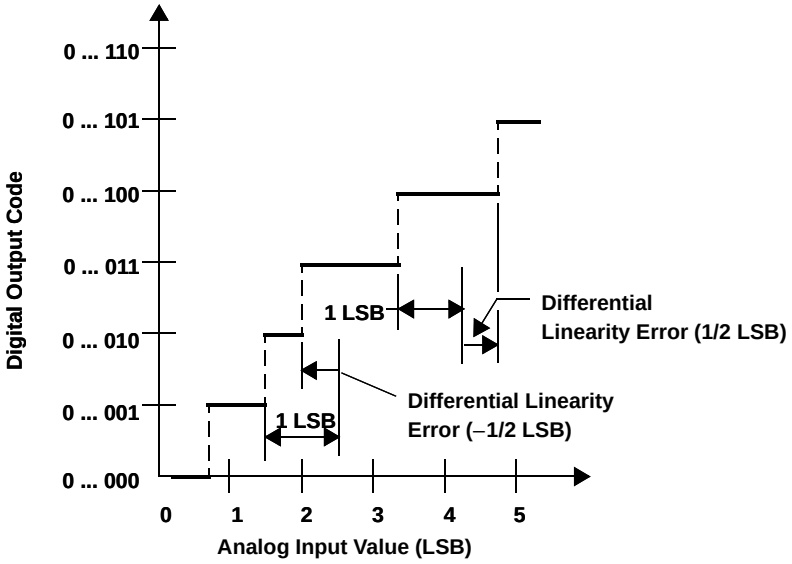


Figure 23. MibADC Timing Diagram

multi-buffered A-to-D converter (MibADC) (continued)

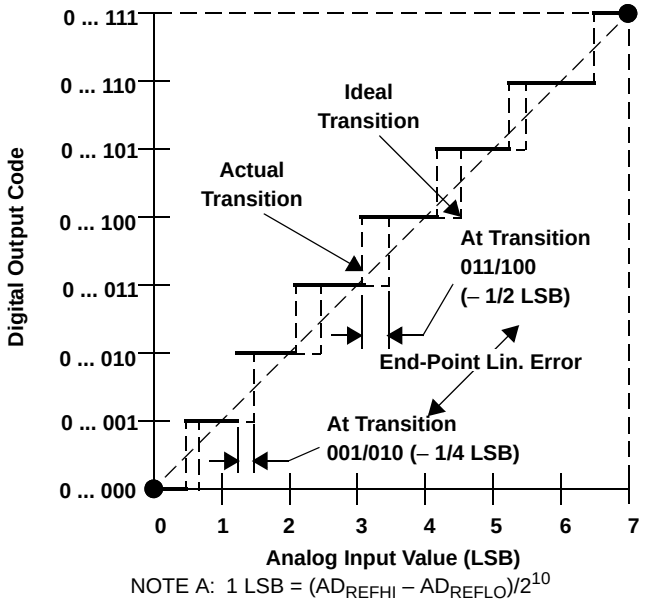
The differential nonlinearity error shown in Figure 24 (sometimes referred to as differential linearity) is the difference between an actual step width and the ideal value of 1 LSB.



NOTE A: 1 LSB = $(AD_{REFHI} – AD_{REFLO})/2^{10}$

Figure 24. Differential Nonlinearity (DNL)

The integral nonlinearity error shown in Figure 25 (sometimes referred to as linearity error) is the deviation of the values on the actual transfer function from a straight line.

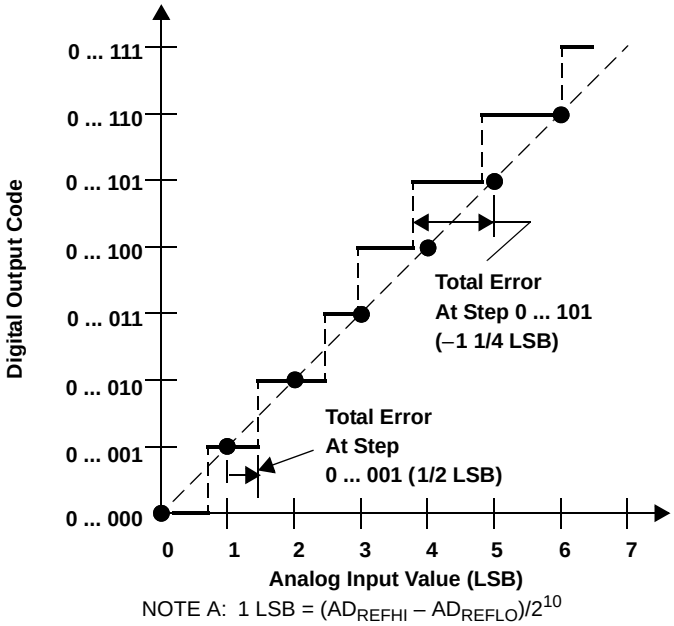


NOTE A: 1 LSB = $(AD_{REFHI} – AD_{REFLO})/2^{10}$

Figure 25. Integral Nonlinearity (INL) Error

multi-buffer A-to-D converter (MibADC) (continued)

The absolute accuracy or total error of an MibADC as shown in Figure 26 is the maximum value of the difference between an analog value and the ideal midstep value.

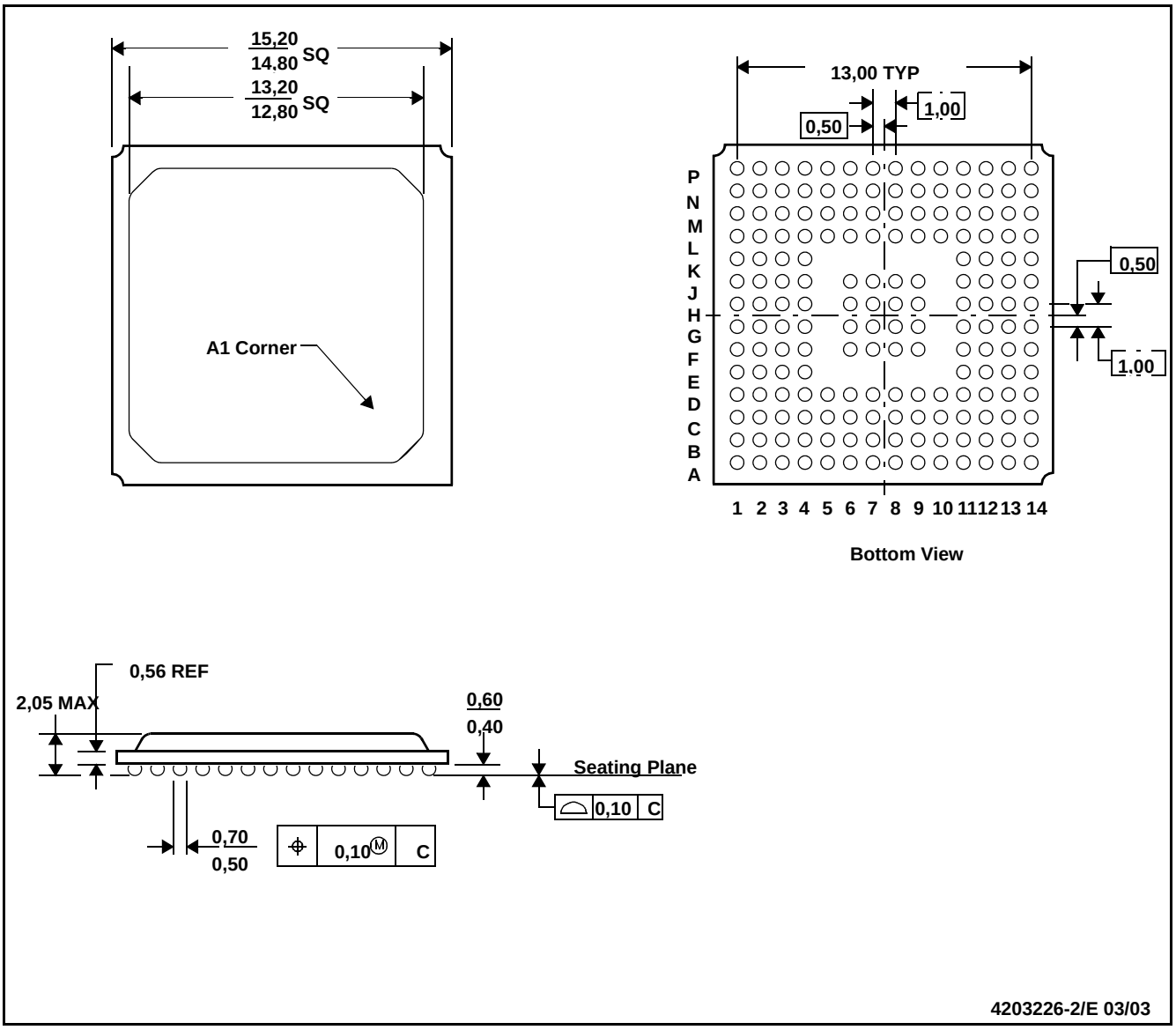


NOTE A: 1 LSB = $(AD_{REFHI} – AD_{REFLO})/2^{10}$

Figure 26. Absolute Accuracy (Total) Error

MECHANICAL DATA

GJZ (S-PBGA-N176) **PLASTIC BALL GRID ARRAY**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.

Thermal Resistance Characteristics†

PARAMETER	°C/W
$R_{\Theta JA}$	34.31
$R_{\Theta JC}$	7.51

†Assuming power dissipation = 0.6W; ambient temperature = 70C;
PCB = 4-layer metal 101.50 x 114.50 x 1.60mm

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REVISION HISTORY

REV	DATE	NOTES
I	10/05	Updates: Page 11, added No Connect pin listing. Page 13, added decoded block size for flash memory. Page 13, moved paragraph about XOR share feature to Description section. Page 13, added information about the OTP to the Flash program and erase section. Page 16, changed "System Address" to 0xFFFF_FFCC. Page 30, updated I_{CC} halt maximum value to 1mA. Page 30, removed ICLK parameter from I_{CC} test conditions. Page 30, removed "all frequencies" from halt test conditions. Page 30, changed "all frequencies" to "No DC load" for I_{CCAD} standby test condition. Page 34, changed $f_{(OSCRST)}$ value from MAX to TYP. Page 37, removed note about timing requirements from timing requirements for $\overline{\text{PORRST}}$ table. Page 37, changed V_{CC} to V_{CCIO} in timing#8 and #10. Page 49 - 56, MibSPI timing parameters updated. Page 62, split operating characteristic R_I into R_a and $R_{b.}$ Page 62, removed reference to V_{CCIO} in note under operating characteristics table. Page 63, updated Figure 22. Page 63, added Figure 23.

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