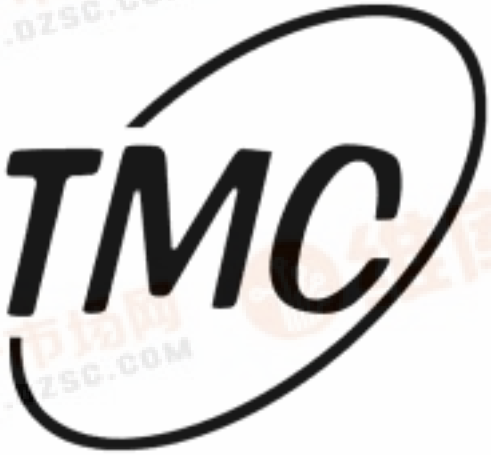
晶揚科技股份有限公司
Taiwan Micropaq Corporation



承 認 書

SPECIFICATION FOR APPROVAL

TM54S816T-6G

新竹縣新竹工業區文化路 4 號
No.4 Wenhua Rd. HsinChu Industrial Park
HuKou , Taiwan, R.O.C.
TEL：886-3-597-9402 ・ FAX：886-3-597-0775
http://www.tmc.com.tw

Description

The **TM54S816T** is organized as 4-bank x 2097152-word x 16-bit(**8Mx16**), fabricated with high performance CMOS technology. Synchronous design allows precise cycle control with the use of system clock I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable burst length and programmable latencies allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

Features

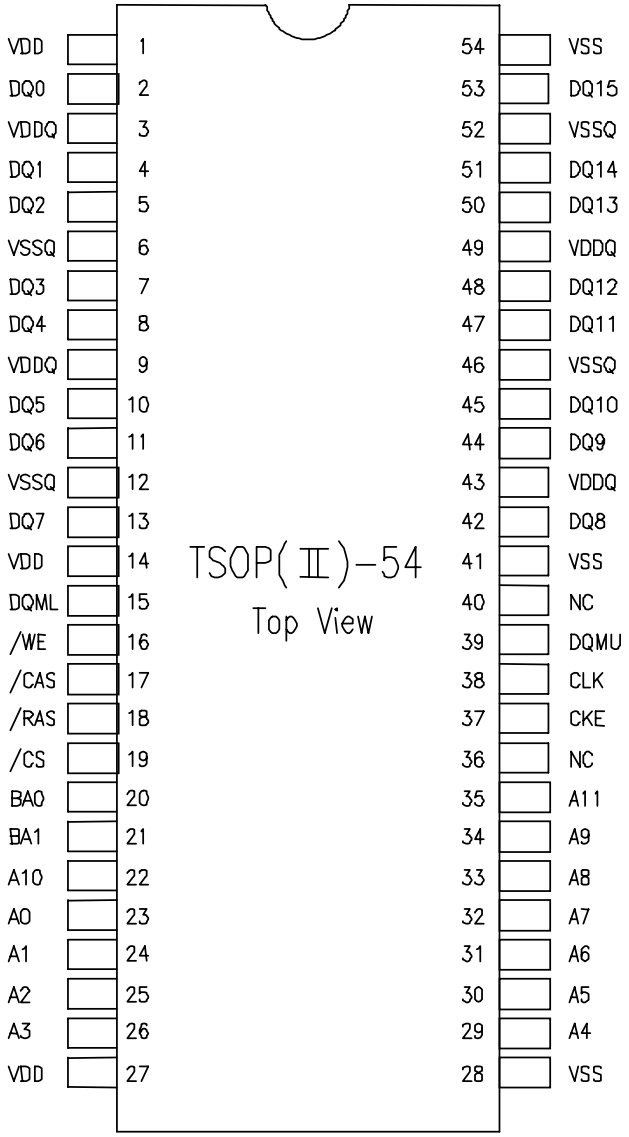
- Package: 400-mil 54-pin TSOP(II)
- JEDEC PC133/PC100 compatible
- Single 3.3V Power Supply
- LVTTL Signal Compatible
- Programmable
  - CAS Latency (3 or 2 clocks)
  - Burst Length (1,2,4, 8 & full page)
  - Burst type (Sequential & Interleave)
- Burst read/write and burst read/single write operations capability
- Byte control(DQML and DQMU)
- Auto and Self Refresh
- 64ms refresh period (4K Refresh)
- 12-Row x 9-Column organization
- 4-Bank operation controlled by BA1,BA0
- Pin36 and 40 are “No Connected”
- Fully synchronous operation referenced to clock rising edge

Frequency vs. AC Parameter

Symbol	Parameter	- 6G	- 7G	- 75G	Unit
f_{CK3}	Max. operating frequency @CL=3	166	143	133	Mhz
f_{CK2}	Max. operating frequency @CL=2	133	133	100	Mhz
t_{CK3}	Min. clock cycle time @CL=3	6.0	7.0	7.5	ns
t_{AC3}	Max. access time from CLK @CL=3	5.0	5.4	5.4	ns
t_{CK2}	Min. clock cycle time @CL=2	7.5	7.5	10	ns
t_{AC2}	Max. access time from CLK @CL=2	5.4	5.4	6.0	ns
t_{rcd}	Min. row to column delay	15	18	18	ns

Pin Description

Pin Name	Function	Pin Name	Function
CLK	Master Clock	DQML/DQMU	Output Disable(Write Mask)
CKE	Clock Enable	A0-11	Address Input
/CS	Chip Select	BA1,BA0	Bank Address
/RAS	Row Address Strobe	Vdd	Power Supply
/CAS	Column Address Strobe	VddQ	Power Supply for Output
/WE	Write Enable	Vss/VssQ	Ground
DQ0~DQ15	Data I/O	NC	No Connection



Pin Function

Pin	Name	Pin Function
CLK	System clock	Active on the positive going edge to sample all inputs.
/CS	Chip select	Disables or enables device operation by masking or enabling all inputs except CLK,CKE and DQML/DQMU.
CKE	Clock enable	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby.
A0~A11	Address input	Row/column addresses are multiplexed on the same pins. Row address:A0~A11, Column address:A0~A7
BA1,BA0	Bank address	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
/RAS	Row address strobe	Latches row addresses on the positive going edge of the CLK with /RAS low. Enables rows access & pre-charge.
/CAS	Column address strobe	Latches column addresses on the positive going edge of the CLK with /CAS low. Enables column access.
/WE	Write enable	Enables write operation and row pre-charge. Latches data in starting from /CAS,/WE active.
DQMU/DQML	Data I/O mask	Makes data output Hi-Z, T_{shz} after the clock and masks the output. Blocks data input when DQML/DQMU active.
$DQ_{0\sim15}$	Data input/output	Data inputs/outputs are multiplexed on the same pins.
Vdd/Vss	Power supply/ground	Power and ground for the input buffers and the core logic.
V_{DDQ}/V_{SSQ}	Data output power / ground	Isolated power supply and ground for the output buffers to provide improved noise immunity.

NC/RFU	No connection / reserved for future use	This pin is recommended to be left no connection on the device.

Absolute maximum ratings

Parameter	Symbol	Ratings	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-0.5 to 4.6	V
Voltage supply relative to Vss	Vdd,Vdd_Q	-0.5 to 4.6	V
Operating temperature	Topr	0 to +70	℃
Power dissipation	P_D	1	W
Output Shorted current	I_{OS}	50	mA

DC OPERATING CONDITIONS

Recommended operating conditions(Referenced to Vss=0V,T_A=0℃ to 70℃)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage	Vdd, Vdd_Q	3.0	3.3	3.6	V
Input Logic High Voltage	V_{IH}	2.0	-	Vdd	V
Input Logic Low Voltage	V_{IL}	-0.3	-	0.8	V
Output Logic High Voltage	V_{OH}	2.4	-	-	V
Output Logic Low Voltage	V_{OL}	-	-	0.4	V
Input/Output Leakage Current	I_{IL}, I_{OL}	-5	-	5	μA

DC Characteristics

(Recommended operating condition T_A = 0℃ to 70℃, unless otherwise noted.)

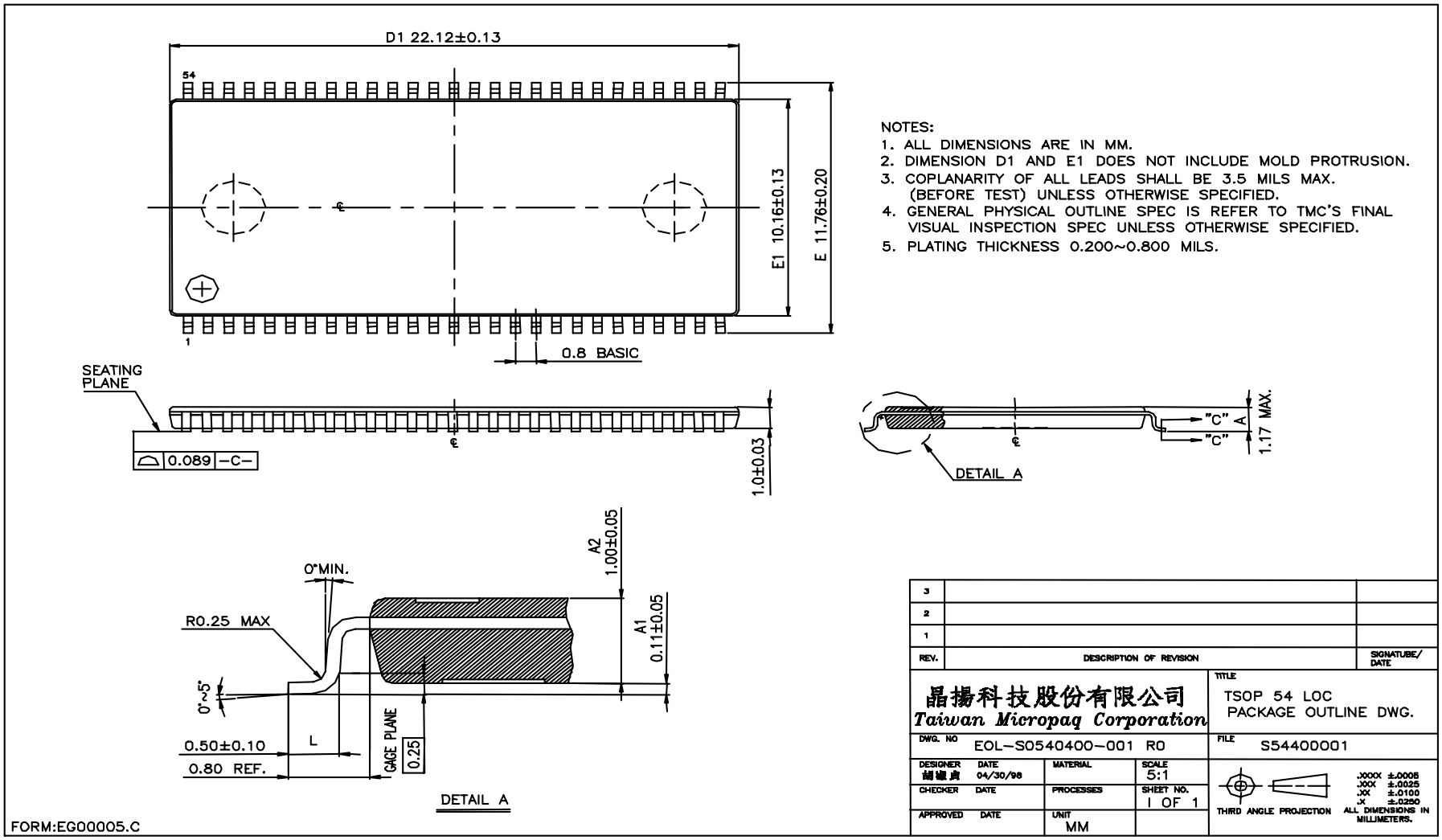
Parameter	Symbol	Test Conditions	Limits			Unit
			-6G	-7G	-75G	
Operating Current (One bank active)	I_{CC1}	Burst length=1, CL=3, t_{RC} = t_{RC}(min), t_{CK} = t_{CK}(min)	120	110	100	mA
Pre-charge Standby Current in Power Down Mode	$I_{CC2}P$	CKE <V_{IL}(max), t_{CK} = 15ns	2			mA
	$I_{CC2}PS$	CKE & CLK<V_{IL}(max)	2			
Pre-charge Standby Current in Non-Power Down Mode	$I_{CC2}N$	/CS =CKE >V_{IH}(min), t_{CK} = 15ns	25			mA
	$I_{CC2}NS$	/CS=CKE >V_{IH}(min), CLK< V_{IL}(max)	15			
Active Standby Current in Power Down Mode	$I_{CC3}P$	CKE<V_{IL}(max), t_{CK} =15ns	7			mA

	$I_{CC3}PS$	CKE & CLK<V_{IL}(max)	5			
Active Standby Current in Non-Power Down Mode	$I_{CC3}N$	/CS=CKE>V_{IH}(min), t_{CK} =15ns	35			mA
	$I_{CC3}NS$	/CS=CKE>V_{IH}(min), CLK < V_{IL}(max)	30			
Operating Current (Burst)	I_{CC4}	BL=4,CL=3,All Banks Active	160	150	140	mA
Auto Refresh Current	I_{CC5}	CBR Command, t_{CK} = t_{CK}(min)	160	150	140	mA
Self Refresh Current	I_{CC6}	CKE < 0.2V	2			mA

AC Characteristics

Recommended operating conditions(Vdd=VddQ=3.3V,Vss=0V,T_A= 0 to 70℃)

	Symbol	Parameter	-6G		-7G		-75G		Unit
			Min	Max	Min	Max	Min	Max	
1	f_{CK3}	Clock Frequency,CL=3		166		143		133	Mhz
2	f_{CK2}	Clock Frequency,CL=2		133		133		100	Mhz
3	t_{CK3}	Clock Cycle Time,CL=3	6.0		7.0		7.5		ns
4	t_{CK2}	Clock Cycle Time,CL=2	7.5		7.5		10		ns
5	t_{AC3}	Clock Access Time,CL=3		5.0		5.4		5.4	ns
6	t_{AC2}	Clock Access Time,CL=2		5.4		5.4		6.0	ns
7	t_{CH}	Clock High Pulse Width	2.5		2.5		2.5		ns
8	t_{CL}	Clock Low Pulse Width	2.5		2.5		2.5		ns
9	t_{IS}	Input Setup time(all inputs)	1.5		1.5		1.5		ns
10	t_{IH}	Input Hold time(all inputs)	0.8		0.8		0.8		ns
11	t_{OH}	Data-out Hold time	1.5		1.8		1.8		ns
12	t_T	Transition time of clock	1.0	10	1.0	10	1.0	10	ns
13	t_{RCD}	Row to Column delay	15		18		18		ns
14	t_{RC}	Row Cycle time	60		63		63		ns
15	t_{RAS}	Row active time	42		42		42		ns
16	t_{RP}	Row Pre-charge time	15		18		18		ns
17	t_{RRD}	Row active to active delay	12		14		14		ns
18	t_{REF}	Refresh time	64		64		64		ms



NOTES:
1. ALL DIMENSIONS ARE IN MM.
2. DIMENSION D1 AND E1 DOES NOT INCLUDE MOLD PROTRUSION.
3. COPLANARITY OF ALL LEADS SHALL BE 3.5 MILS MAX. (BEFORE TEST) UNLESS OTHERWISE SPECIFIED.
4. GENERAL PHYSICAL OUTLINE SPEC IS REFER TO TMC'S FINAL VISUAL INSPECTION SPEC UNLESS OTHERWISE SPECIFIED.
5. PLATING THICKNESS 0.200~0.800 MILS.

REV.	DESCRIPTION OF REVISION	SIGNATUBE/ DATE
3		
2		
1		

晶揚科技股份有限公司
Taiwan Micropaq Corporation

TITLE: TSOP 54 LOC PACKAGE OUTLINE DWG.

DWG. NO	FILE
EOL–S0540400–001 R0	S54400001

DESIGNER / DATE	MATERIAL	SCALE
胡維貞 04/30/98		5:1
CHECKER / DATE	PROCESSES	SHEET NO.
		1 OF 1
APPROVED / DATE	UNIT	
	MM	

THIRD ANGLE PROJECTION

.XXXX ±.0005
.XXX ±.0025
.XX ±.0100
.X ±.0250
ALL DIMENSIONS IN MILLIMETERS.

FORM:EG00005.C