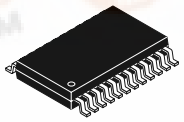
TEXAS INSTRUMENTS



SLOS379A – SEPTEMBER 2001 – REVISED JANUARY 2002

17-W MONO FILTER-FREE CLASS-D AUDIO POWER AMPLIFIER

FEATURES

- 17 W Into 8-Ω Load From 18-V Supply
- Third-Generation Modulation Technique:
  - Filter-Free Operation
  - Improved Efficiency
  - Improved SNR
- Low Supply Current . . . 8 mA Typ at 12 V
- Shutdown Control . . . <1 μA Typ
- Shutdown Pin Is TTL Compatible
- T_A = –40°C to 85°C
- Space-Saving, Thermally-Enhanced PowerPAD™ Packaging

APPLICATIONS

- LCD Monitors
- Hands-Free Car Kits
- Powered Speakers

DESCRIPTION

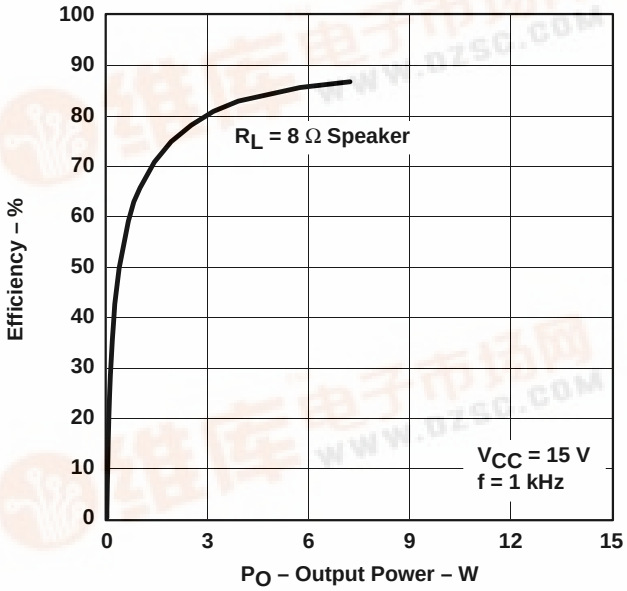
The TPA3000D1 is a 17-W mono bridge-tied load (BTL) filter-free class-D audio power amplifier with high efficiency, eliminating the need for heatsinks. The TPA3000D1 is designed to drive speakers without an output filter.

The gain of the amplifier is controlled by two input terminals, GAIN1 and GAIN0. This allows the amplifier to be configured for a gain of 12, 18, 23.6, and 36 dB. The differential input stage provides high common mode rejection and improved power supply rejection.

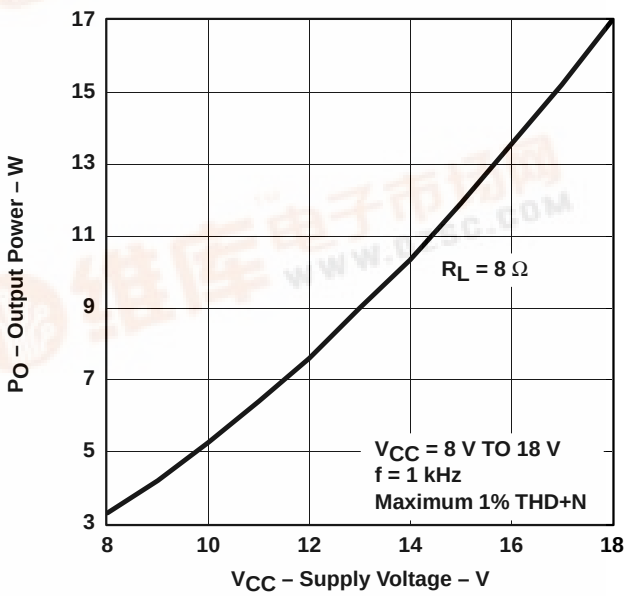
The amplifier also includes depop circuitry to reduce the amount of turnon pop at power-up and when cycling $\overline{\text{SHUTDOWN}}$.

The TPA3000D1 is available in the 24-pin thermally enhanced TSSOP package (PWP) which eliminates the need for an external heat sink when playing music.

EFFICIENCY vs OUTPUT POWER



OUTPUT POWER vs SUPPLY VOLTAGE

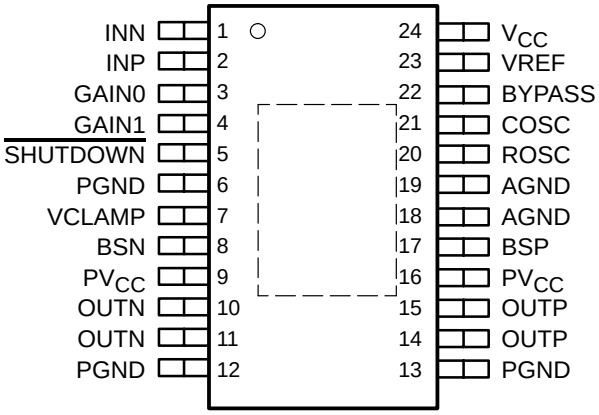


AVAILABLE OPTIONS

T_A	PACKAGED DEVICES
	TSSOP (PWP)†
–40°C to 85°C	TPA3000D1PWP

† The PWP package is available taped and reeled. To order a taped and reeled part, add the suffix R to the part number (e.g., TPA3000D1PWPR).

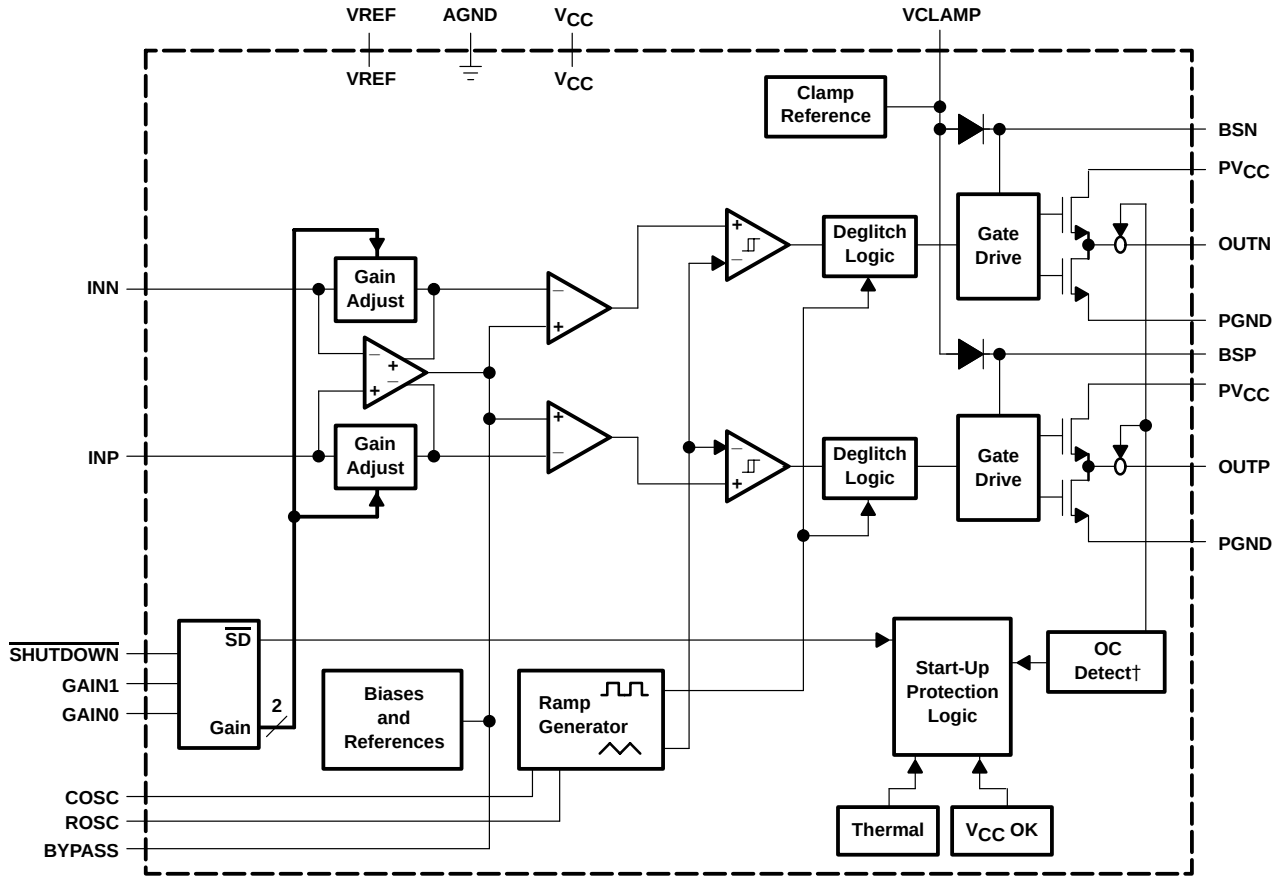
PWP PACKAGE
(TOP VIEW)



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
AGND	18, 19		Analog ground
BSN	8	I	Bootstrap pin for high-side gate drive of negative BTL output (connect a 10-nF capacitor from OUTN to BSN)
BSP	17	I	Bootstrap pin for high-side gate drive of positive BTL output (connect a 10-nF capacitor from OUTP to BSP)
BYPASS	22	I	Connect 0.47 μF capacitor to ground for BYPASS voltage filtering.
COSC	21	I	Connect a 220-pF capacitor to ground to set oscillation frequency.
GAIN0	3	I	Bit 0 of gain control (see Table 1 for gain settings)
GAIN1	4	I	Bit 1 of gain control (see Table 1 for gain settings)
INN	1	I	Negative differential input
INP	2	I	Positive differential input
OUTN	10, 11	O	Negative BTL output
OUTP	14, 15	O	Positive BTL output
PGND	6, 12, 13		Power ground
PV_{CC}	9, 16	I	High-voltage power supply (for output stages)
ROSC	20	I	Connect 120 kΩ resistor to ground to set oscillation frequency.
$\overline{\text{SHUTDOWN}}$	5	I	Shutdown terminal (negative logic), TTL compatible, 21-V compliant
V_{CC}	24	I	Analog high-voltage power supply
VCLAMP	7	O	Connect 100-nF capacitor to ground to provide reference voltage for H-bridge gates
VREF	23	O	5-V internal regulator for control circuitry (connect a 0.1-μF to 1-μF capacitor to ground)

functional block diagram



† Short-circuit protection operates only for shorts from the outputs to ground.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage: V_{CC}, PV_{CC} . . . . . –0.3 V to 21 V
Input voltage: $\overline{SHUTDOWN}$ . . . . . –0.3 V to V_{CC} + 0.3 V
GAIN0, GAIN1 . . . . . –0.3 V to 5.5 V
INN, INP . . . . . –0.3 V to 7 V
Continuous total power dissipation . . . . . (see Dissipation Rating Table)
Operating free-air temperature range, T_A . . . . . –40°C to 85°C
Operating junction temperature range, T_J . . . . . –40°C to 150°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$	DERATING FACTOR	$T_A = 70°C$	$T_A = 85°C$
PWP	2.7 W	21.8 mW/°C	1.7 W	1.4 W

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{CC}, PV_{CC}		8	18	V
High-level input voltage, V_{IH}	GAIN0, GAIN1, $\overline{\text{SHUTDOWN}}$†	2		V
Low-level input voltage, V_{IL}	GAIN0, GAIN1, $\overline{\text{SHUTDOWN}}$†		0.8	V
Operating free-air temperature, T_A		–40	85	°C

† See *Application Information* for more information on the characteristics of the $\overline{\text{SHUTDOWN}}$ terminal.

electrical characteristics at T_A = 25°C, PV_{CC} = V_{CC} = 12 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$\lvert V_{OS}\rvert$	Output offset voltage (measured differentially)	V_I = 0 V,	A_V = 12 dB			50	mV
PSRR	Power supply rejection ratio	PV_{CC} = 11.5 V to 12.5 V			–75		dB
$\lvert I_{IH}\rvert$	High-level input current	PV_{CC} = 12 V,	V_I = PV_{CC}			1	µA
$\lvert I_{IL}\rvert$	Low-level input current	PV_{CC} = 12 V,	V_I = 0 V			–1	µA
I_{CC}	Supply current				8	15	mA
$I_{CC(SD)}$	Supply current, shutdown mode				1	2	µA

operating characteristics, PV_{CC} = V_{CC} = 12 V, T_A = 25°C, R_L = 8 Ω, Gain = 12 dB (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
P_O	Output power	THD = 0.5%,	f = 1 kHz		7		W
THD + N	Total harmonic distortion plus noise	P_O = 15 W,	f = 20 Hz to 20 kHz		1%		
B_{OM}	Maximum output power bandwidth	THD = 1%			20		kHz
k_{SVR}	Supply ripple rejection ratio	f = 1 kHz,	$C_{(BYPASS)}$ = 0.47 µF		–70		dB
SNR	Signal-to-noise ratio	P_O = 12 W			95		dB
V_n	Noise output voltage	$C_{(BYPASS)}$ = 0.47 µF, No weighting filter used	f = 20 Hz to 22 kHz,		86		µV(rms)
					–81		dBV
		$C_{(BYPASS)}$ = 0.47 µF, A-weighted filter	f = 20 Hz to 22 kHz,		66		µV(rms)
					–84		dBV
Z_i	Input impedance				>23		kΩ

operating characteristics, PV_{CC} = V_{CC} = 18 V, T_A = 25°C, R_L = 8 Ω, Gain = 12 dB (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
P_O	Output power	THD = 0.5%,	f = 1 kHz		17		W
THD + N	Total harmonic distortion plus noise	P_O = 15 W,	f = 20 Hz to 20 kHz		1%		
B_{OM}	Maximum output power bandwidth	THD = 1%			20		kHz
k_{SVR}	Supply ripple rejection ratio	f = 1 kHz,	C_{BYPASS} = 0.47 µF		70		dB
SNR	Signal-to-noise ratio	P_O = 17 W			102		dB
V_n	Noise output voltage	$C_{(BYPASS)}$ = 0.47 µF, No weighting filter used	f = 20 Hz to 20 kHz,		86		µV(rms)
					–81		dBV
		$C_{(BYPASS)}$ = 0.47 µF, A-weighted filter	f = 20 Hz to 22 kHz,		66		µV(rms)
					–84		dBV
Z_i	Input impedance				>23		kΩ

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
	Efficiency	vs Output power	1, 2, 3
P_O	Output power	vs Supply voltage	4
I_{CC}	Supply current		5
$I_{O(sd)}$	Shutdown current		6
THD+N	Total harmonic distortion + noise	vs Output power	7, 8, 9, 10
		vs Frequency	11, 12, 13, 14
k_{SVR}	Supply voltage rejection ratio	vs Frequency	15, 16, 17
	Gain and phase		18
CMRR	Common-mode rejection ratio		19
V_{IO}	Input offset voltage	vs Common-mode input voltage	20, 21, 22

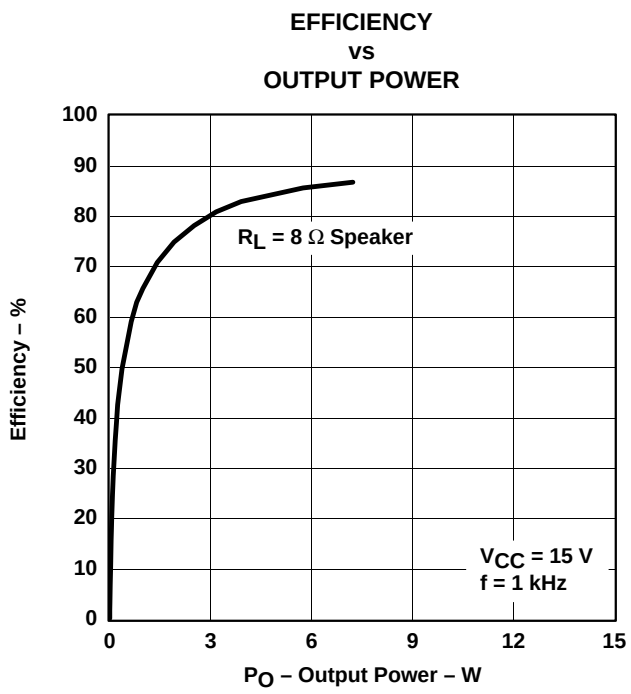


Figure 1

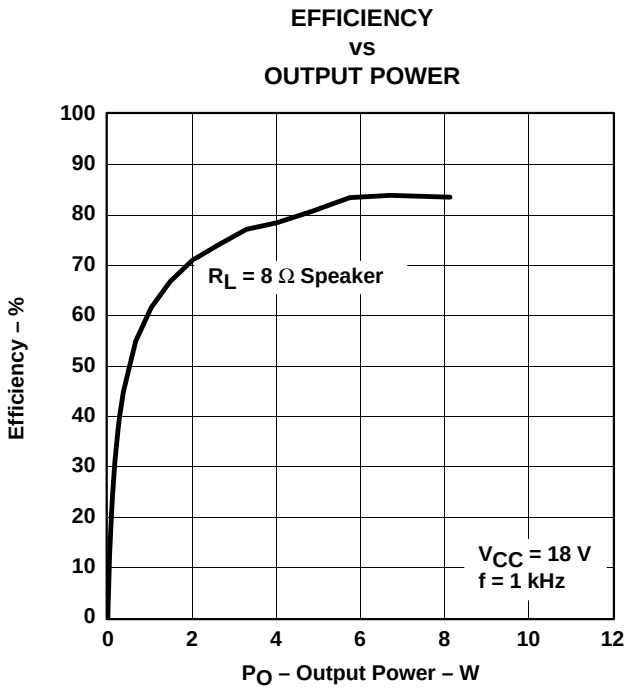


Figure 2

TYPICAL CHARACTERISTICS

EFFICIENCY vs OUTPUT POWER

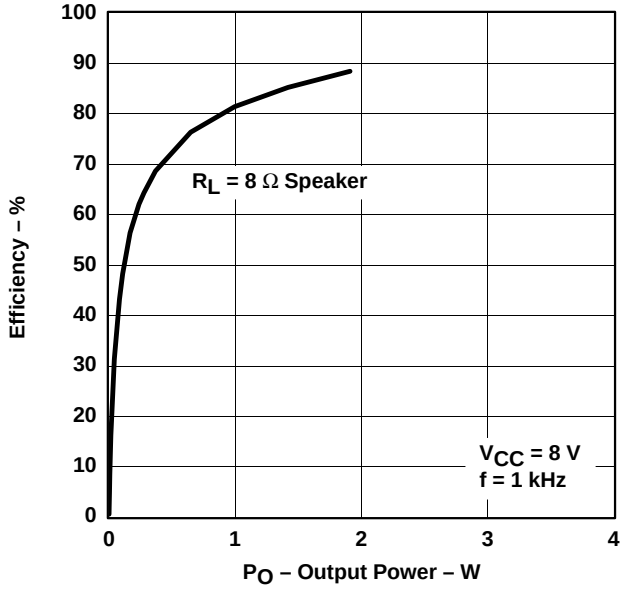


Figure 3

OUTPUT POWER vs SUPPLY VOLTAGE

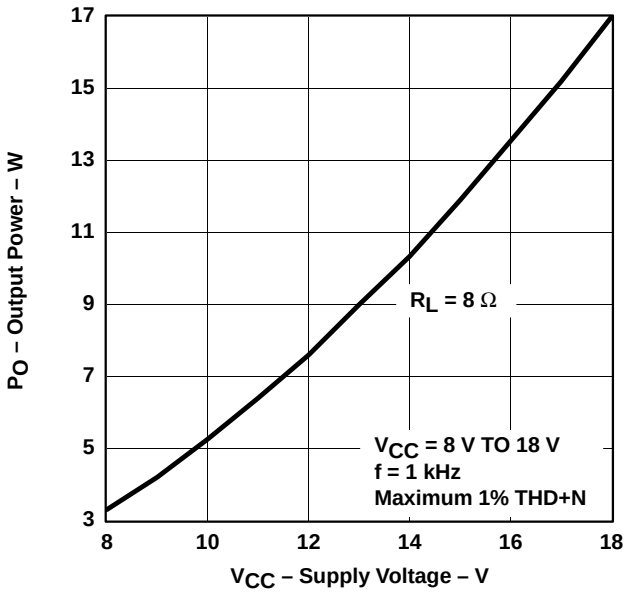


Figure 4

SUPPLY CURRENT vs SUPPLY VOLTAGE

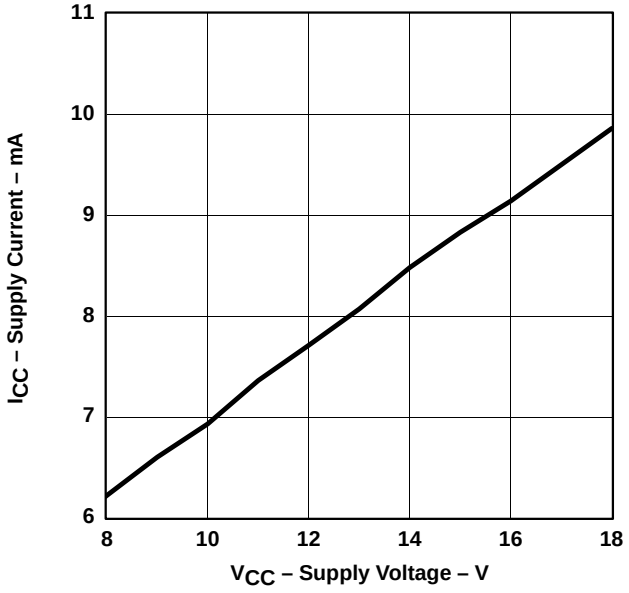


Figure 5

SHUTDOWN CURRENT vs SUPPLY VOLTAGE

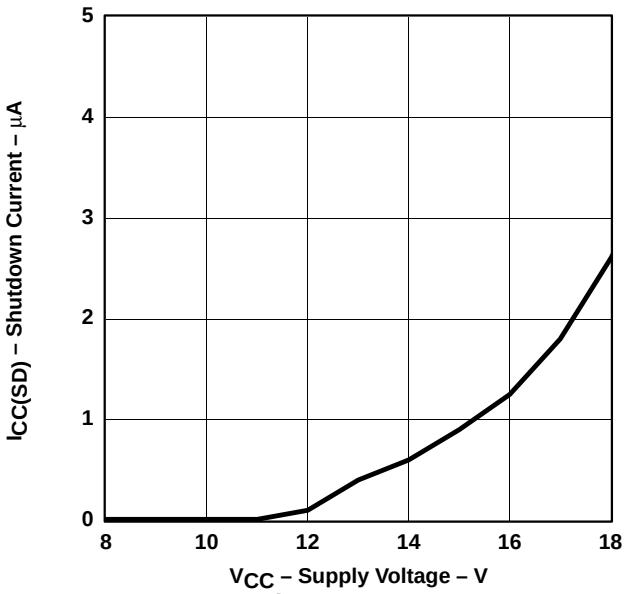


Figure 6

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION + NOISE
vs
OUTPUT POWER

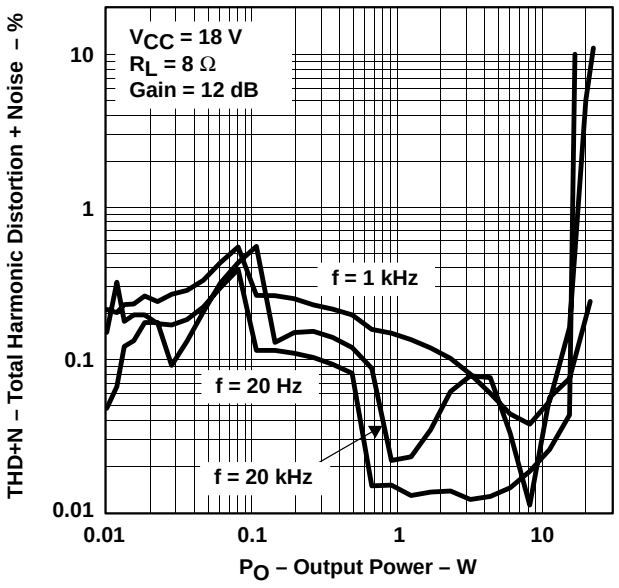


Figure 7

TOTAL HARMONIC DISTORTION + NOISE
vs
OUTPUT POWER

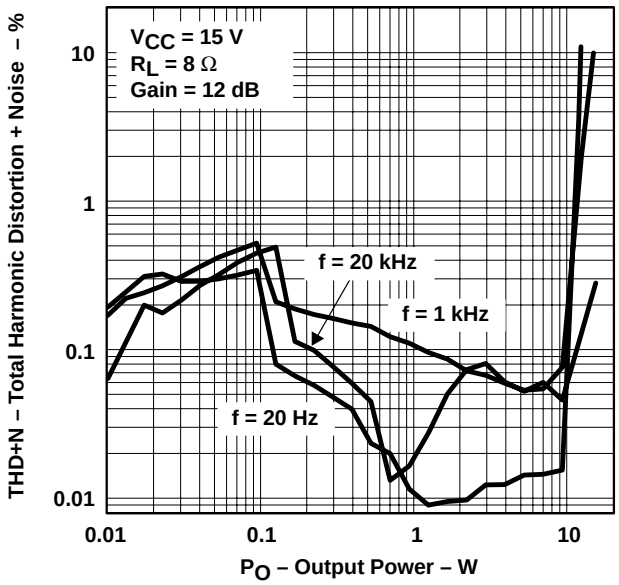


Figure 8

TOTAL HARMONIC DISTORTION + NOISE
vs
OUTPUT POWER

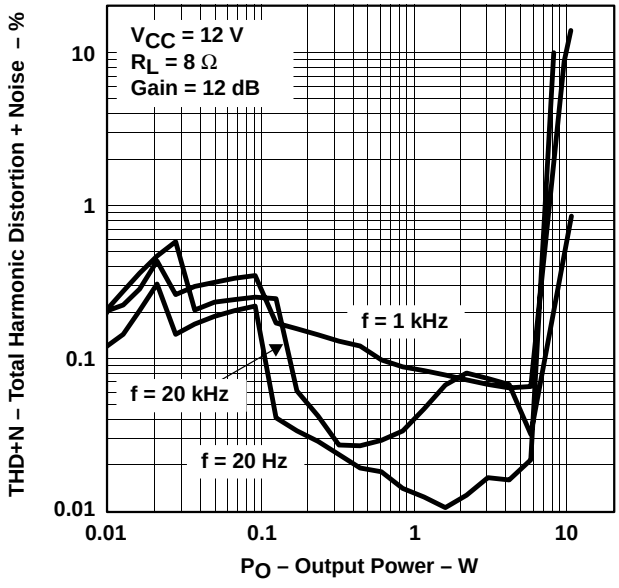


Figure 9

TOTAL HARMONIC DISTORTION + NOISE
vs
OUTPUT POWER

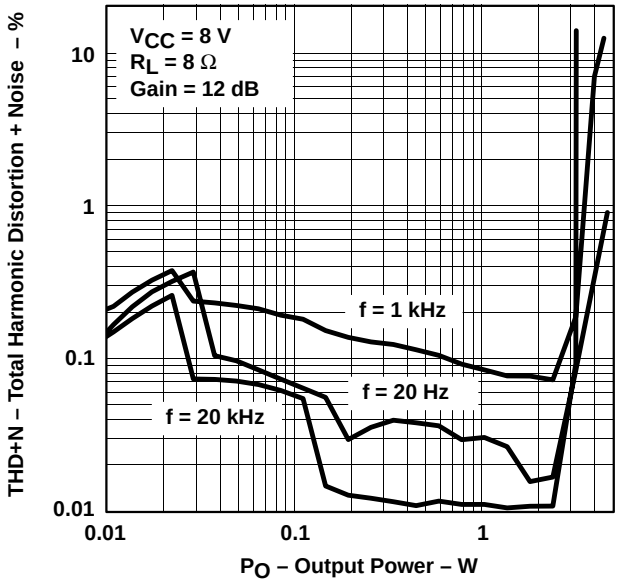


Figure 10

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION + NOISE
vs
FREQUENCY

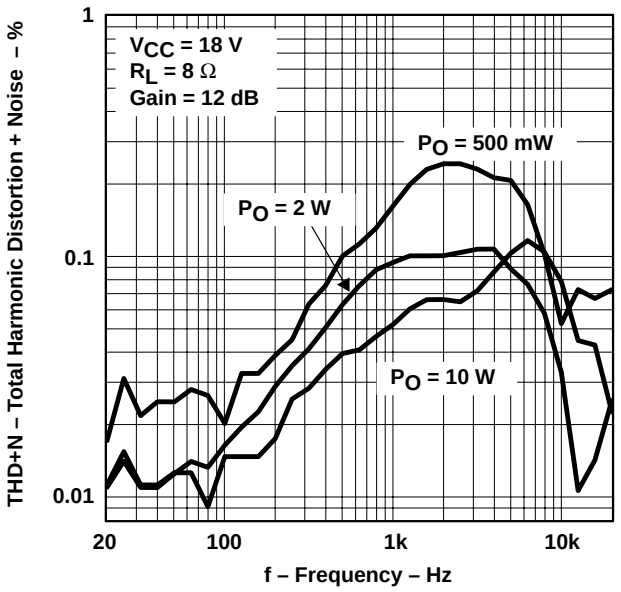


Figure 11

TOTAL HARMONIC DISTORTION + NOISE
vs
FREQUENCY

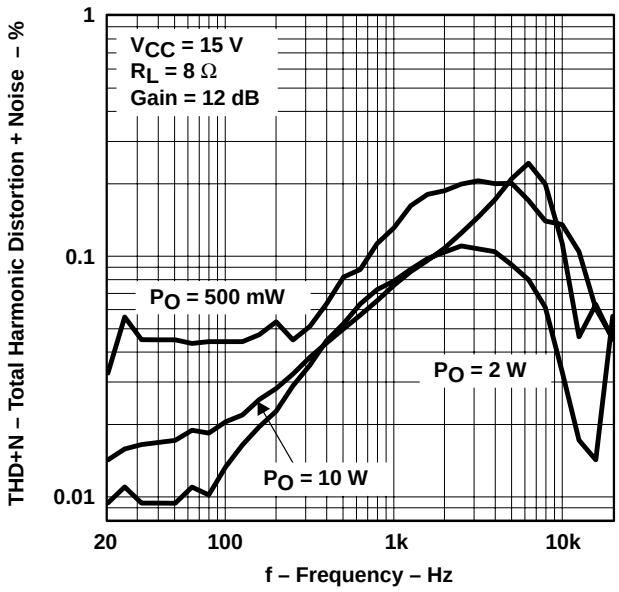


Figure 12

TOTAL HARMONIC DISTORTION + NOISE
vs
FREQUENCY

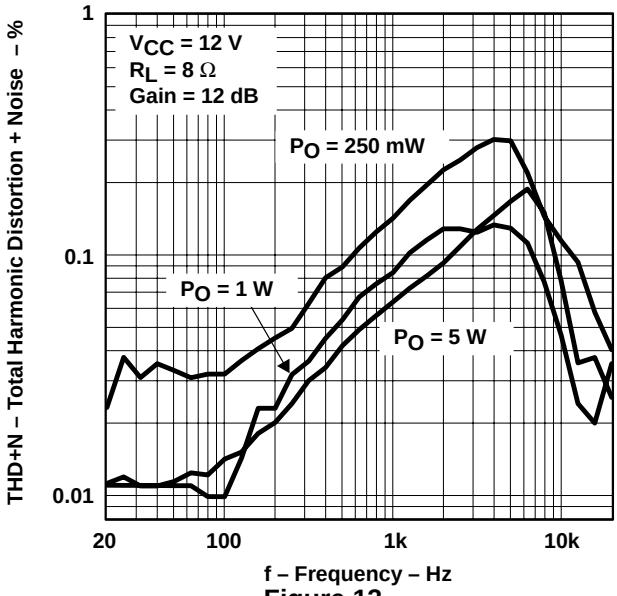


Figure 13

TOTAL HARMONIC DISTORTION + NOISE
vs
FREQUENCY

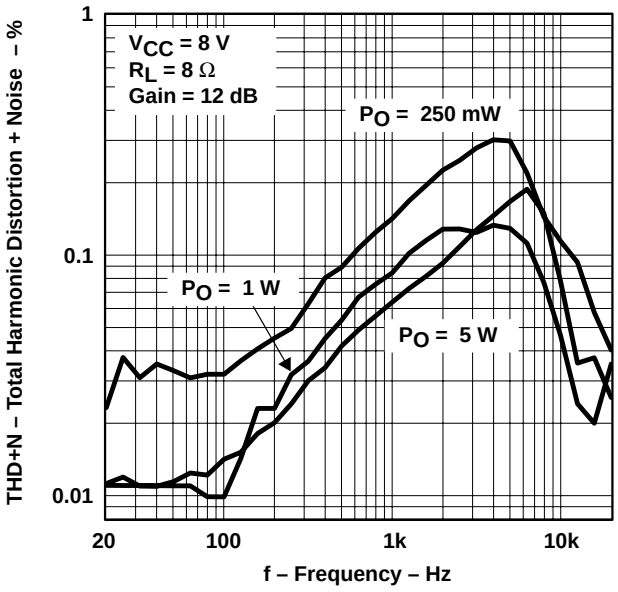


Figure 14

TYPICAL CHARACTERISTICS

SUPPLY VOLTAGE REJECTION RATIO vs FREQUENCY

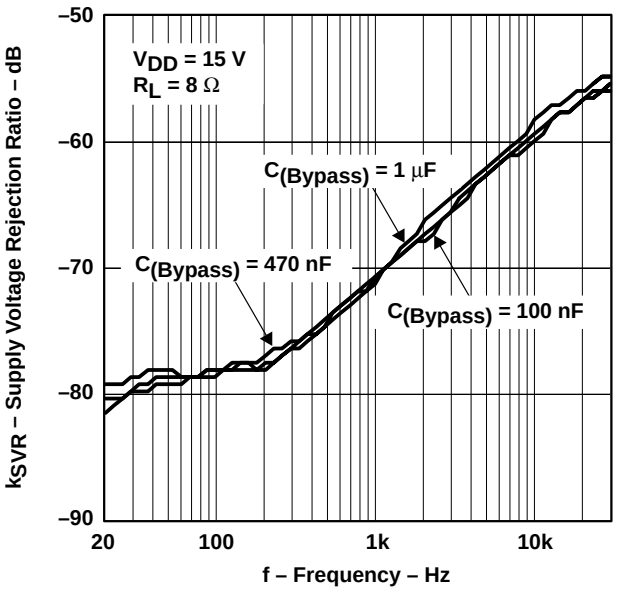


Figure 15

SUPPLY VOLTAGE REJECTION RATIO vs FREQUENCY

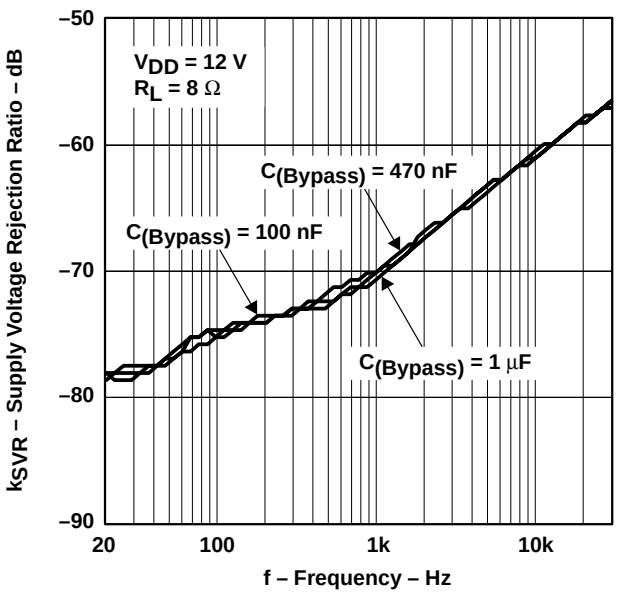


Figure 16

SUPPLY VOLTAGE REJECTION RATIO vs FREQUENCY

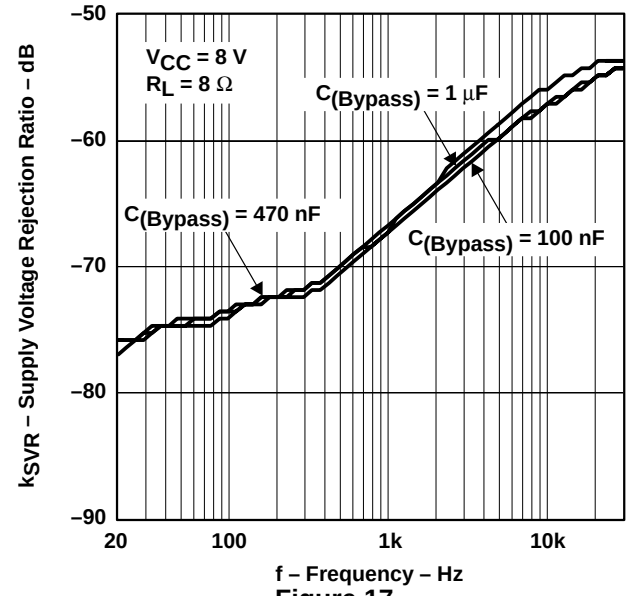


Figure 17

GAIN and PHASE vs FREQUENCY

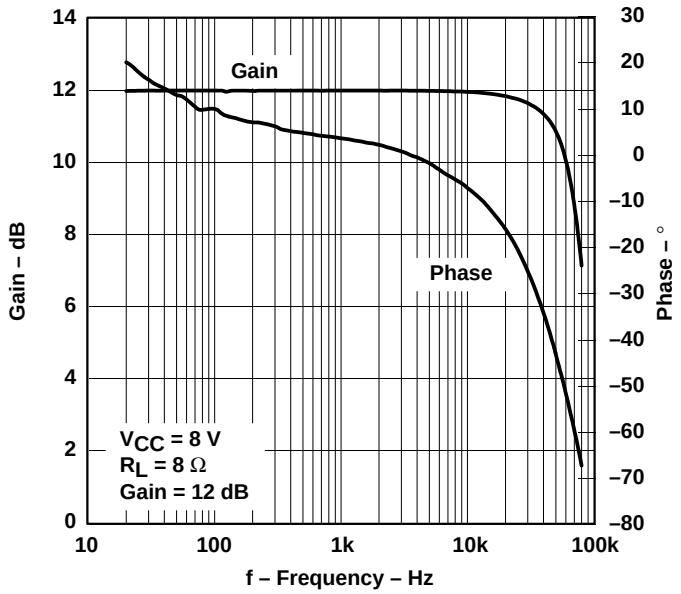


Figure 18

TYPICAL CHARACTERISTICS

COMMON-MODE REJECTION RATIO vs FREQUENCY

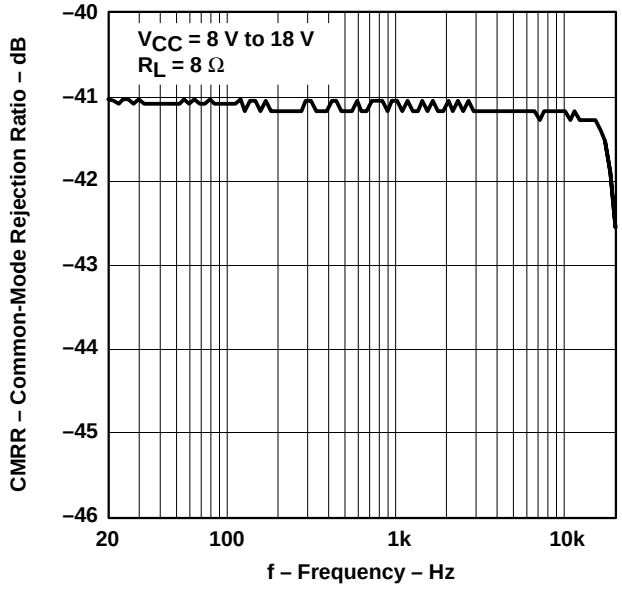


Figure 19

INPUT OFFSET VOLTAGE vs COMMON-MODE INPUT VOLTAGE

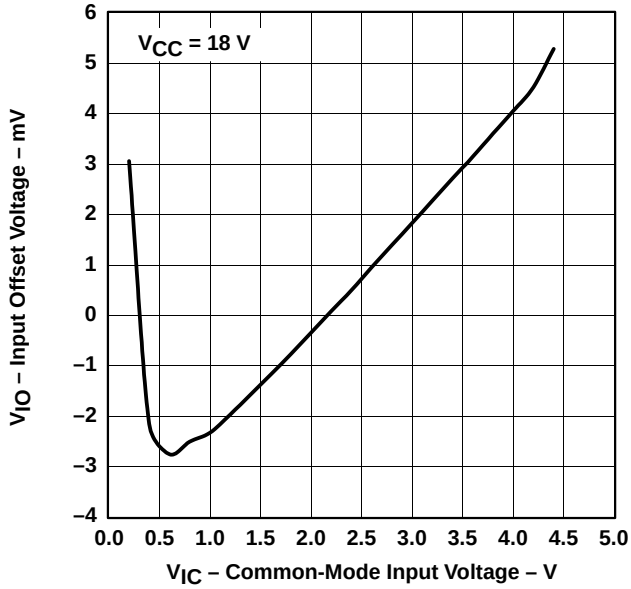


Figure 20

INPUT OFFSET VOLTAGE vs COMMON-MODE INPUT VOLTAGE

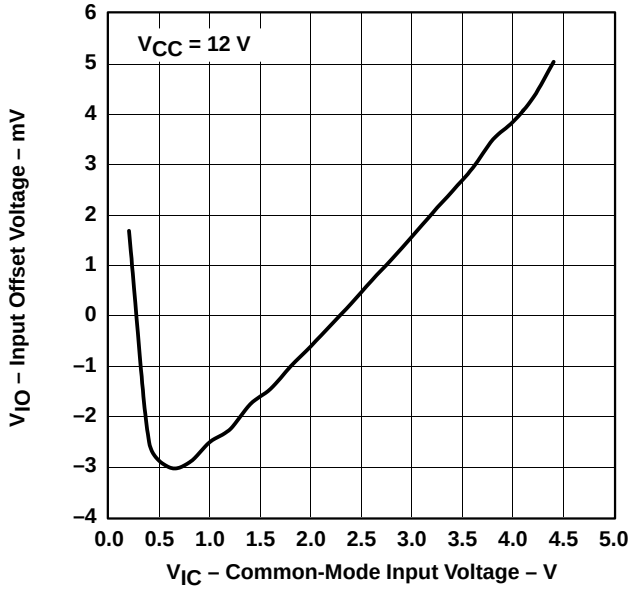


Figure 21

INPUT OFFSET VOLTAGE vs COMMON-MODE INPUT VOLTAGE

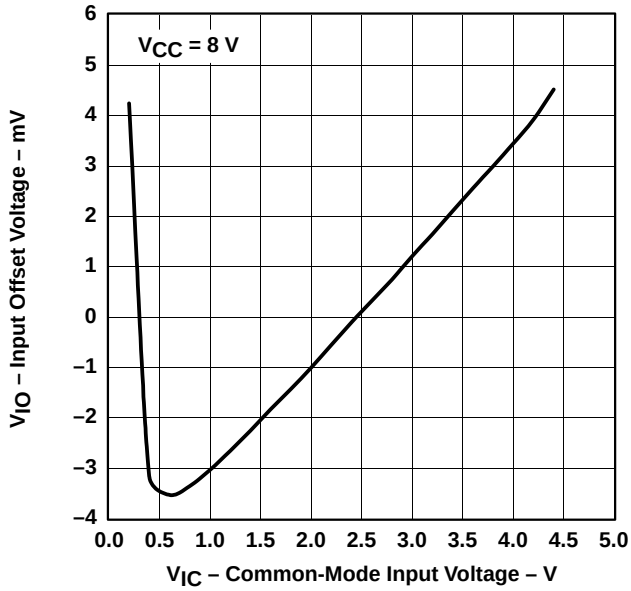


Figure 22

APPLICATION INFORMATION

eliminating the output filter with the TPA3000D1

This section focuses on how the user can eliminate the output filter with the TPA3000D1.

effect on audio

The class-D amplifier outputs a pulse-width modulated (PWM) square wave, which is the sum of the switching waveform and the amplified input audio signal. The human ear acts as a band-pass filter such that only the frequencies between approximately 20 Hz and 20 kHz are passed. The switching frequency components are much greater than 20 kHz, so the only signal heard is the amplified input audio signal.

traditional class-D modulation scheme

The traditional class-D modulation scheme, which is used in the TPA032D0x family, has a differential output where each output is 180 degrees out of phase and changes from ground to the supply voltage, V_{CC}. Therefore, the differential prefiltered output varies between positive and negative V_{CC}, where filtered 50% duty cycle yields 0 V across the load. The traditional class-D modulation scheme with voltage and current waveforms is shown in Figure 23. Note that even at an average of 0 V across the load (50% duty cycle), the current to the load is high, causing high loss, thus causing a high supply current.

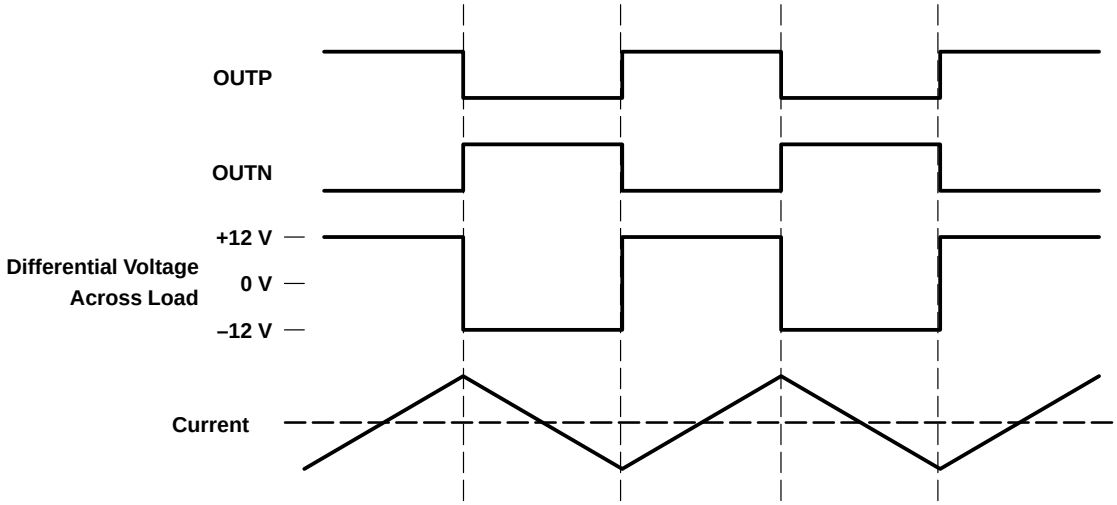


Figure 23. Traditional Class-D Modulation Scheme's Output Voltage and Current Waveforms Into an Inductive Load With No Input

TPA3000D1 modulation scheme

The TPA3000D1 uses a modulation scheme that still has each output switching from 0 to the supply voltage. However, OUTP and OUTN are now in phase with each other with no input. The duty cycle of OUTP is greater than 50% and OUTN is less than 50% for positive output voltages. The duty cycle of OUTP is less than 50% and OUTN is greater than 50% for negative output voltages. The voltage across the load sits at 0 V throughout most of the switching period, greatly reducing the switching current, which reduces any I^2R losses in the load.

APPLICATION INFORMATION

TPA3000D1 modulation scheme (continued)

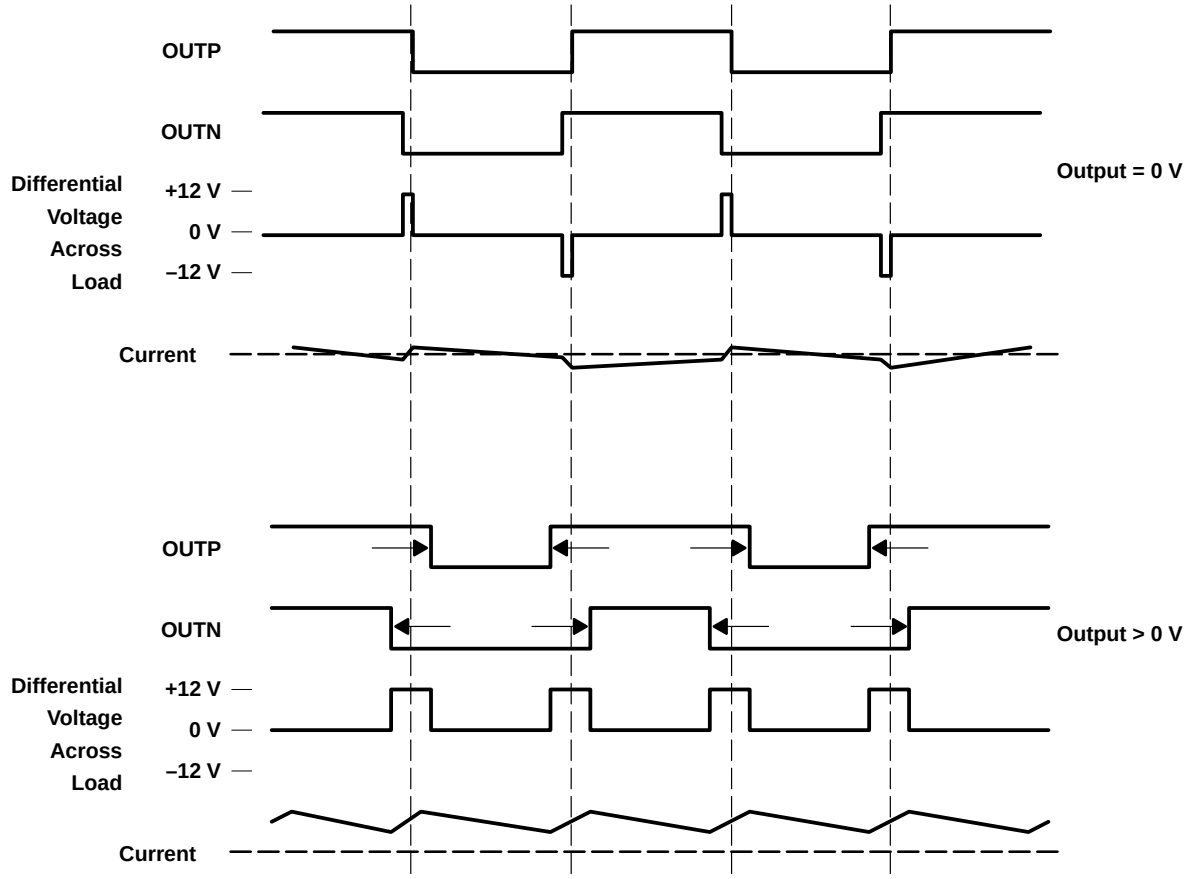


Figure 24. The TPA3000D1 Output Voltage and Current Waveforms Into an Inductive Load

efficiency: filter required with the traditional class-D modulation scheme

The main reason that the traditional class-D amplifier needs an output filter is that the switching waveform results in maximum current flow. This causes more loss in the load, which causes lower efficiency. The ripple current is large for the traditional modulation scheme, because the ripple current is proportional to voltage multiplied by the time at that voltage. The differential voltage swing is $2 \times V_{CC}$, and the time at each voltage is half the period for the traditional modulation scheme. An ideal LC filter is needed to store the ripple current from each half cycle for the next half cycle, while any resistance causes power dissipation. The speaker is both resistive and reactive, whereas an LC filter is almost purely reactive.

The TPA3000D1 modulation scheme has very little loss in the load without a filter because the pulses are very short and the change in voltage is V_{CC} instead of $2 \times V_{CC}$. As the output power increases, the pulses widen, making the ripple current larger. Ripple current could be filtered with an LC filter for increased efficiency, but for most applications the filter is not needed.

An LC filter with a cutoff frequency less than the class-D switching frequency allows the switching current to flow through the filter instead of the load. The filter has less resistance than the speaker, which results in less power dissipation, therefore increasing efficiency.

APPLICATION INFORMATION

effects of applying a square wave into a speaker

Audio specialists have advised for years not to apply a square wave to speakers. If the amplitude of the waveform is high enough and the frequency of the square wave is within the bandwidth of the speaker, the square wave could cause the voice coil to jump out of the air gap and/or scar the voice coil. A 250-kHz switching frequency, however, does not significantly move the voice coil, as the cone movement is proportional to $1/f^2$ for frequencies beyond the audio band.

Damage may occur if the voice coil cannot handle the additional heat generated from the high-frequency switching current. The amount of power dissipated in the speaker may be estimated by first considering the overall efficiency of the system. If the on-resistance ($r_{ds(on)}$) of the output transistors is considered to cause the dominant loss in the system, then the maximum theoretical efficiency for the TPA3000D1 with an 8-Ω load is as follows:

$$\text{Efficiency (theoretical, \%)} = R_L / \left(R_L + r_{ds(on)} \right) \times 100\% = 8/(8 + 0.4) \times 100\% = 95.24\% \quad (1)$$

The maximum measured output power is approximately 17 W with an 18-V power supply. The total theoretical power supplied ($P_{(total)}$) for this worst-case condition would therefore be as follows:

$$P_{(total)} = P_O / \text{Efficiency} = 17 \text{ W} / 0.9524 = 17.85 \text{ W} \quad (2)$$

The efficiency measured in the lab using an 8-Ω speaker was 89%. The power not accounted for as dissipated across the $r_{ds(on)}$ may be calculated by simply subtracting the theoretical power from the measured power:

$$\text{Other losses} = P_{(total)}\text{(measured)} - P_{(total)}\text{ (theoretical)} = 19.1 - 17.85 = 1.25 \text{ W} \quad (3)$$

The quiescent supply current at 18 V is measured to be 9.8 mA. It can be assumed that the quiescent current encapsulates all remaining losses in the device, i.e., biasing and switching losses. It may be assumed that any remaining power is dissipated in the speaker and is calculated as follows:

$$P_{(dis)} = 1.25 \text{ W} - (18 \text{ V} \times 9.8 \text{ mA}) = 1.07 \text{ W} \quad (4)$$

Note that these calculations are for the worst-case condition of 17 W delivered to the speaker. Since the 1.07 W is only 6.3% of the power delivered to the speaker, it may be concluded that the amount of power actually dissipated in the speaker is relatively insignificant. Furthermore, this power dissipated is well within the specifications of most loudspeaker drivers in a system, as the power rating is typically selected to handle the power generated from a clipping waveform.

when to use an output filter

Design the TPA3000D1 without the filter if the traces from amplifier to speaker are short. Powered speakers, where the speaker is in the same enclosure as the amplifier, is a typical application for class-D without a filter.

A ferrite bead filter may be used if the design is failing radiated emissions without a filter, or if a frequency sensitive circuit is operating higher than 1 MHz. The ferrite filter reduces EMI around 1 MHz and higher (FCC and CE only test radiated emissions greater than 30 MHz). When selecting a ferrite bead, choose one with high impedance at high frequencies, but very low impedance at low frequencies.

Use a LC output filter if there are low frequency (<1 MHz) EMI sensitive circuits and/or there are long wires from the amplifier to the speaker.

APPLICATION INFORMATION

when to use an output filter (continued)

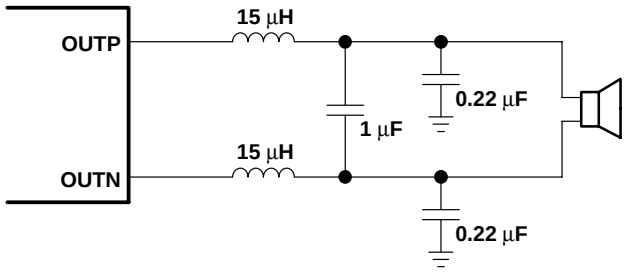


Figure 25. Typical LC Output Filter, Cutoff Frequency of 41 kHz

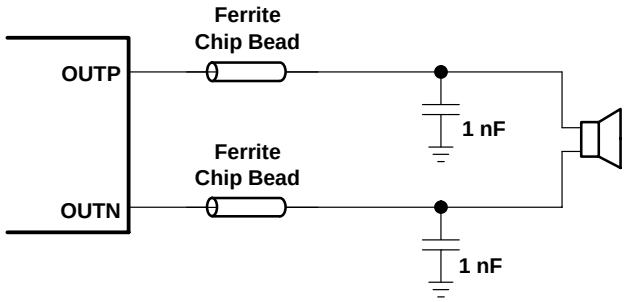


Figure 26. Typical Ferrite Chip Bead Filter (Chip bead example: Fair-Rite 2512067007Y3)

gain setting via GAIN0 and GAIN1 inputs

The gain of the TPA3000D1 is set by two input terminals, GAIN0 and GAIN1.

The gains listed in Table 1 are realized by changing the taps on the input resistors inside the amplifier. This causes the input impedance (Z_i) to be dependent on the gain setting. The actual gain settings are controlled by ratios of resistors, so the actual gain distribution from part-to-part is quite good. However, the input impedance may shift by 30% due to shifts in the actual resistance of the input resistors.

For design purposes, the input network (discussed in the next section) should be designed assuming an input impedance of 23 kΩ, which is the absolute minimum input impedance of the TPA3000D1. At the lower gain settings, the input impedance could increase as high as 313 kΩ.

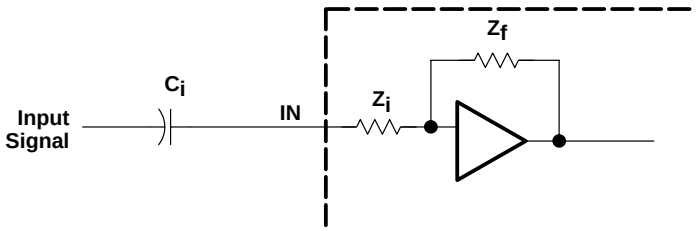
Table 1. Gain Settings

GAIN0	GAIN1	AMPLIFIER GAIN (dB)	INPUT IMPEDANCE (kΩ)
		TYP	TYP
0	0	12	241
0	1	18	168
1	0	23.5	104
1	1	36	33

APPLICATION INFORMATION

input resistance

Each gain setting is achieved by varying the input resistance of the amplifier, which can range from its smallest value to over six times that value. As a result, if a single capacitor is used in the input high-pass filter, the –3 dB or cutoff frequency also changes by over six times.



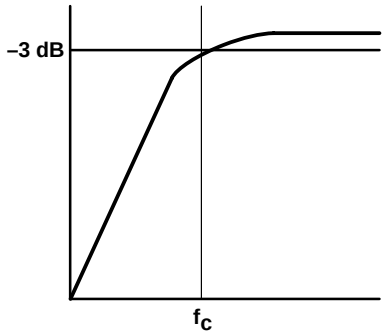
The –3-dB frequency can be calculated using equation 5.

$$f = \frac{1}{2\pi Z_i C_i} \tag{5}$$

input capacitor, C_i

In the typical application an input capacitor (C_i) is required to allow the amplifier to bias the input signal to the proper dc level for optimum operation. In this case, C_i and the input impedance of the amplifier (Z_i) form a high-pass filter with the corner frequency determined in equation 6.

$$f_c = \frac{1}{2\pi Z_i C_i} \tag{6}$$



The value of C_i is important, as it directly affects the bass (low frequency) performance of the circuit. Consider the example where Z_i is 241 kΩ and the specification calls for a flat bass response down to 20 Hz. Equation 6 is reconfigured as equation 7.

$$C_i = \frac{1}{2\pi Z_i f_c} \tag{7}$$

In this example, C_i is 33 nF, so one would likely choose a value of 0.1 μF as this value is commonly used. If the gain is known and will be constant, use Z_i from Table 1 to calculate C_i. A further consideration for this capacitor is the leakage path from the input source through the input network (C_i) and the feedback network to the load. This leakage current creates a dc offset voltage at the input to the amplifier that reduces useful headroom, especially in high gain applications. For this reason a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications as the dc level there is held at 2.5 V, which is likely higher than the source dc level. Note that it is important to confirm the capacitor polarity in the application.

APPLICATION INFORMATION

power supply decoupling, C_S

The TPA3000D1 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents oscillations for long lead lengths between the amplifier and the speaker. The optimum decoupling is achieved by using two capacitors of different types that target different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1 μF placed as close as possible to the device V_{CC} lead works best. For filtering lower-frequency noise signals, a larger aluminum electrolytic capacitor of 10 μF or greater placed near the audio power amplifier is recommended.

BSN and BSP capacitors

The full H-bridge output stage uses only NMOS transistors. It therefore requires bootstrap capacitors for the high side of each output to turn on correctly. A 10-nF ceramic capacitor, rated for at least 25 V, must be connected from each output to its corresponding bootstrap input. Specifically, one 10-nF capacitor must be connected from OUTP to BSP, and one 10-nF capacitor must be connected from OUTN to BSN. (See the evaluation circuit diagram at the end of this data sheet.)

VCLAMP capacitors

To ensure that the maximum gate-to-source voltage for the NMOS output transistors is not exceeded, an internal regulator clamps the gate voltage. A 0.1-μF capacitor must be connected from VCLAMP (pin 7) to ground and must be rated for at least 25 V. The voltage at VCLAMP (pin 7) varies with V_{CC} and may not be used for powering any other circuitry.

midrail bypass capacitor, C_{BYPASS}

The midrail bypass capacitor (C_{BYPASS}) is the most critical capacitor and serves several important functions. During start-up or recovery from shutdown mode, C_{BYPASS} determines the rate at which the amplifier starts up. The second function is to reduce noise produced by the power supply caused by coupling into the output drive signal. This noise is from the midrail generation circuit internal to the amplifier, which appears as degraded PSRR and THD+N.

Bypass capacitor (C_{BYPASS}) values of 0.47-μF to 1-μF ceramic or tantalum low-ESR capacitors are recommended for the best THD noise, and depop performance.

VREF decoupling capacitor

The VREF terminal (pin 23) is the output of an internally-generated 5-V supply, used for the oscillator and gain setting logic. It requires a 0.1-μF to 1-μF capacitor to ground to keep the regulator stable. The regulator may not be used to power any additional circuitry.

differential input

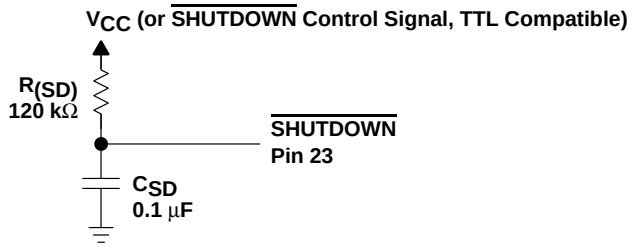
The differential input stage of the amplifier cancels any noise that appears on both input lines of the channel. To use the TPA3000D1 EVM with a differential source, connect the positive lead of the audio source to the INP input and the negative lead from the audio source to the INN input. To use the TPA3000D1 with a single-ended source, ac ground the INN input through a capacitor and apply the audio single to the input. In a single-ended input application, the INN input should be ac-grounded at the audio source instead of at the device input for best noise performance.

,APPLICATION INFORMATION

$\overline{\text{SHUTDOWN}}$ operation

The TPA3000D1 employs a shutdown mode of operation designed to reduce supply current (I_{CC}) to the absolute minimum level during periods of nonuse for battery-power conservation. The $\overline{\text{SHUTDOWN}}$ input terminal should be held high during normal operation when the amplifier is in use. Pulling $\overline{\text{SHUTDOWN}}$ low causes the outputs to mute and the amplifier to enter a low-current state, $I_{CC(SD)}$ = 1 μA. $\overline{\text{SHUTDOWN}}$ should never be left unconnected, because amplifier operation would be unpredictable.

Ideally, the device should be held in shutdown when the system powers up and brought out of shutdown once any digital circuitry has settled. However, if $\overline{\text{SHUTDOWN}}$ is to be left unused or if the device is to be powered up with $\overline{\text{SHUTDOWN}}$ held high, the circuit below should be used.



The values for R_{SD} and C_{SD} should be chosen for a time constant ($\tau = R_{SD}C_{SD}$) of at least 10 ms for proper operation. The maximum output current of the $\overline{\text{SHUTDOWN}}$ control signal source must not be exceeded.

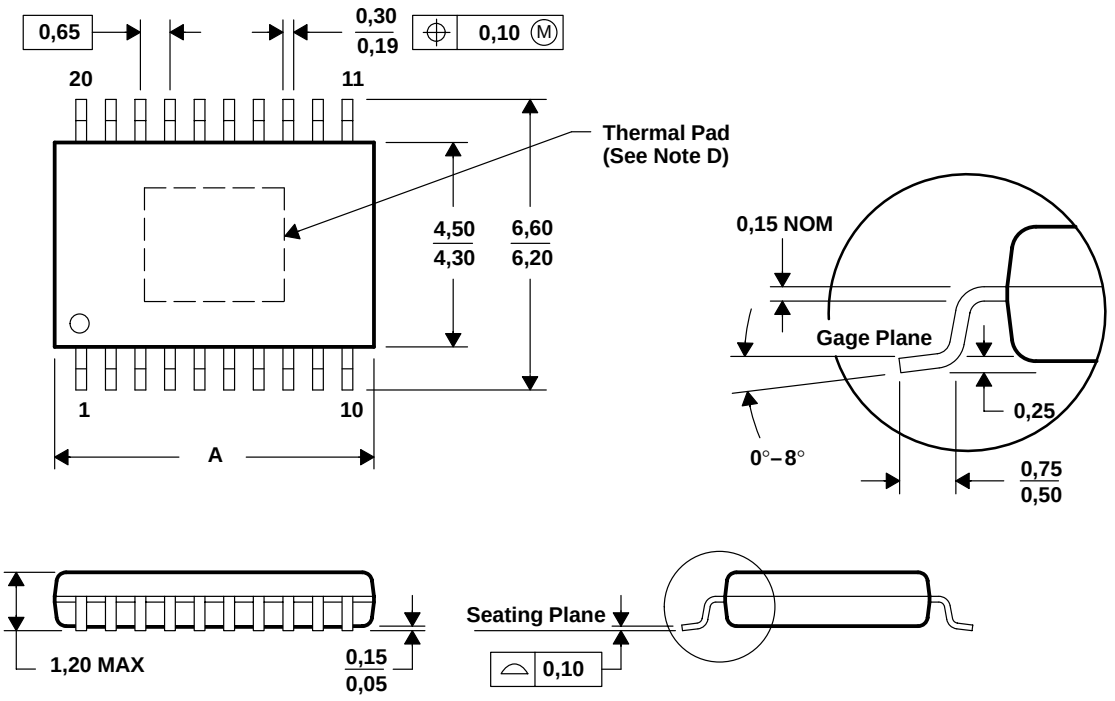
using low-ESR capacitors

Low-ESR capacitors are recommended throughout this application section. A real (as opposed to ideal) capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this resistor minimizes the beneficial effects of the capacitor in the circuit. The lower the equivalent value of this resistance the more the real capacitor behaves like an ideal capacitor.

MECHANICAL DATA

PWP (R-PDSO-G)** **PowerPAD™ PLASTIC SMALL-OUTLINE**

20 PINS SHOWN



DIM \ PINS **	14	16	20	24	28
A MAX	5,10	5,10	6,60	7,90	9,80
A MIN	4,90	4,90	6,40	7,70	9,60

4073225/F 10/98

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions.
D. The package thermal performance may be enhanced by bonding the thermal pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected leads.
E. Falls within JEDEC MO-153

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