

TOSHIBA Transistor Silicon PNP Epitaxial Type

TPCP8603

High-Speed Switching Applications

DC/DC Converters

Strobe Applications

Unit: mm

- High DC current gain: $h_{FE} = 120 \sim 300$ ($I_C = -0.1$ A)
- Low collector-emitter saturation voltage: $V_{CE(sat)} = -0.2$ V (max)
- High-speed switching: $t_f = 120$ ns (typ.)

Absolute Maximum Ratings (Ta = 25°C)

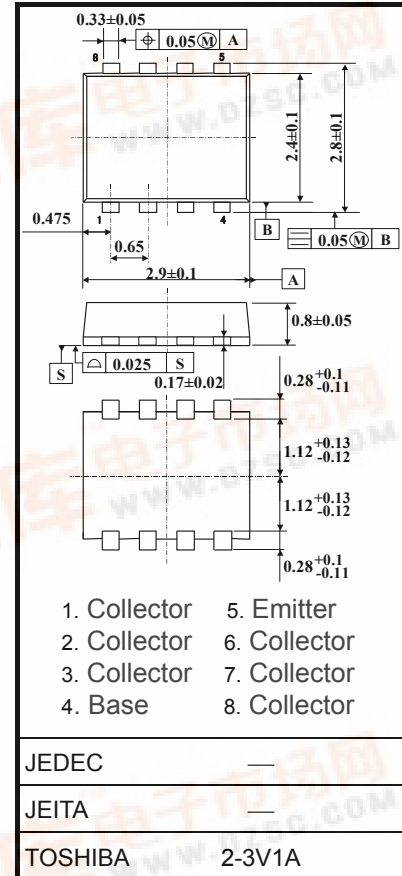
Characteristic	Symbol	Rating	Unit	
Collector-base voltage	V_{CBO}	-120	V	
Collector-emitter voltage	V_{CEO}	-120	V	
Collector-emitter voltage	V_{EBO}	-7	V	
Collector current	DC (Note 1)	I_C	-1.0	A
	Pulsed (Note 1)	I_{CP}	-2.0	A
Base current	I_B	0.1	A	
Collector power dissipation	t = 10 s	P_C (Note 2)	3.00	W
	DC		1.25	W
Junction temperature	T_j	150	°C	
Storage temperature range	T_{stg}	-55~150	°C	

Note 1: Ensure that the channel temperature does not exceed 150°C during use of the device.

Note 2: Mounted on the FR4 board (glass-epoxy; 1.6 mm thick; Cu area, 645 mm²)

Note 3: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/Derating Concept and Methods) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).



Weight: 0.017 g (typ.)

Figure 1. Circuit Configuration

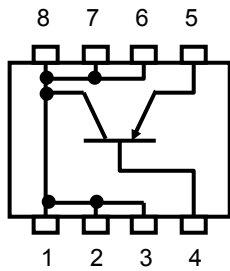
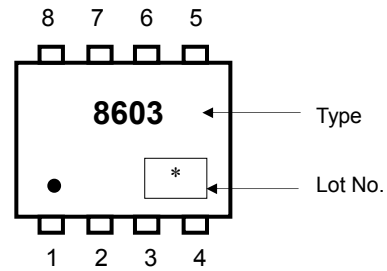
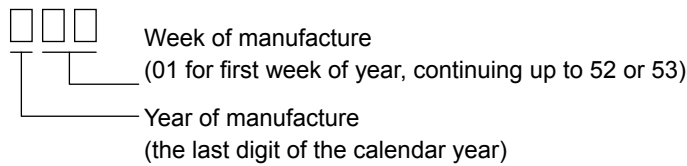


Figure 2. Marking (Note4)



Note 4: ● on the lower left of the marking indicates Pin 1.

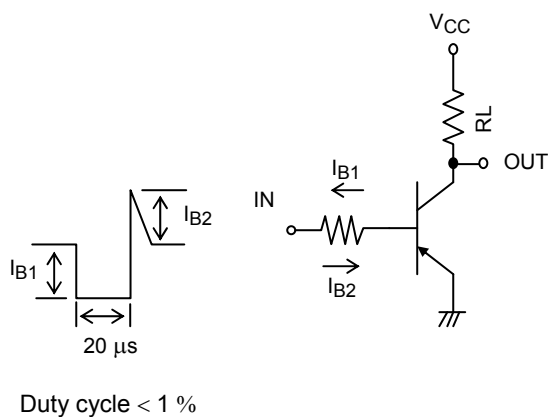
* Weekly code (three digits):

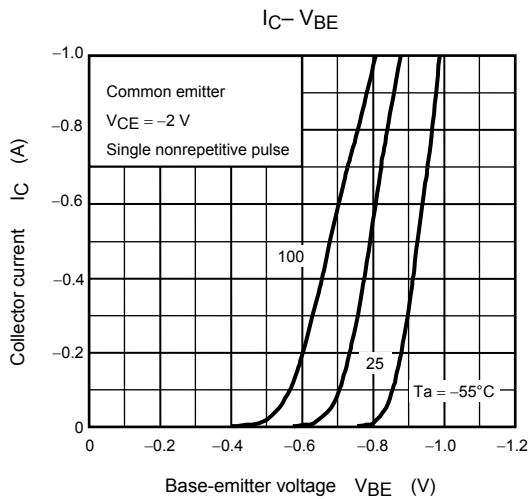
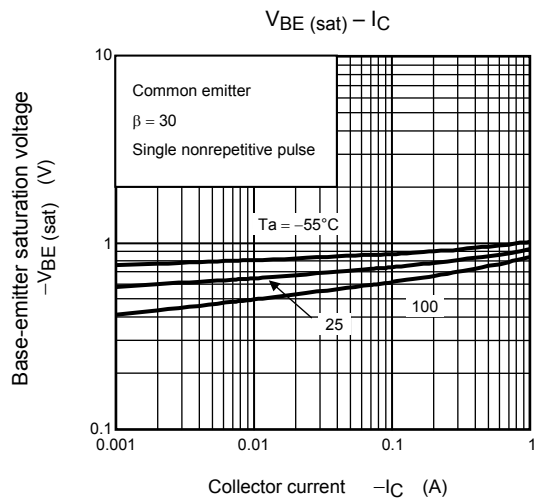
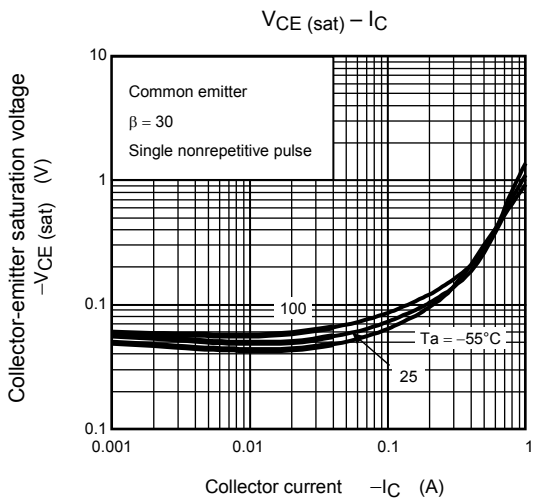
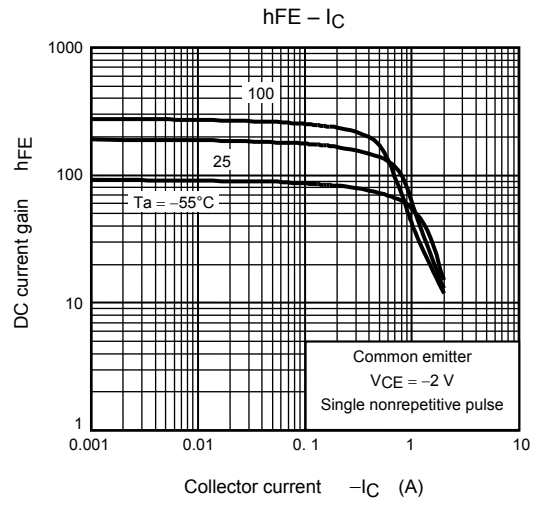
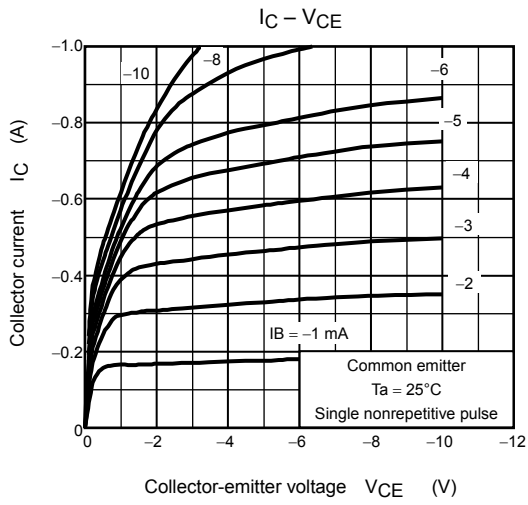


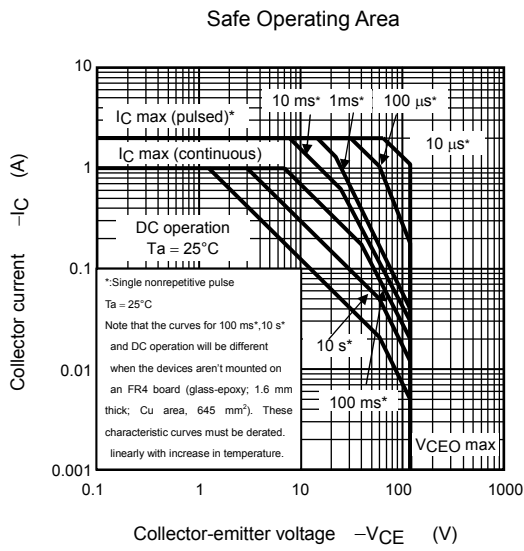
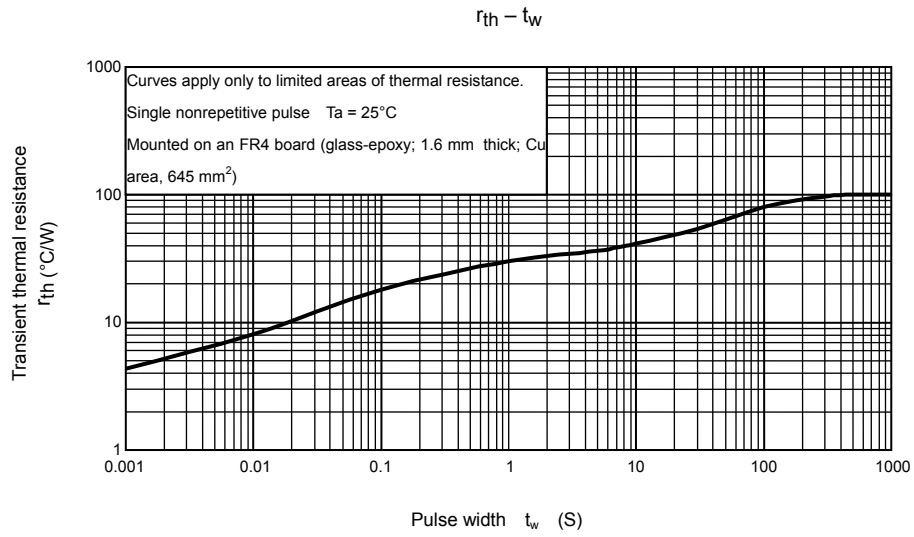
Electrical Characteristics (Ta = 25°C)

Characteristic		Symbol	Test Condition	Min	Typ.	Max	Unit
Collector cutoff current		I_{CBO}	$V_{CB} = -120\text{ V}, I_E = 0$	—	—	-100	nA
Emitter cutoff current		I_{EBO}	$V_{EB} = -7\text{ V}, I_C = 0$	—	—	-100	nA
Collector-emitter breakdown voltage		$V_{(BR)CEO}$	$I_C = -10\text{ mA}, I_B = 0$	-120	—	—	V
DC current gain		$h_{FE(1)}$	$V_{CE} = -2\text{ V}, I_C \cong -0.1\text{ A}$	120	—	300	
		$h_{FE(2)}$	$V_{CE} = -2\text{ V}, I_C \cong -0.3\text{ A}$	60	—	—	
Collector-emitter saturation voltage		$V_{CE(sat)}$	$I_C = -0.3\text{ A}, I_B = -0.01\text{ A}$	—	—	-0.2	V
Base-emitter saturation voltage		$V_{BE(sat)}$	$I_C = -0.3\text{ A}, I_B = -0.01\text{ A}$	—	—	-1.1	V
Switching time	Storage time	t_r	See Figure 3 circuit diagram.	—	130	—	ns
	Storage time	t_{stg}	$V_{CC} \cong 72\text{ V}, R_L = 240\ \Omega$	—	650	—	
	Fall time	t_f	$-I_{B1} = I_{B2} = -10\text{ mA}$	—	120	—	

Figure 3. Switching Time Test Circuit & Timing Chart







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20070701-EN

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