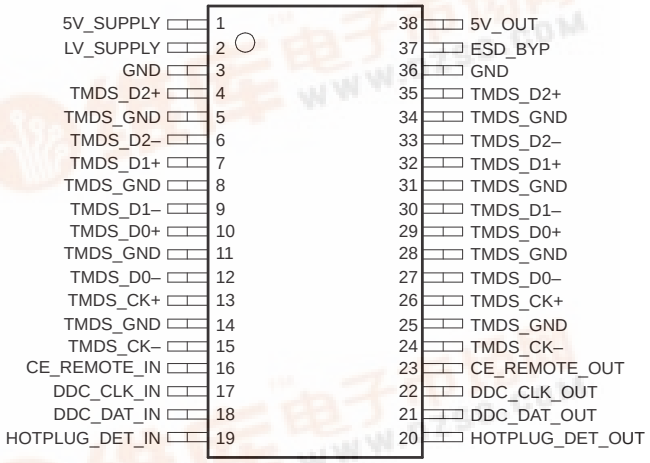
FEATURES

- **Single-Chip ESD Solution for High-Definition Multimedia Interface (HDMI) Driver**
- **0.9 pF Capacitance for High-Speed Transition Minimized Differential Signaling (TMDS) Lines**
- **0.05-pF Matching Capacitance Between the Differential Signal Pair**
- **Integrated Level Shifting for the Control Lines**
- **±8-kV Contact ESD Protection on External Lines**
- **38-Pin Thin Shrink Small-Outline Package (TSSOP) Provides Seamless Layout Option With HDMI Connector**
- **Backdrive Protection**
- **Lead-Free Package**
- **On-Chip Current Regulator With 55-mA Current Output**

DBT PACKAGE
(TOP VIEW)



APPLICATIONS

- **PCs**
- **Consumer Electronics**
- **Set-Top Boxes**
- **DVDRW Players**

DESCRIPTION/ORDERING INFORMATION

The TPD12S521 is a single-chip ESD solution for the high-definition multimedia interface (HDMI) transmitter port. In many cases, the core ICs, such as the scalar chipset, may not have robust ESD cells to sustain system-level ESD strikes. In these cases, the TPD12S521 provides the desired system level ESD protection, such as the the IEC61000-4-2 (Level 4) ESD, by absorbing the energy associated with the ESD strike.

While providing the ESD protection, the TPD12S521 adds little or no additional glitch in the high-speed differential signals (see Figure 3 and Figure 4). The high-speed transition minimized differential signaling (TMDS) lines add only 0.9 pF capacitance to the lines. In addition, the monolithic integrated circuit technology ensures that there is excellent matching between the two-signal pair of the differential line. This is a direct advantage over discrete ESD clamp solutions where variations between two different ESD clamps may significantly degrade the differential signal quality.

The low-speed control lines offer voltage-level shifting to eliminate the need for an external voltage level-shifter IC. The control line ESD clamps add 3.5 pF capacitance to the control lines. The 38-pin DBT package offers seamless layout routing option to eliminate the routing glitch for the differential signal pair.

The TPD12S521 provides an on-chip regulator with current output ratings of 55 mA at pin 38. Maximum overcurrent protection output drop at 55 mA on 5V_OUT is 100 mV. This current enables the HDMI receiver detection even when the receiver device is powered-off. DBT package pitch (0.5 mm) matches with HDMI connector pitch. In addition, pin mapping follows the same order as the HDMI connector pin mapping. This HDMI receiver port protection and interface device is specifically designed for next-generation HDMI transmitter protection.

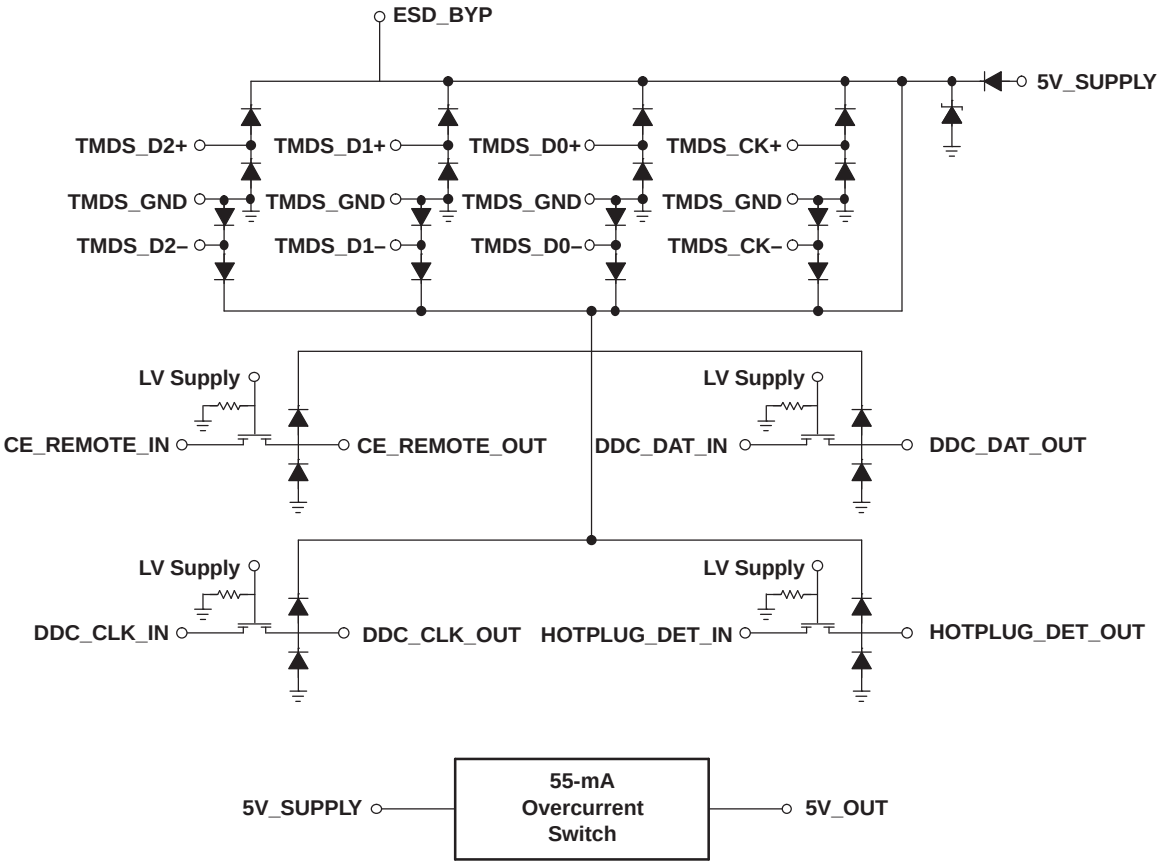
PRODUCT PREVIEW

ORDERING INFORMATION

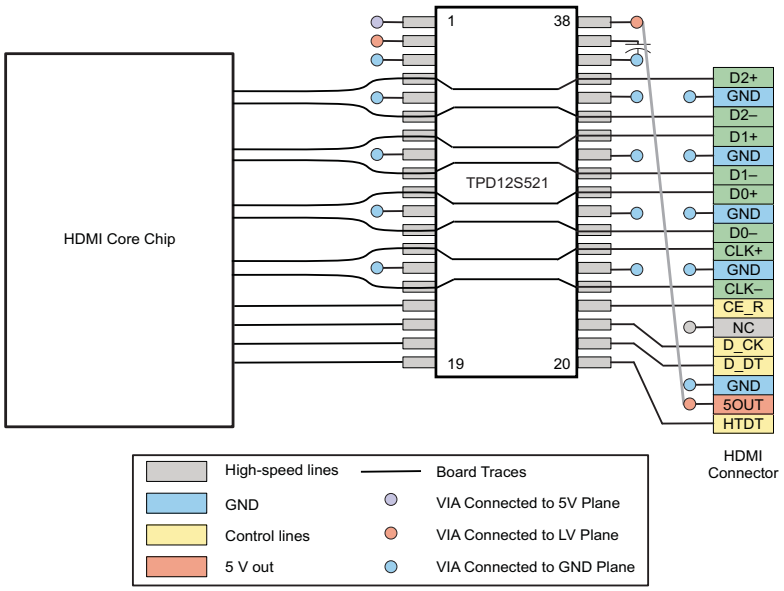
T_A	PACKAGE(1)(2)	STANDARD FINISH		LEAD-FREE FINISH	
		ORDERABLE PART NUMBER(3)	TOP-SIDE MARKING	ORDERABLE PART NUMBER(3)	TOP-SIDE MARKING
–40°C to 85°C	TSSOP-38	TPD12S521DBTR	PREVIEW	TPD12S521DBTR	PREVIEW

(1) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(3) Parts are shipped in tape-and-reel form, unless otherwise specified.

ELECTRICAL SCHEMATIC



PRODUCT PREVIEW



A. External bypass capacitors and resistor components not included

Figure 1. Board Layout for HDMI Transmitter Using TPD12S521DBTR

PIN DESCRIPTION

PIN NO.	NAME	DESCRIPTION
4, 35	TMDS_D2+	TMDS 0.9-pF ESD protection(1)
6, 33	TMDS_D2–	TMDS 0.9-pF ESD protection(1)
7, 32	TMDS_D1+	TMDS 0.9-pF ESD protection(1)
9, 30	TMDS_D1–	TMDS 0.9-pF ESD protection(2)
10, 29	TMDS_D0+	TMDS 0.9-pF ESD protection(2)
12, 27	TMDS_D0–	TMDS 0.9-pF ESD protection(2)
13, 26	TMDS_CK+	TMDS 0.9-pF ESD protection(2)
15, 24	TMDS_CK–	TMDS 0.9-pF ESD protection(2)
16	CE_REMOTE_IN	LV_SUPPLY referenced logic level in
23	CE_REMOTE_OUT	5V_SUPPLY referenced logic level out, plus 3.5-pF ESD
17	DDC_CLK_IN	LV_SUPPLY referenced logic level in
22	DDC_CLK_OUT	5V_SUPPLY referenced logic level out, plus 3.5-pF ESD
18	DDC_DAT_IN	LV_SUPPLY referenced logic level in
21	DDC_DAT_OUT	5V_SUPPLY referenced logic level out, plus 3.5-pF ESD
19	HOTPLUG_DET_IN	LV_SUPPLY referenced logic level in
20	HOTPLUG_DET_OUT	5V_SUPPLY referenced logic level out, plus 3.5-pF ESD
2	LV_SUPPLY	Bias for CE/DDC/HOTPLUG level shifters
1	5V_SUPPLY	Current source for 5V_OUT
38	5V_OUT	55-mA minimum overcurrent protected 5-V output. This output must be bypassed with a 0.1-µF ceramic capacitor.
37	ESD_BYP	ESD bypass. This pin must be connected to a 0.1-µF ceramic capacitor.
3, 5, 8, 11, 14, 25, 28, 31, 34, 36	GND/TMDS_GND	GND reference

(1) These two pins must be connected together inline on the PCB.
(2) These two pins must be connected together inline on the PCB.

PRODUCT PREVIEW

Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC5} V_{CC3}			6	V
	DC voltage at any channel input	GND – 0.5	V_{CC} + 0.5	V
T_{stg}	Storage temperature range	–65	150	°C

Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
Operating supply voltage	5V_SUPPLY		5	5.5	V
Bias supply voltage	LV_SUPPLY	1	3.3	5.5	V
Operating temperature range		–40		85	°C

PRODUCT PREVIEW

Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
I_{CC5}	Operating supply current	5V_SUPPLY = 5 V				110	130	µA
I_{CC3}	Bias supply current	LV_SUPPLY = 3.3 V				1	5	µA
V_{DROP}	5V_OUT overcurrent output drop	5V_SUPPLY = 5 V, I_{OUT} = 55 mA				65	100	mV
I_{SC}	5V_OUT short-circuit current limit	5V_SUPPLY= 5 V, 5V_OUT = GND			90	135	175	mA
I_{OFF}	OFF-state leakage current, level-shifting NFET	LV_SUPPLY = 0 V				0.1	5	µA
$I_{BACKDRIVE}$	Current conducted from output pins to V_SUPPLY rails when powered down	5V_SUPPLY < V_{CH_OUT}	TMDS_D[2:0]+/–, TMDS_CK+/–, CE_REMOTE_OUT, DDC_DAT_OUT, DDC_CLK_OUT, HOTPLUG_DET_OUT, 5V_OUT			0.1	5	µA
V_{ON}	Voltage drop across level-shifting NFET when ON	LV_SUPPLY = 2.5 V, V_S = GND, I_{DS} = 3 mA			75	95	140	mV
V_F	Diode forward voltage	I_F = 8 mA, T_A = 25°C(1)	Top diode		0.6	0.85	0.95	V
			Bottom diode		0.6	0.85	0.95	
V_{ESD}	ESD withstand voltage	Pins 4, 7, 10, 13, 20–24, 27, 30, 33(1)(2)		IEC	±8			kV
		Pins 1, 2, 16–19, 37, 38(1)(3)		HBM	±2			
V_{CL}	Channel clamp voltage at 8-kV HBM ESD	T_A = 25°C(1)(3)	Positive transients			9		V
			Negative transients			–9		
R_{DYN}	Dynamic resistance	I = 1 A, T_A = 25°C(4)	Positive transients			3		Ω
			Negative transients			1.5		
I_{LEAK}	TMDS channel leakage current	T_A = 25°C(1)				0.01	1	µA
C_{IN}, TMDS	TMDS channel input capacitance	5V_SUPPLY= 5 V, Measured at 1 MHz, V_{BIAS} = 2.5 V(1)				0.9	1.1	pF
ΔC_{IN}, TMDS	TMDS channel input capacitance matching	5V_SUPPLY= 5 V, Measured at 1 MHz, V_{BIAS} = 2.5 V(1)(5)				0.05		pF
C_{MUTUAL}	Mutual capacitance between signal pin and adjacent signal pin	5V_SUPPLY= 0 V, Measured at 1 MHz, V_{BIAS} = 2.5 V(1)				0.07		pF
C_{IN}	Level-shifting input capacitance, capacitance to GND	5V_SUPPLY= 0 V, Measured at 100 KHz, V_{BIAS} = 2.5 V(1)		DDC		3.5	4	pF
				CEC		3.5	4	
				HP		3.5	4	

(1) This parameter is specified by design and verified by device characterization.
(2) Standard IEC 61000-4-2, $C_{DISCHARGE}$ = 150 pF, $R_{DISCHARGE}$ = 330 Ω
(3) Human-Body Model (HBM) per MIL-STD-883, Method 3015, $C_{DISCHARGE}$ = 100 pF, $R_{DISCHARGE}$ = 1.5 kΩ
(4) These measurements performed with no external capacitor on ESD_BYP.
(5) Intrapair matching, each TMDS pair (i.e., D+, D–)

PRODUCT PREVIEW

TYPICAL PERFORMANCE

Typical Filter Performance (T_A = 25°C, DC Bias = 0 V, 50-Ω Environment)

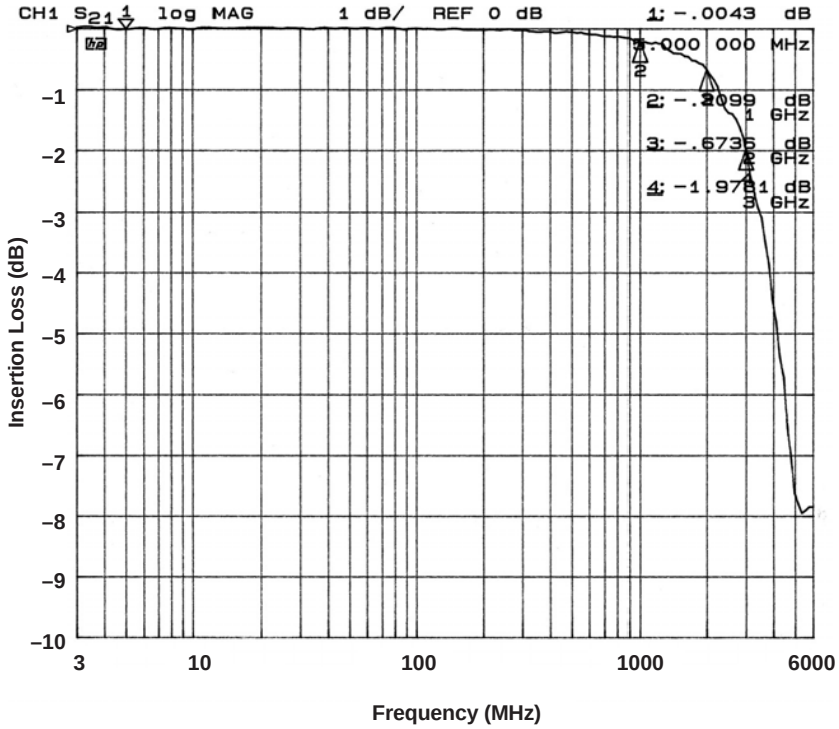


Figure 2. Insertion Loss vs Frequency (TMDS_D1– to GND)

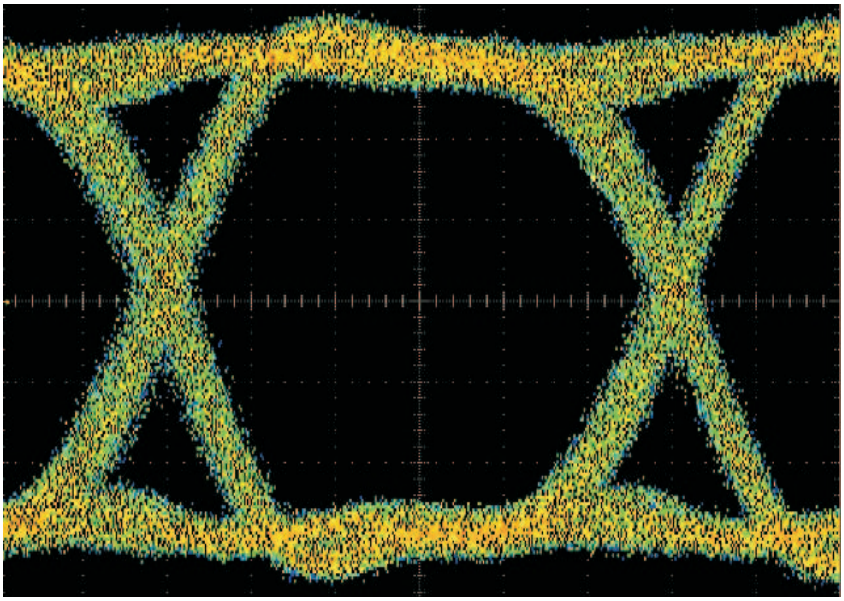


Figure 3. Eye Diagram With TPD12S521

TYPICAL PERFORMANCE (continued)

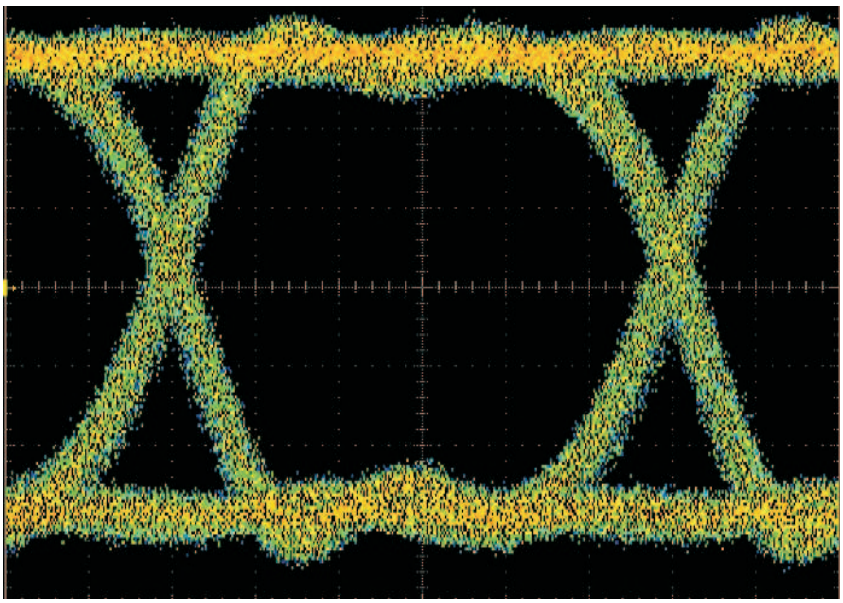


Figure 4. Eye Diagram Without TPD12S521

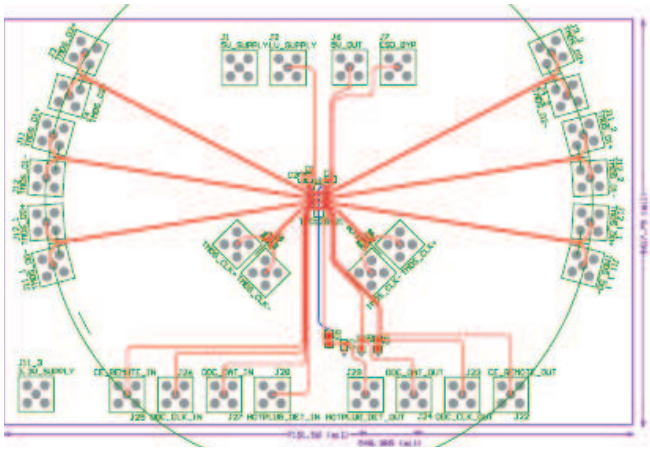


Figure 5. Test Board to Measure Eye Diagram for the TPD12S521 (Refer to Eye Diagram Plot)

PRODUCT PREVIEW

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