

FEATURES

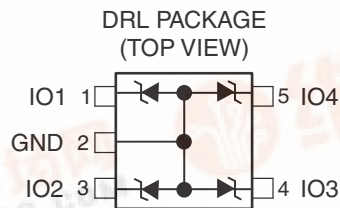
- Four Unidirectional Voltage Suppression Diodes for use in ESD Protection
- I/O Breakdown Voltage, $V_{BR} = 6.1 \text{ V Min}$
- Low I/O Capacitance (11 pF at 0 V)
- Low I/O Leakage Current <100 nA
- No Power Supply Routing is Required since there is no V_{DD} Pin
- Very Small Printed Circuit Board (PCB) Area <2.6 mm²
- ESD Protection Exceeds
 - ±15-kV Human Body Model (HBM)
 - ±15-kV IEC 61000-4-2 Contact Discharge

APPLICATIONS

- Where Transient Overvoltage Protection in ESD-Sensitive Equipment is Required, Such as:
 - Computers
 - Printers
 - Communication Systems and Cellular Phones
 - Video Equipment

BENEFITS

- High ESD Protection Level
- High Integration
- Suitable for High-Density Boards



DESCRIPTION/ORDERING INFORMATION

The TPD4E002 is a monolithic array designed to protect up to four lines against ESD transients. Monolithic circuit design allows superior matching between the channels and reduced crosstalk. This device is ideal for applications where both reduced line capacitance and board space-saving are required.

ORDERING INFORMATION

T_A	PACKAGE ⁽¹⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 125°C	1.6 × 1.6 DRL	Reel of 4000	TPD4E002DRLR	28S

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

Absolute Maximum Ratings

		MIN	MAX	UNIT
V_{PP} ESD discharge	Human Body Model (HBM)		±15	kV
	IEC 61000-4-2 Contact Discharge		±15	
T_J Junction temperature			125	°C
T_{stg} Storage temperature range		–55	150	°C
T_{op} Operating temperature range		–40	125	°C

Thermal Resistance

PARAMETER		VALUE	UNIT
$R_{\theta JA}$	Junction to ambient on printed circuit on recommended pad layout	220	°C/W

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

TPD4E002
QUAD LOW-CAPACITANCE ARRAY
WITH ±15-kV ESD PROTECTION



SLVS615B–JULY 2006–REVISED MARCH 2007

Electrical Characteristics

T_{amb} = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{BR}	I/O Breakdown voltage	I _R = 1 mA	6.1		7.2	V
I _{RM}	I/O Leakage current	V _{RM} = 3 V			0.1	μA
αT	Voltage temperature coefficient			45		10 ⁻⁴ /°C
C	I/O Capacitance per line			11		pF
R _d	Dynamic resistance ⁽¹⁾			2		Ω

(1) R_d is measured under reverse breakdown condition with inrush current in the range 1Amps using pulse technique

TYPICAL CHARACTERISTICS

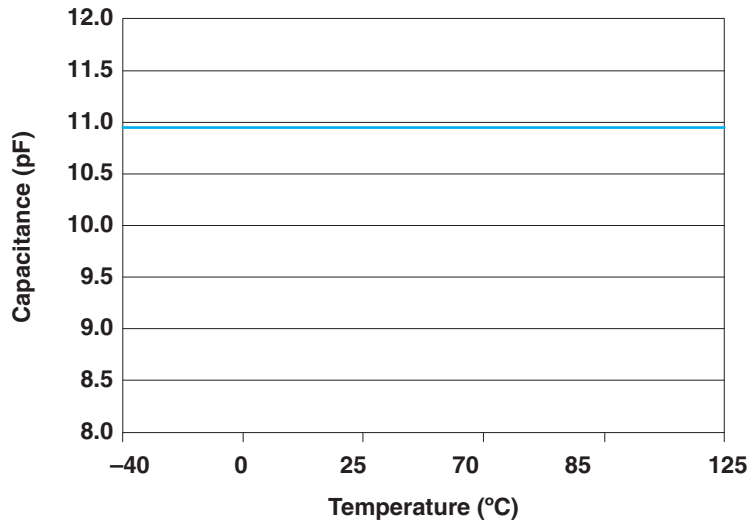


Figure 1. I/O Capacitance vs Temperature

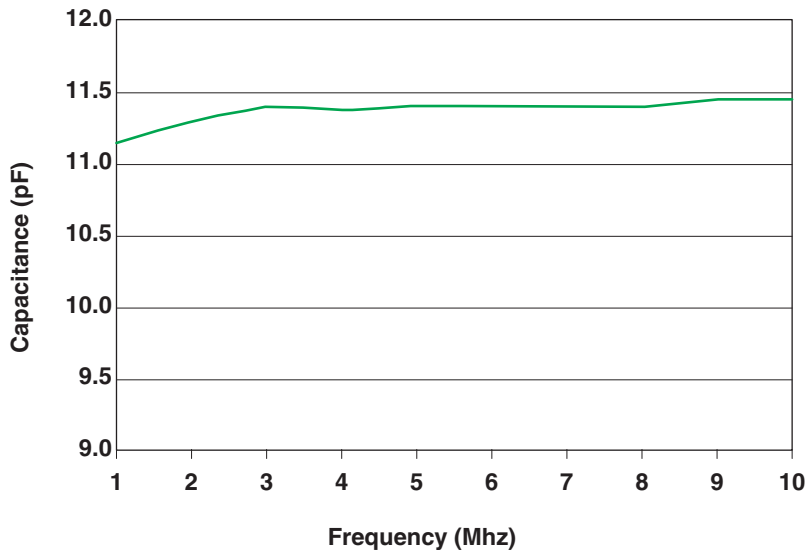


Figure 2. I/O Capacitance vs Frequency (Typical Values)

TYPICAL CHARACTERISTICS (continued)

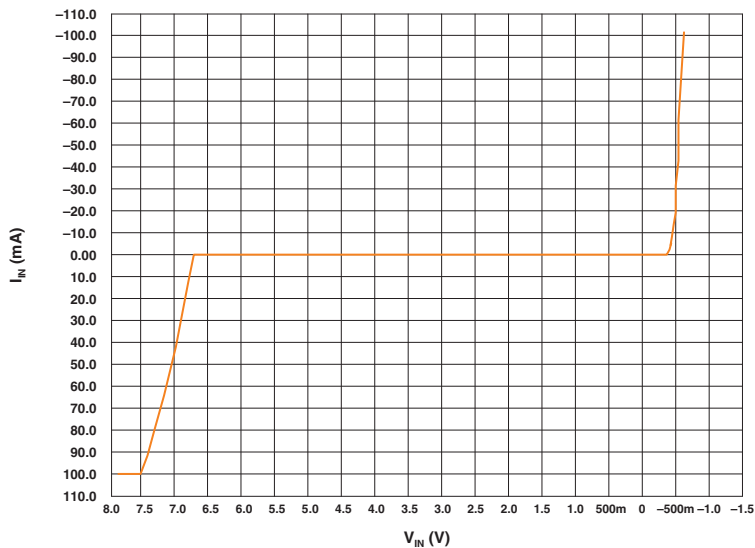


Figure 3. Diode Current Across I/O Voltage (Typical Values)

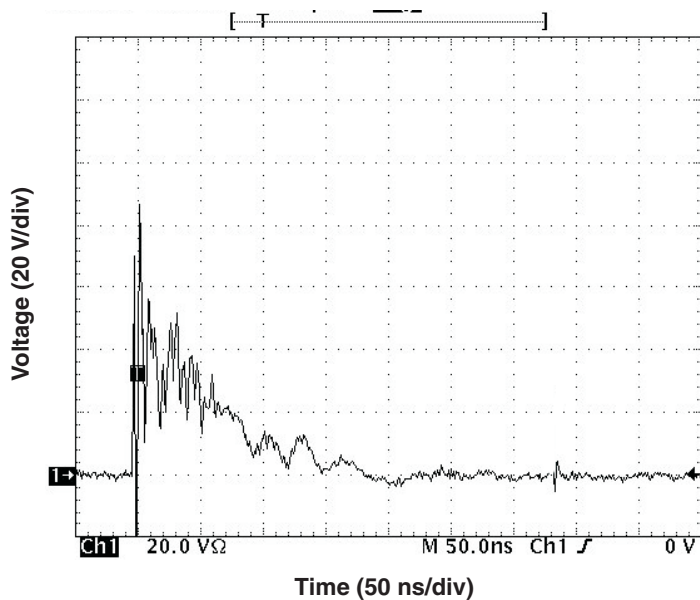


Figure 4. ESD Clamp Voltage At I/O Pins: IEC6100-4-2 15 kV Contact Discharge

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
TPD4E002DRLR	ACTIVE	SOT-553	DRL	5	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPD4E002DRLRG4	ACTIVE	SOT-553	DRL	5	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

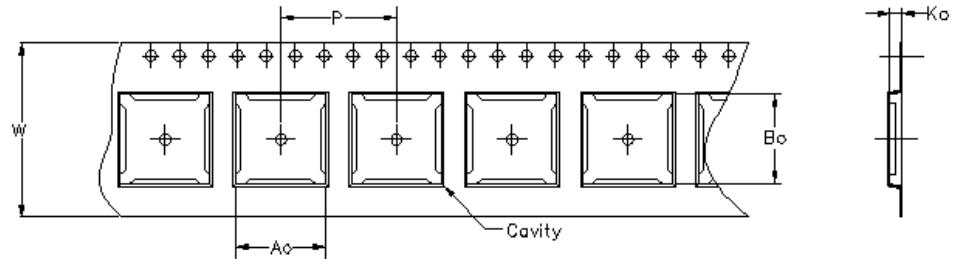
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

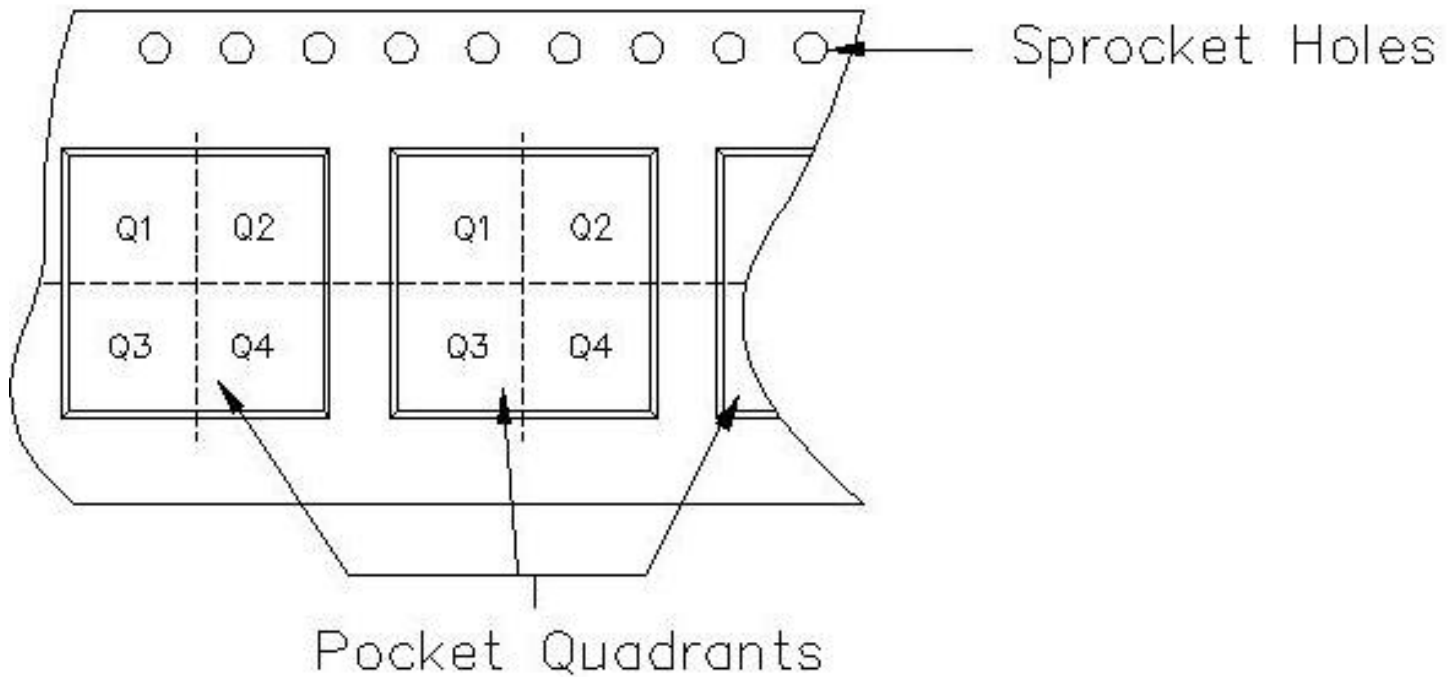
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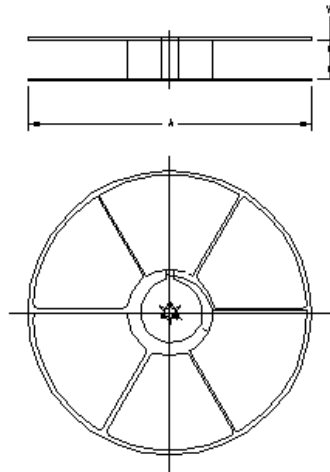
Carrier tape design is defined largely by the component length, width, and thickness.

A_0 = Dimension designed to accommodate the component width.
B_0 = Dimension designed to accommodate the component length.
K_0 = Dimension designed to accommodate the component thickness.
W = Overall width of the carrier tape.
P = Pitch between successive cavity centers.



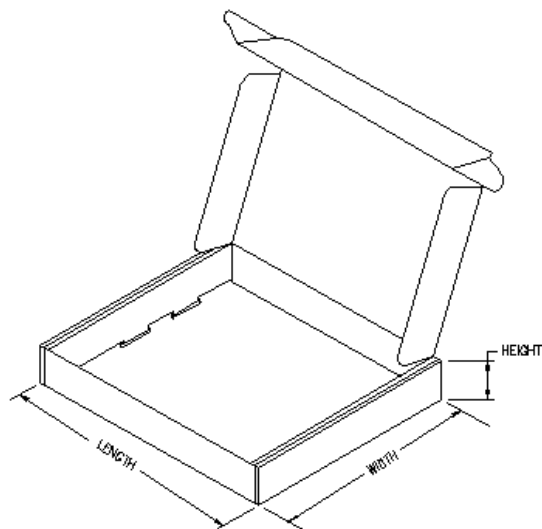
TAPE AND REEL INFORMATION

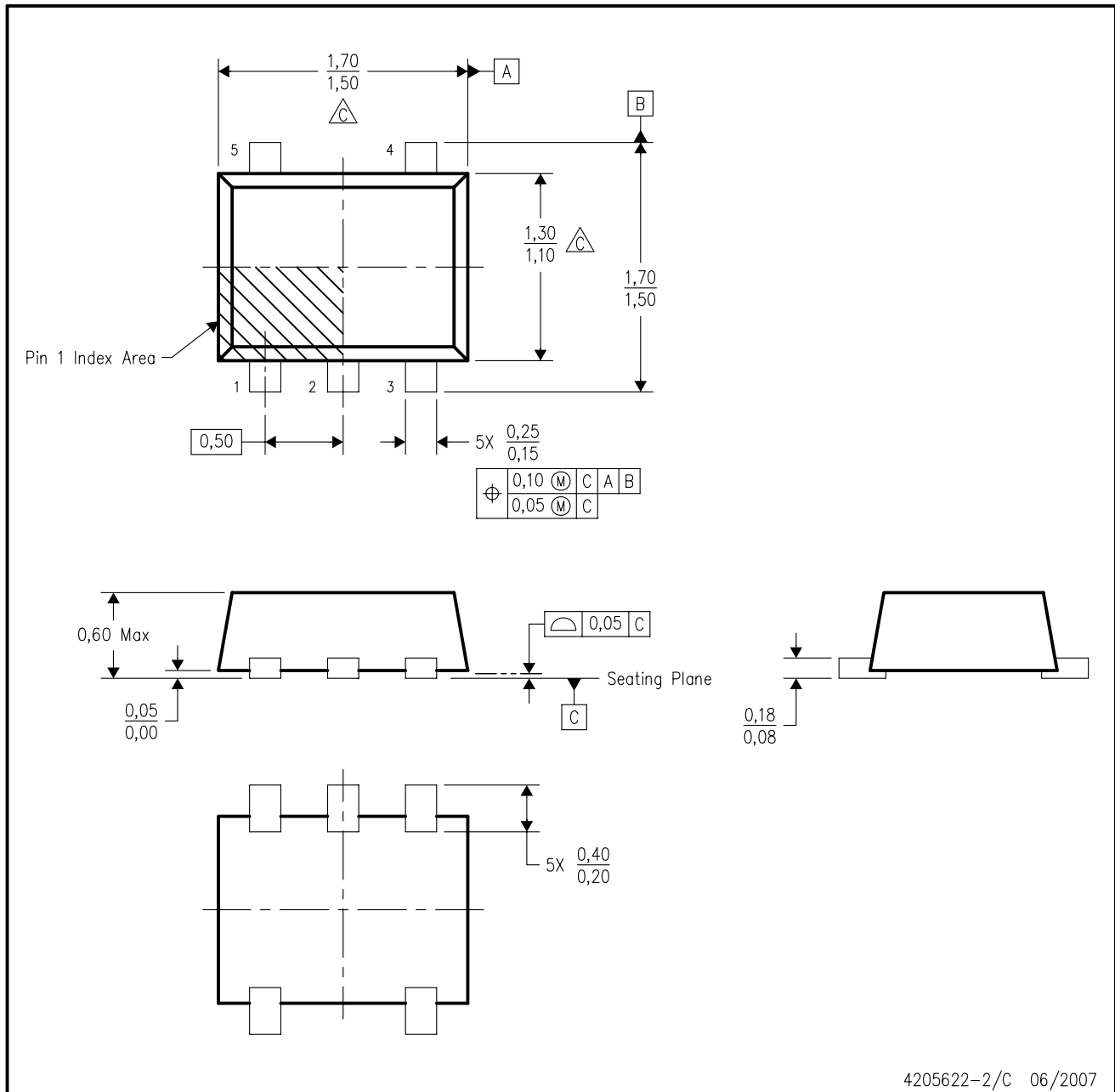
Device	Package	Pins	Site	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPD4E002DRLR	DRL	5	HNT	180	9	1.78	1.78	0.69	4	8	Q3



TAPE AND REEL BOX INFORMATION

Device	Package	Pins	Site	Length (mm)	Width (mm)	Height (mm)
TPD4E002DRLR	DRL	5	HNT	201.0	192.0	26.0





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- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash, interlead flash, protrusions, or gate burrs. Mold flash, interlead flash, protrusions, or gate burrs shall not exceed 0,15 per end or side.
 - D. JEDEC package registration is pending.

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